

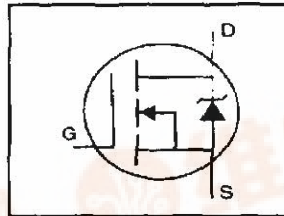
International  
**IOR** Rectifier

PD - 94880

# IRF740LCPbF

## HEXFET® Power MOSFET

- Ultra Low Gate Charge
- Reduced Gate Drive Requirement
- Enhanced 30V V<sub>GS</sub> Rating
- Reduced C<sub>iss</sub>, C<sub>oss</sub>, C<sub>rss</sub>
- Extremely High Frequency Operation
- Repetitive Avalanche Rated
- Lead-Free

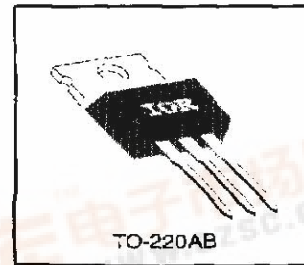


$V_{DSS} = 400V$   
 $R_{DS(on)} = 0.55\Omega$   
 $I_D = 10A$

### Description

This new series of Low Charge HEXFETs achieve significantly lower gate charge over conventional MOSFETs. Utilizing the new LCDMOS technology, the device improvements are achieved without added product cost, allowing for reduced gate drive requirements and total system savings. In addition, reduced switching losses and improved efficiency are achievable in a variety of high frequency applications. Frequencies of a few MHz at high current are possible using the new Low Charge MOSFETs.

These device improvements combined with the proven ruggedness and reliability that are characteristic of HEXFETs offer the designer a new standard in power transistors for switching applications.



### Absolute Maximum Ratings

Parameter	Max.	Units
$I_D @ T_C = 25^\circ C$	10	A
$I_D @ T_C = 100^\circ C$	6.3	A
$I_{DM}$	32	A
$P_D @ T_C = 25^\circ C$	125	W
	1.0	W/°C
$V_{GS}$	±30	V
$E_{AS}$	520	mJ
$I_{AR}$	10	A
$E_{AR}$	13	mJ
$dv/dt$	4.0	V/ns
$T_J$	-55 to +150	°C
$T_{STG}$		
	300 (1.6mm from case)	
	10 lbf.in (1.1 N.m)	

### Thermal Resistance

Parameter	Min.	Typ.	Max.	Units
$R_{\theta JC}$	—	—	1.0	°C/W
$R_{\theta CS}$	—	0.50	—	°C/W
$R_{\theta JA}$	—	—	62	°C/W



## Electrical Characteristics @ T<sub>J</sub> = 25°C (unless otherwise specified)

Parameter	Min.	Typ.	Max.	Units	Test Conditions
V <sub>(BR)DSS</sub>	400	—	—	V	V <sub>GS</sub> =0V, I <sub>D</sub> =250μA
ΔV <sub>(BR)DSS</sub> /ΔT <sub>J</sub>	—	0.76	—	V/°C	Reference to 25°C, I <sub>D</sub> =1mA
R <sub>DS(on)</sub>	—	—	0.55	Ω	V <sub>GS</sub> =10V, I <sub>D</sub> =6.0A ①
V <sub>GS(th)</sub>	2.0	—	4.0	V	V <sub>DS</sub> =V <sub>GS</sub> , I <sub>D</sub> =250μA
g <sub>fs</sub>	3.0	—	—	S	V <sub>DS</sub> =50V, I <sub>D</sub> =6.0A ①
I <sub>DSS</sub>	—	—	25	μA	V <sub>DS</sub> =400V, V <sub>GS</sub> =0V
I <sub>GSS</sub>	—	—	100	nA	V <sub>GS</sub> =20V
Q <sub>g</sub>	—	—	39	nC	I <sub>D</sub> =10A
Q <sub>gs</sub>	—	—	10	nC	V <sub>DS</sub> =320V
Q <sub>gd</sub>	—	—	19	nC	V <sub>GS</sub> =10V See Fig. 6 and 13 ①
t <sub>d(on)</sub>	—	11	—	ns	V <sub>DD</sub> =200V
t <sub>r</sub>	—	31	—	ns	I <sub>D</sub> =10A
t <sub>d(off)</sub>	—	25	—	ns	R <sub>G</sub> =9.1Ω
t <sub>f</sub>	—	20	—	ns	R <sub>D</sub> =20Ω See Figure 10 ①
L <sub>D</sub>	—	4.5	—	nH	Between lead, 6 mm (0.25in.) from package and center of die contact
L <sub>S</sub>	—	7.5	—	nH	
C <sub>iss</sub>	—	1100	—	pF	V <sub>GS</sub> =0V
C <sub>oss</sub>	—	190	—	pF	V <sub>DS</sub> =25V
C <sub>rss</sub>	—	18	—	pF	f=1.0MHz See Figure 5

## Source-Drain Ratings and Characteristics

Parameter	Min.	Typ.	Max.	Units	Test Conditions
I <sub>S</sub>	—	—	10	A	MOSFET symbol showing the integral reverse p-n junction diode.
I <sub>SM</sub>	—	—	32	A	
V <sub>SD</sub>	—	—	2.0	V	T <sub>J</sub> =25°C, I <sub>S</sub> =10A, V <sub>GS</sub> =0V ①
t <sub>rr</sub>	—	380	570	ns	T <sub>J</sub> =25°C, I <sub>F</sub> =10A
Q <sub>rr</sub>	—	2.8	4.2	μC	di/dt=100A/μs ①
t <sub>on</sub>	Intrinsic turn-on time is negligible (turn-on is dominated by L <sub>S</sub> +L <sub>D</sub> )				

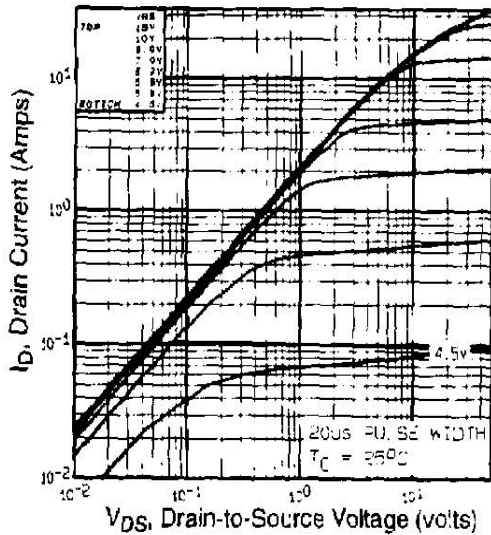
### Notes:

① Repetitive rating; pulse width limited by max. junction temperature (See Figure 11)

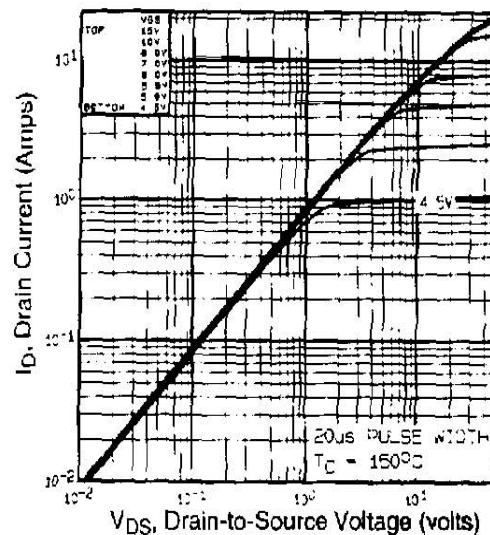
② I<sub>SD</sub>≤10A, di/dt≤120A/μs, V<sub>DS</sub>≤V<sub>(BR)DSS</sub>, T<sub>J</sub>≤150°C

③ V<sub>DD</sub>=50V, starting T<sub>J</sub>=25°C, L=9.1mH, R<sub>G</sub>=25Ω, I<sub>AS</sub>=10A (See Figure 12)

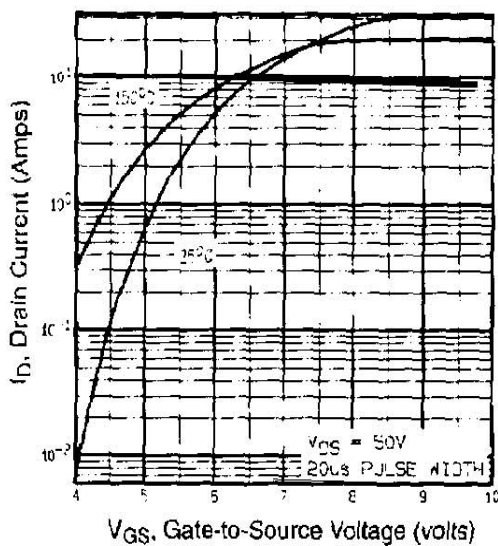
④ Pulse width ≤ 300 μs; duty cycle ≤2%.



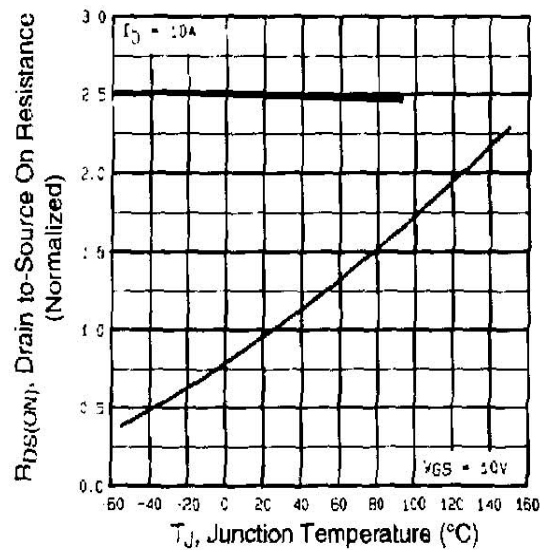
**Fig 1.** Typical Output Characteristics,  
 $T_C = 25^\circ\text{C}$



**Fig 2.** Typical Output Characteristics,  
 $T_C = 150^\circ\text{C}$



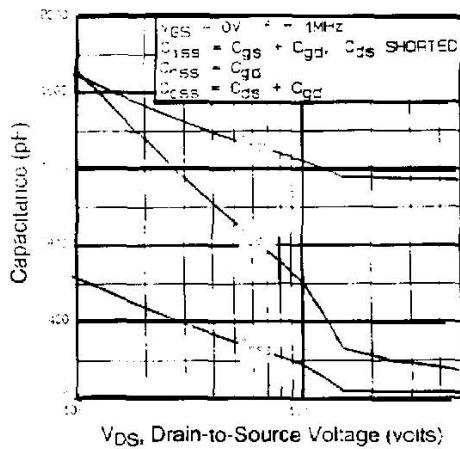
**Fig 3.** Typical Transfer Characteristics



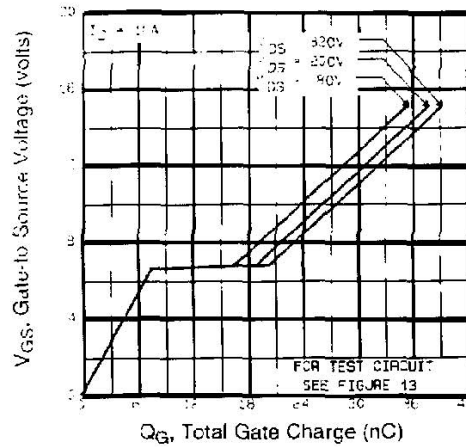
**Fig 4.** Normalized On-Resistance  
Vs. Temperature

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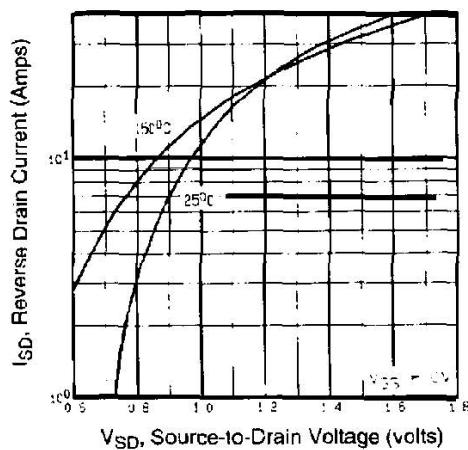
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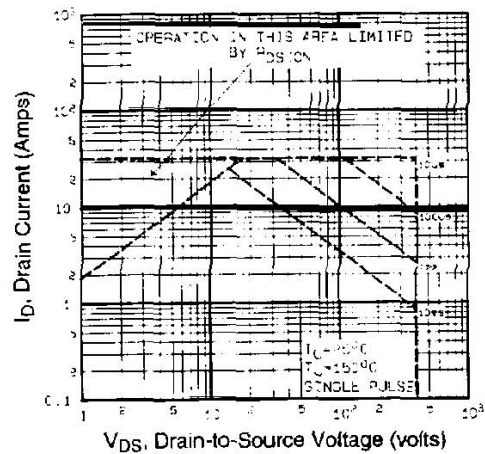
**Fig 5.** Typical Capacitance Vs. Drain-to-Source Voltage



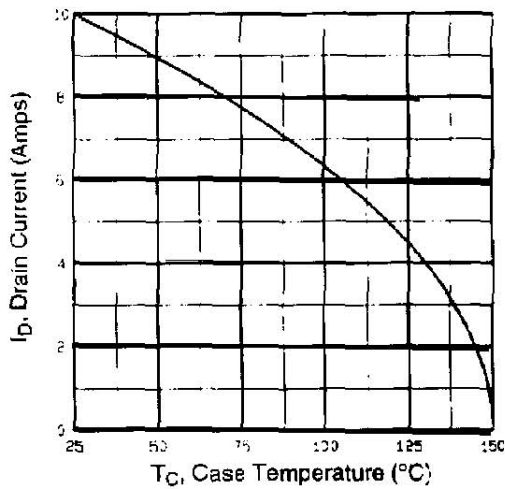
**Fig 6.** Typical Gate Charge Vs. Gate-to-Source Voltage



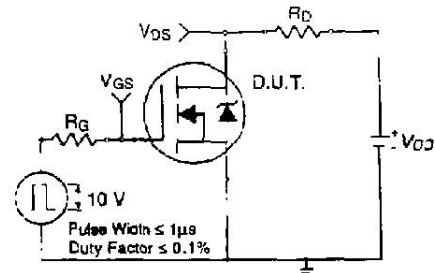
**Fig 7.** Typical Source-Drain Diode Forward Voltage



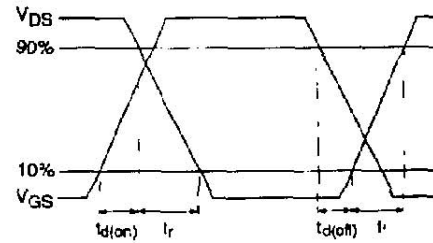
**Fig 8.** Maximum Safe Operating Area



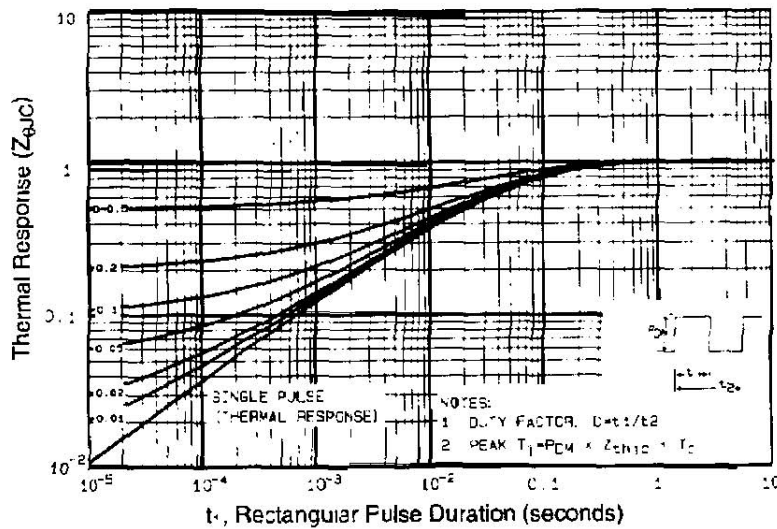
**Fig 9.** Maximum Drain Current Vs. Case Temperature



**Fig 10a.** Switching Time Test Circuit



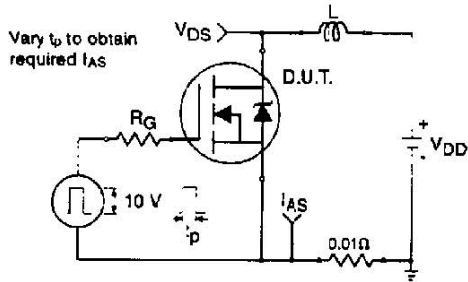
**Fig 10b.** Switching Time Waveforms



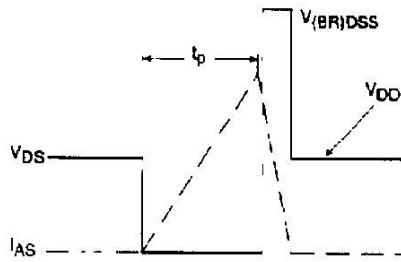
**Fig 11.** Maximum Effective Transient Thermal Impedance, Junction-to-Case

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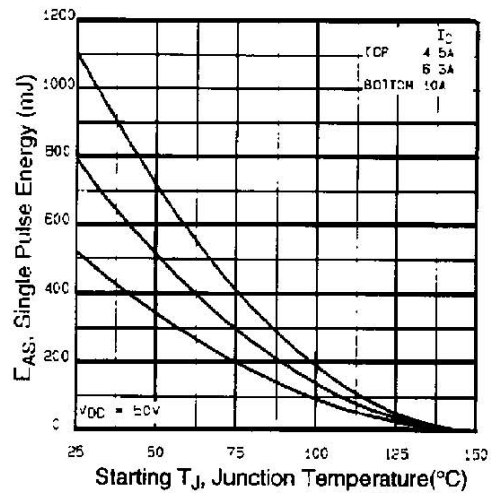
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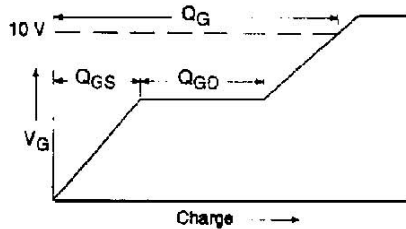
**Fig 12a.** Unclamped Inductive Test Circuit



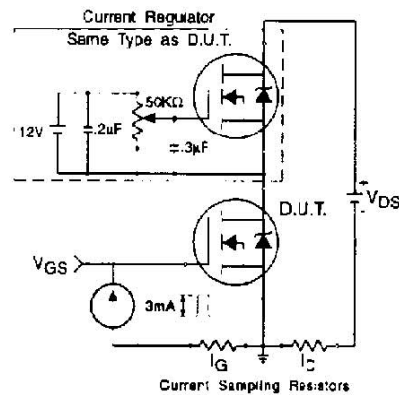
**Fig 12b.** Unclamped Inductive Waveforms



**Fig 12c.** Maximum Avalanche Energy Vs. Drain Current



**Fig 13a.** Basic Gate Charge Waveform



**Fig 13b.** Gate Charge Test Circuit

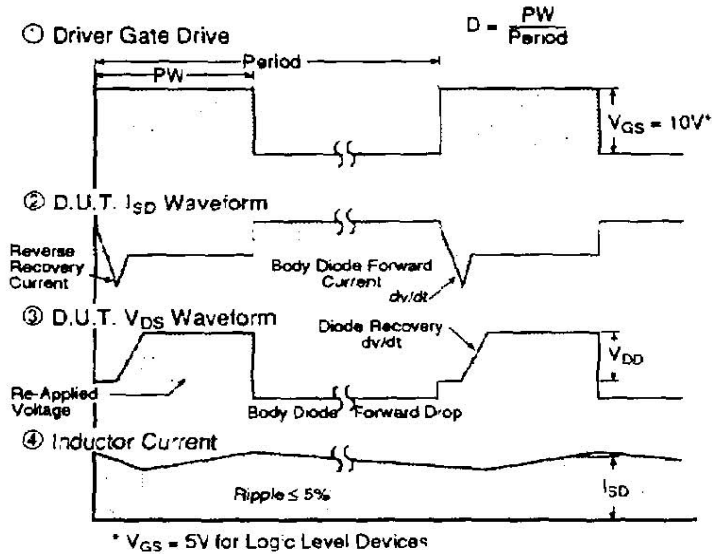
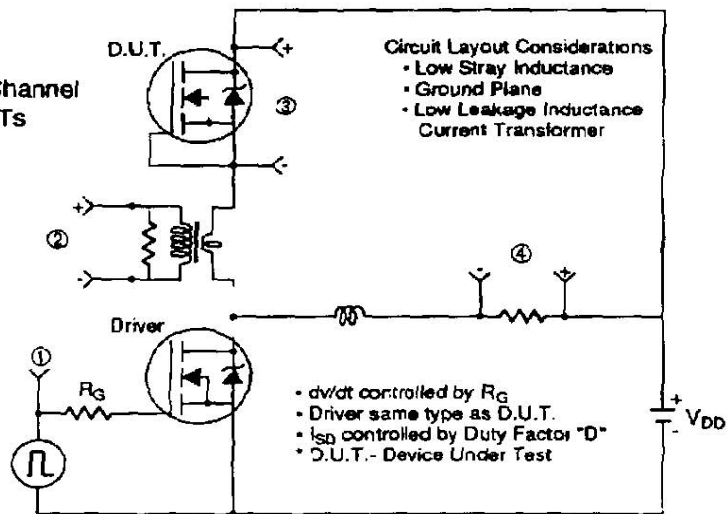
**Appendix A:** Figure 14, Peak Diode Recovery  $dv/dt$  Test Circuit

**Appendix B:** Package Outline Mechanical Drawing

Appendix A

Peak Diode Recovery  $dv/dt$  Test Circuit

Fig 14. For N-Channel HEXFETs

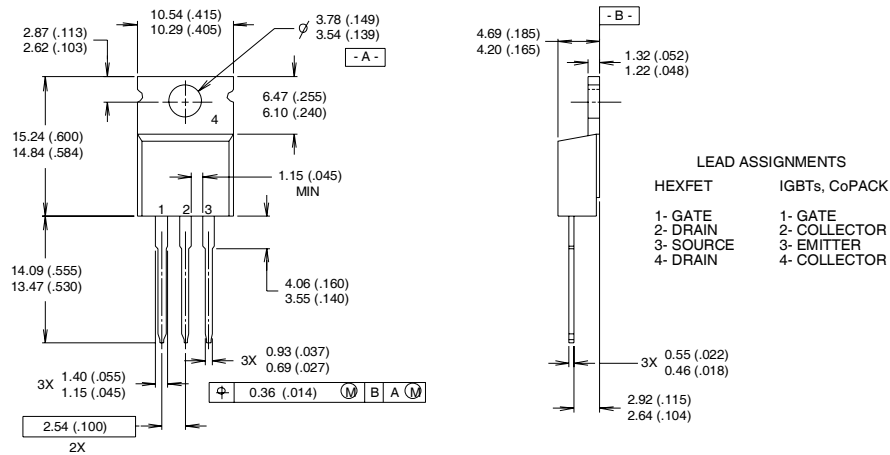


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## TO-220AB Package Outline

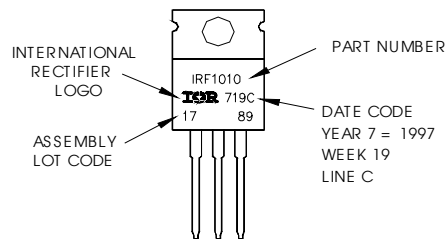
Dimensions are shown in millimeters (inches)



- NOTES:
- 1 DIMENSIONING & TOLERANCING PER ANSI Y14.5M, 1982.
  - 2 CONTROLLING DIMENSION : INCH
  - 3 OUTLINE CONFORMS TO JEDEC OUTLINE TO-220AB.
  - 4 HEATSINK & LEAD MEASUREMENTS DO NOT INCLUDE BURRS.

## TO-220AB Part Marking Information

EXAMPLE: THIS IS AN IRF1010  
 LOT CODE 1789  
 ASSEMBLED ON WW 19, 1997  
 IN THE ASSEMBLY LINE "C"  
**Note:** "P" in assembly line  
 position indicates "Lead-Free"



Data and specifications subject to change without notice.

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**IR WORLD HEADQUARTERS:** 233 Kansas St., El Segundo, California 90245, USA Tel: (310) 252-7105  
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