Low Noise, Low Power, I^2C® Bus, 128 Taps

The ISL22326 integrates two digitally controlled potentiometers (XDCP) and non-volatile memory on a monolithic CMOS integrated circuit.

The digitally controlled potentiometers are implemented with a combination of resistor elements and CMOS switches. The position of the wipers are controlled by the user through the I^2C bus interface. Each potentiometer has an associated volatile Wiper Register (WR) and a non-volatile Initial Value Register (IVR) that can be directly written to and read by the user. The contents of the WR controls the position of the wiper. At power-up the device recalls the contents of the two DCP's IVR to the corresponding WRs.

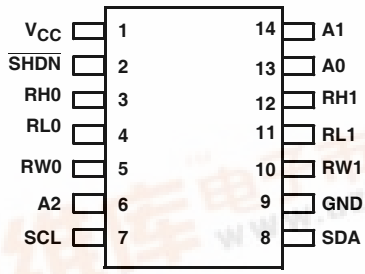
The DCPs can be used as three-terminal potentiometers or as two-terminal variable resistors in a wide variety of applications including control, parameter adjustments, and signal processing.

Features

- Two potentiometers in one package
- 128 resistor taps
- I^2C serial interface
  - Three address pins, up to eight devices/bus
- Non-volatile storage of wiper position
- Wiper resistance: 70Ω typical @ 3.3V
- Shutdown mode
- Shutdown current 5µA max
- Power supply: 2.7V to 5.5V
- 50kΩ or 10kΩ total resistance
- High reliability
  - Endurance: 1,000,000 data changes per bit per register
  - Register data retention: 50 years @ T ≤55°C
- 14 Ld TSSOP
- Pb-free plus anneal product (RoHS compliant)

Pinout

ISL22326
(14 LD TSSOP)
TOP VIEW



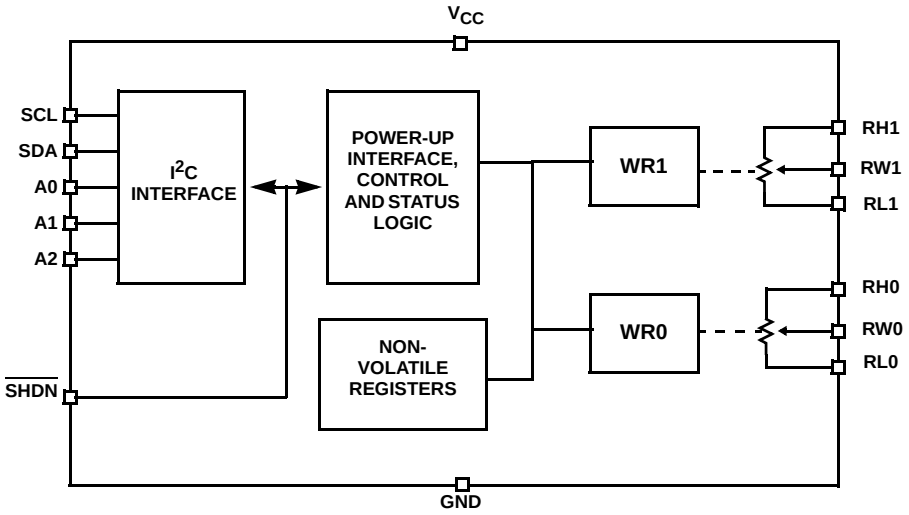
Ordering Information

PART NUMBER	PART MARKING	RESISTANCE OPTION (kΩ)	TEMP. RANGE (°C)	PACKAGE	PKG. DWG. #
ISL22326UFV14Z (Notes 1, 2)	22326 UFVZ	50	-40 to +125	14 Ld TSSOP (Pb-free)	M14.173
ISL22326WFV14Z (Notes 1, 2)	22326 WFVZ	10	-40 to +125	14 Ld TSSOP (Pb-free)	M14.173

NOTES:

1. Intersil Pb-free plus anneal products employ special Pb-free material sets; molding compounds/die attach materials and 100% matte tin plate termination finish, which are RoHS compliant and compatible with both SnPb and Pb-free soldering operations. Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.
2. Add "-TK" suffix for 1,000 Tape and Reel option

Block Diagram



Pin Descriptions

TSSOP PIN	SYMBOL	DESCRIPTION
1	V_{CC}	Power supply pin
2	$\overline{SHDN}$	Shutdown active low input
3	RH0	“High” terminal of DCP0
4	RL0	“Low” terminal of DCP0
5	RW0	“Wiper” terminal of DCP0
6	A2	Device address input for the I^2C interface
7	SCL	Open drain I^2C interface clock input
8	SDA	Open drain Serial data I/O for the I^2C interface
9	GND	Device ground pin
10	RW1	“Wiper” terminal of DCP1
11	RL1	“Low” terminal of DCP1
12	RH1	“High” terminal of DCP1
13	A0	Device address input for the I^2C interface
14	A1	Device address input for the I^2C interface

Absolute Maximum Ratings

Storage Temperature . . . . . -65°C to +150°C
Voltage at any Digital Interface Pin
with Respect to GND . . . . . -0.3V to V_{CC}+0.3
V_{CC} . . . . . -0.3V to +6V
Voltage at any DCP Pin with Respect to GND. . . . . -0.3V to V_{CC}
Lead Temperature (Soldering, 10s) . . . . . 300°C
I_W (10s) . . . . . ±6mA
Latchup (Note 4) . . . . . Class II, Level B @ +125°C
ESD (HBM) 2.5kV
(CDM) 1kV

Thermal Information

Thermal Resistance (Typical, Note 3)	θ_{JA} (°C/W)
14 Lead TSSOP package	100

Recommended Operating Conditions

Temperature Range (Extended Industrial). . . . . -40°C to +125°C
V_{CC} . . . . . 2.7V to 5.5V
Power Rating of each DCP 5mW
Wiper Current of each DCP. . . . . ±3.0mA

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTES:

3. θ_{JA} is measured with the component mounted on a high effective thermal conductivity test board in free air. See Tech Brief TB379 for details.
4. Jedec Class II pulse conditions and failure criterion used. Level B exceptions are: using a max positive pulse of 6.5V on the SHDN pin, and using a max negative pulse of -0.8V for all pins.

Analog Specifications

Over recommended operating conditions unless otherwise stated.

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP (NOTE 5)	MAX	UNIT
R_{TOTAL}	R_H to R_L Resistance	W option		10		kΩ
		U option		50		kΩ
	R_H to R_L Resistance Tolerance	W and U option	-20		+20	%
	End-to-End Temperature Coefficient	W option		±50		ppm/°C (Note 19)
		U option		±80		ppm/°C (Note 19)
R_W	Wiper Resistance	V_{CC} = 3.3V @ +25°C, wiper current = V_{CC}/R_{TOTAL}		70	200	Ω
V_{RH}, V_{RL}	V_{RH} and V_{RL} Terminal Voltages	V_{RH} and V_{RL} to GND	0		V_{CC}	V
$C_H/C_L/C_W$ (Note 19)	Potentiometer Capacitance			10/10/25		pF
I_{LkgDCP}	Leakage on DCP Pins	Voltage at pin from GND to V_{CC}		0.1	1	µA
VOLTAGE DIVIDER MODE (0V @ R_Li; V_{CC} @ R_Hi; measured at R_Wi, unloaded; i = 0 or 1)						
INL (Note 10)	Integral Non-linearity	Monotonic over all tap positions	-1		1	LSB (Note 6)
DNL (Note 9)	Differential Non-linearity	Monotonic over all tap positions	-0.5		0.5	LSB (Note 6)
ZSerror (Note 7)	Zero-scale Error	W option	0	1	5	LSB (Note 6)
		U option	0	0.5	2	
FSerror (Note 8)	Full-scale Error	W option	-5	-1	0	LSB (Note 6)
		U option	-2	-1	0	
V_{MATCH} (Note 11)	DCP to DCP Matching	Any two DCPs at same tap position, same voltage at all RH terminals, and same voltage at all RL terminals	-2		2	LSB (Note 6)
TC_V (Note 12)	Ratiometric Temperature Coefficient	DCP register set to 40 hex		±4		ppm/°C

Analog Specifications

Over recommended operating conditions unless otherwise stated. **(Continued)**

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP (NOTE 5)	MAX	UNIT
RESISTOR MODE (Measurements between $R_W i$ and $R_L i$ with $R_H i$ not connected, or between $R_W i$ and $R_H i$ with $R_L i$ not connected. i = 0 or 1)						
RINL (Note 16)	Integral Non-linearity	DCP register set between 10h and 7Fh; monotonic over all tap positions	-1		1	MI (Note 13)
RDNL (Note 15)	Differential Non-linearity	DCP register set between 10h and 7Fh; monotonic over all tap positions	-0.5		0.5	MI (Note 13)
Roffset (Note 14)	Offset	W option	0	1	5	MI (Note 13)
		U option	0	0.5	2	MI (Note 13)
R_{MATCH} (Note 17)	DCP to DCP Matching	Any two DCPs at the same tap position with the same terminal voltages	-2		2	MI (Note 13)

Operating Specifications

Over the recommended operating conditions unless otherwise specified.

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP (NOTE 5)	MAX	UNIT
I_{CC1}	V_{CC} Supply Current (volatile write/read)	f_{SCL} = 400kHz; SDA = Open; (for I^2C, active, read and write states)			0.5	mA
I_{CC2}	V_{CC} Supply Current (non-volatile write/read)	f_{SCL} = 400kHz; SDA = Open; (for I^2C, active, read and write states)			3	mA
I_{SB}	V_{CC} Current (standby)	V_{CC} = +5.5V @ +85°C, I^2C interface in standby state			5	µA
		V_{CC} = +5.5V @ +125°C, I^2C interface in standby state			7	µA
		V_{CC} = +3.6V @ +85°C, I^2C interface in standby state			3	µA
		V_{CC} = +3.6V @ +125°C, I^2C interface in standby state			5	µA
I_{SD}	V_{CC} Current (shutdown)	V_{CC} = +5.5V @ +85°C, I^2C interface in standby state			3	µA
		V_{CC} = +5.5V @ +125°C, I^2C interface in standby state			5	µA
		V_{CC} = +3.6V @ +85°C, I^2C interface in standby state			2	µA
		V_{CC} = +3.6V @ +125°C, I^2C interface in standby state			4	µA
I_{LkgDig}	Leakage Current, at Pins A0, A1, A2, $\overline{SHDN}$, SDA, and SCL	Voltage at pin from GND to V_{CC}	-1		1	µA
t_{WRT} (Note 18)	DCP Wiper Response Time	SCL falling edge of last bit of DCP data byte to wiper new position		1.5		µs
$t_{ShdnRec}$ (Note 18)	DCP Recall Time from Shutdown Mode	From rising edge of $\overline{SHDN}$ signal to wiper stored position and RH connection		1.5		µs
		SCL falling edge of last bit of ACR data byte to wiper stored position and RH connection		1.5		µs
Vpor	Power-on Recall Voltage	Minimum V_{CC} at which memory recall occurs	2.0		2.6	V
VccRamp	V_{CC} Ramp Rate		0.2			V/ms
t_D	Power-up Delay	V_{CC} above Vpor, to DCP Initial Value Register recall completed, and I^2C Interface in standby state			3	ms

Operating Specifications Over the recommended operating conditions unless otherwise specified. **(Continued)**

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP (NOTE 5)	MAX	UNIT
EEPROM SPECIFICATION						
	EEPROM Endurance		1,000,000			Cycles
	EEPROM Retention	Temperature T ≤55°C	50			Years
t_{WC} (Note 20)	Non-volatile Write Cycle Time			12	20	ms
SERIAL INTERFACE SPECS						
V_{IL}	A2, A1, A0, $\overline{SHDN}$, SDA, and SCL Input Buffer LOW Voltage		-0.3		$0.3*V_{CC}$	V
V_{IH}	A2, A1, A0, $\overline{SHDN}$, SDA, and SCL Input Buffer HIGH Voltage		$0.7*V_{CC}$		$V_{CC}+0.3$	V
Hysteresis	SDA and SCL Input Buffer Hysteresis		$0.05*V_{CC}$			V
V_{OL}	SDA Output Buffer LOW Voltage, Sinking 4mA		0		0.4	V
Cpin (Note 19)	A2, A1, A0, $\overline{SHDN}$, SDA, and SCL Pin Capacitance				10	pF
f_{SCL}	SCL Frequency				400	kHz
t_{sp}	Pulse Width Suppression Time at SDA and SCL Inputs	Any pulse narrower than the max spec is suppressed			50	ns
t_{AA}	SCL falling edge to SDA output data valid	SCL falling edge crossing 30% of V_{CC}, until SDA exits the 30% to 70% of V_{CC} window			900	ns
t_{BUF}	Time the Bus Must be Free Before the Start of a New Transmission	SDA crossing 70% of V_{CC} during a STOP condition, to SDA crossing 70% of V_{CC} during the following START condition	1300			ns
t_{LOW}	Clock LOW Time	Measured at the 30% of V_{CC} crossing	1300			ns
t_{HIGH}	Clock HIGH Time	Measured at the 70% of V_{CC} crossing	600			ns
$t_{SU:STA}$	START Condition Setup Time	SCL rising edge to SDA falling edge; both crossing 70% of V_{CC}	600			ns
$t_{HD:STA}$	START Condition Hold Time	From SDA falling edge crossing 30% of V_{CC} to SCL falling edge crossing 70% of V_{CC}	600			ns
$t_{SU:DAT}$	Input Data Setup Time	From SDA exiting the 30% to 70% of V_{CC} window, to SCL rising edge crossing 30% of V_{CC}	100			ns
$t_{HD:DAT}$	Input Data Hold Time	From SCL rising edge crossing 70% of V_{CC} to SDA entering the 30% to 70% of V_{CC} window	0			ns
$t_{SU:STO}$	STOP Condition Setup Time	From SCL rising edge crossing 70% of V_{CC}, to SDA rising edge crossing 30% of V_{CC}	600			ns
$t_{HD:STO}$	STOP Condition Hold Time for Read, or Volatile Only Write	From SDA rising edge to SCL falling edge; both crossing 70% of V_{CC}	1300			ns
t_{DH}	Output Data Hold Time	From SCL falling edge crossing 30% of V_{CC}, until SDA enters the 30% to 70% of V_{CC} window	0			ns
t_R	SDA and SCL Rise Time	From 30% to 70% of V_{CC}	20 + 0.1 * Cb		250	ns
t_F	SDA and SCL Fall Time	From 70% to 30% of V_{CC}	20 + 0.1 * Cb		250	ns
Cb	Capacitive Loading of SDA or SCL	Total on-chip and off-chip	10		400	pF
Rpu	SDA and SCL Bus Pull-up Resistor Off-chip	Maximum is determined by t_R and t_F For Cb = 400pF, max is about 2~2.5kΩ For Cb = 40pF, max is about 15~20kΩ	1			kΩ

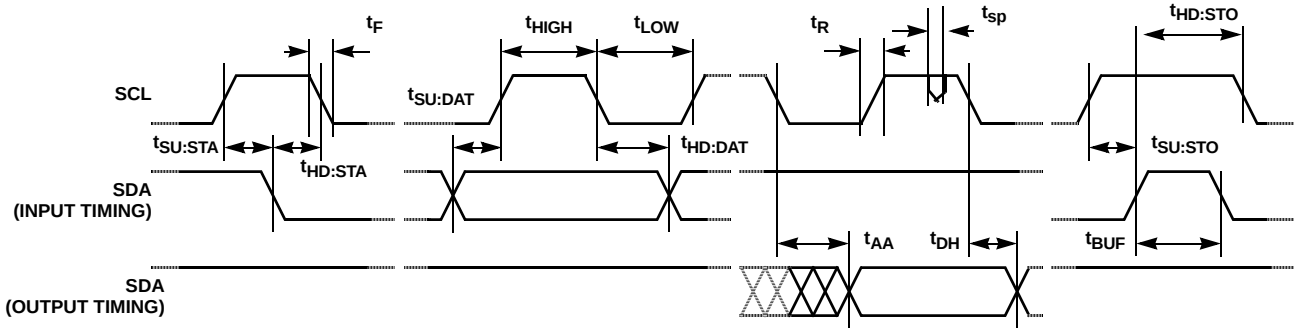
Operating Specifications Over the recommended operating conditions unless otherwise specified. **(Continued)**

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP (NOTE 5)	MAX	UNIT
$t_{SU:A}$	A2, A1 and A0 Setup Time	Before START condition	600			ns
$t_{HD:A}$	A2, A1 and A0 Hold Time	After STOP condition	600			ns

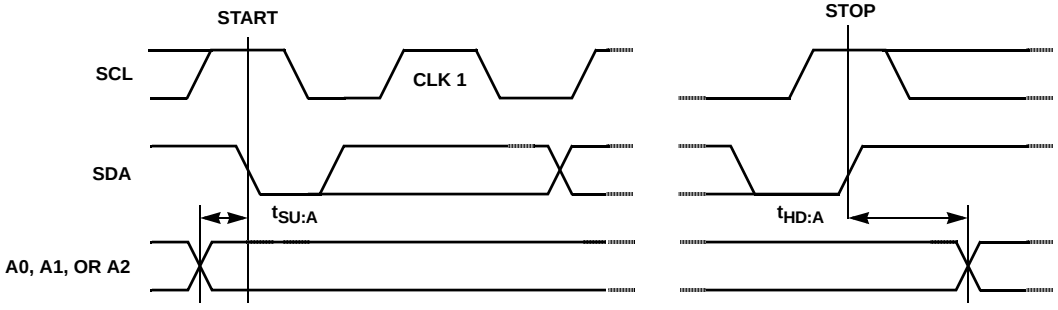
NOTES:

5. Typical values are for T_A = +25°C and 3.3V supply voltage
6. LSB: $[V(R_W)_{127} – V(R_W)_0]/127$. $V(R_W)_{127}$ and $V(R_W)_0$ are $V(R_W)$ for the DCP register set to 7F hex and 00 hex respectively. LSB is the incremental voltage when changing from one tap to an adjacent tap.
7. ZS error = $V(RW)_0$/LSB.
8. FS error = $[V(RW)_{127} – V_{CC}]$/LSB.
9. DNL = $[V(RW)_i – V(RW)_{i-1}]$/LSB-1, for i = 1 to 127. i is the DCP register setting.
10. INL = $[V(RW)_i – i • LSB – V(RW)_0]$/LSB for i = 1 to 127.
11. V_{MATCH} = $[V(RWx)_i – V(RWy)_i]$/LSB, for i = 1 to 127, x = 0 to 1 and y = 0 to 1.
12. $TC_V = \frac{Max(V(RW)_i) – Min(V(RW)_i)}{[Max(V(RW)_i) + Min(V(RW)_i)]/2} \times \frac{10^6}{165°C}$ for i = 16 to 112 decimal, T = -40°C to +125°C. Max( ) is the maximum value of the wiper voltage and Min ( ) is the minimum value of the wiper voltage over the temperature range.
13. MI = $|RW_{127} – RW_0|$/127. MI is a minimum increment. RW_{127} and RW_0 are the measured resistances for the DCP register set to 7F hex and 00 hex respectively.
14. Roffset = RW_0/MI, when measuring between RW and RL.
    Roffset = RW_{127}/MI, when measuring between RW and RH.
15. RDNL = $(RW_i – RW_{i-1})$/MI -1, for i = 16 to 127.
16. RINL = $[RW_i – (MI • i) – RW_0]$/MI, for i = 16 to 127.
17. R_{MATCH} = $(RW_{i,x} – RW_{i,y})$/MI, for i = 1 to 127, x = 0 to 1 and y = 0 to 1.
18. $TC_R = \frac{[Max(Ri) – Min(Ri)]}{[Max(Ri) + Min(Ri)]/2} \times \frac{10^6}{165°C}$ for i = 16 to 112, T = -40°C to +125°C. Max( ) is the maximum value of the resistance and Min ( ) is the minimum value of the resistance over the temperature range.
19. This parameter is not 100% tested.
20. t_{WC} is the time from a valid STOP condition at the end of a Write sequence of I^2C serial interface, to the end of the self-timed internal non-volatile write cycle.

SDA vs SCL Timing



A0, A1, and A2 Pin Timing



Typical Performance Curves

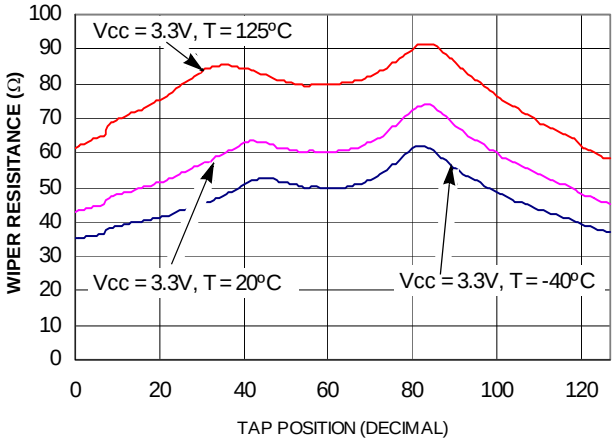


FIGURE 1. WIPER RESISTANCE vs TAP POSITION [I(RW) = V_{CC}/R_{TOTAL}] FOR 10kΩ (W)

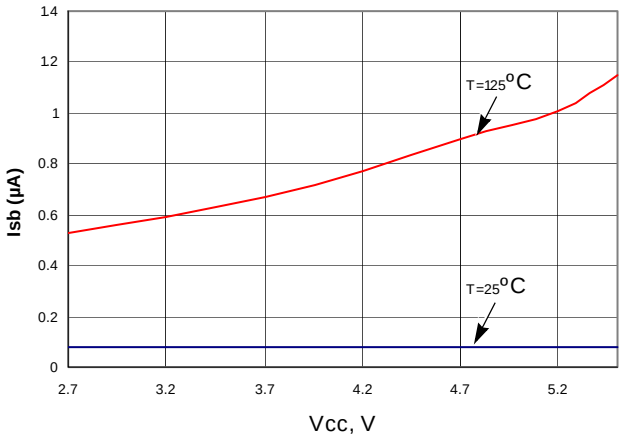


FIGURE 2. STANDBY I_{CC} vs V_{CC}

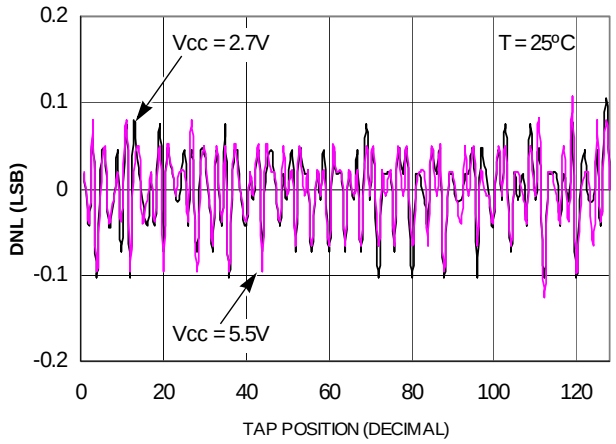


FIGURE 3. DNL vs TAP POSITION IN VOLTAGE DIVIDER MODE FOR 10kΩ (W)

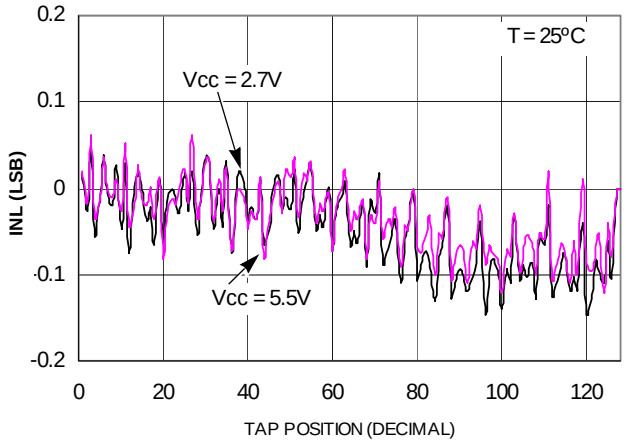


FIGURE 4. INL vs TAP POSITION IN VOLTAGE DIVIDER MODE FOR 10kΩ (W)

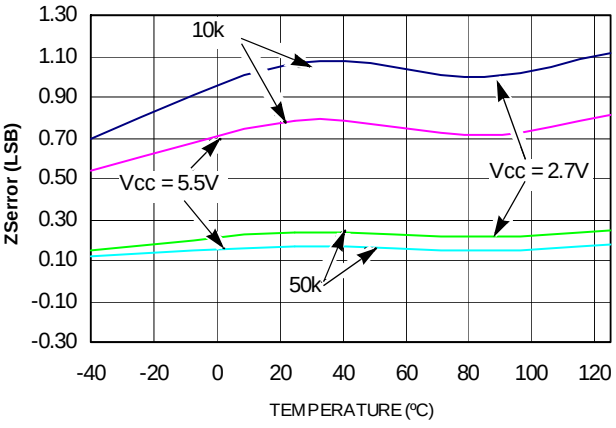


FIGURE 5. ZSerror vs TEMPERATURE

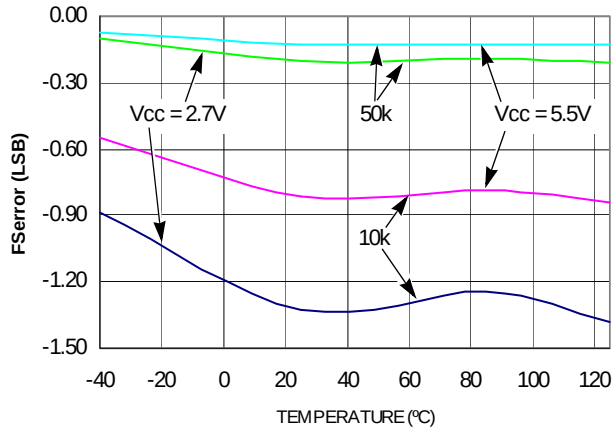


FIGURE 6. FSerror vs TEMPERATURE

Typical Performance Curves (Continued)

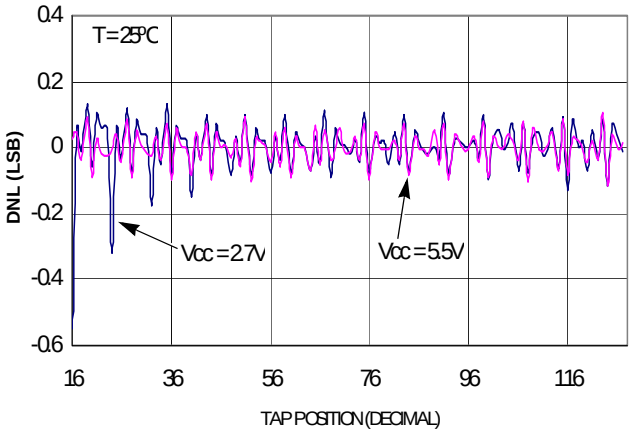


FIGURE 7. DNL vs TAP POSITION IN Rheostat MODE FOR 10kΩ (W)

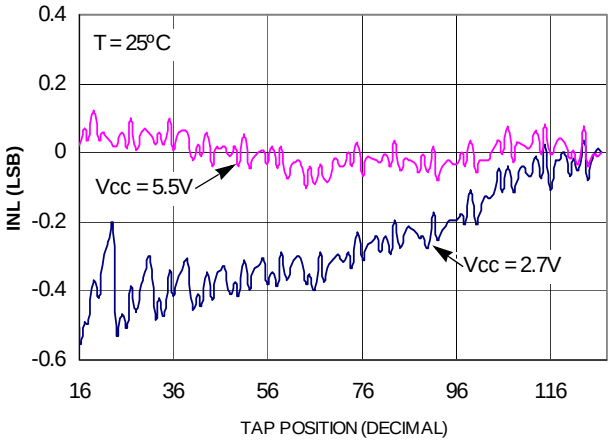


FIGURE 8. INL vs TAP POSITION IN Rheostat MODE FOR 10kΩ (W)

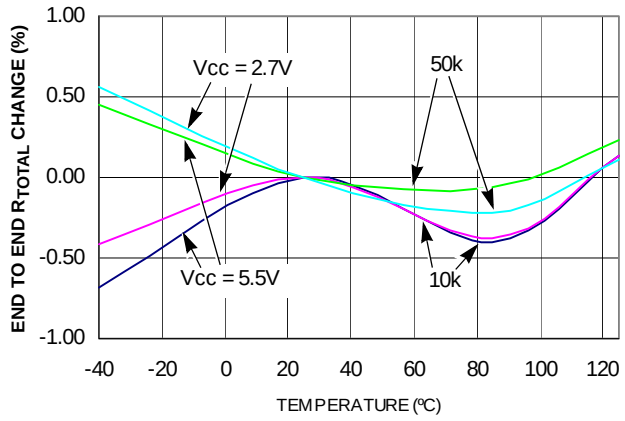


FIGURE 9. END TO END R_{TOTAL} % CHANGE vs TEMPERATURE

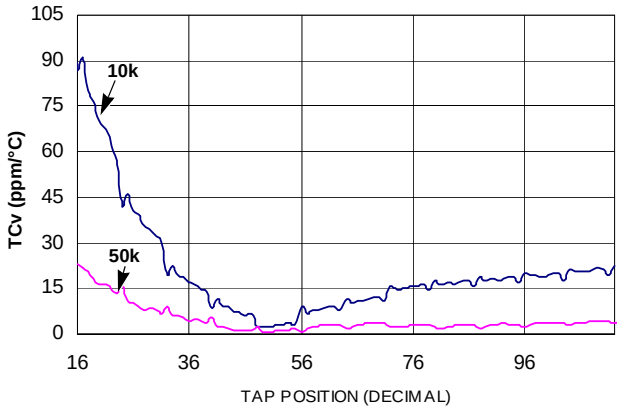


FIGURE 10. TC FOR VOLTAGE DIVIDER MODE IN ppm

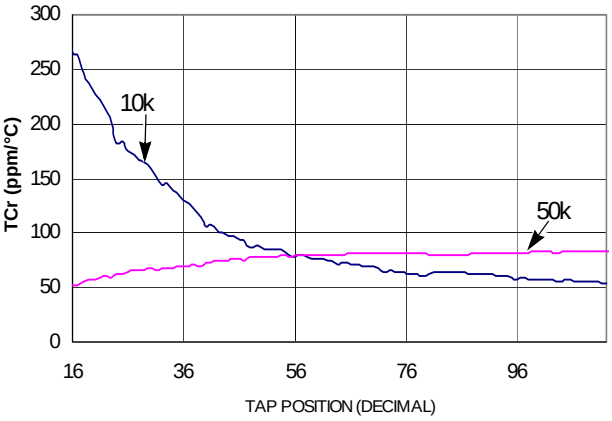


FIGURE 11. TC FOR Rheostat MODE IN ppm

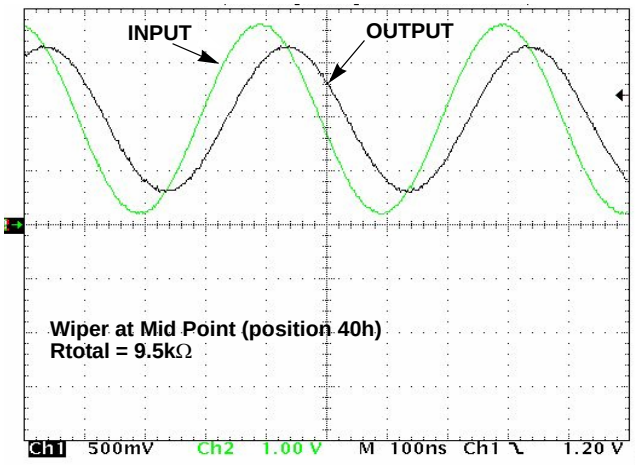


FIGURE 12. FREQUENCY RESPONSE (2.6MHz)

Typical Performance Curves (Continued)

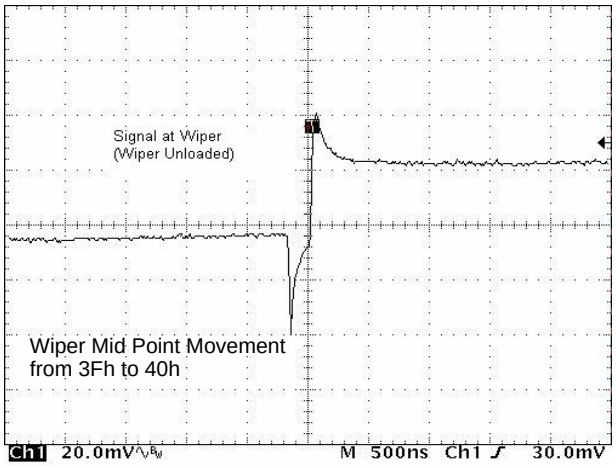


FIGURE 13. MIDSCALE GLITCH, CODE 3Fh TO 40h

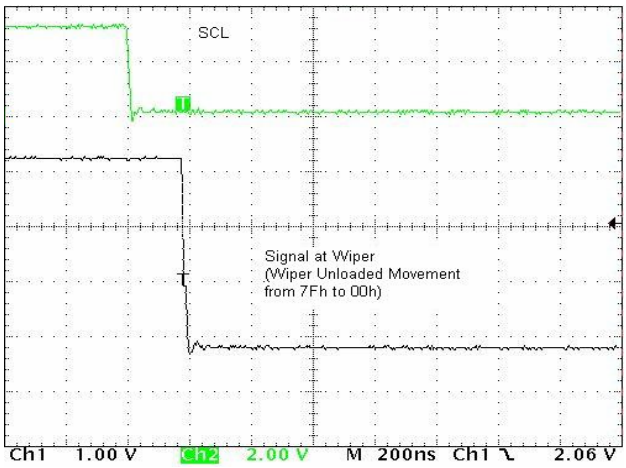


FIGURE 14. LARGE SIGNAL SETTLING TIME

Pin Descriptions

Potentiometers Pins

RHi and RLi (i = 0, 1)

The high (RHi) and low (RLi) terminals of the ISL22326 are equivalent to the fixed terminals of a mechanical potentiometer. RHi and RLi are referenced to the relative position of the wiper and not the voltage potential on the terminals. With WRi set to 127 decimal, the wiper will be closest to RHi, and with the WRi set to 0, the wiper is closest to RLi.

RWi (i = 0,1)

RWi is the wiper terminal and is equivalent to the movable terminal of a mechanical potentiometer. The position of the wiper within the array is determined by the WRi register.

$\overline{\text{SHDN}}$

The $\overline{\text{SHDN}}$ pin forces the resistor to end-to-end open circuit condition on RHi and shorts RWi to RLi. When $\overline{\text{SHDN}}$ is returned to logic high, the previous latch settings put RWi at the same resistance setting prior to shutdown. This pin is logically OR'd with SHDN bit in ACR register. I^2C interface is still available in shutdown mode and all registers are accessible. This pin must remain HIGH for normal operation.

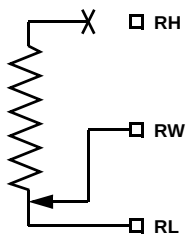


FIGURE 15. DCP CONNECTION IN SHUTDOWN MODE

Bus Interface Pins

Serial Data Input/Output (SDA)

The SDA is a bidirectional serial data input/output pin for I^2C interface. It receives device address, operation code, wiper address and data from an I^2C external master device at the rising edge of the serial clock SCL, and it shifts out data after each falling edge of the serial clock.

SDA requires an external pull-up resistor, since it is an open drain input/output.

Serial Clock (SCL)

This is the serial clock input of the I^2C serial interface. SCL requires an external pull-up resistor, since it is an open drain input.

Device Address (A2 - A0)

The address inputs are used to set the least significant 3 bits of the 7-bit I^2C interface slave address. A match in the slave address serial data stream must match with the Address input pins in order to initiate communication with the ISL22326. A maximum of 8 ISL22326 devices may occupy the I^2C serial bus.

Principles of Operation

The ISL22326 is an integrated circuit incorporating two DCPs with their associated registers, non-volatile memory and an I^2C serial interface providing direct communication between a host and the potentiometers and memory. The resistor arrays are comprised of individual resistors connected in series. At either end of the array and between each resistor is an electronic switch that transfers the potential at that point to the wiper.

The electronic switches on the device operate in a "make before break" mode when the wiper changes tap positions.

When the device is powered down, the last value stored in IVRi will be maintained in the non-volatile memory. When power is restored, the contents of the IVRi are recalled and loaded into the corresponding WRi to set the wipers to the initial value.

DCP Description

Each DCP is implemented with a combination of resistor elements and CMOS switches. The physical ends of each DCP are equivalent to the fixed terminals of a mechanical potentiometer (RH and RL pins). The RW pin of each DCP is connected to intermediate nodes, and is equivalent to the wiper terminal of a mechanical potentiometer. The position of the wiper terminal within the DCP is controlled by volatile Wiper Register (WR). Each DCP has its own WR. When the WR of a DCP contains all zeroes (WR[6:0]= 00h), its wiper terminal (RW) is closest to its “Low” terminal (RL). When the WR register of a DCP contains all ones (WR[6:0]= 7Fh), its wiper terminal (RW) is closest to its “High” terminal (RH). As the value of the WR increases from all zeroes (0) to all ones (127 decimal), the wiper moves monotonically from the position closest to RL to the closest to RH. At the same time, the resistance between RW and RL increases monotonically, while the resistance between RH and RW decreases monotonically.

While the ISL22326 is being powered up, all WRs are reset to 40h (64 decimal), which locates RW roughly at the center between RL and RH. After the power supply voltage becomes large enough for reliable non-volatile memory reading, all WRs will be reload with the value stored in corresponding non-volatile Initial Value Registers (IVRs).

The WRs can be read or written to directly using the I^2C serial interface as described in the following sections. The I^2C interface Address Byte has to be set to 00h or 01h to access the WR of DCP0 or DCP1 respectively.

Memory Description

The ISL22326 contains seven non-volatile and three volatile 8-bit registers. Memory map of ISL22326 is on Table 1. The two non-volatile registers (IVRi) at address 0 and 1, contain initial wiper value and volatile registers (WRi) contain current wiper position. In addition, five non-volatile General Purpose registers from address 2 to address 6 are available.

TABLE 1. MEMORY MAP

ADDRESS	NON-VOLATILE	VOLATILE
8	—	ACR
7	Reserved	
6	General Purpose	Not Available
5	General Purpose	Not Available
4	General Purpose	Not Available
3	General Purpose	Not Available
2	General Purpose	Not Available
1	IVR1	WR1
0	IVR0	WR0

The non-volatile IVRi and volatile WRi registers are accessible with the same address.

The Access Control Register (ACR) contains information and control bits described below in Table 2. The VOL bit at access control register (ACR[7]) determines whether the access is to wiper registers WRi or initial value registers IVRi.

TABLE 2. ACCESS CONTROL REGISTER (ACR)

VOL	SHDN	WIP	0	0	0	0	0

If VOL bit is 0, the non-volatile IVRi registers are accessible. If VOL bit is 1, only the volatile WRi are accessible. Note, value is written to IVRi register also is written to the corresponding WRi. The default value of this bit is 0.

The SHDN bit (ACR[6]) disables or enables Shutdown mode. This bit is logically OR’d with $\overline{SHDN}$ pin. When this bit is 0, DCP is in Shutdown mode. Default value of SHDN bit is 1.

The WIP bit (ACR[5]) is read only bit. It indicates that non-volatile write operation is in progress. It is impossible to write to the IVRi, WRi or ACR while WIP bit is 1.

I^2C Serial Interface

The ISL22326 supports an I^2C bidirectional bus oriented protocol. The protocol defines any device that sends data onto the bus as a transmitter and the receiving device as the receiver. The device controlling the transfer is a master and the device being controlled is the slave. The master always initiates data transfers and provides the clock for both transmit and receive operations. Therefore, the ISL22326 operates as a slave device in all applications.

All communication over the I^2C interface is conducted by sending the MSB of each byte of data first.

Protocol Conventions

Data states on the SDA line must change only during SCL LOW periods. SDA state changes during SCL HIGH are reserved for indicating START and STOP conditions (See Figure 16). On power-up of the ISL22326 the SDA pin is in the input mode.

All I^2C interface operations must begin with a START condition, which is a HIGH to LOW transition of SDA while SCL is HIGH. The ISL22326 continuously monitors the SDA and SCL lines for the START condition and does not respond to any command until this condition is met (See Figure 16). A START condition is ignored during the power-up of the device.

All I^2C interface operations must be terminated by a STOP condition, which is a LOW to HIGH transition of SDA while SCL is HIGH (See Figure 16). A STOP condition at the end of a read operation, or at the end of a write operation places the device in its standby mode.

An ACK, Acknowledge, is a software convention used to indicate a successful data transfer. The transmitting device, either master or slave, releases the SDA bus after transmitting eight bits. During the ninth clock cycle, the receiver pulls the SDA line LOW to acknowledge the reception of the eight bits of data (See Figure 17).

The ISL22326 responds with an ACK after recognition of a START condition followed by a valid Identification Byte, and once again after successful receipt of an Address Byte. The ISL22326 also responds with an ACK after receiving a Data Byte of a write operation. The master must respond with an ACK after receiving a Data Byte of a read operation.

A valid Identification Byte contains 1010 as the four MSBs, and the following three bits matching the logic values present at pins A2, A1, and A0. The LSB is the Read/$\overline{\text{Write}}$ bit. Its value is “1” for a Read operation, and “0” for a Write operation (See Table 3).

TABLE 3. IDENTIFICATION BYTE FORMAT

				Logic values at pins A2, A1, and A0 respectively			
1	0	1	0	A2	A1	A0	R/$\overline{\text{W}}$
(MSB)							(LSB)

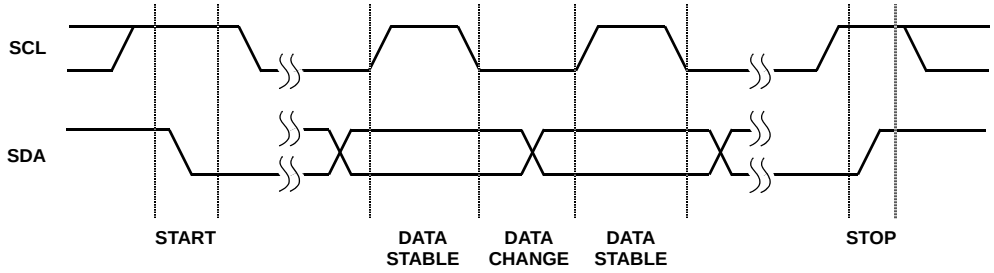


FIGURE 16. VALID DATA CHANGES, START AND STOP CONDITIONS

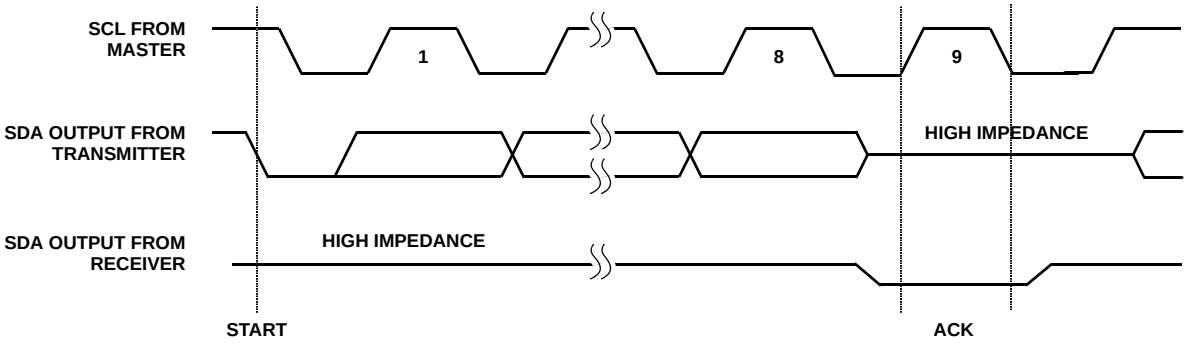


FIGURE 17. ACKNOWLEDGE RESPONSE FROM RECEIVER

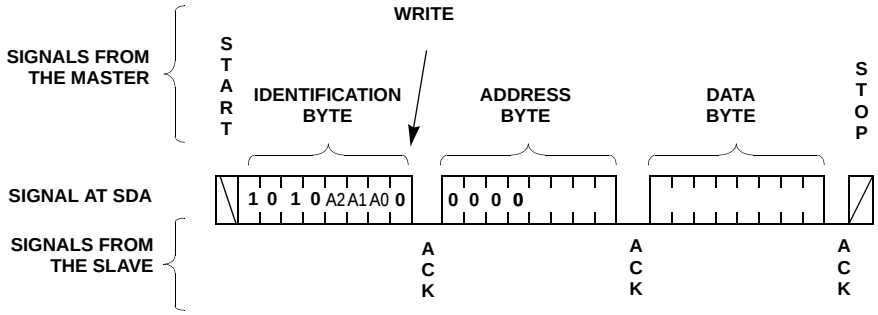


FIGURE 18. BYTE WRITE SEQUENCE

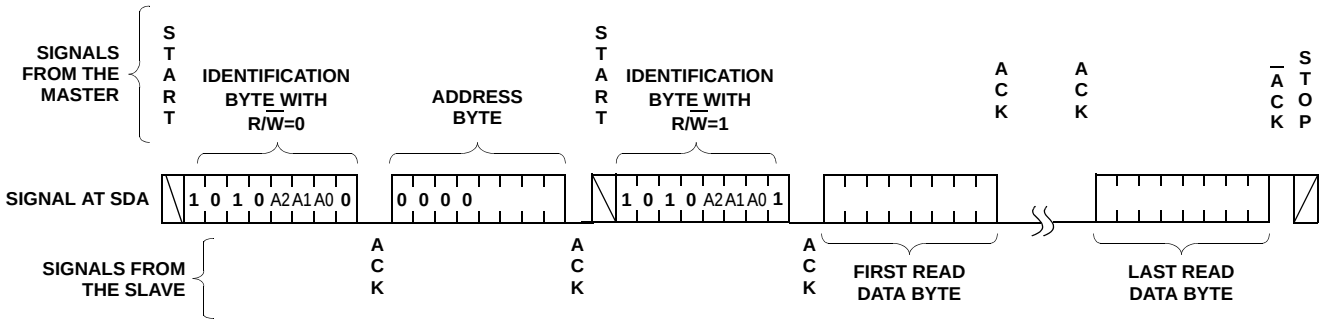


FIGURE 19. READ SEQUENCE

Write Operation

A Write operation requires a START condition, followed by a valid Identification Byte, a valid Address Byte, a Data Byte, and a STOP condition. After each of the three bytes, the ISL22326 responds with an ACK. At this time, the device enters its standby state (See Figure 18). Device can receive more than one byte of data by auto incrementing the address after each received byte. Note after reaching the address 08h, the internal pointer “rolls over” to address 00h. The non-volatile write cycle starts after STOP condition is determined and it requires up to 20ms delay for the next non-volatile write. Thus, non-volatile registers must be written individually.

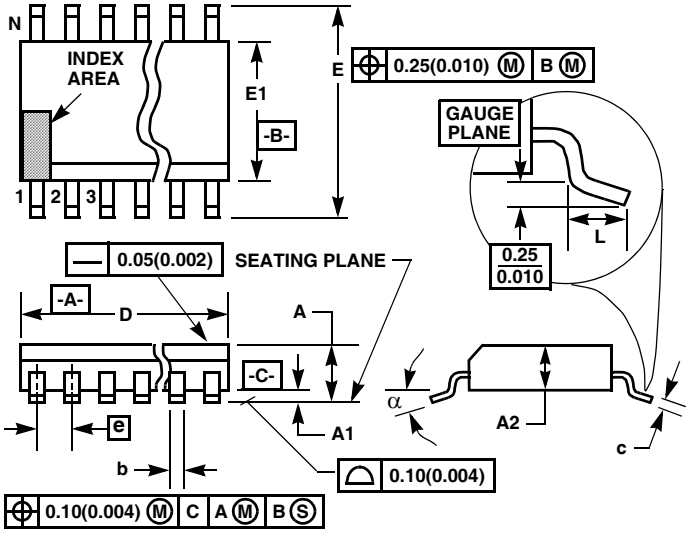
Read Operation

A Read operation consist of a three byte instruction followed by one or more Data Bytes (See Figure 19). The master initiates the operation issuing the following sequence: a START, the Identification byte with the R/$\overline{W}$ bit set to “0”, an Address Byte, a second START, and a second Identification byte with the R/$\overline{W}$ bit set to “1”. After each of the three bytes, the ISL22326 responds with an ACK. Then the ISL22326 transmits Data Bytes as long as the master responds with an ACK during the SCL cycle following the eighth bit of each byte. The master terminates the read operation (issuing a $\overline{ACK}$ and a STOP condition) following the last bit of the last Data Byte (See Figure 19).

The Data Bytes are from the registers indicated by an internal pointer. This pointer initial value is determined by the Address Byte in the Read operation instruction, and increments by one during transmission of each Data Byte. After reaching the memory location 08h, the pointer “rolls over” to 00h, and the device continues to output data for each ACK received.

In order to read back the non-volatile IVR, it is recommended that the application reads the ACR first to verify the WIP bit is 0. If the WIP bit (ACR[5]) is not 0, the host should repeat its reading sequence again.

Thin Shrink Small Outline Plastic Packages (TSSOP)



NOTES:

1. These package dimensions are within allowable dimensions of JEDEC MO-153-AC, Issue E.
2. Dimensioning and tolerancing per ANSI Y14.5M-1982.
3. Dimension “D” does not include mold flash, protrusions or gate burrs. Mold flash, protrusion and gate burrs shall not exceed 0.15mm (0.006 inch) per side.
4. Dimension “E1” does not include interlead flash or protrusions. Interlead flash and protrusions shall not exceed 0.15mm (0.006 inch) per side.
5. The chamfer on the body is optional. If it is not present, a visual index feature must be located within the crosshatched area.
6. “L” is the length of terminal for soldering to a substrate.
7. “N” is the number of terminal positions.
8. Terminal numbers are shown for reference only.
9. Dimension “b” does not include dambar protrusion. Allowable dambar protrusion shall be 0.08mm (0.003 inch) total in excess of “b” dimension at maximum material condition. Minimum space between protrusion and adjacent lead is 0.07mm (0.0027 inch).
10. Controlling dimension: MILLIMETER. Converted inch dimensions are not necessarily exact. (Angles in degrees)

M14.173

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SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	-	0.047	-	1.20	-
A1	0.002	0.006	0.05	0.15	-
A2	0.031	0.041	0.80	1.05	-
b	0.0075	0.0118	0.19	0.30	9
c	0.0035	0.0079	0.09	0.20	-
D	0.195	0.199	4.95	5.05	3
E1	0.169	0.177	4.30	4.50	4
e	0.026 BSC		0.65 BSC		-
E	0.246	0.256	6.25	6.50	-
L	0.0177	0.0295	0.45	0.75	6
N	14		14		7
α	0^o	8^o	0^o	8^o	-

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