Micropower, Single Supply, Rail-to-Rail Input and Output (RRIO) Instrumentation Amplifier

The ISL28270 and ISL28273 are dual channel micropower instrumentation amplifiers (in-amps) and the ISL28470 is a Quad-channel in-amp optimized for low 2.4V to 5V single supplies.

All three devices feature an Input Range Enhancement Circuit (IREC) which maintains CMRR performance for input voltages equal to the positive supply and down to 50mV above the negative supply rail. The input signal is capable of swinging above the positive supply rail and to 10mV above the negative supply with only a slight degradation of the CMRR performance. The output operation is rail to rail.

The ISL28273 is compensated for a minimum gain of 10 or more. For higher gain applications, the ISL28270 and ISL28470 are compensated for a minimum gain of 100. The in-amps have bipolar input devices for best offset and excellent 1/f noise performance. The amplifiers can be operated from one lithium cell or two Ni-Cd batteries.

Ordering Information

PART NUMBER (Note)	PART MARKING	TAPE & REEL	PACKAGE (Pb-Free)	PKG. DWG. #
ISL28270IAZ (Note)	28270 IAZ	97/Tube	16 Ld QSOP (Pb-free)	MDP0040
ISL28270IAZ-T13 (Note)	28270 IAZ	13” (1k pcs)	16 Ld QSOP (Pb-free)	MDP0040
Coming Soon ISL28273FAZ (Note)	28273 FAZ	97/Tube	16 Ld QSOP (Pb-free)	MDP0040
Coming Soon ISL28273FAZ-T7 (Note)	28273 FAZ	7” (1k pcs)	16 Ld QSOP (Pb-free)	MDP0040
ISL28470FAZ (Note)	ISL28470FAZ	48/Tube	28 Ld QSOP (Pb-free)	M28.15
ISL28470FAZ-T7 (Note)	ISL28470FAZ	7” (1k pcs)	28 Ld QSOP (Pb-free)	M28.15
ISL28270INEVAL1Z (Note)	Evaluation Platform			
ISL28273INEVAL1Z	Evaluation Platform			
Coming Soon ISL28470EVAL1Z	Evaluation Platform			

NOTE: Intersil Pb-free plus anneal products employ special Pb-free material sets; molding compounds/die attach materials and 100% matte tin plate termination finish, which are RoHS compliant and compatible with both SnPb and Pb-free soldering operations. Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.

Features

- 60µA supply current per channel ISL28270
- 150µV max offset voltage
- 2nA max input bias current ISL28270
- 110dB CMRR, PSRR
- 0.7µV/°C offset voltage temperature coefficient
- 240kHz -3dB bandwidth (G = 100) ISL28270, ISL28470
- 230kHz -3dB bandwidth (G = 10) ISL28273
- 0.5V/µs slew rate
- Single supply operation
- Rail-to-rail input and output (RRIO)
- Input is capable of swinging above V+ and below V- (ground sensing)
- Output sources and sinks ±29mA load current
- 0.5% gain error
- Pb-free plus anneal available (RoHS compliant)

Applications

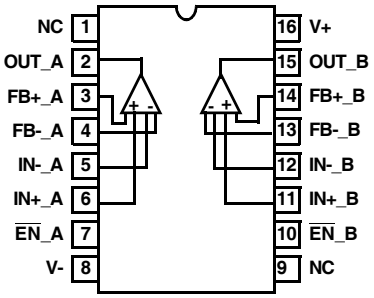
- Battery or solar-powered systems
- Strain gauge
- Sensor signal conditioning
- Medical devices
- Industrial instrumentations

Related Literature

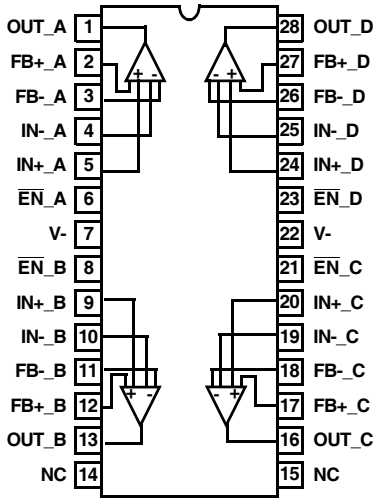
- AN1290, ISL2827xINEVAL1Z Evaluation Board User’s Guide
- AN1298, Instrumentation Amplifier Application Note

Pinouts

ISL28270, ISL28273
(16 LD QSOP)
TOP VIEW



ISL28470
(28 LD QSOP)
TOP VIEW



Absolute Maximum Ratings (T_A = +25°C)

Supply Voltage 5.5V
Supply Turn On Voltage Slew Rate 1V/µs
Input Current (IN, FB) ISL28270, ISL28470 . . . . . 5mA
Differential Input Voltage (IN, FB) ISL28270, ISL28470 . . . . . 0.5V
Input Current (IN, FB) ISL28273 . . . . . 5mA
Differential Input (IN, FB) Voltage ISL28273 . . . . . 1.0V
Input Voltage . . . . . V- - 0.5V to V+ + 0.5V
ESD Tolerance
Human Body Model 3kV
Machine Model 300V

Thermal Information

Thermal Resistance	θ_{JA} (°C/W)
16 Ld QSOP Package	112
28 Ld QSOP Package	79

Output Short-Circuit Duration . . . . . .Indefinite
Ambient Operating Temperature Range . . . . . .-40°C to +125°C
Storage Temperature Range . . . . . .-65°C to +150°C
Operating Junction Temperature . . . . . .+125°C
Pb-free reflow profile . . . . . .see link below
http://www.intersil.com/pbfree/Pb-FreeReflow.asp

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

IMPORTANT NOTE: All parameters having Min/Max specifications are guaranteed. Typical values are for information purposes only. Unless otherwise noted, all tests are at the specified temperature and are pulsed tests, therefore: $T_J = T_C = T_A$

Electrical Specifications

V_+ = +5V, V_M = GND, V_{CM} = 1/2V_+, T_A = +25°C, unless otherwise specified. **Boldface limits apply over the operating temperature range, -40°C to +125°C**.

PARAMETER	DESCRIPTION	CONDITIONS		MIN	TYP	MAX	UNIT
V_{OS}	Input Offset Voltage	ISL28270, ISL28470		-150 **-225**	±35	150 **225**	µV
		ISL28273			TBD		µV
TCV_{OS}	Input Offset Voltage Temperature Coefficient	Temperature = -40°C to +125°C			0.7		µV/°C
I_{OS}	Input Offset Current between IN+ and IN-, and between FB+ and FB-	ISL28270		-1 **-1.5**	±0.25	1 **1.5**	nA
		ISL28470		-1.5 **-2.0**	±0.25	1.5 **2**	nA
		ISL28273			TBD		nA
I_B	Input Bias Current (IN+, IN-, FB+, and FB- terminals)	ISL28270		-2.0 **-2.5**	±0.5	2.0 **2.5**	nA
		ISL28470		-2.5 **-3.0**	±0.5	2.5 **3.0**	nA
		ISL28273			TBD		nA
e_N	Input Noise Voltage	ISL28270, ISL28470	f = 0.1Hz to 10Hz		3.5		μV_{P-P}
		ISL28273			3.5		μV_{P-P}
	Input Noise Voltage Density	ISL28270, ISL28470	f_0 = 1kHz		60		nV/√Hz
		ISL28273			210		nV/√Hz
i_N	Input Noise Current Density	ISL28270, ISL28470	f_0 = 1kHz		0.48		pA/√Hz
		ISL28273			0.65		pA/√Hz
R_{IN}	Input Resistance	ISL28270, ISL28470			3		MΩ
		ISL28273			15		MΩ
V_{IN}	Input Voltage Range	V_+ = 2.4V to 5.0V		0		V_+	V

Electrical Specifications V_+ = +5V, V_M = GND, V_{CM} = 1/2V_+, T_A = +25°C, unless otherwise specified. **Boldface limits apply over the operating temperature range, -40°C to +125°C. (Continued)**

PARAMETER	DESCRIPTION	CONDITIONS		MIN	TYP	MAX	UNIT
CMRR	Common Mode Rejection Ratio	ISL28270	V_{CM} = 0.05V to 5V	90 **TBD**	110		dB
		ISL28273			TBD		dB
		ISL28470		90 **85**	110		dB
PSRR	Power Supply Rejection Ratio	ISL28270	V_+ = 2.4V to 5V	90 **TBD**	110		dB
		ISL28273			TBD		dB
		ISL28470		90 **65**	110		dB
E_G	Gain Error	ISL28270, ISL28470	R_L = 100kΩ to 2.5V		+0.5		%
		ISL28273			TBD		%
V_{OUT}	Maximum Voltage Swing	Output low, 100kΩ to 2.5V			4	10	mV
		Output low, 1kΩ to 2.5V			130	250 **300**	mV
		Output high, 100kΩ to 2.5V		4.990	4.996		V
		Output high, 1kΩ to GND		4.75 **4.70**	4.88		V
SR	Slew Rate	R_L = 1kΩ to GND		0.3 **0.25**	0.5	0.7 **0.75**	V/µs
-3dB BW	-3dB Bandwidth	ISL28270, ISL28470	Gain = 100		240		kHz
			Gain = 200		84		kHz
			Gain = 500		30		kHz
			Gain = 1000		13		kHz
		ISL28273	Gain = 10		265		kHz
			Gain = 20		100		kHz
			Gain = 50		25		kHz
			Gain = 100		13		kHz
$I_{S,EN}$	Supply Current, Enabled	ISL28270 - Both A and B channels enabled, $\overline{EN}$ = V-			120	156 **195**	µA
		ISL28470 - A, B, C and D channels enabled, $\overline{EN}$ = V-			260	335	µA
$I_{S,DIS}$	Supply Current, Disabled	ISL28270 - Both A and B channels disabled, $\overline{EN}$ = V+			4	7 **9**	µA
		ISL28470 - A, B, C and D channels disabled, $\overline{EN}$ = V+			10	12 **15**	µA
V_{ENH}	$\overline{EN}$ Pin for Shut-down			**2**			V
V_{ENL}	$\overline{EN}$ Pin for Power-On					**0.8**	V
I_{ENH}	$\overline{EN}$ Input Current High	$\overline{EN}$ = V+			0.8	1 **1.3**	µA
I_{ENL}	$\overline{EN}$ Input Current Low	$\overline{EN}$ = V-			26	50 **100**	nA
V_+	Minimum Supply Voltage			**2.4**			V

Electrical Specifications V_+ = +5V, V_M = GND, V_{CM} = 1/2V_+, T_A = +25°C, unless otherwise specified. **Boldface limits apply over the operating temperature range, -40°C to +125°C. (Continued)**

PARAMETER	DESCRIPTION	CONDITIONS	MIN	TYP	MAX	UNIT
I_{SC}	Short Circuit Output Current	V_+ = 5V, R_{LOAD} = 10Ω	±20 **±18**	±29		mA
		V_+ = 2.4V, R_{LOAD} = 10Ω		±8		mA

Typical Performance Curves

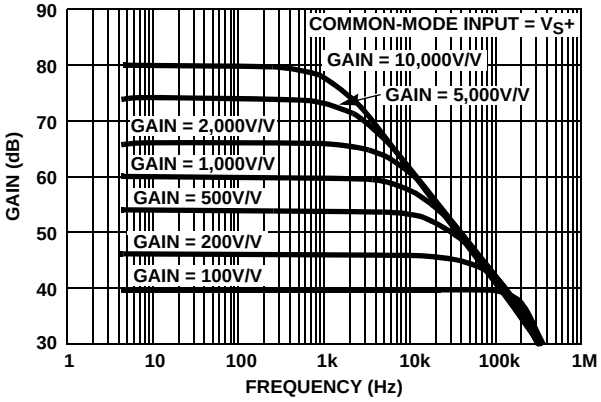


FIGURE 1. ISL28270, ISL28470 FREQUENCY RESPONSE vs CLOSED LOOP GAIN (V+ = V_{CM} = 5V)

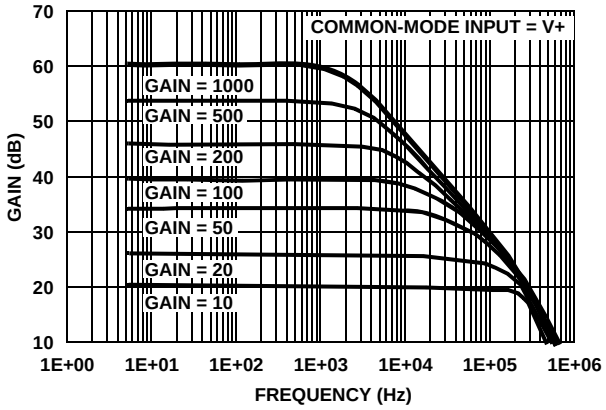


FIGURE 2. ISL28273 FREQUENCY RESPONSE vs CLOSED LOOP GAIN (V_{CM} = V+)

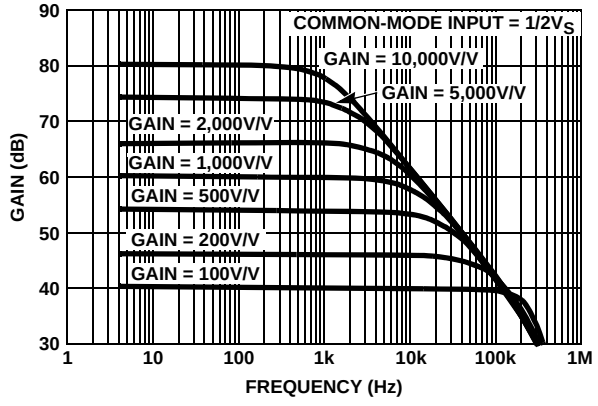


FIGURE 3. ISL28270, ISL28470 FREQUENCY RESPONSE vs CLOSED LOOP GAIN (V+ = 5V, V_{CM} = 1/2V+)

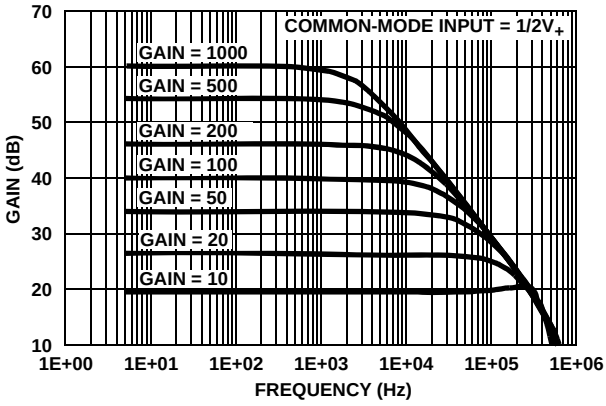


FIGURE 4. ISL28273 FREQUENCY RESPONSE vs CLOSED LOOP GAIN (V_{CM} = 1/2V+)

Typical Performance Curves (Continued)

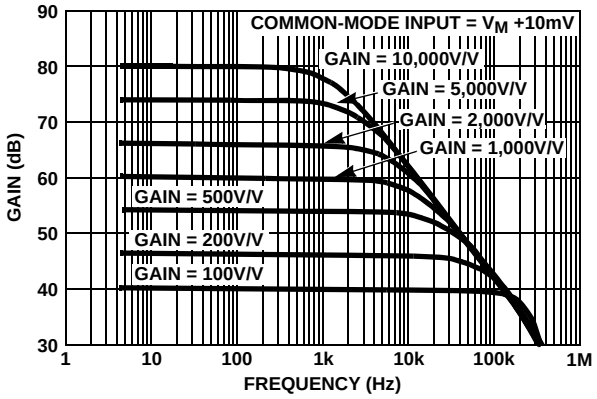


FIGURE 5. ISL28270, ISL28470 FREQUENCY RESPONSE vs CLOSED LOOP GAIN (V+ = 5V, V_{CM} = 10mV)

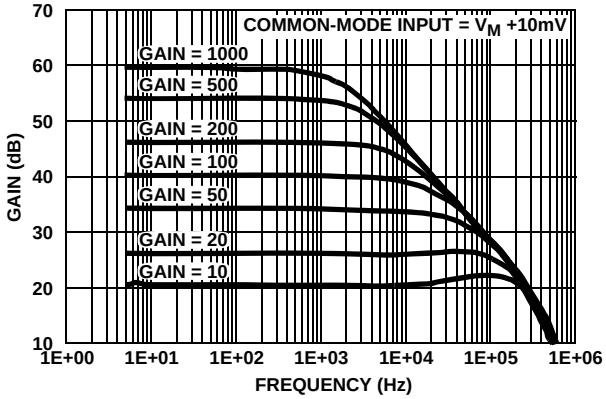


FIGURE 6. ISL28273 FREQUENCY RESPONSE vs CLOSED LOOP GAIN (VCM = V-)

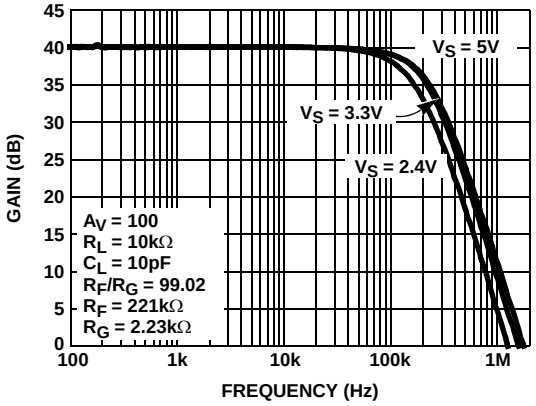


FIGURE 7. ISL28270, ISL28470 FREQUENCY RESPONSE vs SUPPLY VOLTAGE

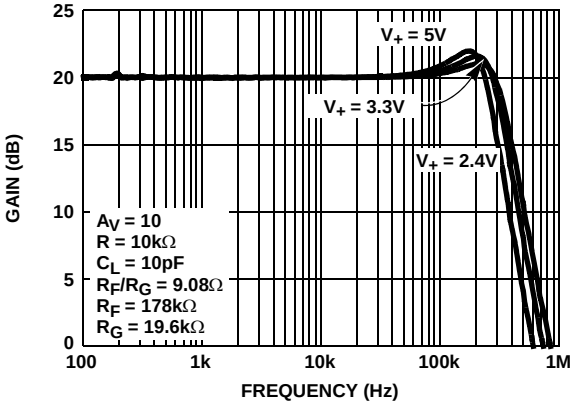


FIGURE 8. ISL28273 FREQUENCY RESPONSE vs SUPPLY VOLTAGE

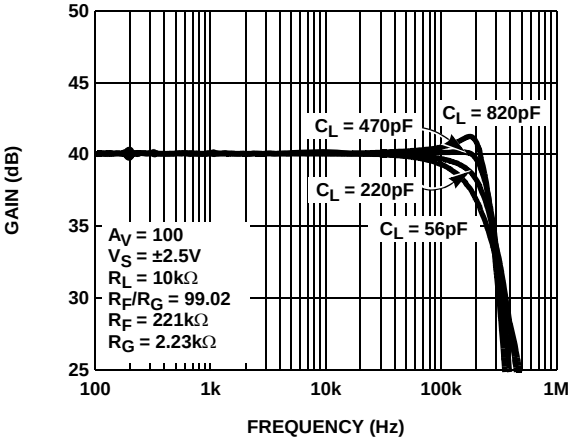


FIGURE 9. ISL28270, ISL28470 FREQUENCY RESPONSE vs C_{LOAD}

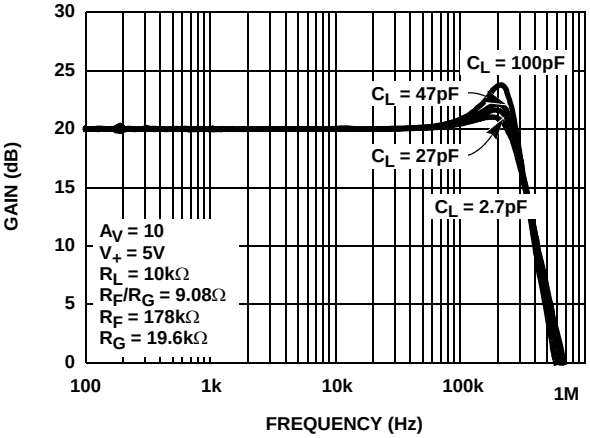


FIGURE 10. ISL28273 FREQUENCY RESPONSE vs C_{LOAD}

Typical Performance Curves (Continued)

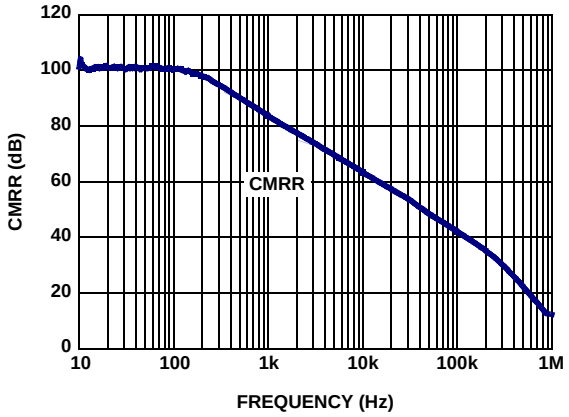


FIGURE 11. ISL28270, ISL28470 CMRR vs FREQUENCY

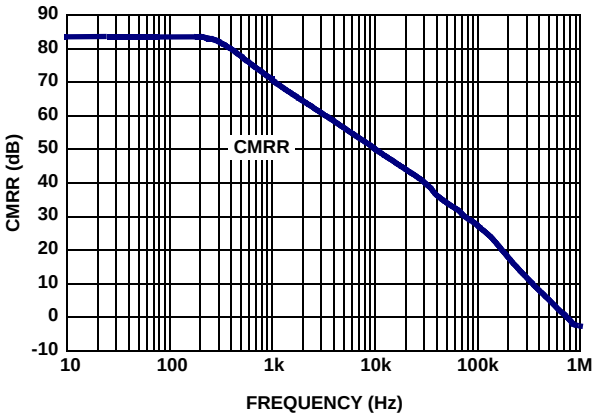


FIGURE 12. ISL28273 CMRR vs FREQUENCY

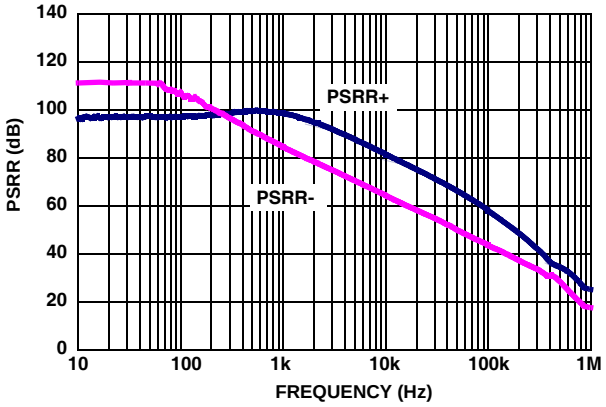


FIGURE 13. ISL28270, ISL28470 PSRR vs FREQUENCY

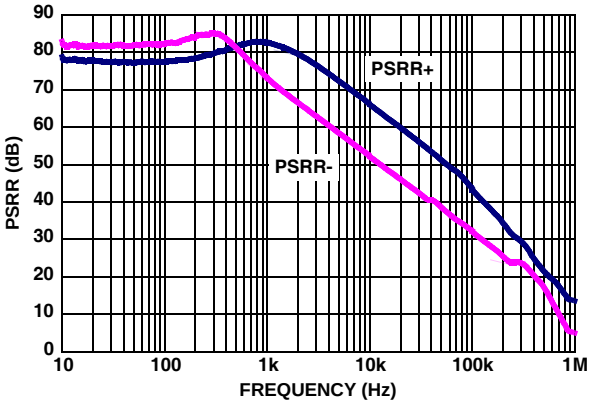


FIGURE 14. ISL28273 PSRR vs FREQUENCY

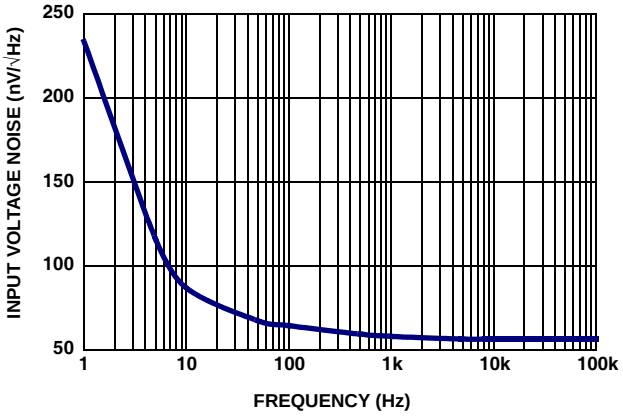


FIGURE 15. ISL28270, ISL28470 INPUT VOLTAGE NOISE SPECTRAL DENSITY (GAIN = 100)

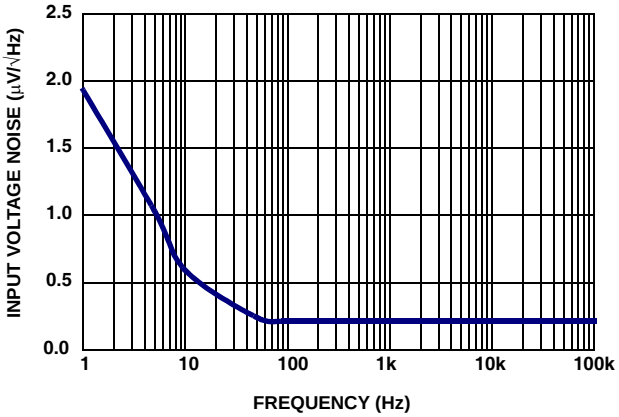


FIGURE 16. ISL28273 INPUT VOLTAGE NOISE SPECTRAL DENSITY (GAIN = 10)

Typical Performance Curves (Continued)

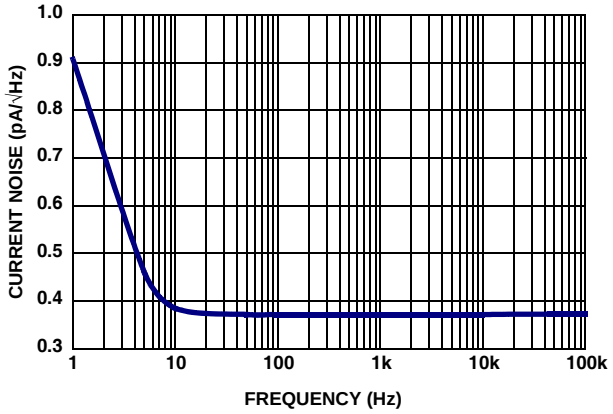


FIGURE 17. ISL28270, ISL28470 INPUT CURRENT NOISE SPECTRAL DENSITY (GAIN = 100)

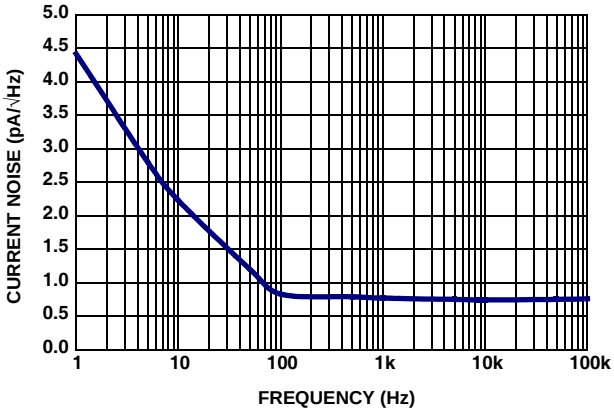


FIGURE 18. ISL28273 INPUT CURRENT NOISE SPECTRAL DENSITY (GAIN = 10)

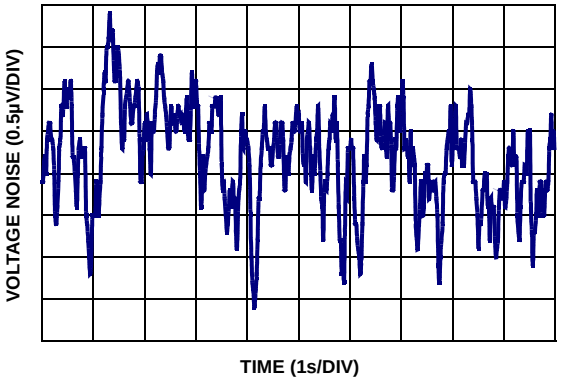


FIGURE 19. ISL28270, ISL28470 0.1 Hz TO 10Hz INPUT VOLTAGE NOISE (GAIN = 100)

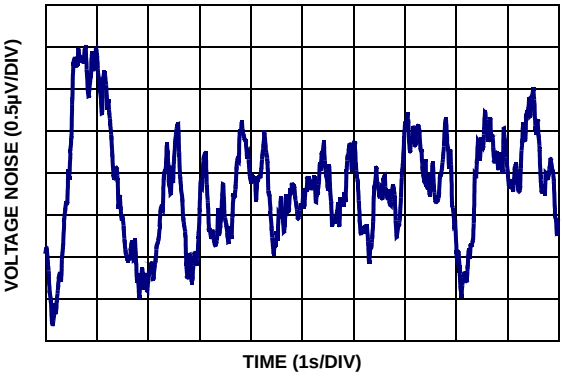


FIGURE 20. ISL28273 0.1 Hz TO 10Hz INPUT VOLTAGE NOISE (GAIN = 10)

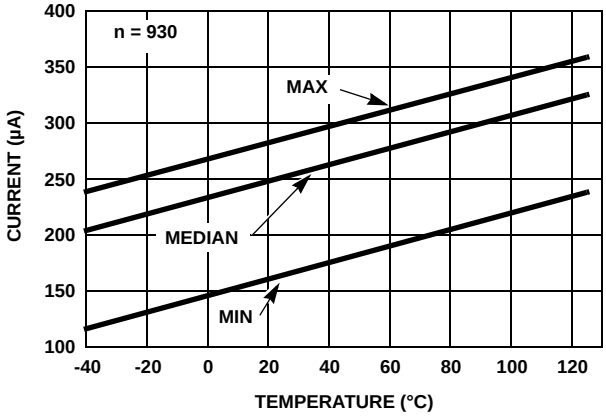


FIGURE 21. SUPPLY CURRENT vs TEMPERATURE V_S = ±2.5V ENABLED (R_L = INF)

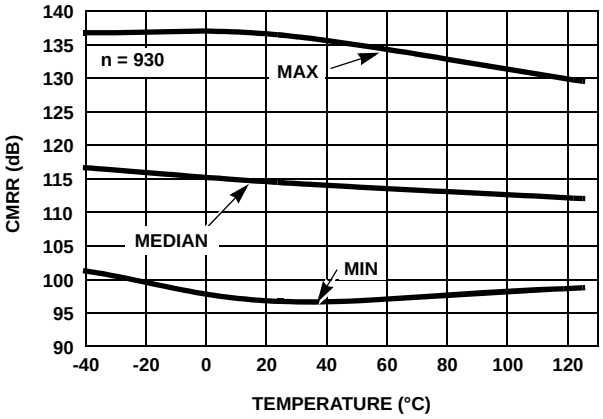


FIGURE 22. CMRR vs TEMPERATURE (V_{CM} = +2.5V TO -2.5V)

Typical Performance Curves (Continued)

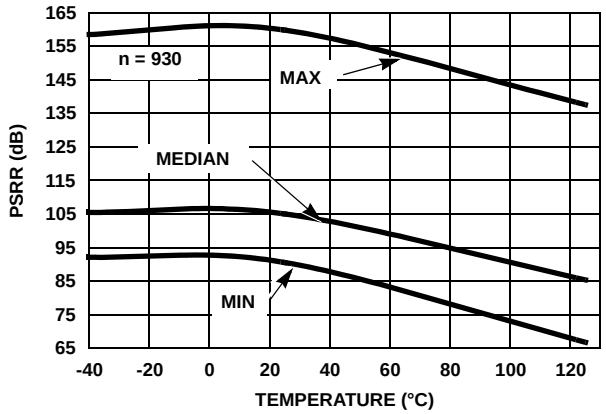


FIGURE 23. PSRR vs TEMPERATURE (V_S = ±2.5V)

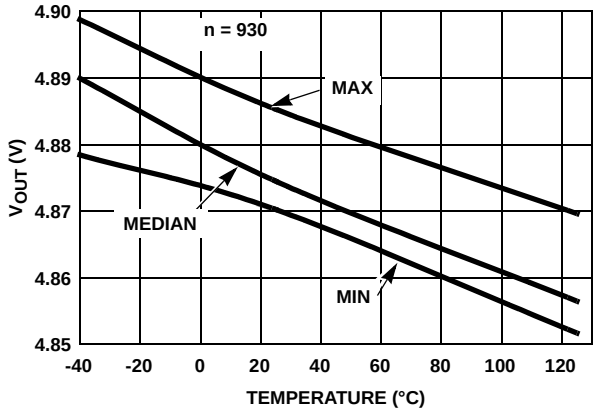


FIGURE 24. POSITIVE V_{OUT} vs TEMPERATURE (R_L = 1k, V_S = ±2.5V)

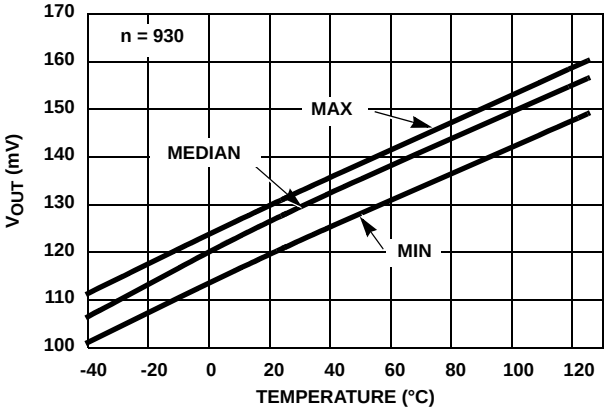


FIGURE 25. NEGATIVE V_{OUT} vs TEMPERATURE (R_L = 1k, V_S = ±2.5V)

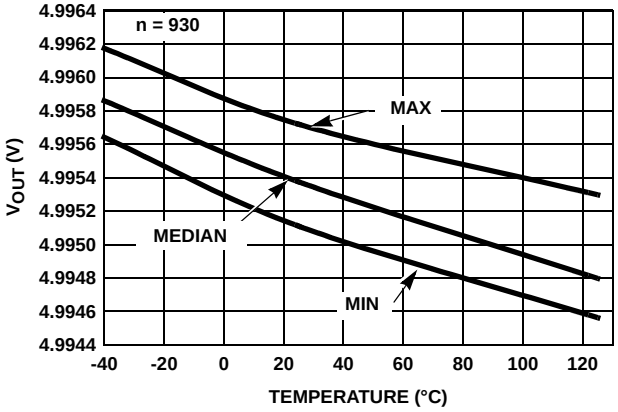


FIGURE 26. POSITIVE V_{OUT} vs TEMPERATURE (R_L = 100k, V_S = ±2.5V)

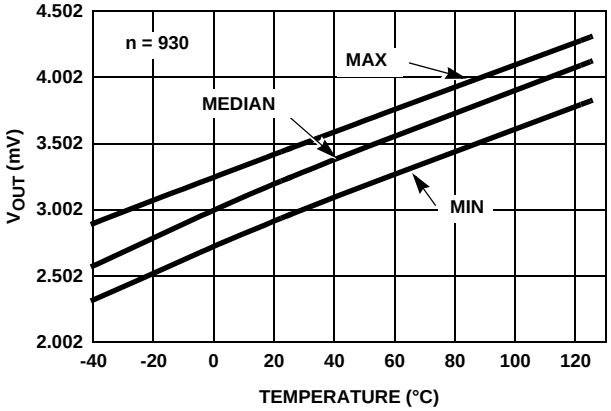
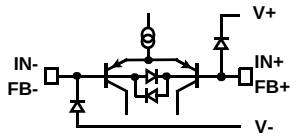


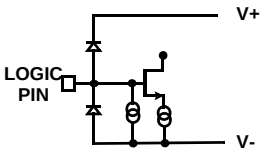
FIGURE 27. NEGATIVE V_{OUT} vs TEMPERATURE (R_L = 100k, V_S = ±2.5V)

Pin Descriptions

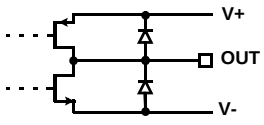
ISL28270 16 Ld QSOP	ISL28273 16 Ld QSOP	ISL28470 28 Ld QSOP	PIN NAME	EQUIVALENT CIRCUIT	PIN FUNCTION
2, 15	2, 15	1, 13 16, 28	OUT_A,B C_D	Circuit 3	Output Voltage. A complementary Class AB common-source output stage drives the output of each channel. When disabled, the outputs are in a high impedance state
3, 14	3, 14	2, 12 17, 27	FB+_A,B C_D	Circuit 1A, Circuit 1B	Positive Feedback high impedance terminals. ISL28270 and ISL28470 input circuit is shown in Circuit 1A, and the ISL28273 input circuit is shown in Circuit 1B. ISL28273: to avoid offset drift, it is recommended that the terminals of the ISL28273 are not overdriven beyond 1V and the input current must never exceed 5mA.
4, 13	4, 13	3, 11 18, 26	FB-_A,B C_D	Circuit 1A, Circuit 1B	Negative Feedback high impedance terminals. The FB- pins connect to an external resistor divider to individually set the desired gain of the in-amp. ISL28270 and ISL28470 input circuit is shown in Circuit 1A, and the ISL28273 input circuit is shown in Circuit 1B. ISL28273: to avoid offset drift, it is recommended that the terminals of the ISL28273 are not overdriven beyond 1V and the input current must never exceed 5mA.
5, 12	5, 12	4, 10 19, 25	IN-_A,B C_D	Circuit 1A, Circuit 1B	High impedance Inverting input terminals. Connect to the low side of the input source signal. ISL28270 and ISL28470 input circuit is shown in Circuit 1A, and the ISL28273 input circuit is shown in Circuit 1B. ISL28273: to avoid offset drift, it is recommended that the terminals of the ISL28273 are not overdriven beyond 1V and the input current must never exceed 5mA.
6, 11	6, 11	5, 9 20, 24	IN+_A,B C_D	Circuit 1A, Circuit 1B	High impedance Non-inverting input terminals. Connect to the high side of the input source signal. ISL28270 and ISL28470 input circuit is shown in Circuit 1A, and the ISL28273 input circuit is shown in Circuit 1B. ISL28273: to avoid offset drift, it is recommended that the terminals of the ISL28273 are not overdriven beyond 1V and the input current must never exceed 5mA.
7, 10	7, 10	6, 8 21, 23	$\overline{EN}$_A,B C_D	Circuit 2	Active LOW logic pins. When pulled above 2V, the corresponding channel turns off and OUT is high impedance. A channel is enabled when pulled below 0.8V. Built-in pull downs define each $\overline{EN}$ pin LOW when left floating.
16	16	7	V_+	Circuit 4	Positive Supply terminal shared by all channels.
8	8	22	V-	Circuit 4	Negative Supply terminal shared by all channels. Grounded for single supply operation.
1, 9	1, 9	14,15	NC		No Connect, pins can be left floating or grounded



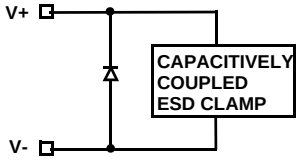
CIRCUIT 1A



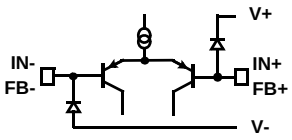
CIRCUIT 2



CIRCUIT 3



CIRCUIT 4



CIRCUIT 1B

Application Information

Product Description

The ISL28270 and ISL28273 are dual channel micropower instrumentation amplifiers (in-amps) and the ISL28470 is a Quad-channel which delivers rail-to-rail input amplification and rail-to-rail output swing. The in-amps also deliver excellent DC and AC specifications while consuming only about 60µA per channel. Because the independent pair of feedback terminals set the gain and adjust the output 0 level, the ISL28270, ISL28273 and ISL28470 achieve high CMRR regardless of the tolerance of the gain setting resistors. The ISL28270 and ISL28470 are internally compensated for a minimum gain of 100. The ISL28273 is internally compensated for a minimum gain of 10.

$\overline{EN}$ pins are available to independently enable or disable a channel. When all channels are off, current consumption is down to typically 4µA.

Input Protection

All input terminals and feedback terminals have internal ESD protection diodes to both positive and negative supply rails, limiting the input voltage to within one diode beyond the supply rails. Input signals originating from low impedance sources should have current limiting resistors in series with the IN+ and IN- pins to prevent damaging currents during power supply sequencing and other transient conditions. The ISL28270 and ISL28470 have additional back-to-back diodes across the input terminals and also across the feedback terminals. If overdriving the inputs is necessary, the external input current must never exceed 5mA. External series resistors may be used as an external protection to limit excessive external voltage and current from damaging the inputs. On the other hand, the ISL28273 has no clamps to limit the differential voltage on the input terminals allowing higher differential input voltages at lower gain applications. It is recommended, however, that the terminals of the ISL28273 are not overdriven beyond 1V to avoid offset drift.

Input Stage and Input Voltage Range

The input terminals (IN+ and IN-) of the in-amps are a single differential pair of bipolar PNP devices aided by an Input Range Enhancement Circuit (IREC), to increase the headroom of operation of the common-mode input voltage. The feedback terminals (FB+ and FB-) also have a similar topology. As a result, the input common-mode voltage range is rail-to-rail regardless of the feedback terminal settings and regardless of the gain settings. They are able to handle input voltages that are at or slightly beyond the supply and close to ground making these in-amps well suited for single 5V down to 2.4V supply systems. There is no need to bias the common-mode input to achieve symmetrical input voltage. It is recommended, however, that the common-mode input be biased at least 10mV above the negative supply rail to achieve top performance. See “Input Bias Cancellation/Compensation” on page 11.

The IREC enables rail-to-rail input amplification without the problems usually associated with the dual differential stage topology. The IREC ensures that there are no drastic changes in offset voltage over the entire range of the input. See Input Offset Voltage vs Common-Mode Input Voltage in performance charts. IREC also cures the abrupt change and even reverse polarity of the input bias current over the whole range of input.

Input Bias Cancellation/Compensation

All three parts have an Input Bias Cancellation/Compensation Circuit for both the input and feedback terminals (IN+, IN-, FB+ and FB-), achieving a low input bias current throughout the input common-mode range and the operating temperature range. While the PNP bipolar input stages are biased with an adequate amount of biasing current for speed and increased noise performance, the Input Bias Cancellation/Compensation Circuit sinks most of the base current of the input transistors leaving a small portion as input bias current, typically 500pA. In addition, the Input Bias Cancellation/Compensation Circuit maintains a smooth and flat behavior of input bias current over the common mode range and over the operating temperature range. The Input Bias Cancellation/Compensation Circuit operates from input voltages of 10mV above the negative supply to input voltages slightly above the positive supply.

Output Stage and Output Voltage Range

A Class AB common-source output stage drives the output. The pair of complementary MOSFET devices drive the output VOUT to within a few millivolts of the supply rails. At a 100kΩ load, the PMOS sources current and pulls the output up to 4mV below the positive supply. The NMOS sinks current and pulls the output down to 4mV above the negative supply, or ground in the case of a single supply operation. The current sinking and sourcing capability are internally limited to 29mA. When disabled, the outputs are in a high impedance state.

Gain Setting

VIN (the potential difference across IN+ and IN-), is replicated (less the input offset voltage) across FB+ and FB-. The function of the in-amp is to maintain the differential voltage across FB- and FB+ equal to IN+ and IN-; (FB- - FB+) = (IN+ - IN-). Consequently, the transfer function can be derived. The in-amp gain is set by two external resistors, the feedback resistor RF, and the gain resistor RG.

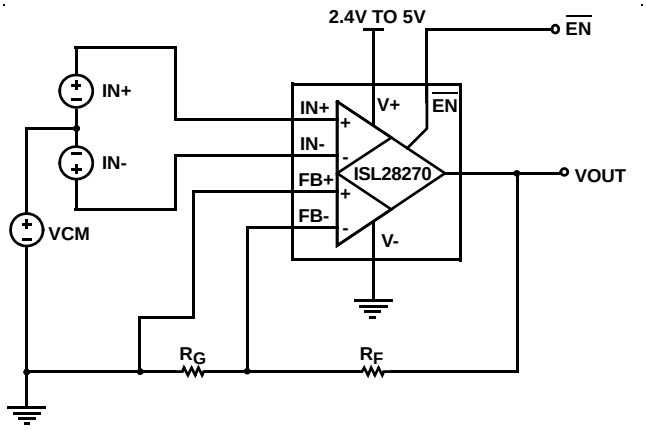


FIGURE 28. GAIN IS SET BY TWO EXTERNAL RESISTORS, R_F AND R_G

$$V_{IN} = IN+ - IN-$$

$$V_{OUT} = \left(1 + \frac{R_F}{R_G}\right) V_{IN} \quad \text{(EQ. 1)}$$

In Figure 28, the FB+ pin and one end of resistor RG are connected to GND. With this configuration, the gain equation (Equation 1) is only true for a positive swing in VIN; negative input swings will be ignored because the output will be at ground.

Reference Connection

Unlike a three op-amp in-amp realization, a finite series resistance seen at the REF terminal does not degrade the high CMRR performance, eliminating the need for an additional external buffer amplifier. Figure 29 uses the FB+ pin to provide a high impedance REF terminal.

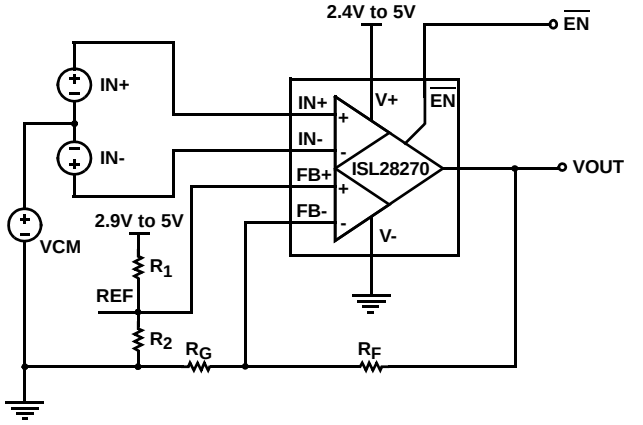


FIGURE 29. GAIN SETTING AND REFERENCE CONNECTION

$$V_{IN} = IN+ - IN-$$

$$V_{OUT} = \left(1 + \frac{R_F}{R_G}\right)(V_{IN}) + \left(1 + \frac{R_F}{R_G}\right)(V_{REF}) \quad \text{(EQ. 2)}$$

The FB+ pin is used as a REF terminal to center or to adjust the output. Because the FB+ pin is a high impedance input, an economical resistor divider can be used to set the voltage at the REF terminal without degrading or affecting the CMRR performance. Any voltage applied to the REF terminal will shift V_{OUT} by V_{REF} times the closed loop gain, which is set by resistors R_F and R_G. See Figure 29.

The FB+ pin can also be connected to the other end of resistor, R_G. See Figure 30. Keeping the basic concept that the in-amp maintains constant differential voltage across the input terminals and feedback terminals (FB- - FB+) = (IN+ - IN-), the transfer function of Figure 30 can be derived.

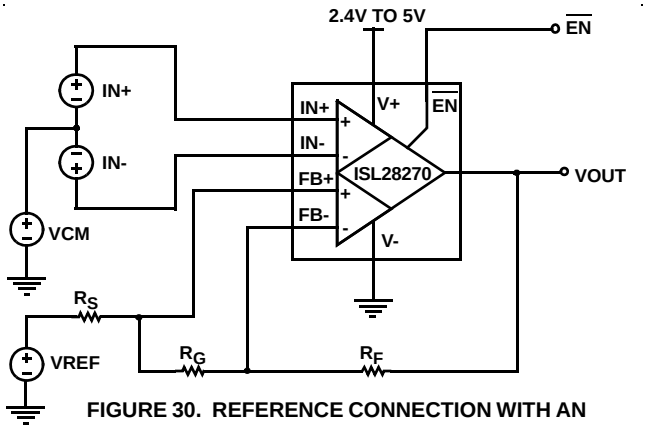


FIGURE 30. REFERENCE CONNECTION WITH AN AVAILABLE VREF

$$V_{IN} = IN+ - IN-$$

$$V_{OUT} = \left[1 + \frac{R_S + R_F}{R_G}\right] + V_{REF} \quad \text{(EQ. 3)}$$

$$V_{OUT} = \left(1 + \frac{R_F}{R_G}\right)(V_{IN}) + (V_{REF}) \quad \text{(EQ. 4)}$$

A finite resistance RS in series with the V_{REF} source, adds an output offset of $V_{IN}*(R_S/R_G)$. As the series resistance RS approaches zero, Equation 3 is simplified to Equation 4 for Figure 30. V_{OUT} is simply shifted by an amount V_{REF}.

External Resistor Mismatches

Because of the independent pair of feedback terminals provided by the in-amps, the CMRR is not degraded by any resistor mismatches. Hence, unlike a three op-amp and especially a two op-amp in-amp realization, the ISL28270, ISL28273 and ISL28470 reduce the cost of external components by allowing the use of 1% or more tolerance resistors without sacrificing CMRR performance. The CMRR will be typically 110dB regardless of the tolerance of the resistors used. Instead, a resistor mismatch results in a higher deviation from the theoretical gain - gain Error.

Gain Error and Accuracy

The gain error indicated in the “Electrical Specifications” Table on page 3 is the inherent gain error alone. The gain error specification listed does not include the gain error contributed by the resistors. There is an additional gain error

due to the tolerance of the resistors used. The resulting non-ideal transfer function effectively becomes Equation 5:

$$V_{OUT} = \left(1 + \frac{R_F}{R_G}\right) \times [1 \pm (E_{RG} + E_{RF} + E_G)] \times V_{IN} \quad \text{(EQ. 5)}$$

Where:

E_{RG} = Tolerance of RG

E_{RF} = Tolerance of RF

E_G = Gain Error of the ISL28270

The term [1 - (E_{RG} +E_{RF} +E_G)] is the deviation from the theoretical gain. Thus, (E_{RG} +E_{RF} +E_G) is the total gain error. For example, if 1% resistors are used, the total gain error would be as follows in Equation 6:

$$\text{TotalGainError} = \pm(E_{RG} + E_{RF} + E_G(\text{typical})) \quad \text{(EQ. 6)}$$

$$\text{TotalGainError} = \pm(0.01 + 0.01 + 0.005) = \pm 2.5\%$$

Disable/Power-Down

The ISL28270, ISL28273 and ISL28470 have an enable/disable pin for each channel. They can be powered down to reduce the supply current to typically 4µA when all channels are off. When disabled, the corresponding output is in a high impedance state. The active low $\overline{EN}$ pin has an internal pull down and hence can be left floating and the in-amp enabled by default. When the $\overline{EN}$ is connected to an external logic, the in-amp will shutdown when the $\overline{EN}$ pin is pulled above 2V, and will power up when the $\overline{EN}$ bar is pulled below 0.8V.

Unused Channels

The ISL28270, ISL28273 and ISL28470 are Dual-channel and Quad-channel op-amps. If the application only requires one channel when using the ISL28270, ISL28273 or less than 4-channels when using the ISL28470, the user must configure the unused channel(s) to prevent them from oscillating. The unused channel(s) will oscillate if the input and output pins are floating. This will result in higher than expected supply currents and possible noise injection into the channel being used. The proper way to prevent this oscillation is to short the output to the negative input and ground the positive input (as shown in Figure 31).

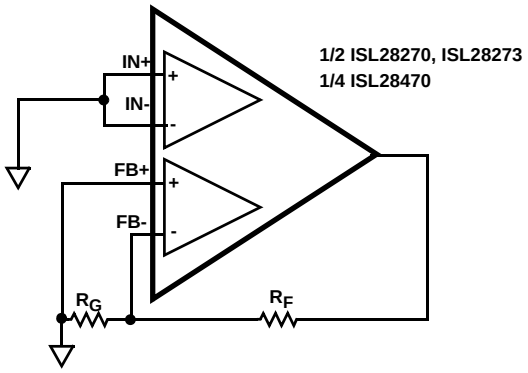
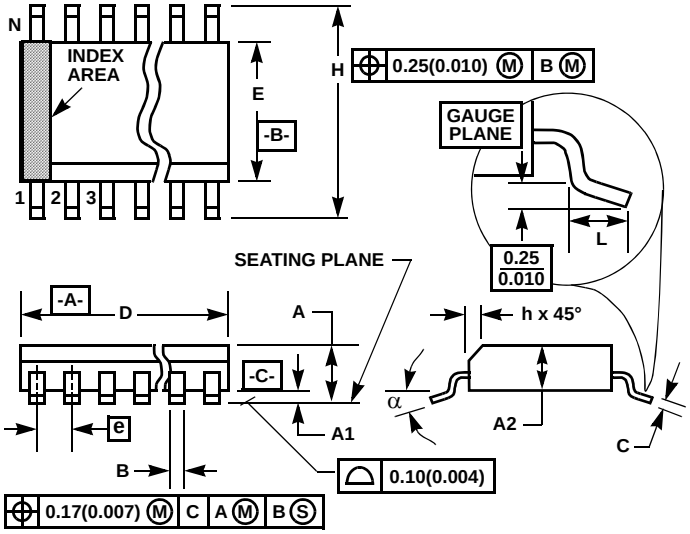


FIGURE 31. PREVENTING OSCILLATIONS IN UNUSED CHANNELS

Shrink Small Outline Plastic Packages (SSOP)
Quarter Size Outline Plastic Packages (QSOP)



NOTES:

1. Symbols are defined in the “MO Series Symbol List” in Section 2.2 of Publication Number 95.
2. Dimensioning and tolerancing per ANSI Y14.5M-1982.
3. Dimension “D” does not include mold flash, protrusions or gate burrs. Mold flash, protrusion and gate burrs shall not exceed 0.15mm (0.006 inch) per side.
4. Dimension “E” does not include interlead flash or protrusions. Interlead flash and protrusions shall not exceed 0.25mm (0.010 inch) per side.
5. The chamfer on the body is optional. If it is not present, a visual index feature must be located within the crosshatched area.
6. “L” is the length of terminal for soldering to a substrate.
7. “N” is the number of terminal positions.
8. Terminal numbers are shown for reference only.
9. Dimension “B” does not include dambar protrusion. Allowable dambar protrusion shall be 0.10mm (0.004 inch) total in excess of “B” dimension at maximum material condition.
10. Controlling dimension: INCHES. Converted millimeter dimensions are not necessarily exact.

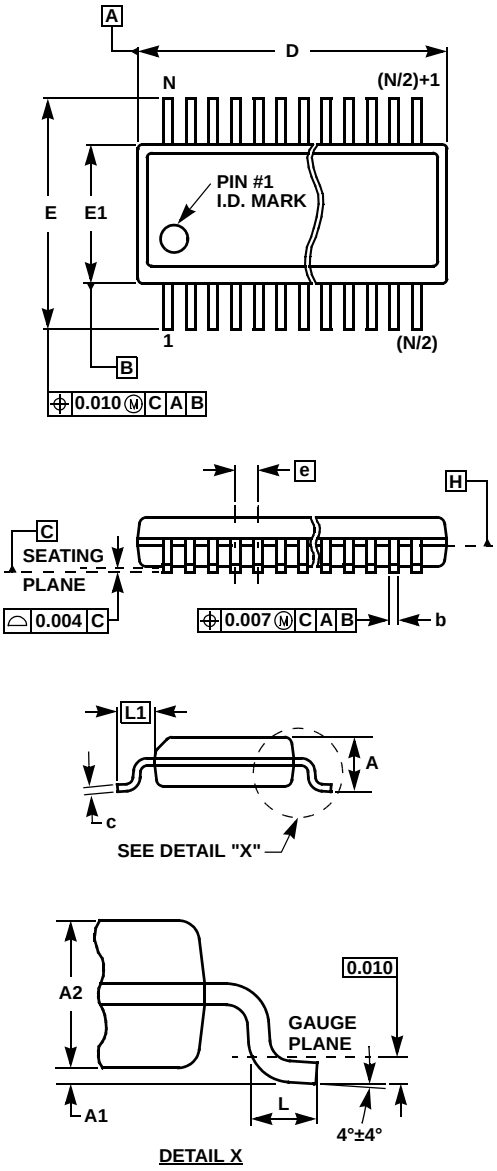
M28.15

28 LEAD SHRINK SMALL OUTLINE PLASTIC PACKAGE (0.150” WIDE BODY)

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.053	0.069	1.35	1.75	-
A1	0.004	0.010	0.10	0.25	-
A2	-	0.061	-	1.54	-
B	0.008	0.012	0.20	0.30	9
C	0.007	0.010	0.18	0.25	-
D	0.386	0.394	9.81	10.00	3
E	0.150	0.157	3.81	3.98	4
e	0.025 BSC		0.635 BSC		-
H	0.228	0.244	5.80	6.19	-
h	0.0099	0.0196	0.26	0.49	5
L	0.016	0.050	0.41	1.27	6
N	28		28		7
α	0°	8°	0°	8°	-

Rev. 1 6/04

Quarter Size Outline Plastic Packages Family (QSOP)



MDP0040

QUARTER SIZE OUTLINE PLASTIC PACKAGES FAMILY

SYMBOL	INCHES			TOLERANCE	NOTES
	QSOP16	QSOP24	QSOP28		
A	0.068	0.068	0.068	Max.	-
A1	0.006	0.006	0.006	±0.002	-
A2	0.056	0.056	0.056	±0.004	-
b	0.010	0.010	0.010	±0.002	-
c	0.008	0.008	0.008	±0.001	-
D	0.193	0.341	0.390	±0.004	1, 3
E	0.236	0.236	0.236	±0.008	-
E1	0.154	0.154	0.154	±0.004	2, 3
e	0.025	0.025	0.025	Basic	-
L	0.025	0.025	0.025	±0.009	-
L1	0.041	0.041	0.041	Basic	-
N	16	24	28	Reference	-

Rev. F 2/07

NOTES:

1. Plastic or metal protrusions of 0.006” maximum per side are not included.
2. Plastic interlead protrusions of 0.010” maximum per side are not included.
3. Dimensions “D” and “E1” are measured at Datum Plane “H”.
4. Dimensioning and tolerancing per ASME Y14.5M-1994.