IT500-IT505

IT500-IT505
Monolithic Dual Cascoded N-Channel JFET General Purpose Amplifier

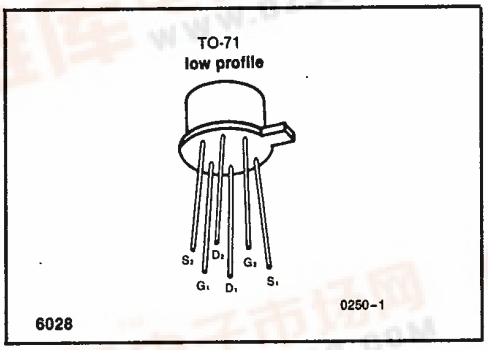
INTERSIL

T-29-27

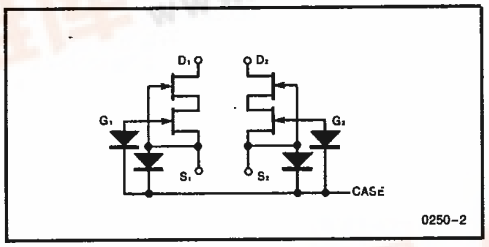
GENERAL DESCRIPTION

A low noise, low leakage FET that employs a cascode structure to accomplish very low I_G at high voltage levels, while giving high transconductance and very high common, mode rejection ratio.

PIN CONFIGURATION



SCHEMATIC DIAGRAM



FEATURES

- C_{MRR} > 120dB
- I_G < 5pA @ 50V_{DG}
- C_{rss} < 0.5pF
- g_{os} > .025μs

ABSOLUTE MAXIMUM RATINGS

(T_A = 25°C unless otherwise specified)

Drain-Source and Drain-Gate Voltages (Note 1)	60V
Drain Current (Note 1)	50mA
Gate-Gate Voltage	±60V
Storage Temperature	−65°C to +200°C
Operating Temperature	−55°C to +150°C
Lead Temperature (Soldering, 10sec)	+300°C

	One Side	Both Sides
Power Dissipation (Note 3)	250mW	500mW
Derate above 25°C	3.8mW/°C	7.7mW/°C

NOTE 1. Per transistor.
NOTE 2. Due to the non-symmetrical structure of these devices, the drain and source ARE NOT interchangeable.
NOTE 3. @ 85°C free air temp.

NOTE: *Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

ORDERING INFORMATION

TO-71
IT500
IT501
IT502
IT503
IT504
IT505

NOTE: All typical values have been characterized but are not tested.

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ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise specified)

Symbol	Characteristics	Test Conditions		Limits Min	Limits Max	Units
I_{GSS}	Gate Reverse Current	$V_{GS}=-20V$, $V_{DS}=0$, $T_A=125°C$			−100	pA
					−5	nA
BV_{GSS}	Gate-Source Breakdown Voltage	$I_G=-1\mu A$, $V_{DS}=0$		−50		V
$V_{GS(off)}$	Gate-Source Cutoff Voltage	$V_{DS}=20V$, $I_D=1nA$		−0.7	−4	V
V_{GS}	Gate-Source Voltage	$V_{DG}=35V$, $I_D=200\mu A$, $T_A=125°C$		−0.2	−3.8	V
I_G	Gate Operating Current				−5	pA
					−5	nA
I_{DSS}	Saturation Drain Current (Note 1)	$V_{DS}=20V$, $V_{GS}=0$		0.7	7	mA
g_{fs}	Common-Source Forward Transconductance (Note 1)	$V_{DS}=20V$, $V_{GS}=0$	f=1kHz	1000	4000	μs
g_{fs}	Common-Source Forward Transconductance (Note 1)	$V_{DG}=20V$, $I_D=200\mu A$	f=1kHz	500	1600	μs
g_{os}	Common-Source Output Conductance	$V_{DS}=20V$, $V_{GS}=0$	f=1kHz		1	μs
g_{os}	Common-Source Output Conductance	$V_{DS}=20V$, $I_D=200\mu A$	f=1kHz		0.025	μs
C_{g1g2}	Gate to Gate Capacitance (Note 4)	$V_{G1}=V_{G2}=10V$	f=1MHz		3.5	pF
C_{iss}	Common-Source Input Capacitance (Note 4)	$V_{DS}=20V$, $V_{GS}=0$	f=1MHz		7	pF
C_{rss}	Common-Source Reverse Transfer Capacitance (Note 3, 4)	$V_{DS}=20V$, $V_{GS}=0$	f=1MHz		0.5	pF
NF	Spot Noise Figure (Note 4)	$V_{DS}=20V$, $V_{GS}=0$	f=100Hz, $R_G=10M\Omega$		0.5	dB
$\bar{e}_n$	Equivalent Input Noise Voltage (Note 4)	$V_{DS}=20V$, $V_{GS}=0$	f=10Hz		50	$\frac{\mu V}{\sqrt{Hz}}$
		$V_{DS}=20V$, $V_{GS}=0$	f=1kHz		15	$\frac{\mu V}{\sqrt{Hz}}$

Symbol	Characteristics	Test Conditions		IT500 Min	IT500 Max	IT501 Min	IT501 Max	IT502 Min	IT502 Max	IT503 Min	IT503 Max	IT504 Min	IT504 Max	IT505 Min	IT505 Max	Units
$I_{G1}-I_{G2}$	Differential Gate Current	$V_{DG}=20V$, $I_D=200\mu A$, $T_A=125°C$			5		5		5		5		10		15	nA
$\frac{I_{DSS1}}{I_{DSS2}}$	Saturation Drain Current Ratio (Note 1)	$V_{DS}=20V$, $V_{GS}=0V$		0.95	1	0.95	1	0.95	1	0.95	1	0.9	1	0.85	1	
g_{fs1}/g_{fs2}	Transconductance Ratio (Note 1)		f=1kHz	0.97	1	0.97	1	0.95	1	0.95	1	0.90	1	0.85	1	

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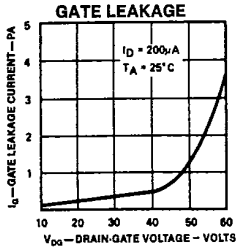
ELECTRICAL CHARACTERISTICS (Continued) (T_A = 25°C unless otherwise specified)

Symbol	Characteristics	Test Conditions		IT500		IT501		IT502		IT503		IT504		IT505		Units
				Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
$V_{GS1}-V_{GS2}$	Differential Gate-Source Voltage	V_{DG} = 20V, I_D = 200µA			5		5		10		15		25		50	mV
$\frac{\Delta V_{GS1}-V_{GS2}}{\Delta T}$	Gate-Source Differential Voltage		T_A = 25°C, T_B = 125°C		5		10		20		40		100		200	µV/°C
	Change with Temp. (Note 2, 4)		T_A = −55°C, T_B = 25°C		5		10		20		40		100		200	
C_{MRR} (Note 5)	Common Mode Rejection Ratio (Note 4)	Δ V_{DD} = 10V, I_D = 200µA		120		120		120		120		120		120		dB

NOTES: 1. Pulse test required, pulsewidth = 300µs, duty cycle ≤ 3%.
2. Measured at end points, T_A and T_B.
3. With case guarded C_{rss} is typically < 0.15pF.
4. For design reference only, not 100% tested.
5. $C_{MRR} = 20 \log_{10} \Delta V_{DD} / \Delta [V_{gs1} - V_{gs2}]$, $\Delta V_{DD} = 10/-20V$

TYPICAL PERFORMANCE CHARACTERISTICS

GATE LEAKAGE



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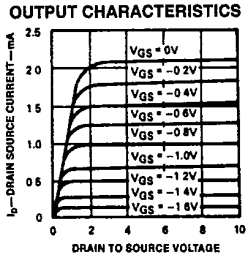
OUTPUT CHARACTERISTICS



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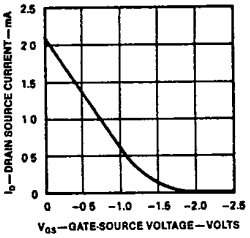
OUTPUT CHARACTERISTICS



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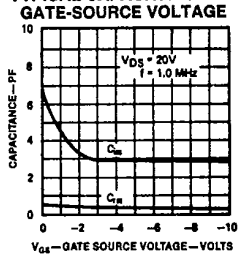
TYPICAL CAPACITANCE VS. GATE-SOURCE VOLTAGE



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