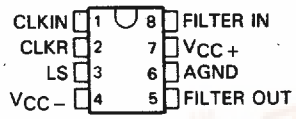
TLC04/MF4A-50, TLC14/MF4A-100
BUTTERWORTH FOURTH-ORDER LOW-PASS SWITCHED-CAPACITOR FILTERS

D2970, NOVEMBER 1986—REVISED NOVEMBER 1988

- **Low Clock-to-Cutoff-Frequency Ratio Error**
  TLC04/MF4A-50 . . . ±0.8%
  TLC14/MF4A-100 . . . ±1%
- **Filter Cutoff Frequency Dependent Only on External-Clock Frequency Stability**
- **Minimum Filter Response Deviation Due to External Component Variations Over Time and Temperature**
- **Cutoff Frequency Range from 0.1 Hz to 30 kHz, $V_{CC\pm}$ = ±2.5 V**
- **5-V to 12-V Operation**
- **Self Clocking or TTL-Compatible and CMOS-Compatible Clock Inputs**
- **Low Supply Voltage Sensitivity**
- **Designed to be Interchangeable with National MF4-50 and MF4-100**

D OR P PACKAGE
(TOP VIEW)



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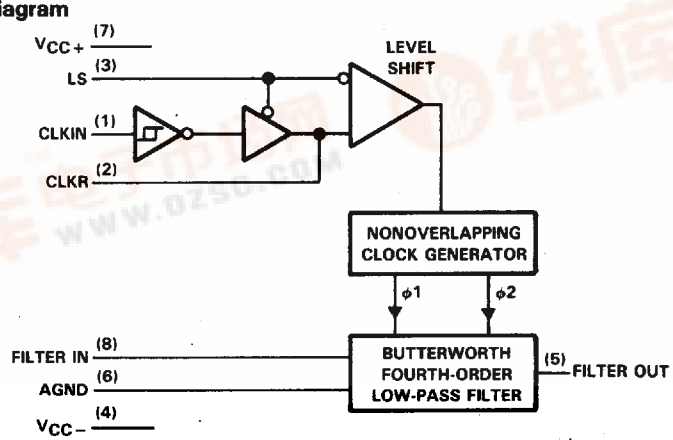
description

The TLC04/MF4A-50 and TLC14/MF4A-100 are monolithic Butterworth low-pass switched-capacitor filters. Each is designed as a low-cost, easy-to-use device providing accurate fourth-order low-pass filter functions in circuit design configurations.

Each filter features cutoff frequency stability that is dependent only on the external-clock frequency stability. The cutoff frequency is clock tunable and has a clock-to-cutoff frequency ratio of 50:1 with less than ±0.8% error for the TLC04/MF4A-50 and a clock-to-cutoff frequency ratio of 100:1 with less than ±1% error for the TLC14/MF4A-100. The input clock features self-clocking or TTL- or CMOS-compatible options in conjunction with the level shift (LS) pin.

The TLC04M/MF4A-50M and TLC14M/MF4A-100M are characterized over the full military temperature range of −55°C to 125°C. The TLC04I/MF4A-50I and TLC14I/MF4A-100I are characterized for operation from −40°C to 85°C. The TLC04C/MF4A-50C and TLC14C/MF4A-100C are characterized for operation from 0°C to 70°C.

functional block diagram



TLC04/MF4A-50, TLC14/MF4A-100
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AVAILABLE OPTIONS

T_A	CLOCK-TO-CUTOFF FREQUENCY RATIO	PACKAGE	
		SMALL OUTLINE (D)	PLASTIC DIP (P)
0°C to 70°C	50:1	TLC04CD/MF4A-50CD	TLC04CP/MF4A-50CP
	100:1	TLC14CD/MF4A-100CD	TLC14CP/MF4A-100CP
−40°C to 85°C	50:1	TLC04ID/MF4A-50ID	TLC04IP/MF4A-50IP
	100:1	TLC14ID/MF4A-100ID	TLC14IP/MF4A-100IP
−55°C to 125°C	50:1		TLC04MP/MF4A-50MP
	100:1		TLC14MP/MF4A-100MP

The D package is available taped and reeled. Add the suffix R to the device type (e.g., TLC04CDR/MF4A-50CDR).

pin description

PIN NAME	PIN NO.	I/O	DESCRIPTION
AGND	6	I	Analog Ground — The noninverting input to the operational amplifiers of the Butterworth fourth-order low-pass filter.
CLKIN	1	I	Clock In — The clock input terminal for CMOS-compatible clock or self-clocking options. For either option, the Level Shift (LS) terminal is at V_{CC-}. For self-clocking, a resistor is connected between the CLKIN and CLKR terminal pins and a capacitor is connected from the CLKIN terminal pin to ground.
CLKR	2	I	Clock R — The clock input for a TTL-compatible clock. For a TTL clock, the level shift pin is connected to mid-supply and the CLKIN pin may be left open, but it is recommended that it be connected to either V_{CC+} or V_{CC-}.
FILTER IN	8	I	Filter Input
FILTER OUT	5	O	Butterworth fourth-order low-pass Filter Output
LS	3	I	Level Shift — This terminal accommodates the various input clocking options. For CMOS-compatible clocks or self-clocking, the level-shift terminal is at V_{CC-} and for TTL-compatible clocks, the level-shift terminal is at mid-supply.
V_{CC+}	7	I	Positive supply voltage terminal
V_{CC-}	4	I	Negative supply voltage terminal

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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, $V_{CC\pm}$ (see Note 1) . . . . . ±7 V
Operating free-air temperature range: TLC04M/MF4A-50M, TLC14M/MF4A-100M −55°C to 125°C
TLC04I/MF4A-50I, TLC14I/MF4A-100I . . . . . −40°C to 85°C
TLC04C/MF4A-50C, TLC14C/MF4A-100C . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds . . . . . 260°C

NOTE 1: All voltage values are with respect to the AGND terminal.

recommended operating conditions

			TLC04/MF4A-50		TLC14/MF4A-100		UNIT
			MIN	MAX	MIN	MAX	
V_{CC+}	Positive supply voltage		2.25	6	2.25	6	V
V_{CC-}	Negative supply voltage		−2.25	−6	−2.25	−6	V
V_{IH}	High-level input voltage		2		2		V
V_{IL}	Low-level input voltage			0.8		0.8	V
f_{clock}	Clock frequency (see Note 2)	$V_{CC\pm}$ = ±2.5 V	5	1.5×10^6	5	1.5×10^6	Hz
		$V_{CC\pm}$ = ±5 V	5	2×10^6	5	2×10^6	
f_{co}	Cutoff frequency (see Note 3)		0.1	40×10^3	0.05	20×10^3	Hz
T_A	Operating free-air temperature	TLC04M/MF4A-50M, TLC14M/MF4A-100M	−55	125	−55	125	°C
		TLC04I/MF4A-50I, TLC14I/MF4A-100I	−40	85	−40	85	
		TLC04C/MF4A-50C, TLC14C/MF4A-100C	0	70	0	70	

NOTES: 2. Above 250 kHz, the input clock duty cycle should be 50% to allow the operational amplifiers the maximum time to settle while processing analog samples.
3. The cutoff frequency is defined as the frequency where the response is 3.01 dB less than the dc gain of the filter.

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electrical characteristics over recommended operating free-air temperature range, V_{CC+} = 2.5 V, V_{CC-} = −2.5 V, f_{clock} ≤ 250 kHz (unless otherwise noted)

filter section

PARAMETER			TEST CONDITIONS	TLC04/MF4A-50			TLC14/MF4A-100			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{OO}	Output voltage offset				25			50		mV
V_{OM}	Peak output voltages	V_{OM+}	R_L = 10 kΩ	1.8	2		1.8	2		V
		V_{OM-}		−1.25	−1.7		−1.25	−1.7		
I_{OS}	Short-circuit output current	Source	T_A = 25°C, See Note 4		−0.5			−0.5		mA
		Sink			4			4		
I_{CC}	Supply current		f_{clock} = 250 kHz		1.2	2.25		1.2	2.25	mA

NOTE 4: I_{OS} (source current) is measured by forcing the output to its maximum positive voltage and then shorting the output to the negative supply (V_{CC-}) terminal. I_{OS} (sink current) is measured by forcing the output to its maximum negative voltage and then shorting the output to the positive supply (V_{CC+}) terminal.

operating characteristics over recommended operating free-air temperature range, V_{CC+} = 2.5 V, V_{CC-} = −2.5 V (unless otherwise noted)

PARAMETER	TEST CONDITIONS		TLC04/MF4A-50			TLC14/MF4A-100			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
Maximum clock frequency, f_{max}	See Note 2		1.5	3		1.5	3		MHz
Clock-to-cutoff-frequency ratio (f_{clock}/f_{co})	f_{clock} ≤ 250 kHz, T_A = 25°C		49.27	50.07	50.87	99	100	101	
Temperature coefficient of clock-to-cutoff frequency ratio	f_{clock} ≤ 250 kHz			±25			±25		ppm/°C
Frequency response above and below cutoff frequency (see Note 5)	f_{co} = 5 kHz, f_{clk} = 250 kHz, T_A = 25°C	f = 6 kHz	−7.9	−7.57	−7.1				dB
		f = 4.5 kHz	−1.7	−1.46	−1.3				
	f_{co} = 2.5 kHz, f_{clk} = 250 kHz, T_A = 25°C	f = 3 kHz				−7.9	−7.42	−7.1	dB
		f = 2.25 kHz				−1.7	−1.51	−1.3	
Dynamic range (see Note 6)	T_A = 25°C			80			78		dB
Stop-band frequency attentuation at 2 f_{co}	f_{clock} ≤ 250 kHz		24	25		24	25		dB
DC voltage amplification	f_{clock} ≤ 250 kHz, RS ≤ 2 kΩ		−0.15	0	0.15	−0.15	0	0.15	dB
Peak-to-peak clock feedthrough voltage	T_A = 25°C			5			5		mV

† All typical values are at T_A = 25°C.

NOTES: 2. Above 250 kHz, the input clock duty cycle should be 50% to allow the operational amplifiers the maximum time to settle while processing analog samples.

5. The frequency responses at f are referenced to a dc gain of 0 dB.

6. The dynamic range is referenced to 1.06 V rms (1.5 V peak) where the wideband noise over a 30-kHz bandwidth is typically 106 μV rms for the TLC04/MF4A-50 and 135 μV rms for the TLC14/MF4A-100.

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electrical characteristics over recommended operating free-air temperature range, V_{CC+} = 5 V, V_{CC-} = −5 V, f_{clock} ≤ 250 kHz, (unless otherwise noted)

filter section

PARAMETER		TEST CONDITIONS	TLC04/MF4A-50 MIN	TLC04/MF4A-50 TYP†	TLC04/MF4A-50 MAX	TLC14/MF4A-100 MIN	TLC14/MF4A-100 TYP†	TLC14/MF4A-100 MAX	UNIT
V_{OO} Output voltage offset				150			200		mV
V_{OM} Peak output voltages	V_{OM+}	R_L = 10 kΩ	3.75	4.3		3.75	4.5		V
	V_{OM-}		−3.75	−4.1		−3.75	−4.1		
I_{OS} Short-circuit output current	Source	T_A = 25°C, See Note 4		−2			−2		mA
	Sink			5			5		
I_{CC} Supply current		f_{clock} = 250 kHz		1.8	3		1.8	3	mA
k_{SVS} Supply voltage sensitivity (see Figures 1 and 2)				−30			−30		dB

NOTE 4: I_{OS} (source current) is measured by forcing the output to its maximum positive voltage and then shorting the output to the negative supply (V_{CC-}) terminal. I_{OS} (sink current) is measured by forcing the output to its maximum negative voltage and then shorting the output to the positive supply (V_{CC+}) terminal.

clocking section

PARAMETER		TEST CONDITIONS‡		MIN	TYP†	MAX	UNIT
V_{T+} Positive-going input threshold voltage	CLKIN	V_{CC+} = 10 V, V_{CC-} = 0		6.1	7	8.9	V
		V_{CC+} = 5 V, V_{CC-} = 0		3.1	3.5	4.4	
V_{T-} Negative-going input threshold voltage		V_{CC+} = 10 V, V_{CC-} = 0		1.3	3	3.8	V
		V_{CC+} = 5 V, V_{CC-} = 0		0.6	1.5	1.9	
V_{hys}, Hysteresis ($V_{T+} - V_{T-}$)		V_{CC+} = 10 V, V_{CC-} = 0		2.3	4	7.6	V
		V_{CC+} = 5 V, V_{CC-} = 0		1.2	2	3.8	
V_{OH} High-level output voltage	CLKR	V_{CC} = 10 V	I_O = −10 μA	9			V
		V_{CC} = 5 V		4.5			
V_{OL} Low-level output voltage		V_{CC} = 10 V	I_O = 10 μA			1	V
		V_{CC} = 5 V				0.5	
Input leakage current		V_{CC} = 10 V	Level Shift pin at mid-supply,			2	μA
		V_{CC} = 5 V	T_A = 25°C			2	
Output current		V_{CC} = 10 V	CLKR and CLKIN	−3	−7		mA
		V_{CC} = 5 V	shorted to V_{CC-}	−0.75	−2		
Output current		V_{CC} = 10 V	CLKR and CLKIN	3	7		mA
		V_{CC} = 5 V	shorted to V_{CC+}	0.75	2		

†All typical values are at T_A = 25°C.
‡$V_{CC} = V_{CC+} - V_{CC-}$.

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operating characteristics over recommended operating free-air temperature range, V_{CC+} = 5 V, V_{CC-} = −5 V (unless otherwise noted)

PARAMETER	TEST CONDITIONS		TLC04/MF4A-50			TLC14/MF4A-100			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
Maximum clock frequency, f_{max} (see Note 2)			2	4		2	4		MHz
Clock-to-cutoff-frequency ratio (f_{clock}/f_{co})	$f_{clock} \le 250$ kHz, T_A = 25°C		49.58	49.98	50.38	99	100	101	
Temperature coefficient of clock-to-cutoff frequency ratio	$f_{clock} \le 250$ kHz			±15			±15		ppm/°C
Frequency response above and below cutoff frequency (see Note 5)	f_{co} = 5 kHz, f_{clk} = 250 kHz, T_A = 25°C	f = 6 kHz	−7.9	−7.57	−7.1				dB
		f = 4.5 kHz	−1.7	−1.44	−1.3				
	f_{co} = 2.5 kHz, f_{clk} = 250 kHz, T_A = 25°C	f = 3 kHz				−7.9	−7.42	−7.1	dB
		f = 2.25 kHz				−1.7	−1.51	−1.3	
Dynamic range (see Note 7)	T_A = 25°C			86			84		dB
Stop-band frequency attentuation at 2 f_{co}	$f_{clock} \le 250$ kHz		24	25		24	25		dB
DC voltage amplification	$f_{clock} \le 250$ kHz, RS ≤ 2 kΩ		−0.15	0	0.15	−0.15	0	0.15	dB
Peak-to-peak clock feedthrough voltage	T_A = 25°C			7			7		mV

† All typical values are at T_A = 25°C.

NOTES: 2. Above 250 kHz, the input clock duty cycle should be 50% to allow the operational amplifiers the maximum time to settle while processing analog samples.

5. The frequency responses at f are referenced to a dc gain of 0 dB.

7. The dynamic range is referenced to 2.82 V rms (4 V peak) where the wideband noise over a 30-kHz bandwidth is typically 142 μV rms for the TLC04/MF4A-50 and 178 μV rms for the TLC14/MF4A-100.

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TYPICAL CHARACTERISTICS

FILTER OUTPUT
vs
SUPPLY VOLTAGE V_{CC+} RIPPLE FREQUENCY

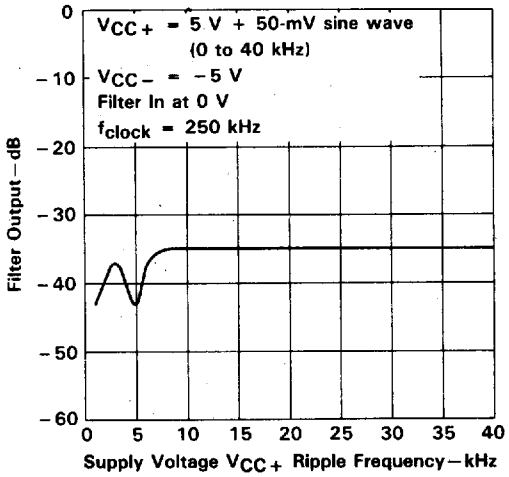

FIGURE 1

FILTER OUTPUT
vs
SUPPLY VOLTAGE V_{CC-} RIPPLE FREQUENCY

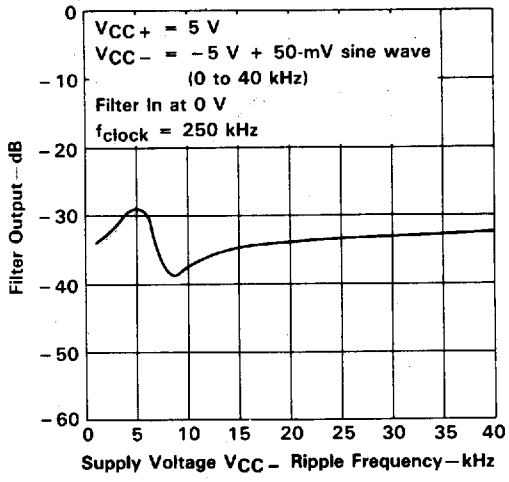

FIGURE 2

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TLC04/MF4A-50, TLC14/MF4A-100
BUTTERWORTH FOURTH-ORDER LOW-PASS
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TYPICAL APPLICATION DATA

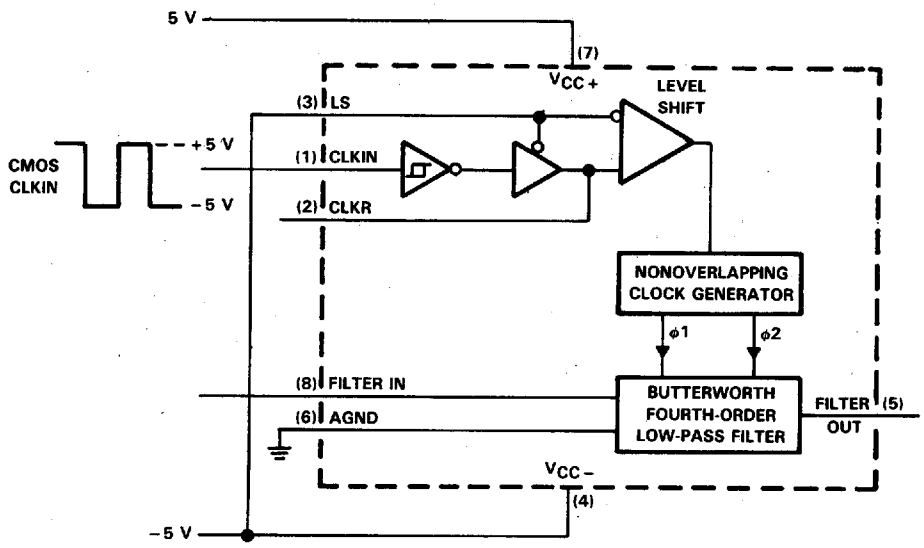

FIGURE 3. CMOS-CLOCK-DRIVEN, DUAL-SUPPLY OPERATION

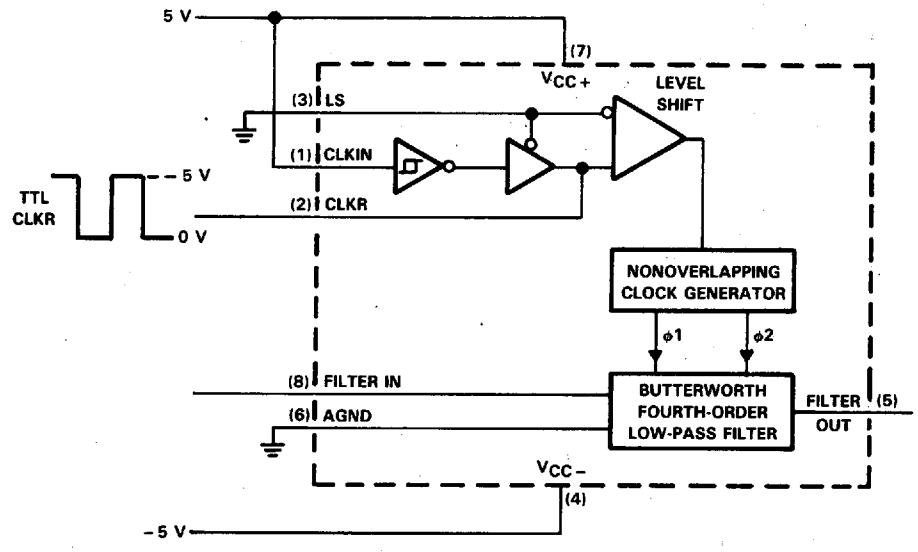

FIGURE 4. TTL-CLOCK-DRIVEN, DUAL-SUPPLY OPERATION

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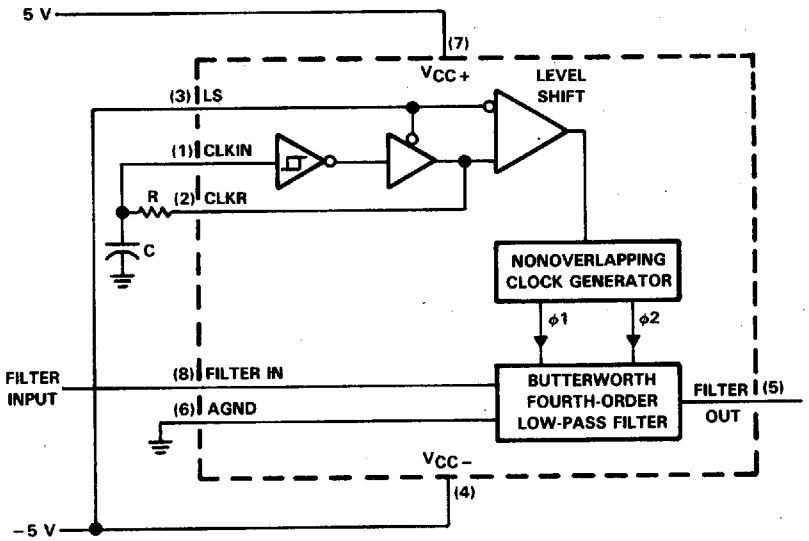
TYPICAL APPLICATION DATA



$$f_{clock} = \frac{1}{RC \times \ln\left[\left(\frac{V_{CC} - V_{T-}}{V_{CC} - V_{T+}}\right)\left(\frac{V_{T+}}{V_{T-}}\right)\right]}$$

For V_{CC} = 10 V,

$$f_{clock} = \frac{1}{1.69\ RC}$$

FIGURE 5. SELF-CLOCKING THROUGH SCHMITT-TRIGGER OSCILLATOR, DUAL-SUPPLY OPERATION

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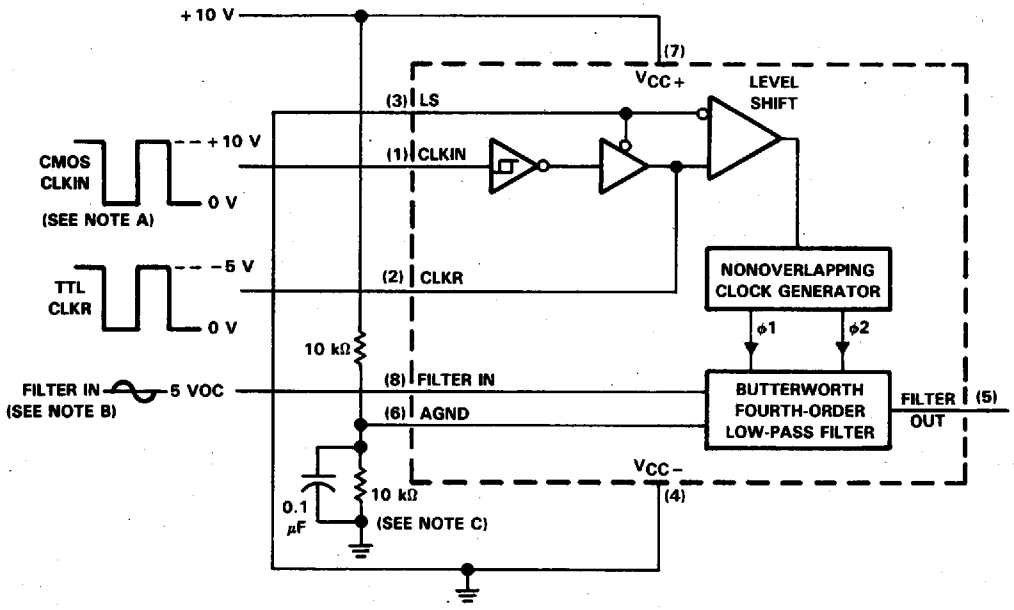
TYPICAL APPLICATION DATA



NOTES: A. The external clock used must be of CMOS level because the clock is input to a CMOS Schmitt trigger.
B. The Filter input signal should be dc-biased to mid-supply or ac-coupled to the terminal.
C. The AGND terminal must be biased to mid-supply.

FIGURE 6. EXTERNAL-CLOCK-DRIVEN SINGLE-SUPPLY OPERATION

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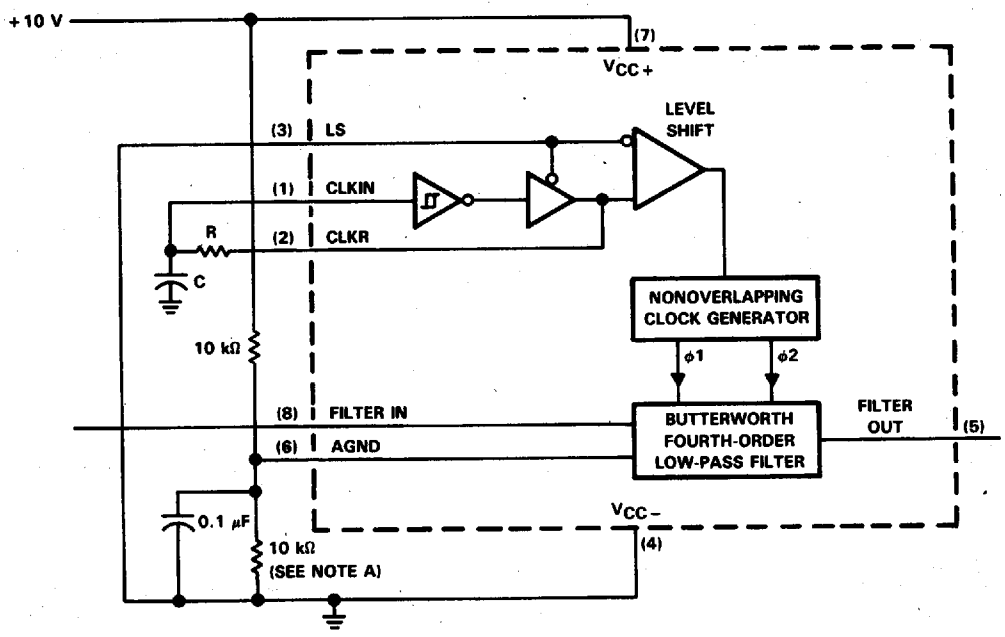
TYPICAL APPLICATION DATA



$$f_{clock} = \frac{1}{RC \times \ln\left[\left(\frac{V_{CC} - V_{T-}}{V_{CC} - V_{T+}}\right)\left(\frac{V_{T+}}{V_{T-}}\right)\right]}$$

For V_{CC} = 10 V,

$$f_{clock} = \frac{1}{1.69\ RC}$$

NOTE A: The AGND terminal must be biased to mid-supply.

FIGURE 7. SELF-CLOCKING THROUGH SCHMITT-TRIGGER OSCILLATOR, SINGLE-SUPPLY OPERATION

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TYPICAL APPLICATION DATA

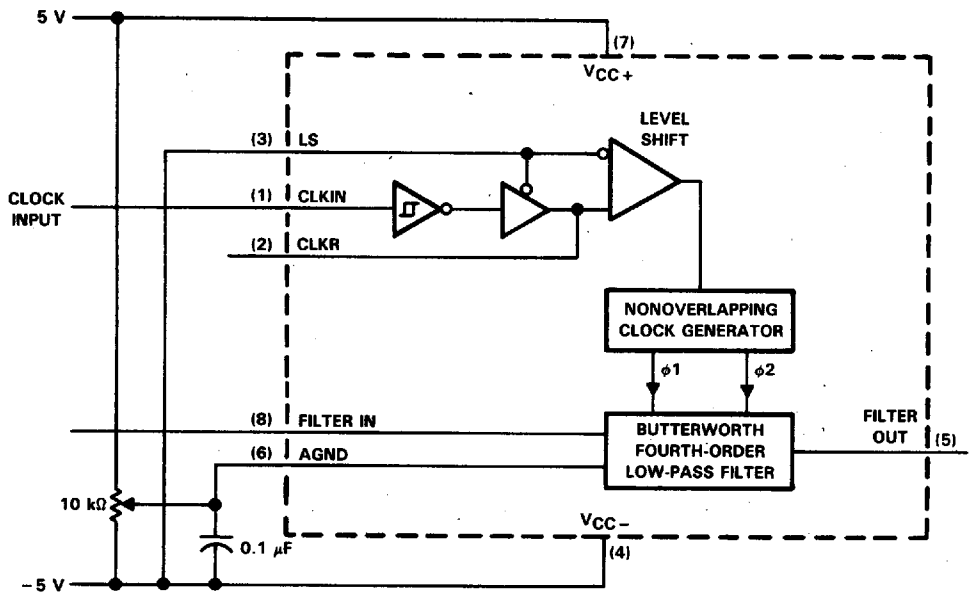

FIGURE 8. DC OFFSET ADJUSTMENT