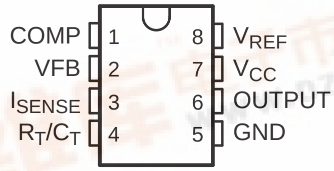
TL284xB, TL384xB
HIGH-PERFORMANCE CURRENT-MODE PWM CONTROLLERS

SLVS610A – AUGUST 2006 – REVISED SEPTEMBER 2006

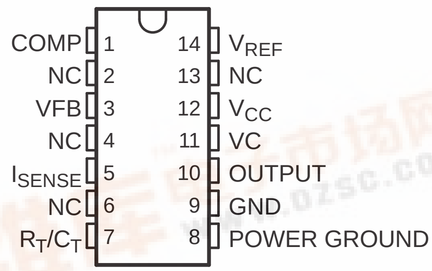
FEATURES

- **Low Start-Up Current (<0.5 mA)**
- **Trimmed Oscillator Discharge Current**
- **Current Mode Operation to 500 kHz**
- **Automatic Feed-Forward Compensation**
- **Latching PWM for Cycle-by-Cycle Current Limiting**
- **Internally Trimmed Reference With Undervoltage Lockout**
- **High-Current Totem-Pole Output Undervoltage Lockout With Hysteresis**
- **Double-Pulse Suppression**

D (SOIC) OR P (PDIP) PACKAGE
(TOP VIEW)



D (SOIC) PACKAGE
(TOP VIEW)



NC − No internal connection

DESCRIPTION/ORDERING INFORMATION

The TL284xB and TL384xB series of control integrated circuits provide the features that are necessary to implement off-line or dc-to-dc fixed-frequency current-mode control schemes, with a minimum number of external components. Internally implemented circuits include an undervoltage lockout (UVLO) and a precision reference that is trimmed for accuracy at the error amplifier input. Other internal circuits include logic to ensure latched operation, a pulse-width modulation (PWM) comparator that also provides current-limit control, and a totem-pole output stage designed to source or sink high-peak current. The output stage, suitable for driving N-channel MOSFETs, is low when it is in the off state.

The TL284xB and TL384xB series are pin compatible with the standard TL284x and TL384x with the following improvements. The start-up current is specified to be 0.5 mA (max), while the oscillator discharge current is trimmed to 8.3 mA (typ). In addition, during undervoltage lockout conditions, the output has a maximum saturation voltage of 1.2 V while sinking 10 mA (V_{CC} = 5 V).

Major differences between members of these series are the UVLO thresholds and maximum duty-cycle ranges. Typical UVLO thresholds of 16 V (on) and 10 V (off) on the TLx842B and TLx844B devices make them ideally suited to off-line applications. The corresponding typical thresholds for the TLx843B and TLx845B devices are 8.4 V (on) and 7.6 V (off). The TLx842B and TLx843B devices can operate to duty cycles approaching 100%. A duty-cycle range of 0% to 50% is obtained by the TLx844B and TLx845B by the addition of an internal toggle flip-flop, which blanks the output off every other clock cycle.The TL284xB-series devices are characterized for operation from –40°C to 85°C. The TL384xB-series devices are characterized for operation from 0°C to 70°C.

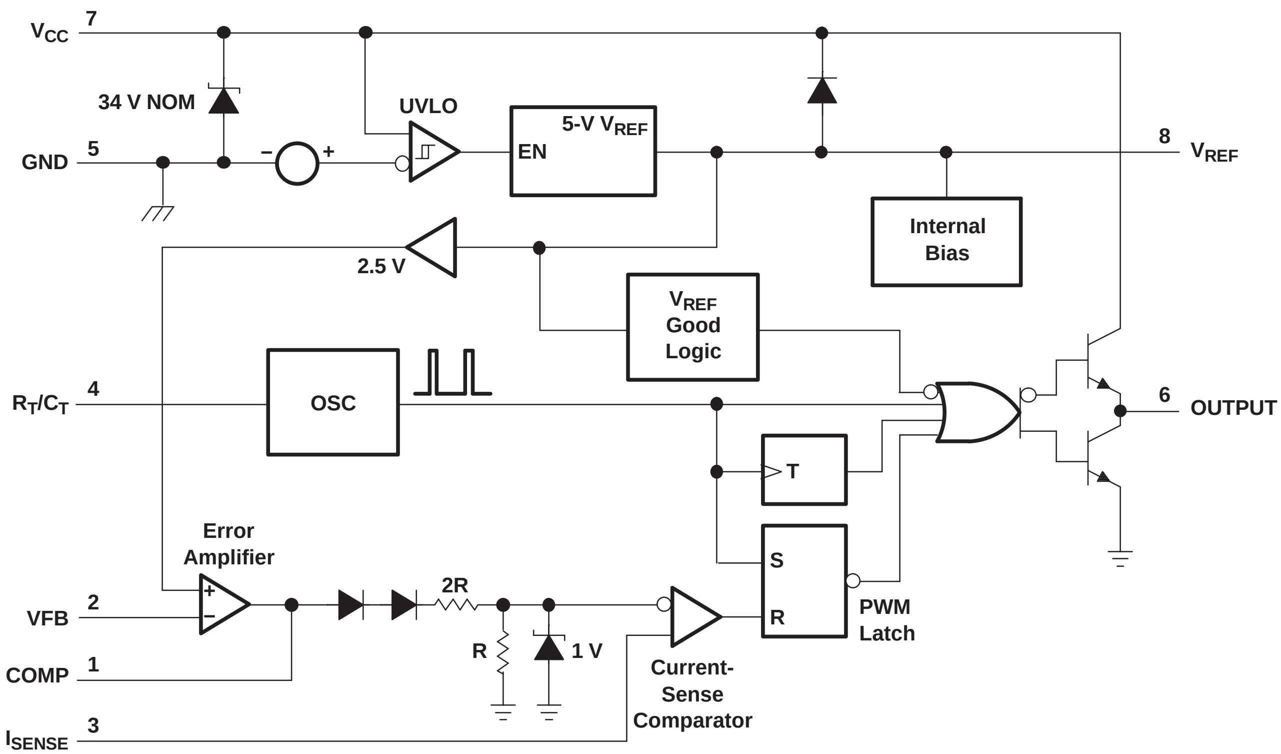
Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

ORDERING INFORMATION

T_A	PACKAGE(1)		ORDERABLE PART NUMBER	TOP-SIDE MARKING
–40°C to 85°C	PDIP – P	Tube of 50	TL2842BP	TL2842BP
			TL2843BP	TL2843BP
			TL2844BP	TL2844BP
			TL2845BP	TL2845BP
	SOIC – D (8 pin)	Tube of 75	TL2842BD-8	2842B
		Reel of 2500	TL2842BDR-8	
		Tube of 75	TL2843BD-8	2843B
		Reel of 2500	TL2843BDR-8	
		Tube of 75	TL2844BD-8	2844B
		Reel of 2500	TL2844BDR-8	
		Tube of 75	TL2845BD-8	2845B
		Reel of 2500	TL2845BDR-8	
	SOIC – D (14 pin)	Tube of 75	TL2842BD	TL2842B
		Reel of 2500	TL2842BDR	
		Tube of 75	TL2843BD	TL2843B
		Reel of 2500	TL2843BDR	
		Tube of 75	TL2844BD	TL2844B
		Reel of 2500	TL2844BDR	
		Tube of 75	TL2845BD	TL2845B
		Reel of 2500	TL2845BDR	
0°C to 70°C	PDIP – P	Tube of 50	TL3842BP	TL3842BP
			TL3843BP	TL3843BP
			TL3844BP	TL3844BP
			TL3845BP	TL3845BP
	SOIC – D (8 pin)	Tube of 75	TL3842BD-8	3842B
		Reel of 2500	TL3842BDR-8	
		Tube of 75	TL3843BD-8	3843B
		Reel of 2500	TL3843BDR-8	
		Tube of 75	TL3844BD-8	3844B
		Reel of 2500	TL3844BDR-8	
		Tube of 75	TL3845BD-8	3845B
		Reel of 2500	TL3845BDR-8	
	SOIC – D (14 pin)	Tube of 75	TL3842BD	TL3842B
		Reel of 2500	TL3842BDR	
		Tube of 75	TL3843BD	TL3843B
		Reel of 2500	TL3843BDR	
		Tube of 75	TL3844BD	TL3844B
		Reel of 2500	TL3844BDR	
		Tube of 75	TL3845BD	TL3845B
		Reel of 2500	TL3845BDR	

(1) Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

FUNCTIONAL BLOCK DIAGRAM



A. Pin numbers shown are for the 8-pin D package.

Absolute Maximum Ratings[1][2]

over operating free-air temperature range (unless otherwise noted)

				MIN	MAX	UNIT
V_{CC}	Supply voltage	Low impedance source			30	V
		I_{CC} < 30 mA			Self limiting	
V_I	Analog input voltage range	VFB and I_{SENSE}		–0.3	6.3	V
I_{CC}	Supply current				30	mA
I_O	Output current				±1	A
$I_{O(sink)}$	Error amplifier output sink current				10	mA
θ_{JA}	Package thermal impedance[3][4]	D package	8 pin		97	°C/W
			14 pin		86	
		P package			85	
	Output energy	Capacitive load			5	μJ
T_J	Virtual junction temperature				150	°C
T_{stg}	Storage temperature range			–65	150	°C
T_{lead}	Lead temperature	Soldering, 10 s			300	°C

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltages are with respect to the device GND terminal.
(3) Maximum power dissipation is a function of T_J(max), θ_{JA}, and T_A. The maximum allowable power dissipation at any allowable ambient temperature is $P_D = (T_J(max) – T_A)/\theta_{JA}$. Operating at the absolute maximum T_J of 150°C can impact reliability.
(4) The package thermal impedance is calculated in accordance with JESD 51-7.

Recommended Operating Conditions

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	V_{CC}			30	V
		VC[1]			30	
V_I	Input voltage	R_T/C_T	0		5.5	V
		VFB and I_{SENSE}	0		5.5	
V_O	Output voltage	OUTPUT	0		30	V
		POWER GROUND[1]	–0.1		1	
I_{CC}	Supply current, externally limited				25	mA
I_O	Average output current				200	mA
$I_{O(ref)}$	Reference output current				–20	mA
f_{osc}	Oscillator frequency			100	500	kHz
T_J	Operating free-air temperature	TL284xB	–40		85	°C
		TL384xB	0		70	

(1) The recommended voltages for VC and POWER GROUND apply only to the 14-pin D package.

Reference Section Electrical Characteristics

V_{CC} = 15 V[(1)], R_T = 10 kΩ, C_T = 3.3 nF, over recommended operating free-air temperature range (unless otherwise specified)

PARAMETER	TEST CONDITIONS	TL284xB			TL384xB			UNIT
		MIN	TYP[(2)]	MAX	MIN	TYP[(2)]	MAX	
Output voltage	I_O = 1 mA, T_J = 25°C	4.95	5	5.05	4.9	5	5.1	V
Line regulation	V_{CC} = 12 V to 25 V		6	20		6	20	mV
Load regulation	I_O = 1 mA to 20 mA		6	25		6	25	mV
Average temperature coefficient of output voltage			0.2	0.4		0.2	0.4	mV/°C
Output voltage, worst-case variation	V_{CC} = 12 V to 25 V, I_O = 1 mA to 20 mA	4.9		5.1	4.82		5.18	V
Output noise voltage	f = 10 Hz to 10 kHz, T_J = 25°C		50			50		µV
Output-voltage long-term drift	After 1000 h at T_J = 25°C		5	25		5	25	mV
Short-circuit output current		–30	–100	–180	–30	–100	–180	mA

(1) Adjust V_{CC} above the start threshold before setting it to 15 V.
(2) All typical values are at T_J = 25°C.

Oscillator Section[(1)] Electrical Characteristics

V_{CC} = 15 V[(2)], R_T = 10 kΩ, C_T = 3.3 nF, over recommended operating free-air temperature range (unless otherwise specified)

PARAMETER	TEST CONDITIONS	TL284xB			TL384xB			UNIT
		MIN	TYP[(3)]	MAX	MIN	TYP[(3)]	MAX	
Initial accuracy	T_J = 25°C, R_T = 62 kΩ, C_T = 1 nF, Min = 225 kHz, Max = 275 kHz	49	52	55	49	52	55	kHz
	T_J = Full range	48		56	48		56	
Voltage stability	V_{CC} = 12 V to 25 V		0.2	1		0.2	1	%
Temperature stability			5			5		%
Amplitude	Peak to peak		1.7			1.7		V
Discharge current	T_J = 25°C, R_T/C_T = 2 V	7.8	8.3	8.8	7.8	8.3	8.8	mA
	R_T/C_T = 2 V	7.5		8.8	7.6		8.8	

(1) Output frequency equals oscillator frequency for the TL3842B and TL3843B. Output frequency is one-half the oscillator frequency for the TL3844B and TL3845B.
(2) Adjust V_{CC} above the start threshold before setting it to 15 V.
(3) All typical values are at T_J = 25°C.

Error-Amplifier Section Electrical Characteristics

V_{CC} = 15 V(1), R_T = 10 kΩ, C_T = 3.3 nF, over recommended operating free-air temperature range (unless otherwise specified)

PARAMETER	TEST CONDITIONS	TL284xB			TL384xB			UNIT
		MIN	TYP(2)	MAX	MIN	TYP(2)	MAX	
Feedback input voltage	COMP = 2.5 V	2.45	2.5	2.55	2.42	2.5	2.58	V
Input bias current			–0.3	–1		–0.3	–2	μA
Open-loop voltage amplification	V_O = 2 V to 4 V	65	90		65	90		dB
Gain-bandwidth product		0.7	1		0.7	1		MHz
Supply-voltage rejection ratio	V_{CC} = 12 V to 25 V	60	70		60	70		dB
Output sink current	VFB = 2.7 V, COMP = 1.1 V	2	6		2	6		mA
Output source current	VFB = 2.3 V, COMP = 5 V	–0.5	–0.8		–0.5	–0.8		mA
High-level output voltage	VFB = 2.3 V, R_L = 15 kΩ to GND	5	6		5	6		V
Low-level output voltage	VFB = 2.7 V, R_L = 15 kΩ to GND		0.7	1.1		0.7	1.1	V

(1) Adjust V_{CC} above the start threshold before setting it to 15 V.
(2) All typical values are at T_J = 25°C.

Current-Sense Section Electrical Characteristics

V_{CC} = 15 V(1), R_T = 10 kΩ, C_T = 3.3 nF, over recommended operating free-air temperature range (unless otherwise specified)

PARAMETER	TEST CONDITIONS	TL284xB			TL384xB			UNIT
		MIN	TYP(2)	MAX	MIN	TYP(2)	MAX	
Voltage amplification(3)(4)		2.85	3	3.15	2.85	3	3.15	V/V
Current-sense comparator threshold(3)	COMP = 5 V	0.9	1	1.1	0.9	1	1.1	V
Supply-voltage rejection ratio(3)	V_{CC} = 12 V to 25 V		70			70		dB
Input bias current			–2	–10		–2	–10	μA
Delay time to output	VFB = 0 V to 2 V		150	300		150	300	ns

(1) Adjust V_{CC} above the start threshold before setting it to 15 V.
(2) All typical values are at T_J = 25°C.
(3) Measured at the trip point of the latch, with VFB at 0 V.
(4) Measured between I_{SENSE} and COMP, with the input changing from 0 V to 0.8 V.

Output Section Electrical Characteristics

V_{CC} = 15 V(1), R_T = 10 kΩ, C_T = 3.3 nF, over recommended operating free-air temperature range (unless otherwise specified)

PARAMETER	TEST CONDITIONS	TL284xB			TL384xB			UNIT
		MIN	TYP(2)	MAX	MIN	TYP(2)	MAX	
High-level output voltage	I_{OH} = –20 mA	13	13.5		13	13.5		V
	I_{OH} = –200 mA	12	13.5		12	13.5		
Low-level output voltage	I_{OL} = 20 mA		0.1	0.4		0.1	0.4	V
	I_{OL} = 200 mA		1.5	2.2		1.5	2.2	
Rise time	C_L = 1 nF, T_J = 25°C		50	150		50	150	ns
Fall time	C_L = 1 nF, T_J = 25°C		50	150		50	150	ns
UVLO saturation	V_{CC} = 5 V, I_{OL} = 1 mA		0.7	1.2		0.7	1.2	V

(1) Adjust V_{CC} above the start threshold before setting it to 15 V.
(2) All typical values are at T_J = 25°C.

Undervoltage-Lockout Section Electrical Characteristics

V_{CC} = 15 V(1), R_T = 10 kΩ, C_T = 3.3 nF, over recommended operating free-air temperature range (unless otherwise specified)

PARAMETER	TEST CONDITIONS	TL284xB			TL384xB			UNIT
		MIN	TYP(2)	MAX	MIN	TYP(2)	MAX	
Start threshold voltage	TLx842B, TLx844B	15	16	17	14.5	16	17.5	V
	TLx843B, TLx845B	7.8	8.4	9	7.8	8.4	9	
Minimum operating voltage after start-up	TLx842B, TLx844B	9	10	11	8.5	10	11.5	V
	TLx843B, TLx845B	7	7.6	8.2	7	7.6	8.2	

(1) Adjust V_{CC} above the start threshold before setting it to 15 V.
(2) All typical values are at T_J = 25°C.

Pulse-Width Modulator Section Electrical Characteristics

V_{CC} = 15 V(1), R_T = 10 kΩ, C_T = 3.3 nF, over recommended operating free-air temperature range (unless otherwise specified)

PARAMETER	TEST CONDITIONS	TL284xB			TL384xB			UNIT
		MIN	TYP(2)	MAX	MIN	TYP(2)	MAX	
Maximum duty cycle	TL3842B, TL3843B	94	96	100	94	96	100	%
	TL3844B, TL3845B	47	48	50	47	48	50	
Minimum duty cycle				0			0	%

(1) Adjust V_{CC} above the start threshold before setting it to 15 V.
(2) All typical values are at T_J = 25°C.

Supply Voltage Electrical Characteristics

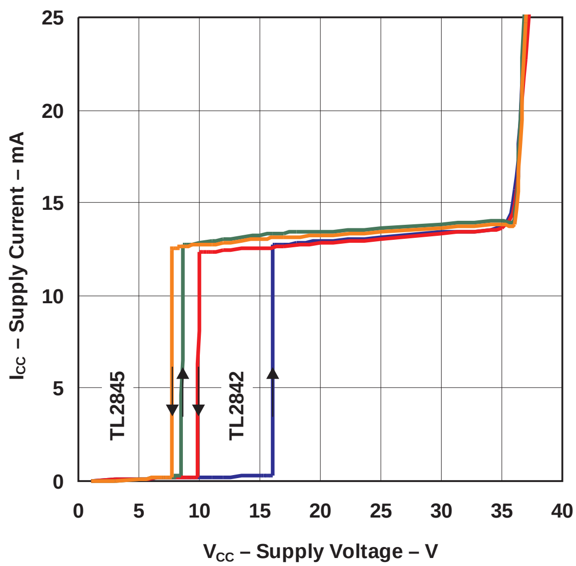
V_{CC} = 15 V(1), R_T = 10 kΩ, C_T = 3.3 nF, over recommended operating free-air temperature range (unless otherwise specified)

PARAMETER	TEST CONDITIONS	TL284xB			TL384xB			UNIT
		MIN	TYP(2)	MAX	MIN	TYP(2)	MAX	
Start-up current			0.3	0.5		0.3	0.5	mA
Operating supply current	VFB and I_{SENSE} at 0 V		11	17		11	17	mA
Limiting voltage	I_{CC} = 25 mA	30	34		30	34		V

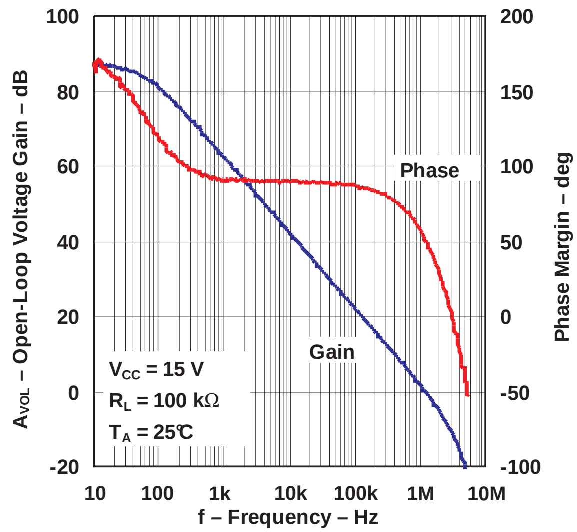
(1) Adjust V_{CC} above the start threshold before setting it to 15 V.
(2) All typical values are at T_J = 25°C.

TYPICAL CHARACTERISTICS

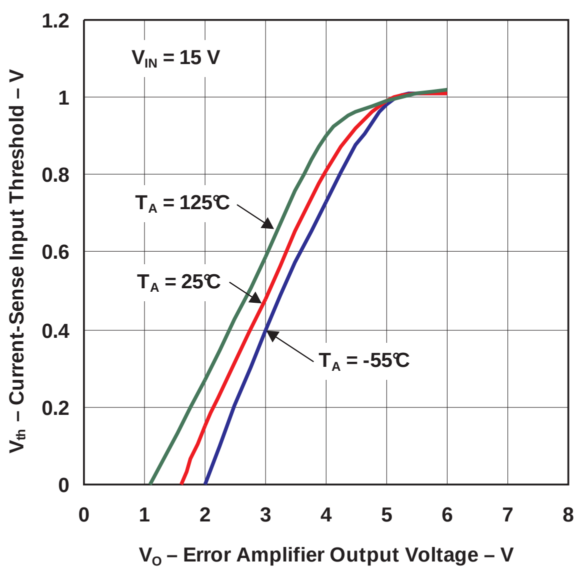
SUPPLY CURRENT vs SUPPLY VOLTAGE



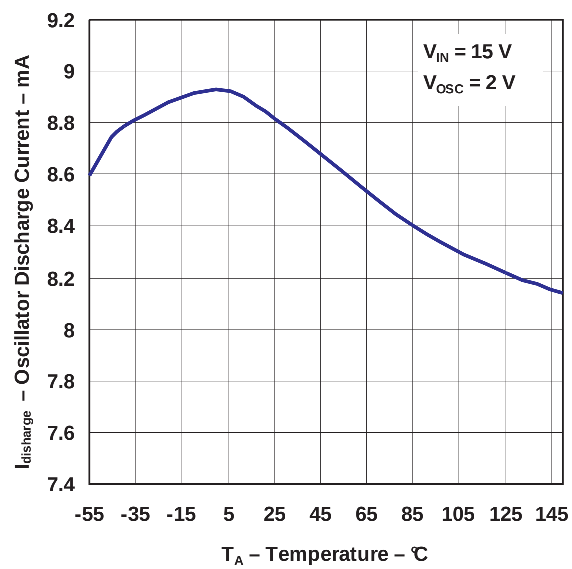
ERROR AMPLIFIER OPEN-LOOP GAIN AND PHASE vs FREQUENCY



CURRENT-SENSE INPUT THRESHOLD vs ERROR AMPLIFIER OUTPUT VOLTAGE

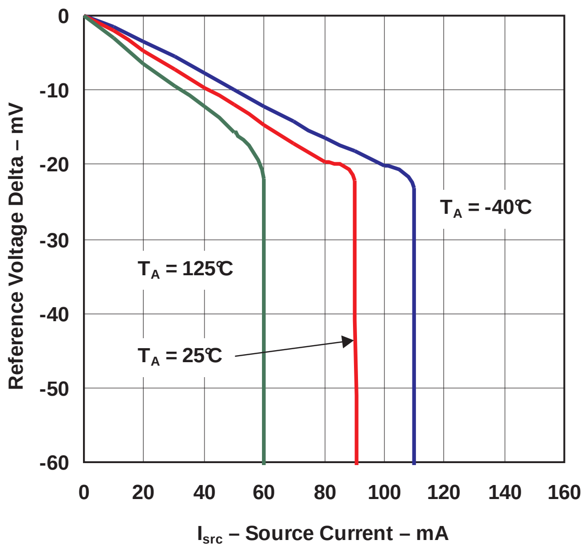


OSCILLATOR DISCHARGE CURRENT vs TEMPERATURE

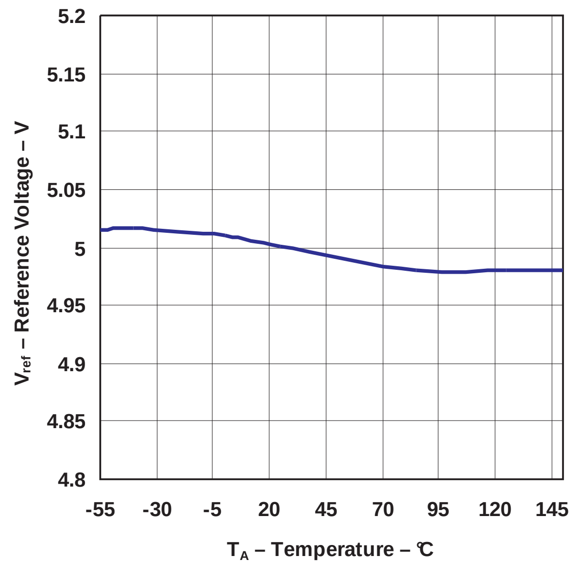


TYPICAL CHARACTERISTICS (continued)

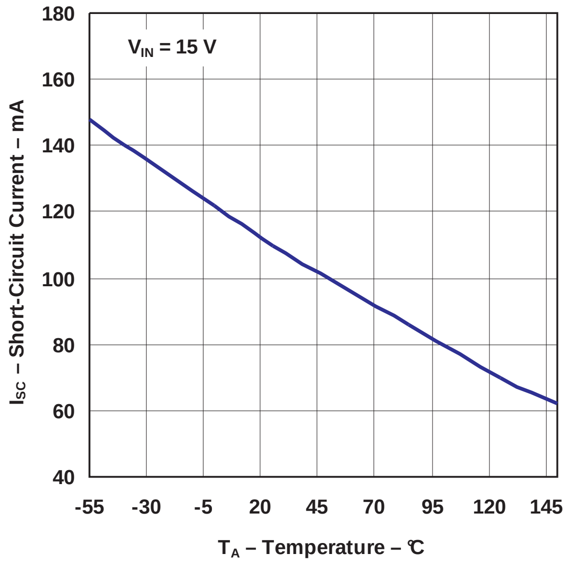
REFERENCE VOLTAGE
vs
SOURCE CURRENT



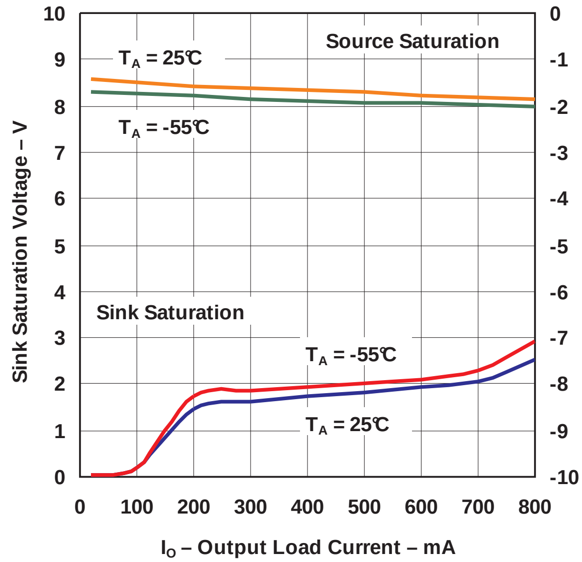
REFERENCE VOLTAGE
vs
TEMPERATURE



REFERENCE SHORT-CIRCUIT CURRENT
vs
TEMPERATURE

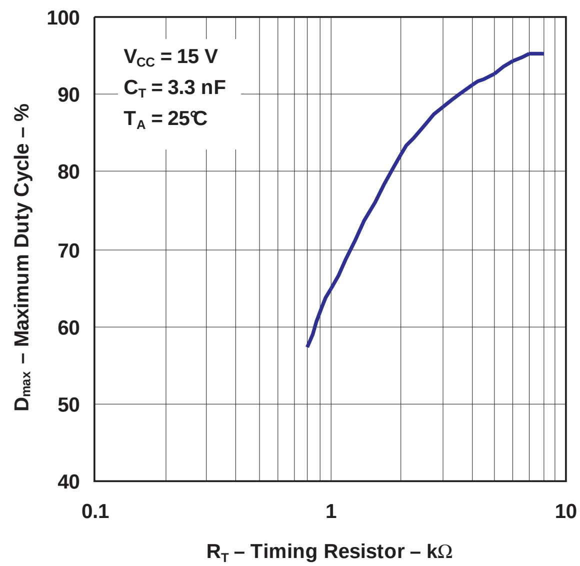


OUTPUT SATURATION VOLTAGE
vs
LOAD CURRENT

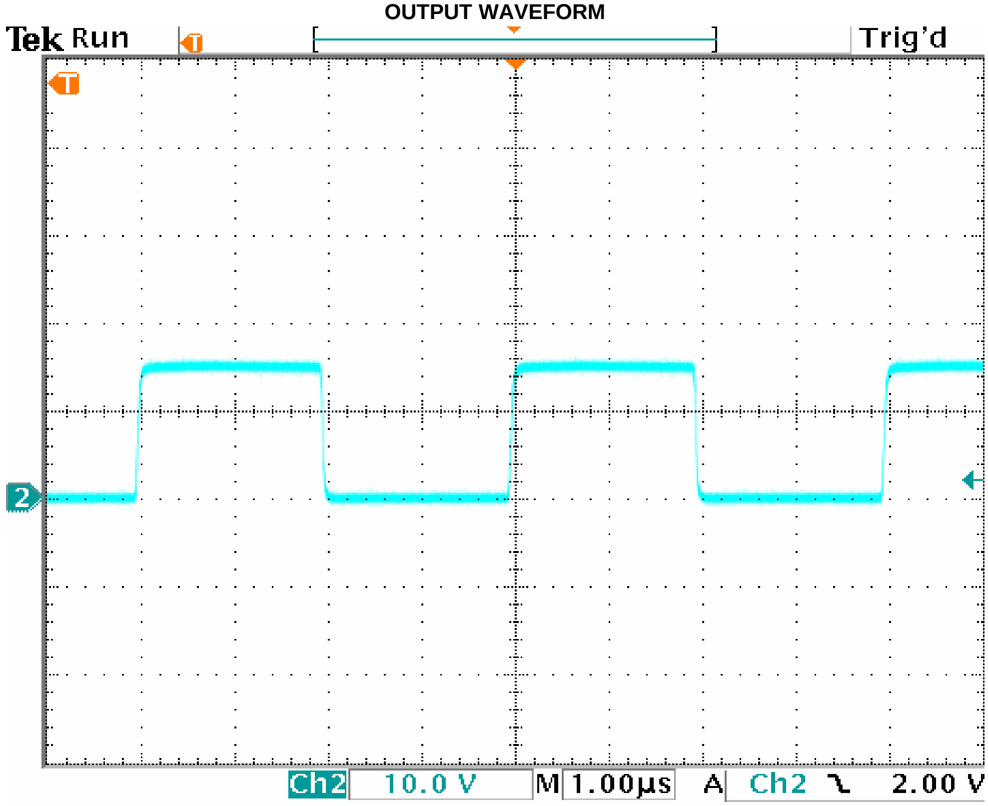


TYPICAL CHARACTERISTICS (continued)

MAXIMUM OUTPUT DUTY CYCLE
vs
TIMING RESISTOR

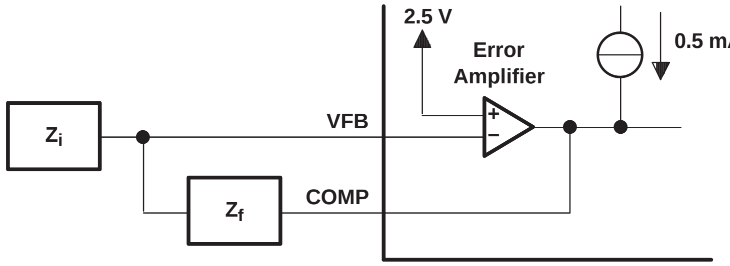


OUTPUT WAVEFORM



APPLICATION INFORMATION

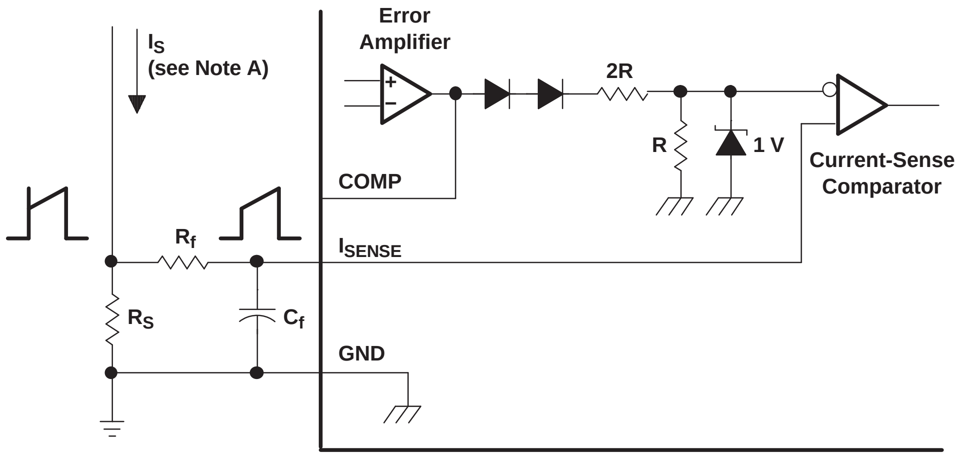
The error-amplifier configuation circuit is shown in Figure 1.



A. Error amplifier can source or sink up to 0.5 mA.

Figure 1. Error-Amplifier Configuration

The current-sense circuit is shown in Figure 2.



A. Peak current (I_S) is determined by the formula: $I_{S(max)} = 1\ V/R_S$

B. A small RC filter formed by resistor R_f and capacitor C_f may be required to suppress switch transients.

Figure 2. Current-Sense Circuit

The oscillator frequency is set using the circuit shown in Figure 3. The frequency is calculated as:

$$f = 1 / R_T C_T$$

For $R_T > 5\ k\Omega$:

$$f \approx 1.72 / R_T C_T$$

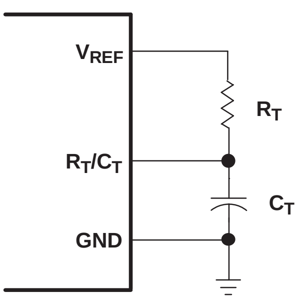
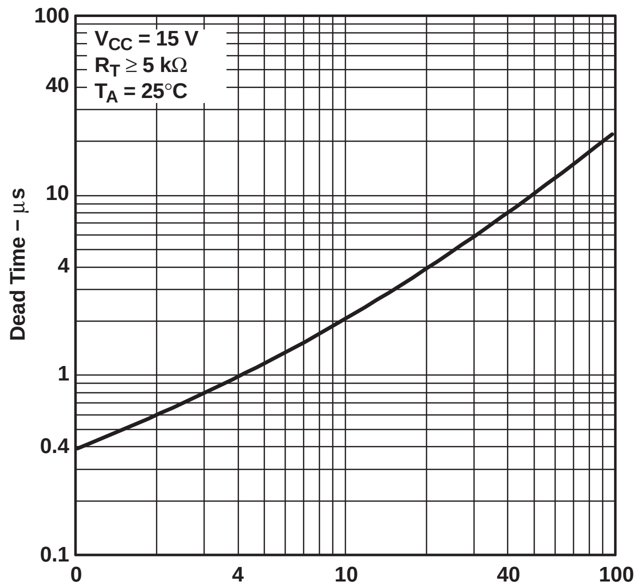


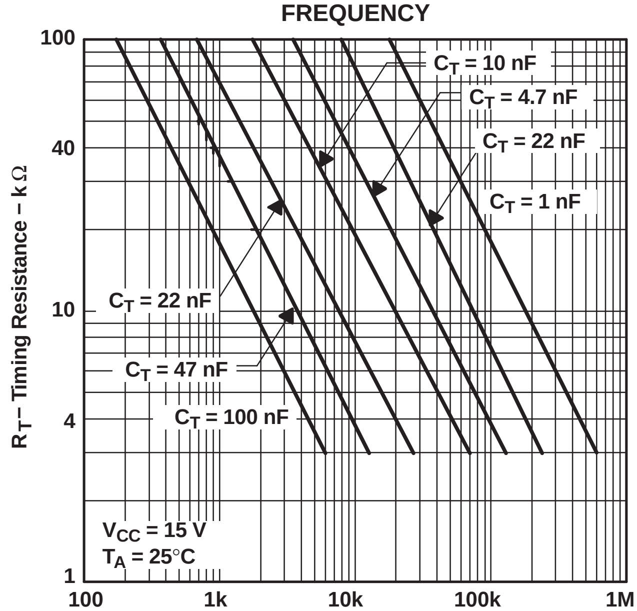
Figure 3. Oscillator Section

APPLICATION INFORMATION (continued)

DEAD TIME
vs
TIMING CAPACITANCE



TIMING RESISTANCE
vs
FREQUENCY



Open-Loop Laboratory Test Fixture

In the open-loop laboratory test fixture (see Figure 4), high peak currents associated with loads necessitate careful grounding techniques. Timing and bypass capacitors should be connected close to the GND terminal in a single-point ground. The transistor and 5-kΩ potentiometer sample the oscillator waveform and apply an adjustable ramp to the I_{SENSE} terminal.

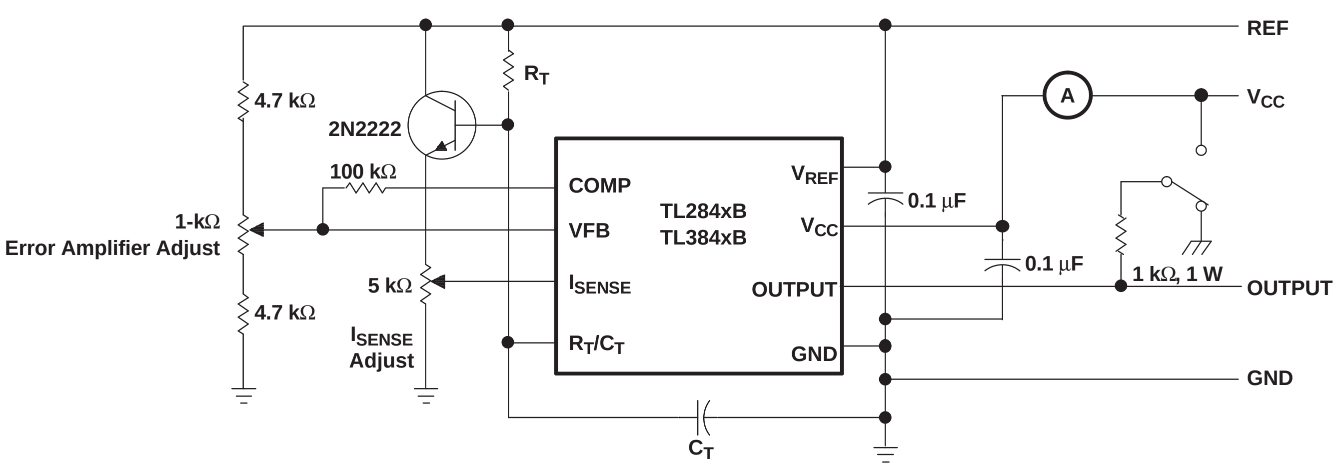


Figure 4. Open-Loop Laboratory Test Fixture

APPLICATION INFORMATION (continued)

Shutdown Technique

The PWM controller (see Figure 5) can be shut down by two methods: either raise the voltage at I_{SENSE} above 1 V or pull the COMP terminal below a voltage two diode drops above ground. Either method causes the output of the PWM comparator to be high (refer to block diagram). The PWM latch is reset dominant so that the output remains low until the next clock cycle after the shutdown condition at the COMP or I_{SENSE} terminal is removed. In one example, an externally latched shutdown can be accomplished by adding an SCR that resets by cycling V_{CC} below the lower UVLO threshold. At this point, the reference turns off, allowing the SCR to reset.

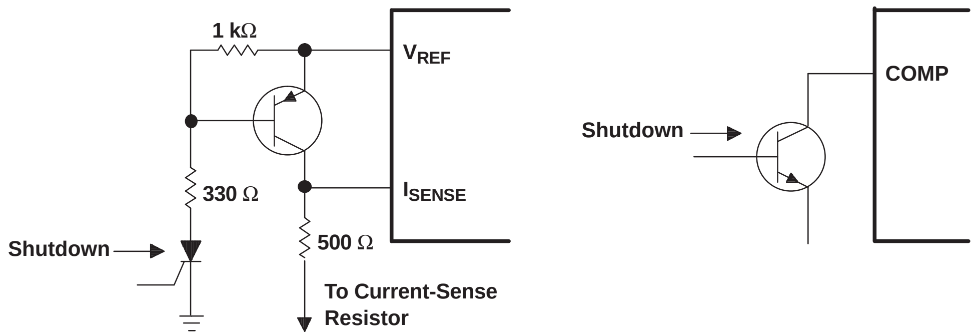


Figure 5. Shutdown Techniques

A fraction of the oscillator ramp can be summed resistively with the current-sense signal to provide slope compensation for converters requiring duty cycles over 50% (see Figure 6). Note that capacitor C forms a filter with R2 to suppress the leading-edge switch spikes.

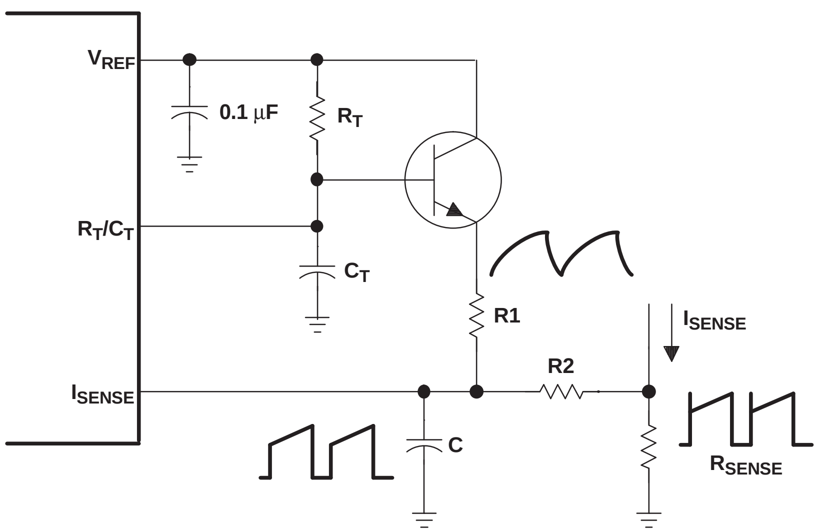


Figure 6. Slope Compensation

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)
TL2842BD	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TL2842BDG4-8	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TL2842BDR	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TL2842BDRG4-8	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TL2842BP	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
TL2842BPE4	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
TL2843BD	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TL2843BD-8	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TL2843BDG4	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TL2843BDG4-8	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TL2843BDR	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TL2843BDR-8	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TL2843BDRG4	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TL2843BDRG4-8	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TL2843BP	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
TL2843BPG4	ACTIVE	PDIP	P	8		TBD	Call TI	Call TI
TL2844BD	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TL2844BD-8	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TL2844BDG4	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TL2844BDG4-8	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TL2844BDR	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TL2844BDR-8	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TL2844BDRG4	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TL2844BDRG4-8	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TL2844BP	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type

Orderable Device	Status [1]	Package Type	Package Drawing	Pins	Package Qty	Eco Plan [2]	Lead/Ball Finish	MSL Peak Temp [3]
TL2844BPE4	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
TL2845BD	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TL2845BD-8	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TL2845BDG4	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TL2845BDR	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TL2845BDR-8	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TL2845BDRG4	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TL2845BP	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
TL2845BPE4	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
TL3842BD	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TL3842BD-8	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TL3842BDG4-8	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TL3842BDR	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TL3842BDR-8	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TL3842BDRG4	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TL3842BDRG4-8	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TL3842BP	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
TL3842BPE4	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
TL3843BD	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TL3843BD-8	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TL3843BDG4	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TL3843BDG4-8	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TL3843BDR	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TL3843BDRG4	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TL3843BP	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
TL3843BPE4	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type

PACKAGE OPTION ADDENDUM

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)
TL3844BD	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TL3844BD-8	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TL3844BDG4	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TL3844BDG4-8	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TL3844BDR-8	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TL3844BDRG4	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TL3844BDRG4-8	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TL3844BP	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
TL3844BPE4	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
TL3845BD	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TL3845BD-8	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TL3845BDG4	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TL3845BDG4-8	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TL3845BDR	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TL3845BDR-8	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TL3845BDRG4	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TL3845BDRG4-8	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TL3845BP	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
TL3845BPE4	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and

package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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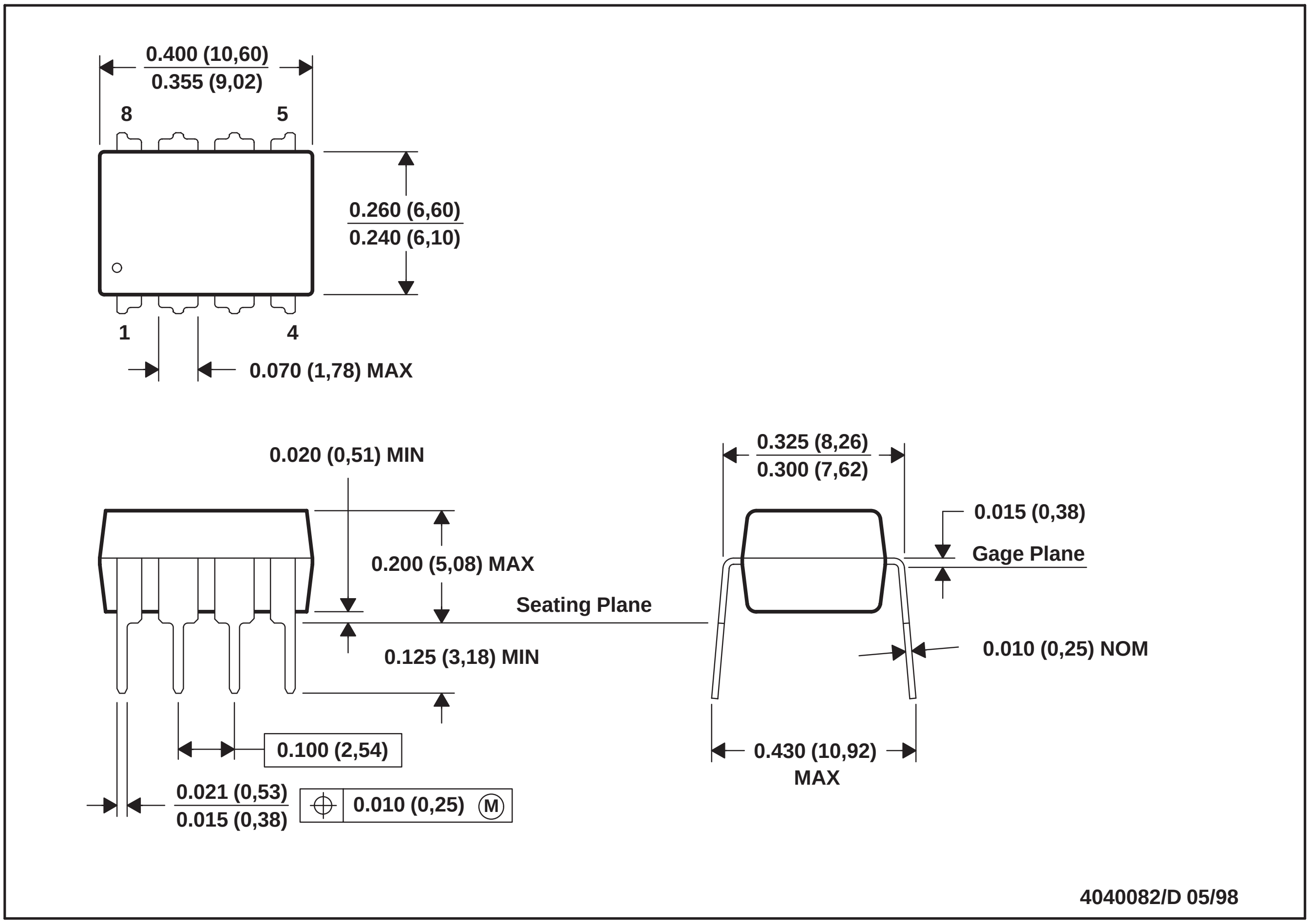
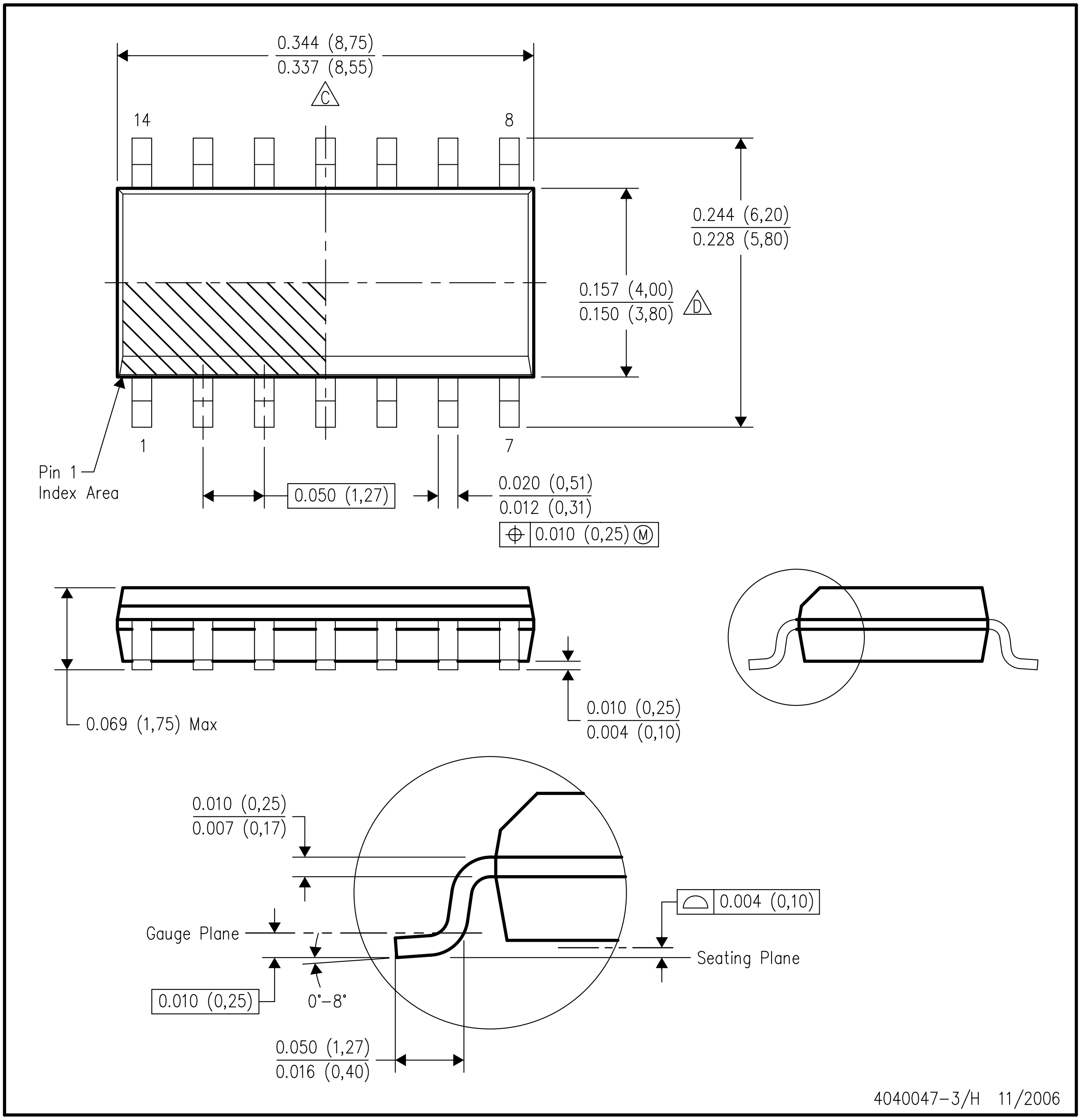
P (R-PDIP-T8) **PLASTIC DUAL-IN-LINE**



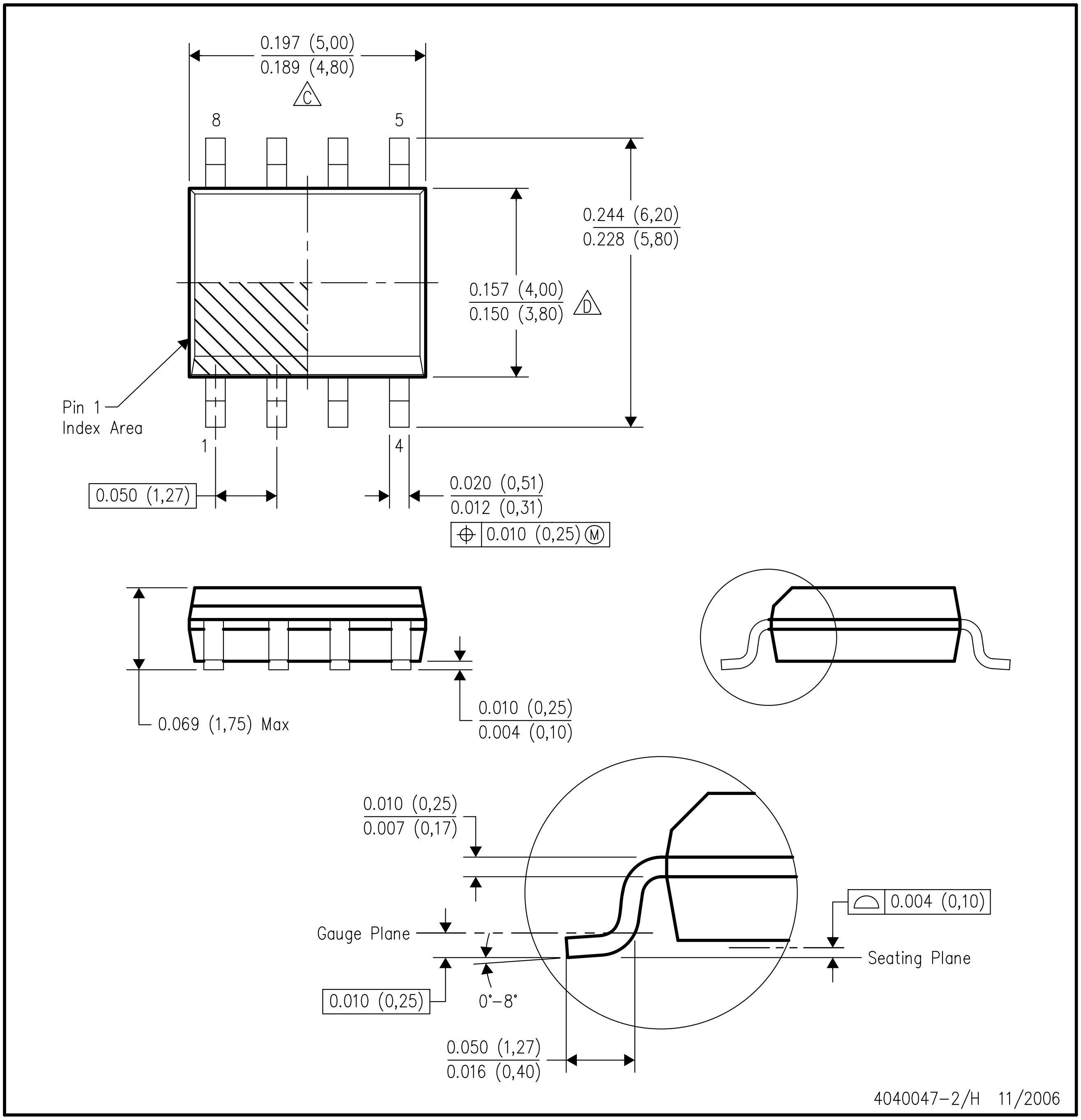
NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS-001

D (R–PDSO–G14) PLASTIC SMALL–OUTLINE PACKAGE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 (0,15) per end.
D. Body width does not include interlead flash. Interlead flash shall not exceed .017 (0,43) per side.
E. Reference JEDEC MS-012 variation AB.

D (R–PDSO–G8) PLASTIC SMALL–OUTLINE PACKAGE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 (0,15) per end.
D. Body width does not include interlead flash. Interlead flash shall not exceed .017 (0,43) per side.
E. Reference JEDEC MS–012 variation AA.

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