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TRF7960/61

SLOS504–AUGUST 2006

Multi-Standard Fully Integrated 13.56-MHz Radio Frequency Identification (RFID) Analog Front End and Data Framing Reader System

FEATURES

- Completely integrated protocol handling (OSI Model Layer 3 and below)
- Separate internal high-PSRR power supplies for analog, digital, and PA sections provides noise isolation for superior read range and reliability
- Dual receiver input with AM and PM demodulation to minimize communication holes (patent pending).
- Receiver AM and PM RSSI
- Reader-to-reader anti-collision
- High Integration reduces total BOM and board area
 - Single external 13.56 MHz crystal oscillator
 - MCU-selectable clock-frequency output of RF, RF/2, or RF/4
 - Adjustable 20 mA, high-PSRR LDO for powering external MCU
- Easy to use with high flexibility
 - Auto-configured default modes for each supported ISO protocol
 - 11 user-programmable registers
 - Selectable receiver gain and AGC
 - Programmable output power (100 mW or 200 mW)
 - Adjustable ASK Modulation Range (8% to 30%)
 - Built in receiver bandpass filter with user selectable corner frequencies
- Wide operating voltage range of 2.7 to 5.5 V

- Ultra-low power modes
 - Power down < 1 μ A
 - Standby 120 μ A
 - Active (Rx only) 10 mA
- Parallel 8-Bit or Serial 4-pin SPI interface with MCU using 12-byte FIFO
- Ultra-small 32-pin QFN Package (5x5mm)
- Available tools
 - Reference design/EVM with development software
 - Source code available for MSP430

APPLICATIONS

- Secure access control
- Product authentication
 - Printer ink cartridges
 - Blood glucose monitors
- Contactless payment systems

DESCRIPTION

The TRF7960/61 is an integrated analog front end & data framing system for a 13.56 MHz RFID reader system. Built-in programming options make it suitable for a wide range of applications both in proximity and vicinity RFID systems.

The reader is configured by selecting the desired protocol in the control registers. Direct access to all control registers allows fine tuning of various reader parameters as needed.

PRODUCT SELECTION TABLE

DEVICE	PROTOCOLS						
	ISO14443A/B				ISO15693	Tag-it™	HF-EPC
	106 kbps	212 kbps	424 kbps	848 kbps			
TRF7960	X	X	X	X	X	X	X
TRF7961					X	X	X



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These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

DESCRIPTION (CONTINUED)

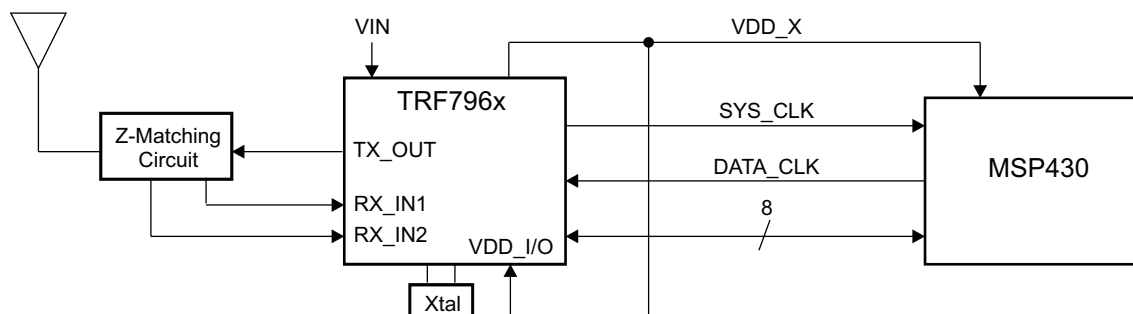


Figure 1. Typical Application

A parallel or serial interface can be used for communication between the MCU & reader. When hardware encoders and decoders are used (accelerators for different standards), transmission and receive functions use a 12-byte FIFO register. For direct transmit or receive functions, the encoders/decoders can be bypassed in order for the MCU to process the data in real time. The transmitter has selectable output-power levels of 100 mW (+20 dBm) or 200 mW (+23 dBm) into a 50 Ω load (at 5 V supply) and is capable of ASK or OOK modulation. Integrated voltage regulators ensure power-supply noise rejection for the complete reader system.

Data transmission comprises low level encoding for ISO15693, modified Miller for ISO14443-A, high-bit-rate systems, Tag-it, and HF-EPC system coding. Included with the data encoding is automatic generation of SOF, EOF, CRC, and/or parity bits.

The receiver system enables AM and PM demodulation using a dual-input architecture. The receiver also includes an automatic gain control option and selectable gain. Also included is a selectable bandwidth to cover a broad range of input sub-carrier signal options. The received signal strength for AM and PM modulation is accessible via the RSSI register. The receiver output is selectable between a digitized sub-carrier signal and any of eleven integrated sub-carrier decoders (two for ISO15693 low bit rate, two for ISO15693 high bit rate, two for ISO14443, three for ISO14443 high bit rates, one for Tag-it, and one for HF-EPC system). Selected decoders also deliver bit stream and a data clock as outputs.

The receiver system also includes a framing system. This system performs the CRC and/or parity check, removes the EOF and SOF settings, and organizes the data in bytes. Framed data is then accessible to the MCU via a 12-byte FIFO register and MCU interface. The framing supports ISO14443 and ISO15693 protocols.

The TRF7960/61 supports data communication levels between 1.8-5.5 V for MCU I/O interface while also providing a data synchronization clock. An auxiliary 20 mA regulator (pin 32) is available for additional system circuits.

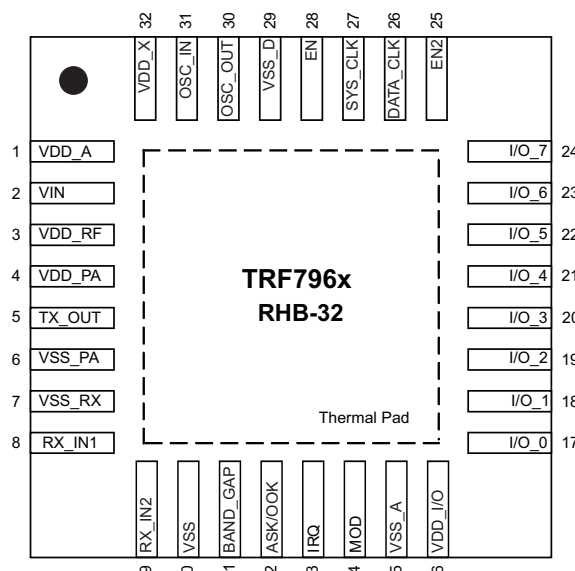


Figure 2. TRF796x Pin Assignments (Top View)

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted)⁽¹⁾

		VALUE	UNIT
V _{IN}	Supply voltage	6	V
I _O	Output current	150	mA
	Continuous power dissipation	See Dissipation Rating Table	
T _J	Maximum junction temperature, any condition ⁽²⁾	140	°C
	Maximum junction temperature, continuous operation, long term reliability ⁽²⁾	125	°C
T _{stg}	Storage temperature range	–55 to 150	°C
	Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	300	°C
ESDS rating:	HBM (Human Body Model)	2	kV
	CDM (Charge Device Model)	500	V
	MM (Machine Model)	200	

- (1) The absolute maximum ratings under any condition is limited by the constraints of the silicon process. Stresses above these ratings may cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability. These are stress ratings only and functional operation of the device at these or any other conditions beyond those specified are not implied.
- (2) The maximum junction temperature for continuous operation is limited by package constraints. Operation above this temperature may result in reduced reliability and/or lifetime of the device.

TABLE 5. PACKAGING/ORDERING INFORMATION⁽¹⁾

PACKAGED DEVICES	PACKAGE TYPE	TRANSPORT MEDIA	QUANTITY
TRF7960RHBT	RHB – 32	Tape and Reel	250
TRF7960RHBR		Tape and Reel	3000
TRF7961RHBT	RHB – 32	Tape and Reel	250
TRF7961RHBR		Tape and Reel	3000

- (1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI Web site at www.ti.com.

DISSIPATION RATINGS TABLE PER PACKAGE

PACKAGE	θ_{JC} (°C/W)	θ_{JA} ⁽¹⁾ (°C/W)	POWER RATING ⁽²⁾	
			T _A ≤ 25°C	T _A = 85°C
RHB (32)	31	36.4	2.7 W	1.1 W

- (1) This data was taken using the JEDEC standard High-K test PCB.
- (2) Power rating is determined with a junction temperature of 125°C. This is the point where distortion starts to substantially increase. Thermal management of the final PCB should strive to keep the junction temperature at or below 125°C for best performance and long term reliability.

RECOMMENDED OPERATING CONDITIONS

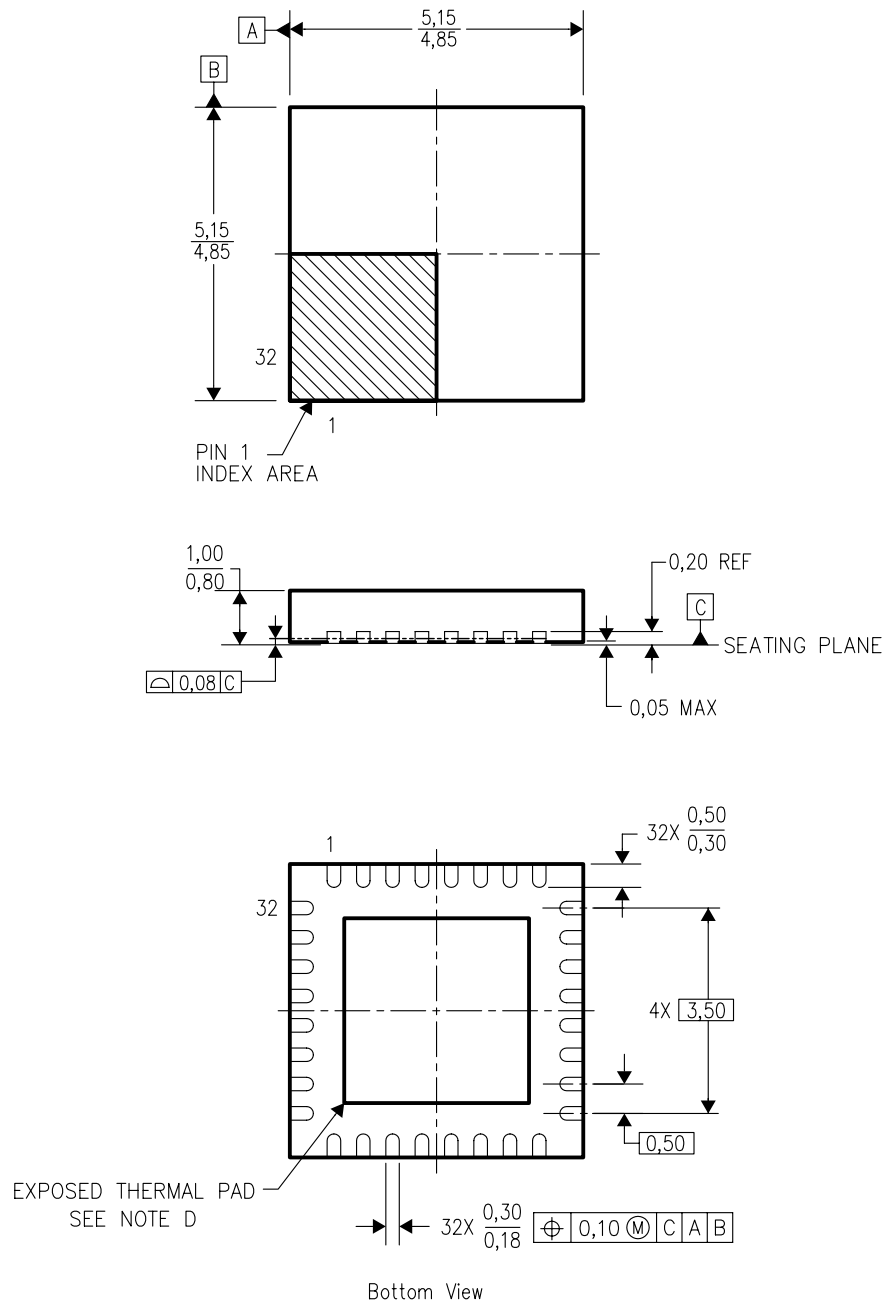
over operating free-air temperature range (unless otherwise noted)

		MIN	TYP	MAX	UNIT
V _{IN}	Supply voltage	2.7	5.0	5.5	V
T _J	Operating virtual junction temperature range	–40		125	°C
T _A	Operating ambient temperature range	–40	25	110	°C
	Load impedance at TX OUT (pin 5)		10		Ω

MECHANICAL DATA

RHB (S-PQFP-N32)

PLASTIC QUAD FLATPACK



4204326/C xx/04

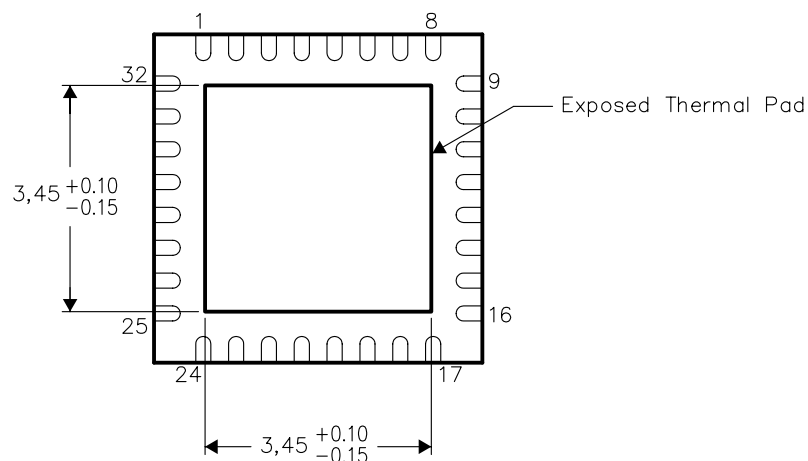
- NOTES:
- All linear dimensions are in millimeters.
 - This drawing is subject to change without notice.
 - QFN (Quad Flatpack No-Lead) Package configuration.
 - The Package thermal pad must be soldered to the board for thermal and mechanical performance. See product data sheet for details regarding the exposed thermal pad dimensions.
 - Falls within JEDEC MO-220.

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to a ground or power plane (whichever is applicable), or alternatively, a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No-Lead (QFN) package and its advantages, refer to Application Report, Quad Flatpack No-Lead Logic Packages, Texas Instruments Literature No. SCBA017. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.

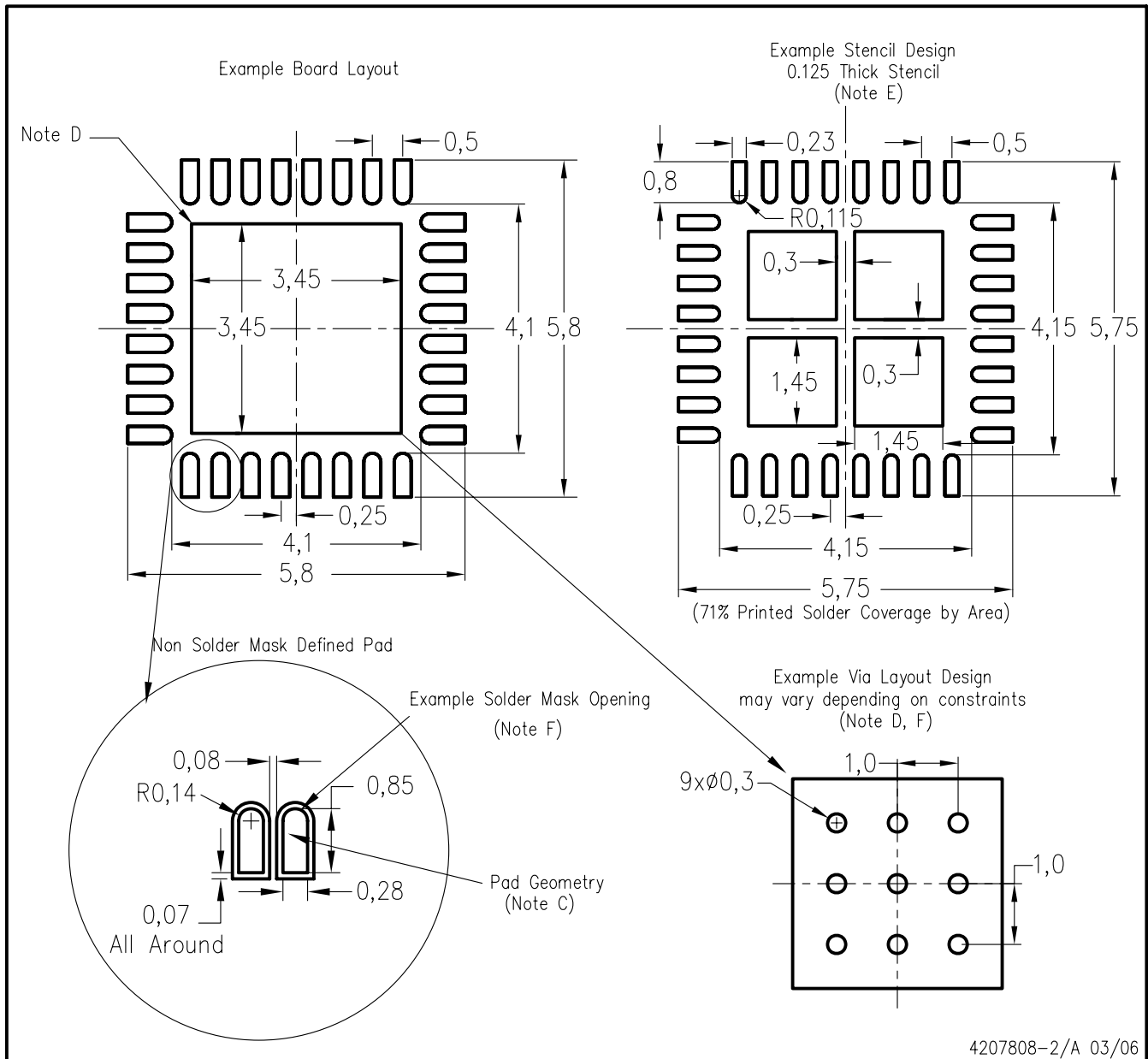


Bottom View

NOTE: All linear dimensions are in millimeters

Exposed Thermal Pad Dimensions

RHB (S-PQFP-N32)



4207808-2/A 03/06

- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Publication IPC-7351 is recommended for alternate designs.
 - D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat-Pack Packages, Texas Instruments Literature No. SCBA017, SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <<http://www.ti.com>>.
 - E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
 - F. Customers should contact their board fabrication site for recommended solder mask tolerances and via tenting recommendations for vias placed in the thermal pad.

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