

## IEEE Std 1394b-2002 PHY AND OHCI LINK DEVICE

### FEATURES

- Fully Supports Provisions of IEEE Std 1394b-2002 Revision 1.33+ at 1-Gigabit Signaling Rates
- Fully Supports Provisions of IEEE Std 1394a-2000 and IEEE Std 1394-1995 for High-Performance Serial Bus
- Fully Interoperable With Firewire™, i.LINK™, and SB1394 Implementations of IEEE Std 1394
- Provides Three Fully Backward-Compatible, (IEEE Std 1394a-2000 Fully Compliant) Bilingual IEEE Std 1394b-2002 Cable Ports at up to 800 Megabits per Second (Mbps)
- Full IEEE Std 1394a-2000 Support Includes:
  - Connection Debounce
  - Arbitrated Short Reset
  - Multispeed Concatenation
  - Arbitration Acceleration
  - Fly-By Concatenation
  - Port Disable/Suspend/Resume
- Extended Resume Signaling for Compatibility With Legacy Digital Video (DV) Devices
- Power-Down Features to Conserve Energy in Battery-Powered Applications
- Low-Power Sleep Mode
- Fully Compliant With Open Host Controller Interface (OHCI) Requirements
- Cable Power Presence Monitoring
- Cable Ports Monitor Line Conditions for Active Connection to Remote Node
- Register Bits Give Software Control of Contender Bit, Power-Class Bits, Link Active Control Bit, and IEEE Std 1394a-2000 Features
- Interoperable With Other 1394 Physical Layers (PHYs) Using 1.8-V, 3.3-V, and 5-V Supplies
- Low-Jitter, External Crystal Oscillator Provides Transmit and Receive Data at 100/200/400/800 Mbps and Link-Layer Controller (LLC) Clock at 49.152 MHz and 98.304 MHz
- Separate Bias (TPBIAS) for Each Port
- Software Device Reset (SWR)
- Fail-Safe Circuitry Senses Sudden Loss of Power to the Device and Disables Ports to Ensure That TSB83AA23 Does Not Load TPBIAS of Any Connected Device and Blocks Any Leakage From the Port Back to Power Plane
- IEEE Std 1394a-2000-Compliant Common-Mode Noise Filter on Incoming Bias Detect Circuit to Filter Out Crosstalk Noise
- Port Programmable to Force IEEE Std 1394a-2000 Mode to Allow Use of IEEE Std 1394a-2000 Connectors (IEEE Std 1394b-2002 Signaling Must Not Be Put Across IEEE Std 1394a-2000 Connectors or Cables)
- 3.3-V and 5-V PCI Signaling Environments
- Serial-Bus Data Rates of 100 Mbps, 200 Mbps, 400 Mbps, and 800 Mbps
- Physical Write Posting of up to Three Outstanding Transactions
- Serial ROM or Boot ROM Interface Supports 2-Wire Serial EEPROM Devices
- 33-MHz/32-Bit PCI Interface
- Multifunction Terminal (MFUNC Terminal 1):
  - PCI\_CLKRUN Protocol Per *PCI Mobile Design Guide*
  - General-Purpose I/O (GPIO)
  - CYCLEIN/CYCLEOUT for External Cycle Timer Control for Customized Synchronization
- PCI Burst Transfers and Deep FIFOs to Tolerate Large Host Latency
  - Transmit FIFO—5K Asynchronous
  - Transmit FIFO—2K Isochronous
  - Receive FIFO—2K Asynchronous
  - Receive FIFO—2K Isochronous
- D0, D1, D2, and D3 Power States and PME Events Per *PCI Bus Power Management Interface Specification*
- Programmable Asynchronous Transmit Threshold
- Isochronous Receive Dual-Buffer Mode

- **Out-of-Order Pipelining for Asynchronous Transmit Requests**
- **Initial-Bandwidth-Available and Initial-Channels-Available Registers**
- **Digital Video and Audio Performance Enhancements**

## DESCRIPTION

The TSB83AA23 is an integrated IEEE Std 1394b-2002 link-layer controller (LLC) design and physical layer (PHY) design combined in a single package to meet the demanding requirements of today's 1394 bus applications. The TSB83AA23 device is capable of exceptional 800-Mbps performance; thus, providing the throughput and bandwidth to move data efficiently and quickly between the PCI and 1394 buses. The TSB83AA23 device also provides outstanding ultralow power operation and intelligent power-management capabilities. The device provides the IEEE 1394 LLC function and PHY function and is compatible with 100-Mbps, 200-Mbps, 400-Mbps, and 800-Mbps serial-bus data rates.

The TSB83AA23 operates as the interface between 33-MHz/32-bit PCI local bus and an IEEE Std 1394a-2000 or IEEE Std 1394b-2002 serial-bus interface. It is capable of supporting serial data rates at 98.304, 196.608, 393.216, 491.52, or 786.432 Mbps (referred to as S100, S200, S400, S400B, or S800 speeds, respectively). When acting as a PCI bus master, the TSB83AA23 device is capable of multiple cache-line bursts of data, which can transfer at 132M bytes/s for 32-bit transfers after connecting to the memory controller.

Due to the high throughput potential of the TSB83AA23 device, it possible to encounter large PCI and legacy 1394 bus latencies, which can cause the 1394 data to be overrun. To overcome this potential problem, the TSB83AA23 implements deep transmit and receive FIFOs to buffer the 1394 data, thus, preventing possible problems due to bus latency. This also ensures that the device can transmit and receive sustained maximum-size isochronous or asynchronous data payloads at S800.

The TSB83AA23 LLC section implements other performance enhancements to improve overall performance of the device, such as a highly-tuned physical data path for enhanced SBP-2 performance, physical post writing buffers, multiple isochronous contexts, and advanced internal arbitration.

The TSB83AA23 LLC section also implements hardware enhancements to better support digital video (DV) and MPEG data stream reception and transmission. These enhancements are enabled through the isochronous receive digital video enhancements register at TI extension offset A80h. These enhancements include automatic time-stamp insertion for transmitted DV and MPEG-formatted streams, and common isochronous packet (CIP) header stripping for received DV streams.

The CIP format is defined by the IEC 61883-1:1998 specification. The enhancements to the isochronous data contexts are implemented as hardware support for the synchronization time stamp for both DV and audio/video CIP formats. The TSB83AA23 device supports modification of the synchronization time-stamp field to ensure that the value inserted via software is not stale — that is, less than the current cycle timer when the packet is transmitted.

The TSB83AA23 performance and enhanced throughput make it an excellent choice for today's 1394 PC market; however, portable, mobile, and even desktop PC power-management schemes continue to require devices to use less and less power, and TI's 1394 product line has continued to raise the bar by providing the lowest-power 1394 devices in the industry. The TSB83AA23 device represents the next evolution of TI commitment to meet the challenge of power-sensitive applications. The TSB83AA23 device has ultralow operational power requirements and intelligent power-management capabilities that allow it to conserve power autonomously based on the device usage. The TSB83AA23 LLC section fully supports D0, D1, D2, and D3<sub>hot/cold</sub> power states, as specified in the *PC 2001 Design Guide* requirements and the *PCI Power Management Specification*. PME wake-event support is subject to operating-system support and implementation.

As required by the *1394 Open Host Controller Interface Specification (OHCI)* and IEEE Std 1394a-2000, internal control registers are memory mapped and nonprefetchable. The PCI configuration header is accessed through configuration cycles as specified by the *PCI Local Bus Specification*, and provides plug-and-play (PnP) compatibility. Furthermore, the TSB83AA23 LLC section is fully compliant with the latest *PCI Local Bus Specification*, *PCI Bus Power Management Interface Specification*, IEEE Std 1394b-2002, IEEE Std 1394a-2000, and *1394 Open Host Controller Interface Specification*.

The TSB83AA23 PHY section provides the digital and analog transceiver functions needed to implement a three-port node in a cable-based IEEE 1394 network. Each cable port incorporates two differential line transceivers. The transceivers include circuitry to monitor the line conditions as needed for determining connection status, for initialization and arbitration, and for packet reception and transmission.

The TSB83AA23 is powered by multiple voltage supplies, 3.3-V supplies for I/O and the LLC section, and a core voltage supply for the PHY section. The core voltage supply is supplied to the PLLVDD\_CORE and DVDD\_CORE terminals in accordance with the requirements in the recommended operating conditions. The PLLVDD\_CORE terminals must be separated from the DVDD\_CORE terminals, the PLLVDD\_CORE terminals are decoupled with 1- $\mu$ F and smaller decoupling capacitors, and the DVDD\_CORE terminals separately decoupled with 1- $\mu$ F and smaller decoupling capacitors. The separation between DVDD\_CORE and PLLVDD\_CORE can be implemented by separate power-supply rails, or by a single power-supply rail, where the DVDD\_CORE and PLLVDD\_CORE are separated by a filter network to keep noise from the PLLVDD\_CORE supply. In addition,  $\overline{\text{REG\_EN}}$  must be asserted low to enable the internal voltage regulator for the LLC section. If  $\overline{\text{REG\_EN}}$  is not pulled low, the a 1.8-V power rail must be applied to the REG18 pins.

The TSB83AA23 requires an external 98.304-MHz crystal oscillator to generate a reference clock. The external clock drives an internal phase-locked loop (PLL), which generates the required reference signal. This reference signal provides the clock signals that control transmission of the outbound encoded information. The power-down (PD) function, when enabled by asserting the PD terminal high, stops operation of the PLL.

Data bits to be transmitted through the cable ports are latched internally, combined serially, encoded, and transmitted at 98.304, 196.608, 393.216, 491.52, or 983.04 Mbps (referred to as S100, S200, S400, S400B, or S800 speed, respectively) as the outbound information stream.

To ensure that the TSB83AA23 conforms to the IEEE Std 1394b-2002 standard, the BMODE terminal must be asserted.

#### NOTE:

The BMODE terminal does not select the cable-interface mode of operation. The BMODE terminal selects the internal PHY section-LLC section interface mode of operation and affects the arbitration modes on the cable. BMODE must be pulled high during normal operation.

The cable interface can follow either the IEEE Std 1394a-2000 protocol or the IEEE Std 1394b-2002 protocol on all ports. The mode of operation is determined by the interface capabilities of the ports being connected. When any of the ports are connected to an IEEE Std 1394a-2000-compliant device, the cable interface on that port operates in the IEEE Std 1394a-2000 data-strobe mode at a compatible S100, S200, or S400 speed. When a bilingual port is connected to an IEEE Std 1394b-2002-compliant node, the cable interface on that port operates per the IEEE Std 1394b-2002 standard at S400B or S800 speed. The TSB83AA23 automatically determines the correct cable interface connection method for the bilingual ports.

To operate a port as an IEEE Std 1394b-2002 bilingual port, the data-strobe-only terminal for the port (DS0 or DS1) must be pulled to ground through a 1-k $\Omega$  resistor. The port must be operated in the IEEE Std 1394b-2002 bilingual mode when an IEEE Std 1394b-2002 bilingual or an IEEE Std 1394b-2002 Beta-only connector is connected to the port. To operate the port as an IEEE Std 1394a-2000-only port, the data-strobe-only terminal (DS0 or DS1) must be pulled to 3.3-V  $V_{CC}$  through a 1-k $\Omega$  resistor. The only time the port must be forced to the data-strobe-only mode is if the port is connected to an IEEE Std 1394a-2000 connector (either 6 pin, which is recommended, or 4 pin). This mode is provided to ensure that IEEE Std 1394b-2002 signaling is never sent across an IEEE Std 1394a-2000 cable.

During packet reception, the serial data bits are split into 2-, 4-, or 8-bit parallel streams by the PHY section and sent to the link-layer controller (LLC) section. The received data is also transmitted (repeated) on the other connected and active cable ports.

Both the twisted pair A (TPA) and the twisted pair B (TPB) cable interfaces incorporate differential comparators to monitor the line states during initialization and arbitration when connected to an IEEE Std 1394a-2000-compliant device. The outputs of these comparators are used by the internal logic to determine the arbitration status. The TPA channel monitors the incoming cable common-mode voltage. The value of this common-mode voltage is used during IEEE Std 1394a-2000-mode arbitration and sets the speed of the next packet transmission. In addition, the TPB channel monitors the incoming cable common-mode voltage on the TPB pair for the presence of the remotely supplied twisted pair bias (TPBIAS) voltage.

When connected to an IEEE Std 1394a-2000-compliant node, the TSB83AA23 PHY section provides a 1.86-V nominal bias voltage at the TPBIAS terminal for port termination. The PHY section contains three independent TPBIAS circuits (one for each port). This bias voltage, when seen through a cable by a remote receiver, indicates the presence of an active connection. This bias voltage source must be stabilized by an external filter capacitor of 1  $\mu$ F.

The line drivers in the TSB83AA23 PHY section are designed to work with external 112- $\Omega$  termination resistor networks to match the 110- $\Omega$  cable impedance. One termination network is required at each end of a twisted-pair cable. Each network is composed of a pair of series-connected 56- $\Omega$  resistors. The midpoint of the pair of resistors that is connected to the TPA terminals is connected to its corresponding TPBIAS voltage terminal. The midpoint of the pair of resistors that is directly connected to the TPB terminals is coupled to ground through a parallel RC network, with recommended values of 5 k $\Omega$  and 270 pF. The values of the external line-termination resistors are selected to meet the standard specifications when connected in parallel with the internal receiver circuits. A precision external resistor connected between the R0 and R1 terminals sets the driver output current, along with other internal operating currents.

When the power supply of the TSB83AA23 is off while the twisted-pair cables are connected, the TSB83AA23 transmitter and receiver circuitry present to the cable a high-impedance signal that does not load the device at the other end of the cable.

When the TSB83AA23 PHY section is used without one or more of the ports brought out to a connector, the twisted-pair terminals of the unused ports must be terminated for reliable operation. For each unused port, the port must be forced to the IEEE Std 1394a-2000-only mode (data-strobe-only mode), after which the TPB+ and TPB– terminals can be tied together and then pulled to ground; or the TPB+ and TPB– terminals can be connected to the suggested normal termination network. The TPA+ and TPA– terminals of an unused port can be left unconnected. The TPBIAS terminal can be connected through a 1- $\mu$ F capacitor to ground or left unconnected.

The TESTM, TESTW, SE, and SM terminals are used to set up various manufacturing test conditions. For normal operation, the TESTM and TESTW terminals must be connected to  $V_{DD}$  through a 1-k $\Omega$  resistor. The SE and SM terminals must be tied to ground through a 1-k $\Omega$  resistor.

Three package terminals are used as inputs to set the default value for three configuration status bits in the self-ID packet. They can be pulled high through a 1-k $\Omega$  resistor or hardwired low as a function of the equipment design. The PC0, PC1, and PC2 terminals indicate the default power class status for the node (the need for power from the cable or the ability to supply power to the cable). The contender bit in the PHY register set indicates that the node is a contender either for the isochronous resource manager (IRM) or for the bus manager (BM). On the TSB83AA23, this bit can be set only by a write to the PHY register set. If a node is to be a contender for IRM or BM, the node software must set this bit in the PHY register set.

The LPS (link power status) terminal of the PHY section works with the LKON terminal to manage the power usage in the node. The PHY\_LPS signal from the LLC section is used with the LCtrl bit to indicate the active/power status of the LLC section. The LPS signal also resets, disables, and initializes the PHY section-LLC section interface (the state of the PHY section-LLC section interface is controlled solely by the LPS input, regardless of the state of the LCtrl bit). The LPS terminal of the PHY section must be connected to the PHY\_LPS terminal of the LLC section during normal operation.

The LPS input is considered inactive if it remains low for more than the LPS\_RESET time (see the LPS terminal definition) and is considered active otherwise. When the PHY section detects that the LPS input is inactive, the PHY section-LLC section interface is placed into a low-power reset state in which the CTL and D outputs are held in the logic 0 state and the LREQ input is ignored; however, the PCLK output remains active. If the LPS input remains low for more than the LPS\_DISABLE time (see the LPS terminal definition), the PHY section-LLC section interface is put into a low-power disabled state in which the PCLK output is also held inactive. The TSB83AA23 continues the necessary PHY repeater functions required for normal network operation, regardless of the state of the PHY section-LLC section interface. When the interface is in the reset or disabled state and the LPS input is again observed active, the PHY section initializes the interface and returns to normal operation. The PHY section-LLC section interface is also held in the disabled state during hardware reset. When the LPS terminal is returned to an active state after being sensed as having entered the LPS\_DISABLE time, the TSB83AA23 issues a bus reset. This broadcasts the node self-ID packet, which contains the updated L bit state (the PHY section and LLC section now being accessible).

The PHY section uses the LKON terminal to notify the LLC section to power up and become active. When activated, the output LKON signal is a square wave. The PHY section activates the LKON output when the LLC section is inactive and a wake-up event occurs. The LLC section is considered inactive when either the LPS input is inactive, as previously described, or the LCtrl bit is cleared to 0. A wake-up event occurs when a link-on PHY packet addressed to this node is received, or conditionally when a PHY interrupt occurs. The PHY section deasserts the LKON output when the LLC section becomes active (both LPS sensed as active and the LCtrl bit set to 1). The PHY section also deasserts the LKON output when a bus reset occurs, unless a PHY interrupt condition exists, which would otherwise cause LKON to be active. If the TSB83AA23 is power cycled and the power class is 0 through 4, the PHY section asserts LKON for approximately 167  $\mu$ s or until both the LPS is active and the LCtrl bit is 1.

**PACKAGING INFORMATION**

Orderable Device	Status <sup>(1)</sup>	Package Type	Package Drawing	Pins	Package Qty	Eco Plan <sup>(2)</sup>	Lead/Ball Finish	MSL Peak Temp <sup>(3)</sup>
TSB83AA23ZAY	ACTIVE	NFBGA	ZAY	167	160	Pb-Free (RoHS)	SNAGCU	Level-3-260C-168 HR

<sup>(1)</sup> The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

<sup>(2)</sup> Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

<sup>(3)</sup> MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

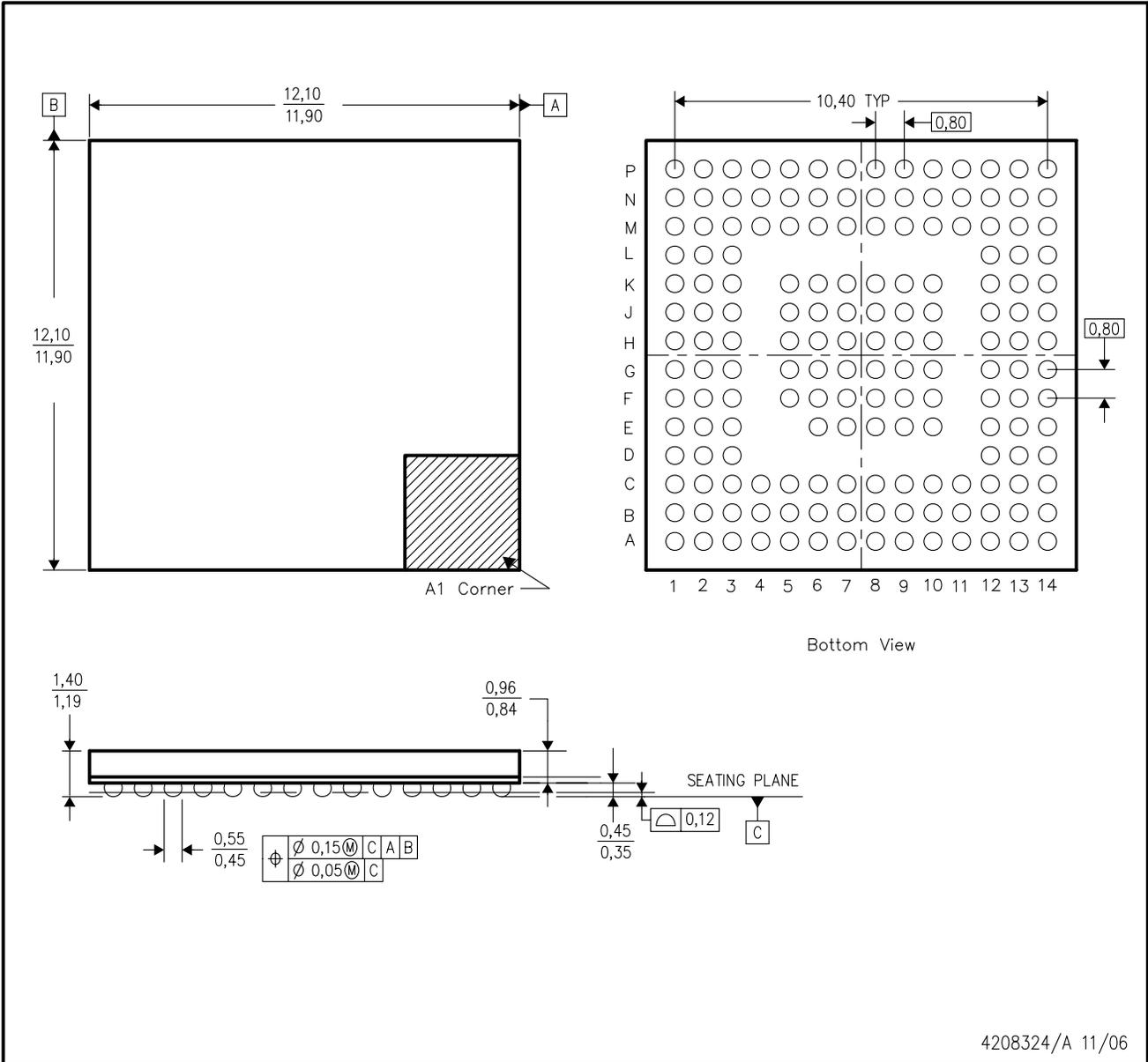
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# MECHANICAL DATA

## ZAY (S-PBGA-N167)

## PLASTIC BALL GRID ARRAY



- NOTES:
- All linear dimensions are in millimeters.
  - This drawing is subject to change without notice.
  - This is a lead-free solder ball design.

4208324/A 11/06

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Logic	<a href="http://logic.ti.com">logic.ti.com</a>	Military	<a href="http://www.ti.com/military">www.ti.com/military</a>
Power Mgmt	<a href="http://power.ti.com">power.ti.com</a>	Optical Networking	<a href="http://www.ti.com/opticalnetwork">www.ti.com/opticalnetwork</a>
Microcontrollers	<a href="http://microcontroller.ti.com">microcontroller.ti.com</a>	Security	<a href="http://www.ti.com/security">www.ti.com/security</a>
RFID	<a href="http://www.ti-rfid.com">www.ti-rfid.com</a>	Telephony	<a href="http://www.ti.com/telephony">www.ti.com/telephony</a>
Low Power Wireless	<a href="http://www.ti.com/lpw">www.ti.com/lpw</a>	Video & Imaging	<a href="http://www.ti.com/video">www.ti.com/video</a>
		Wireless	<a href="http://www.ti.com/wireless">www.ti.com/wireless</a>