TEXAS INSTRUMENTS

TSC2008

1.2V to 3.6V, 12-Bit, Nanopower, 4-Wire Micro TOUCH SCREEN CONTROLLER with SPI™

FEATURES

- 4-Wire Touch Screen Interface
- Single 1.2V to 3.6V Supply/Reference
- Ratiometric Conversion
- Effective Throughput Rate:
  - Up to 20kHz (8 Bit) or 10kHz (12 Bit)
- Preprocessing to Reduce Bus Activity
- SPI Interface
- Simple, Command-Based User Interface:
  - TSC2046 Compatible
  - 8- or 12-Bit Resolution
- On-Chip Temperature Measurement
- Touch Pressure Measurement
- Digital Buffered $\overline{\text{PENIRQ}}$
- On-Chip, Programmable $\overline{\text{PENIRQ}}$ Pullup
- Auto Power-Down Control
- Low Power:
  - 32.4µA at 1.2V, Fast Mode, 8.2kHz Eq Rate
  - 43.8µA at 1.8V, Fast Mode, 8.2kHz Eq Rate
  - 58.4µA at 2.7V, Fast Mode, 8.2kHz Eq Rate
- Software Reset
- Enhanced ESD Protection:
  - ±8kV HBM
  - ±1kV CDM
  - Target ±25kV Air Gap Discharge
  - Target ±15kV Contact Discharge
- 1.5 x 2 WCSP-12 and 4 x 4 QFN-16 Packages

U.S. Patent No. 6246394; other patents pending.

APPLICATIONS

- Cellular Phones
- PDA, GPS, and Media Players
- Portable Instruments
- Point-of-Sale Terminals
- Multiscreen Touch Control

DESCRIPTION

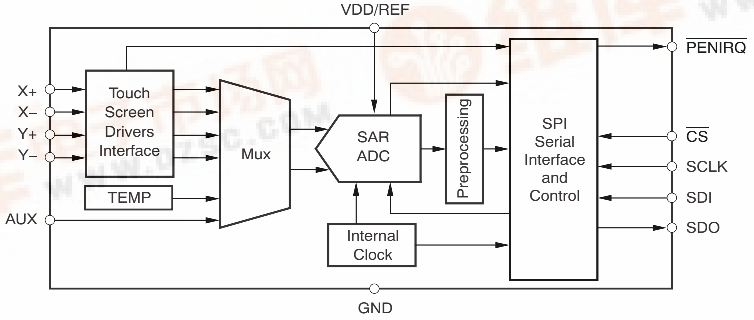
The TSC2008 is a very low-power touch screen controller designed to work with power-sensitive, handheld applications that are based on advanced low-voltage processors. It works with a supply voltage as low as 1.2V, which can be supplied by a single-cell battery. It contains a complete, ultra-low power, 12-bit, analog-to-digital (A/D) resistive touch screen converter, including drivers and the control logic to measure touch pressure.

In addition to these standard features, the TSC2008 offers preprocessing of the touch screen measurements to reduce bus loading, thus reducing the consumption of host processor resources that can then be redirected to more critical functions.

The TSC2008 supports an SPI serial bus and data transmission protocol in all three defined modes: standard, fast, and high-speed. It offers programmable resolution of 8 or 12 bits to accommodate different screen sizes and performance needs.

The TSC2008 is available in a 12-lead, (1,555 ±0,055mm) x (2,055 ±0,055mm) 3 x 4 array, wafer chip-scale package (WCSP), and a 16-pin, 4 x 4 QFN package. The TSC2008 is characterized for the –40°C to +85°C industrial temperature range.

PRODUCT PREVIEW



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ORDERING INFORMATION(1)

PRODUCT	TYPICAL INTEGRAL LINEARITY (LSB)	TYPICAL GAIN ERROR (LSB)	NO MISSING CODES RESOLUTION (BITS)	PACKAGE TYPE	PACKAGE DESIGNATOR	SPECIFIED TEMPERATURE RANGE	PACKAGE MARKING	ORDERING NUMBER	TRANSPORT MEDIA, QUANTITY
TSC2008I	±1.5	–0.2/+4.4	11	16-Pin, 4 x 4 QFN	RGV	–40°C to +85°C	TSC2008I	TSC2008RGVT	Small Tape and Reel, 250
								TSC2008RGVR	Tape and Reel, 25000
				12-Pin, 3 x 4 Matrix, 1.5 x 2 WCSP	YZG	–40°C to +85°C	TSC2008I	TSC2008IYZGT	Small Tape and Reel, 250
								TSC2008IYZGR	Tape and Reel, 3000

(1) For the most current package and ordering information, see the Package Option Addendum located at the end of this data sheet, or see the TI website at www.ti.com.

ABSOLUTE MAXIMUM RATINGS(1)

Over operating free-air temperature range (unless otherwise noted).

PARAMETER			TSC2008	UNIT
Voltage	Analog input X+, Y+, AUX to GND		–0.4 to VDD + 0.1	V
	Analog input X–, Y– to GND		–0.4 to VDD + 0.1	V
Voltage range	VDD to GND		–0.3 to +5	V
Digital input voltage to GND			–0.3 to VDD + 0.3	V
Digital output voltage to GND			–0.3 to VDD + 0.3	V
Power dissipation			$(T_J \text{ Max} - T_A)/\theta_{JA}$	
Thermal impedance, θ_{JA}	QFN package		47	°C/W
	WCSP	Low-K	113	°C/W
		High-K	62	°C/W
Operating free-air temperature range, T_A			–40 to +85	°C
Storage temperature range, T_{STG}			–65 to +150	°C
Junction temperature, T_J Max			+150	°C
Lead temperature	Vapor phase (60 sec)		+215	°C
	Infrared (15 sec)		+220	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated is not implied. Exposure to absolute-maximum rated conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

At T_A = –40°C to +85°C, V_{DD} = +1.2V to +3.6V, unless otherwise noted.

PARAMETER		TEST CONDITIONS		TSC2008			UNIT
				MIN	TYP	MAX	
AUXILIARY ANALOG INPUT							
Input voltage range				0		V_{DD}	V
Input capacitance					12		pF
Input leakage current				–1		+1	µA
A/D CONVERTER							
Resolution		Programmable: 8 or 12 bits				12	Bits
No missing codes		12-bit resolution		11			Bits
Integral linearity					±1.5		LSB(1)
Offset error		V_{DD} = 1.8V			–0.8 to +0.3		LSB
		V_{DD} = 3.0V			+3.2 to +8.9		LSB
Gain error		V_{DD} = 1.8V			–0.2 to 0		LSB
		V_{DD} = 3.0V			+3.8 to +4.4		LSB
TOUCH SENSORS							
$\overline{\text{PENIRQ}}$ pull-up resistor, R_{IRQ}		T_A = +25°C, V_{DD} = 1.8V, command '1011' set '0000'			51		kΩ
		T_A = +25°C, V_{DD} = 1.8V, command '1011' set '0001'			90		kΩ
Switch on-resistance	Y+, X+				6		Ω
	Y–, X–				5		Ω
Switch drivers drive current(2)		100ms duration				50	mA
INTERNAL TEMPERATURE SENSOR							
Temperature range				–40		+85	°C
Resolution		Differential method(3)	V_{DD} = 3V		1.6		°C/LSB
			V_{DD} = 1.6V		1.6		°C/LSB
		TEMP1(4)	V_{DD} = 3V		0.3		°C/LSB
			V_{DD} = 1.6V		0.3		°C/LSB
Accuracy		Differential method(3)	V_{DD} = 3V		±2		°C/LSB
			V_{DD} = 1.6V		±2		°C/LSB
		TEMP1(4)	V_{DD} = 3V		±3		°C/LSB
			V_{DD} = 1.6V		±3		°C/LSB
INTERNAL OSCILLATOR							
Internal clock frequency, f_{CCLK}		8-Bit	V_{DD} = 1.2V		3.19		MHz
			V_{DD} = 1.8V		3.66		MHz
			V_{DD} = 2.7V		3.78		MHz
			V_{DD} = 3.6V		3.82		MHz
		12-Bit	V_{DD} = 1.2V		1.6		MHz
			V_{DD} = 1.8V		1.83		MHz
			V_{DD} = 2.7V		1.88		MHz
			V_{DD} = 3.6V		1.91		MHz
Frequency drift		V_{DD} = 1.6V			0.0056		%/°C
		V_{DD} = 3.0V			0.012		%/°C

(1) LSB means *least significant bit*. With V_{DD} (REF) = +2.5V, 1LSB is 610µV.
(2) Assured by design, but not production tested. Exceeding 50mA source current may result in device degradation.
(3) Difference between TEMP1 and TEMP2 measurement; no calibration necessary.
(4) Temperature drift is –2.1mV/°C.

PRODUCT PREVIEW

ELECTRICAL CHARACTERISTICS (continued)

At T_A = –40°C to +85°C, V_{DD} = +1.2V to +3.6V, unless otherwise noted.

PARAMETER		TEST CONDITIONS			TSC2008			UNIT
					MIN	TYP	MAX	
DIGITAL INPUT/OUTPUT								
Logic family					CMOS			
Logic level	V_{IH}	$1.2V \le V_{DD} < 1.6V$			$0.7 \times V_{DD}$		$V_{DD} + 0.3$	V
		$1.6V \le V_{DD} \le 3.6V$			$0.7 \times V_{DD}$		$V_{DD} + 0.3$	V
	V_{IL}	$1.2V \le V_{DD} < 1.6V$			–0.3		$0.2 \times V_{DD}$	V
		$1.6V \le V_{DD} \le 3.6V$			–0.3		$0.3 \times V_{DD}$	V
	I_{IL}	$\overline{\text{CS}}$, SCLK, and SDI pins			–1		1	µA
	C_{IN}	$\overline{\text{CS}}$, SCLK, and SDI pins					10	pF
	V_{OH}	I_{OH} = 2 TTL loads			$V_{DD} - 0.2$		V_{DD}	V
	V_{OL}	I_{OL} = 2 TTL loads			0		0.2	V
	I_{LEAK}	Floating output			–1		1	µA
	C_{OUT}	Floating output					10	pF
Data format					Straight Binary			
POWER SUPPLY REQUIREMENTS								
Power-supply voltage								
V_{DD}		Specified performance			1.2		3.6	V
Quiescent supply current (V_{DD} with sensor off)		12-bit f_{SCLK} = 10MHz, f_{ADC} = 1MHz, PD[1:0] = 0,0	V_{DD} = 1.2V	36.4k eq rate		128	190	µA
				8.2k eq rate		32.4	48	µA
			V_{DD} = 1.8V	36.4k eq rate		165	240	µA
				8.2k eq rate		43.8	60	µA
			V_{DD} = 2.7V	36.4k eq rate		226.2	335	µA
				8.2k eq rate		63.4	84	µA
Power-down supply current		$\overline{\text{CS}}$ = 1, SDI = SCLK = 1, PD[1:0] = 0,0				0	0.8	µA

PACKAGE OPTION ADDENDUM

23-Jun-2008

PACKAGING INFORMATION

Orderable Device	Status [1]	Package Type	Package Drawing	Pins	Package Qty	Eco Plan [2]	Lead/Ball Finish	MSL Peak Temp [3]
TSC2008IRGVR	PREVIEW	QFN	RGV	16	2500	TBD	Call TI	Call TI
TSC2008IRGVT	PREVIEW	QFN	RGV	16	250	TBD	Call TI	Call TI
TSC2008IYZGR	PREVIEW	DSBGA	YZG	12	3000	TBD	Call TI	Call TI
TSC2008IYZGT	PREVIEW	DSBGA	YZG	12	250	TBD	Call TI	Call TI

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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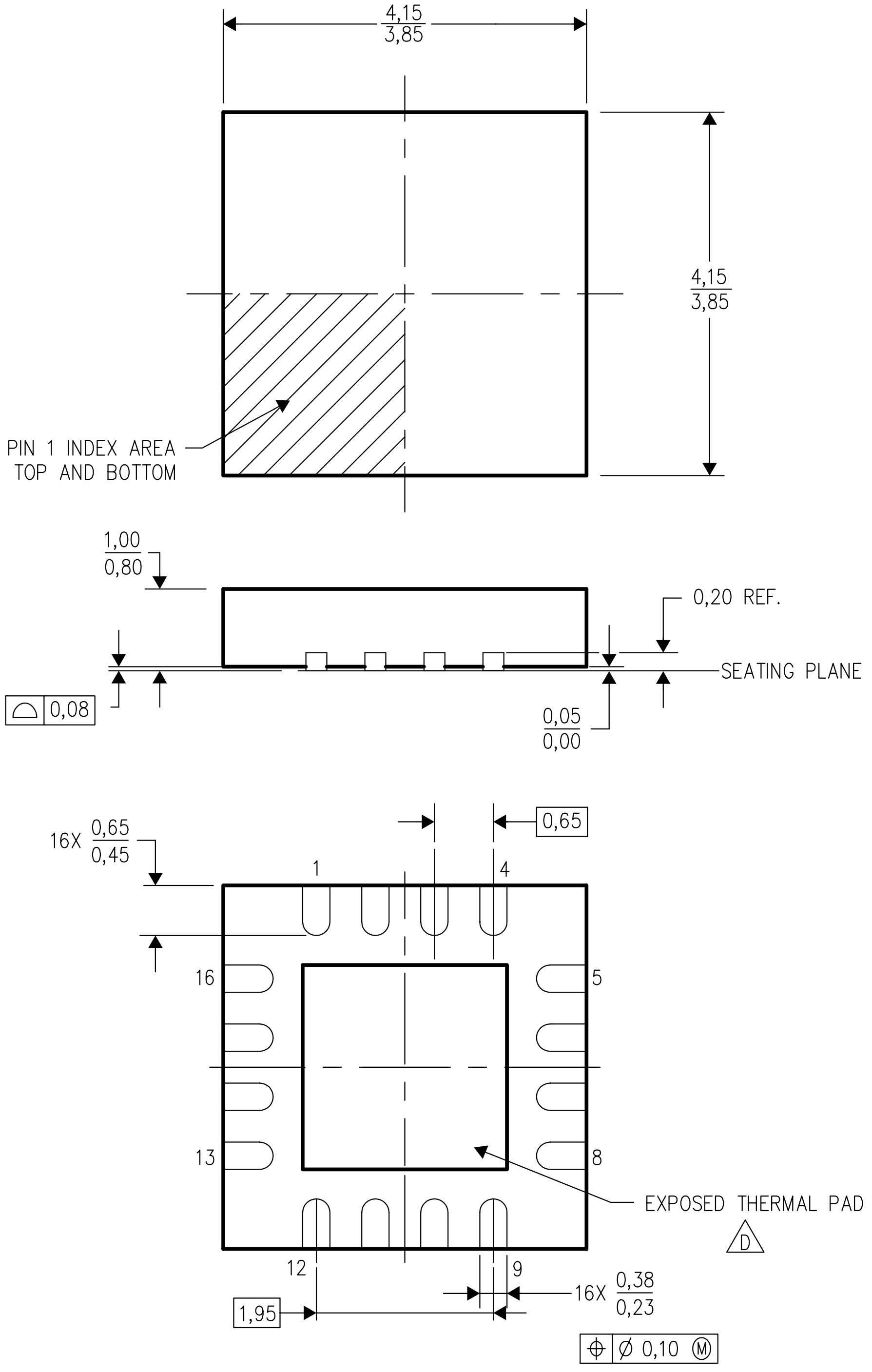
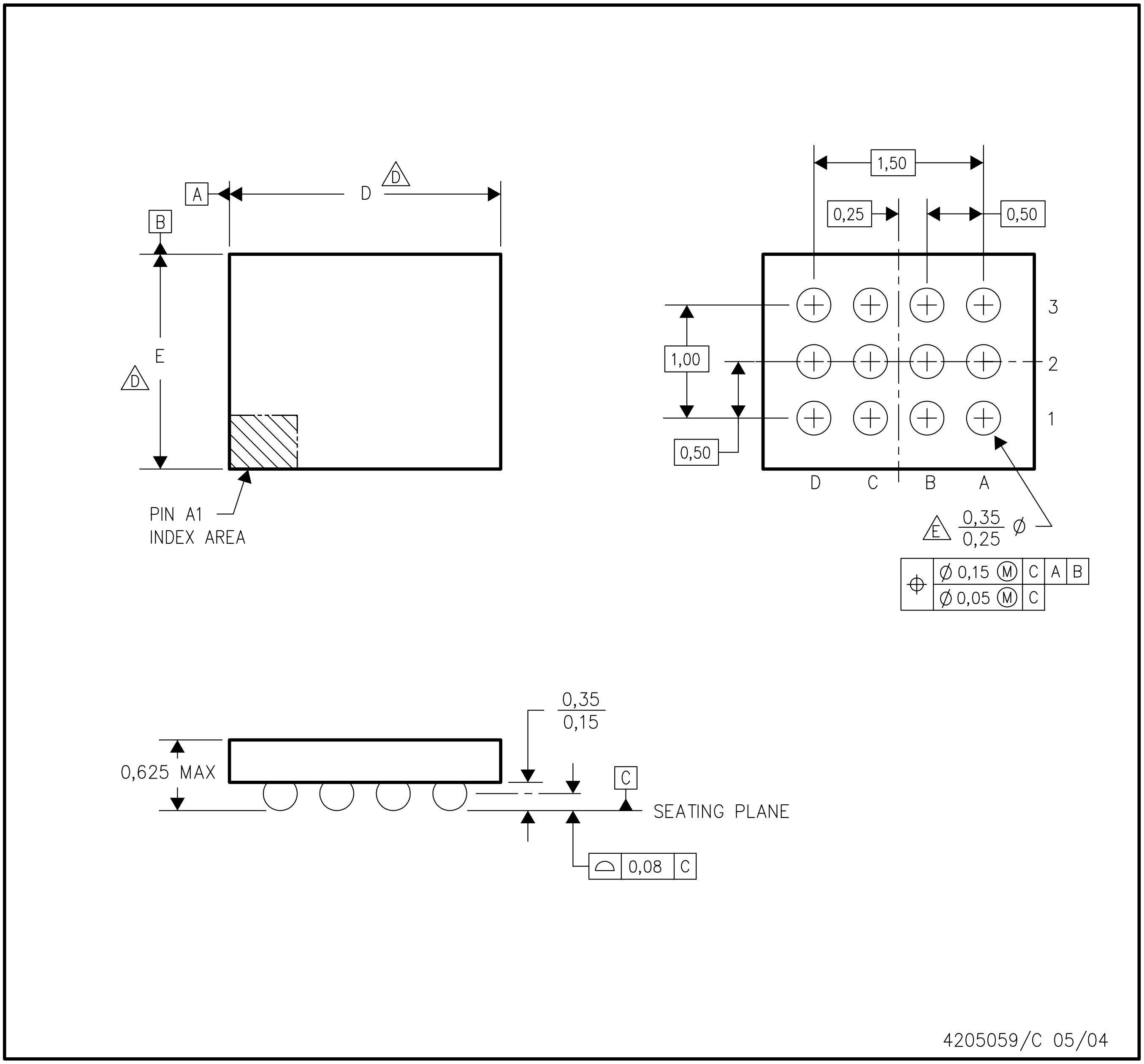
RGV (S-PQFP-N16) PLASTIC QUAD FLATPACK



NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M−1994.
- B. This drawing is subject to change without notice.
- C. Quad Flatpack, No−leads (QFN) package configuration.
- D. The package thermal pad must be soldered to the board for thermal and mechanical performance. See the Product Data Sheet for details regarding the exposed thermal pad dimensions.
- E. Falls within JEDEC MO−220.

YZG (R–XBGA–N12) DIE–SIZE BALL GRID ARRAY



NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. NanoFree™ package configuration.
- D. Devices in YZG package can have dimension D ranging from 1.85 to 2.65 mm and dimension E ranging from 1.35 to 2.15 mm. To determine the exact package size of a particular device, refer to the device datasheet or contact a local TI representative.
- E. Reference Product Data Sheet for array population. 4 x 3 matrix pattern is shown for illustration only.
- F. This package contains lead–free balls. Refer to YEG (Drawing #4204182) for tin–lead (SnPb) balls.

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