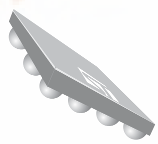
TS472

Very low noise microphone preamplifier with 2.0V bias output and active low standby mode

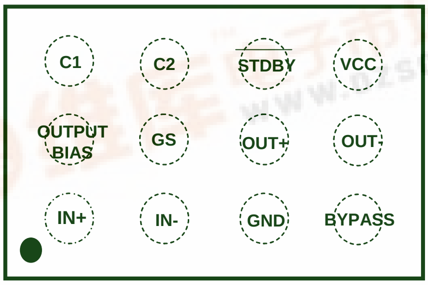
Features

- Low noise: 10nV/√Hz typ. equivalent input noise @ F = 1kHz
- Fully differential input/output
- 2.2V to 5.5V single supply operation
- Low power consumption @20dB: 1.8mA
- Fast start up time @ 0dB: 5ms typ.
- Low distortion: 0.1% typ.
- 40kHz bandwidth regardless of the gain
- Active low standby mode function (1µA max)
- Low noise 2.0V microphone bias output
- Available in flip-chip lead-free package and in QFN24 4x4mm package
- ESD protection (2kV)

Flip-chip - 12 bumps

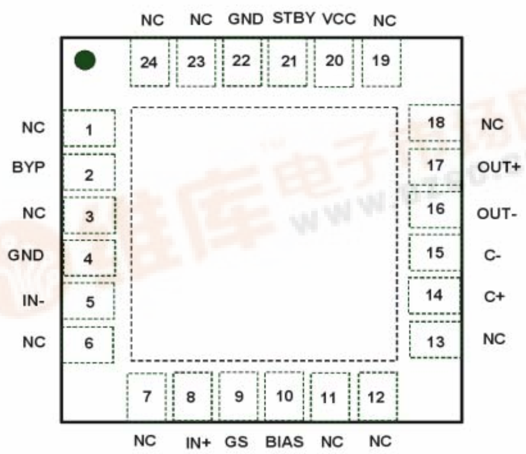


Pin Connections (top view)



QFN24

Pin Connection (top view)



Description

The TS472 is a differential-input microphone preamplifier optimized for high-performance, PDA and notebook audio systems.

This device features an adjustable gain from 0dB to 40dB with excellent power-supply and common-mode rejection ratios. In addition, the TS472 has a very low-noise microphone bias generator of 2V.

It also includes a complete shutdown function, with active low standby mode.

Applications

- Video and photo cameras with sound input
- Sound acquisition & voice recognition
- Video conference systems
- Notebook computers and PDAs

Contents

1 Ordering information

Table 1. Order codes

Part number	Temperature range	Package	Packing	Marking
TS472EIJT	-40°C, +85°C	Flip-chip	Tape & reel	472
TS472IQT	-40°C, +85°C	QFN24 4x4mm	Tape & reel	K472

2 Typical application schematic

Figure 1 shows a typical application schematic for the TS472.

Figure 1. Application schematic (flip-chip)

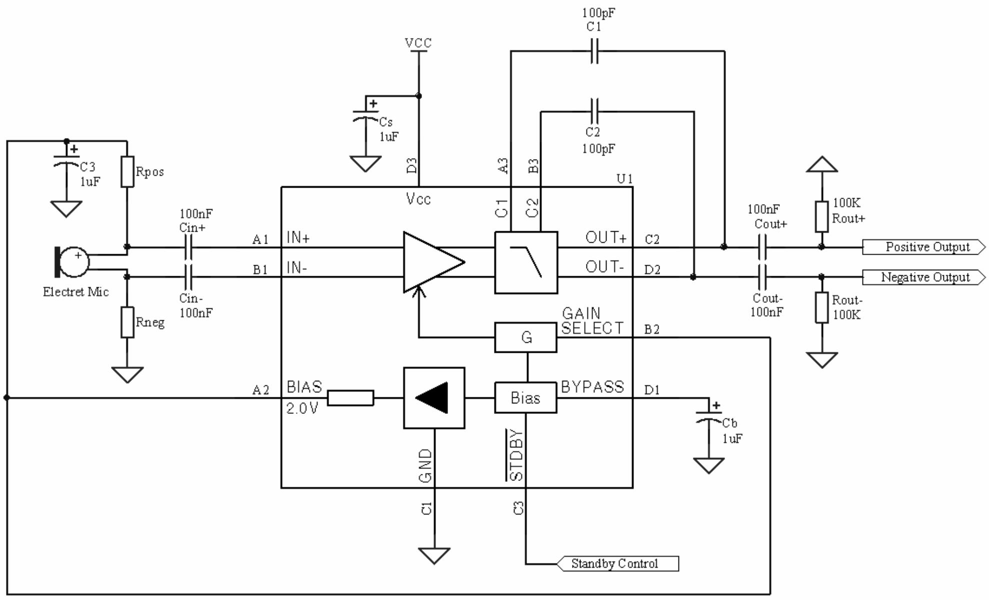


Table 2. External component descriptions

Components	Functional description
C_{in+}, C_{in-}	Input coupling capacitors that block the DC voltage at the amplifier input terminal.
C_{out+}, C_{out-}	Output coupling capacitors that block the DC voltage coming from the amplifier output terminal (pins C2 and D2) and determine *Lower cut-off frequency*.
R_{out+}, R_{out-}	Output load resistors used to charge the output coupling capacitors C_{out}. These output resistors can be represented by an input impedance of a following stage.
R_{pos}, R_{neg}	Polarizing resistors for biasing of a microphone.
C_s	Supply bypass capacitor that provides power supply filtering.
C_b	Bypass pin capacitor that provides half-supply filtering.
C_1, C_2	Low pass filter capacitors allowing to cut the high frequency.

3 Absolute maximum ratings

Table 3. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{CC}	Supply voltage (1)	6	V
V_i	Input voltage	-0.3 to V_{CC}+0.3	V
T_{oper}	Operating free air temperature range	-40 to + 85	°C
T_{stg}	Storage temperature	-65 to +150	°C
T_j	Maximum junction temperature	150	°C
R_{thja}	Thermal resistance junction to ambient: Flip-chip QFN24	180 110	°C/W
ESD	Human body model	2	kV
ESD	Machine model	200	V
	Lead temperature (soldering, 10sec)	250	°C

1. All voltages values are measured with respect to the ground pin.

Table 4. Operating conditions

Symbol	Parameter	Value	Unit
V_{CC}	Supply voltage	2.2 to 5.5	V
A	Typical differential gain (GS connected to 4.7kΩ or bias)	20	dB
V_{STBY}	Standby voltage input: Device ON Device OFF	$1.5 \leq V_{STBY} \leq V_{CC}$ $GND \leq V_{STBY} \leq 0.4$	V
T_{op}	Operational free air temperature range	-40 to +85	°C
R_{thja}	Thermal resistance junction to ambient: Flip-chip QFN24	150 60	°C/W

4 Electrical characteristics

Table 5. Electrical characteristics at V_{CC} = 3V with GND = 0V, T_{amb} = 25°C (unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Unit
e_n	Equivalent input noise voltage density R_{EQ}=100Ω at 1KHz		10		$\frac{nV}{\sqrt{Hz}}$
THD+N	Total harmonic distortion + noise 20Hz ≤ F ≤ 20kHz, Gain=20dB, V_{in}=50mV_{RMS}		0.1		%
V_{in}	Input voltage, Gain=20dB		10	70	mV_{RMS}
B_W	Bandwidth @ -3dB Bandwidth @ -1dB pin A3, B3 floating		40 20		kHz
G	Overall output voltage gain (Rgs variable): Minimum gain, Rgs infinite Maximum gain, Rgs=0	-3 39.5	-1.5 41	0 42.5	dB
Z_{in}	Input impedance referred to GND	80	100	120	kΩ
R_{LOAD}	Resistive load	10			kΩ
C_{LOAD}	Capacitive load			100	pF
I_{CC}	Supply current, Gain=20dB		1.8	2.4	mA
I_{STBY}	Standby current			1	µA
PSRR	Power supply rejection ratio, Gain=20dB, F=217Hz, V_{ripple}=200mVpp, inputs grounded Differential output Single-ended outputs,		-70 -46		dB

Table 6. Bias output: V_{CC} = 3V, GND = 0V, T_{amb} = 25°C (unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{out}	No load condition	1.9	2	2.1	V
R_{out}	Output resistance	80	100	120	W
I_{out}	Output bias current		2		mA
PSRR	Power supply rejection ratio, F=217Hz, V_{ripple}=200mVpp	70	80		dB

Table 7. Differential RMS noise voltage

Gain (dB)	Input referred noise voltage (μV_{RMS})		Output noise voltage (μV_{RMS})	
	Unweighted filter	A-weighted filter	Unweighted filter	A-weighted filter
0	15	10	15	10
20	3.4	2.3	34	23
40	1.4	0.9	141	91

Table 8. Bias output RMS noise voltage

C_{out} (µF)	Unweighted filter (μV_{RMS})	A-weighted filter (μV_{RMS})
1	5	4.4
10	2.2	1.2

Table 9. SNR (signal to noise ratio), THD+N < 0.5%

Gain (dB)	Unweighted filter (dB)			A-weighted filter (dB)		
	V_{CC}=2.2V	V_{CC}=3V	V_{CC}=5.5V	V_{CC}=2.2V	V_{CC}=3V	V_{CC}=5.5V
0	75	76	76	79	80	80
20	82	83	83	89	90	90
40	70	72	74	80	82	84

Note: Unweighted filter = 20Hz ≤ F ≤ 20kHz

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Current consumption vs. power supply voltage	Figure 2 and Figure 3
Current consumption vs. standby voltage	Figure 4 and Figure 5
Standby threshold voltage vs. power supply voltage	Figure 6
Frequency response	Figure 7
Bias output voltage vs. bias output current	Figure 8
Bias output voltage vs. power supply voltage	Figure 9
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Maximum input voltage vs. power supply voltage, THD+N<1%	Figure 21
THD+N vs. input voltage	Figure 22 to Figure 27
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Figure 2. Current consumption vs. power supply voltage

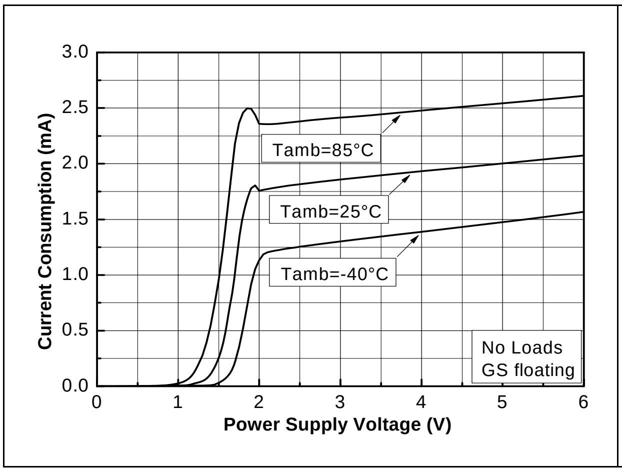


Figure 3. Current consumption vs. power supply voltage

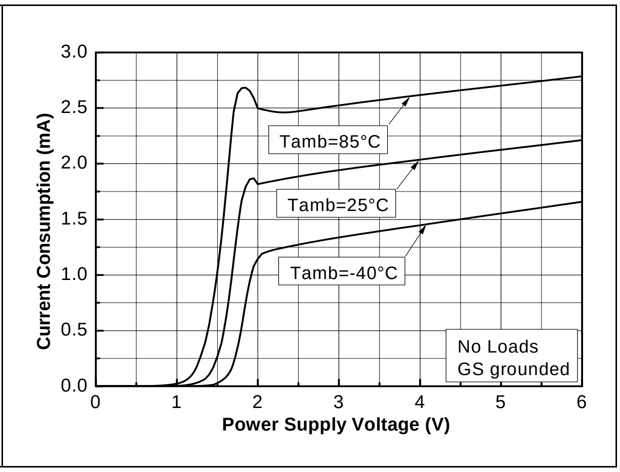


Figure 4. Current consumption vs. standby voltage

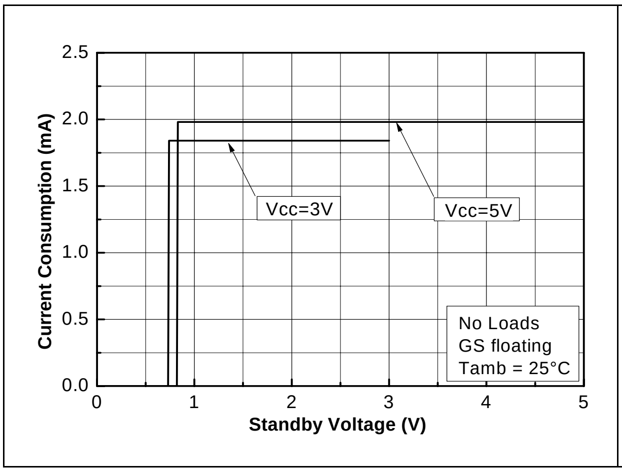


Figure 5. Current consumption vs. standby voltage

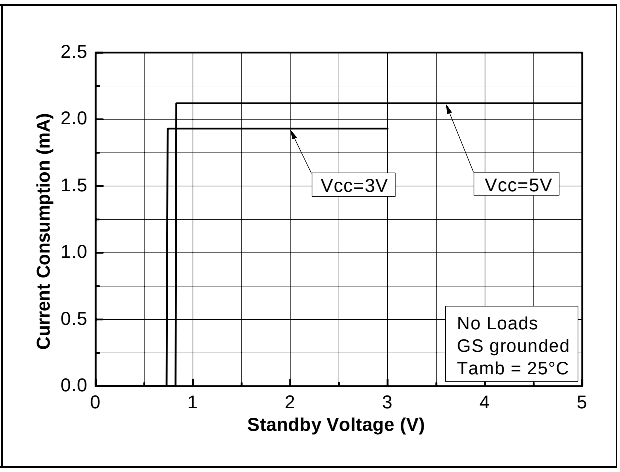


Figure 6. Standby threshold voltage vs. power supply voltage

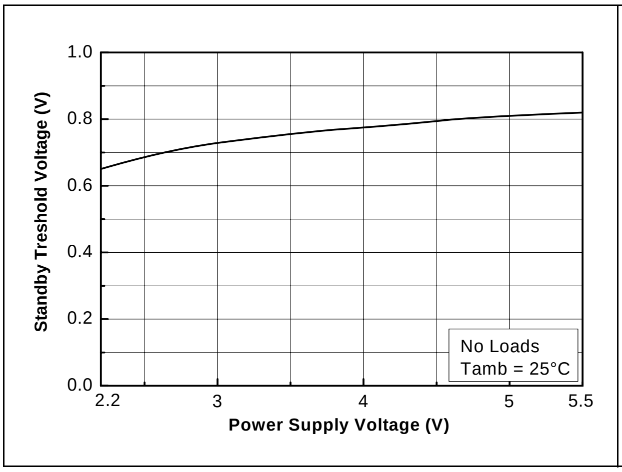


Figure 7. Frequency response

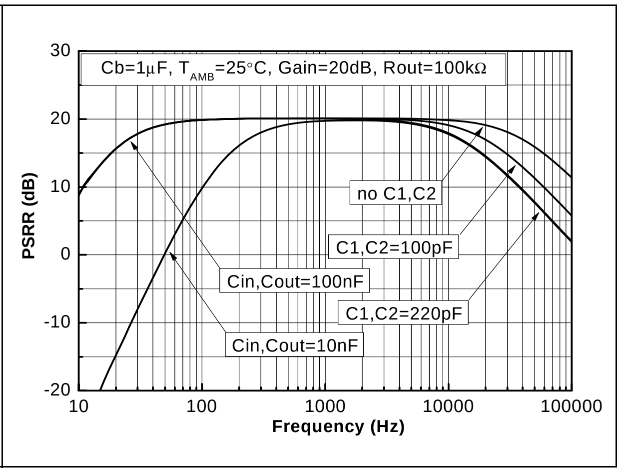


Figure 8. Bias output voltage vs. bias output current

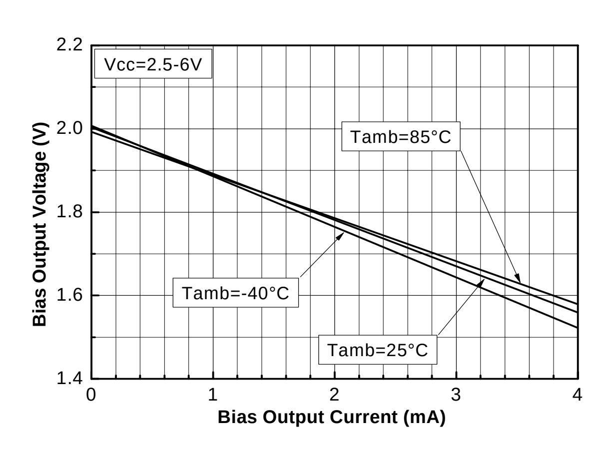


Figure 9. Bias output voltage vs. power supply voltage

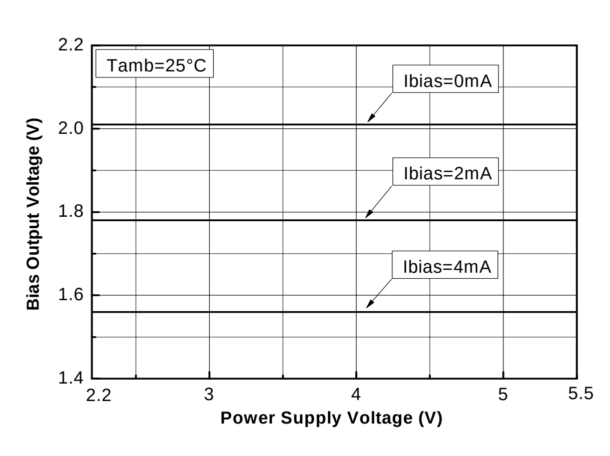


Figure 10. Bias PSRR vs. frequency

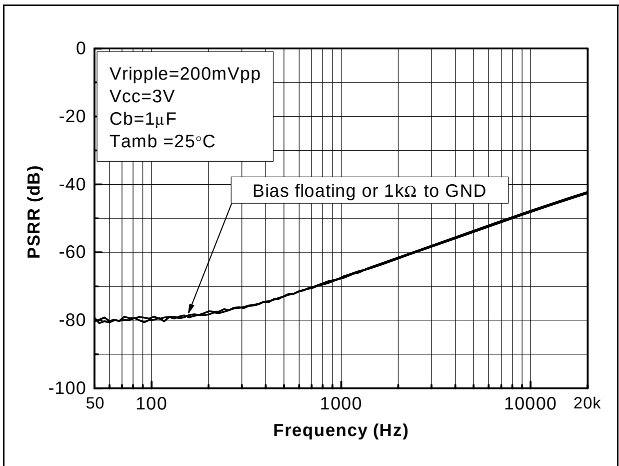


Figure 11. Bias PSRR vs. frequency

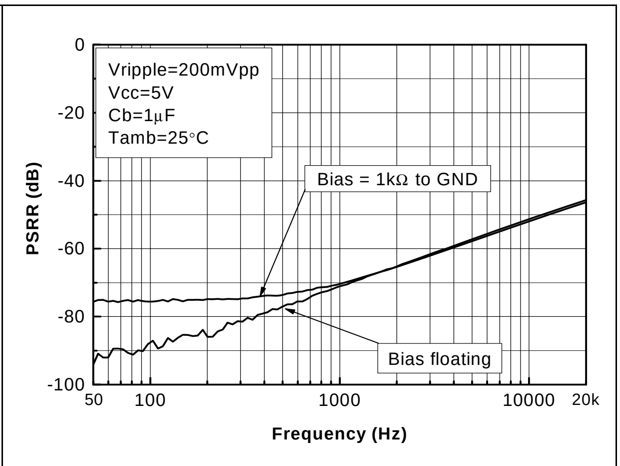


Figure 12. Differential output PSRR vs. frequency

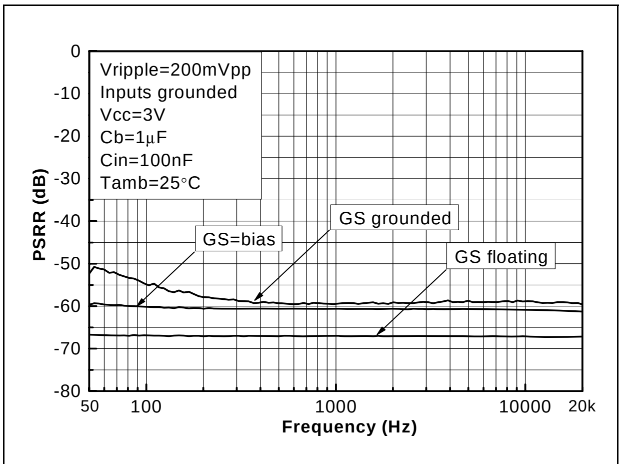


Figure 13. Differential output PSRR vs. frequency

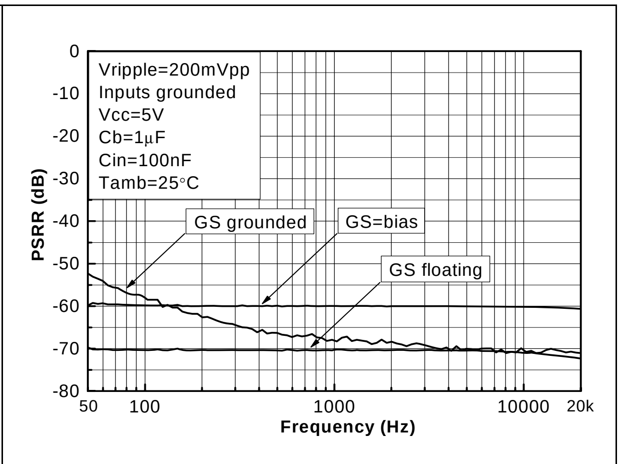


Figure 14. Differential output PSRR vs. frequency

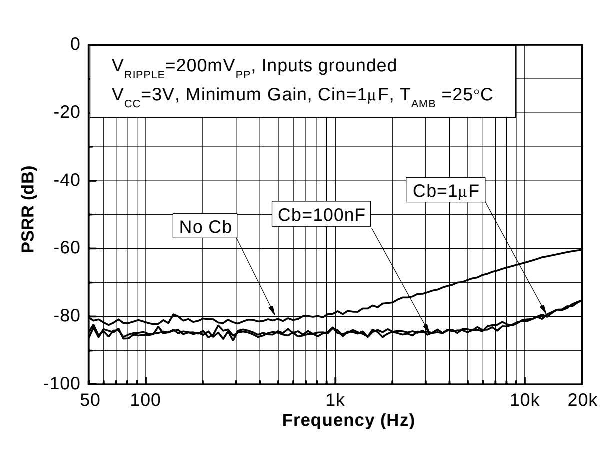


Figure 15. Differential output PSRR vs. frequency

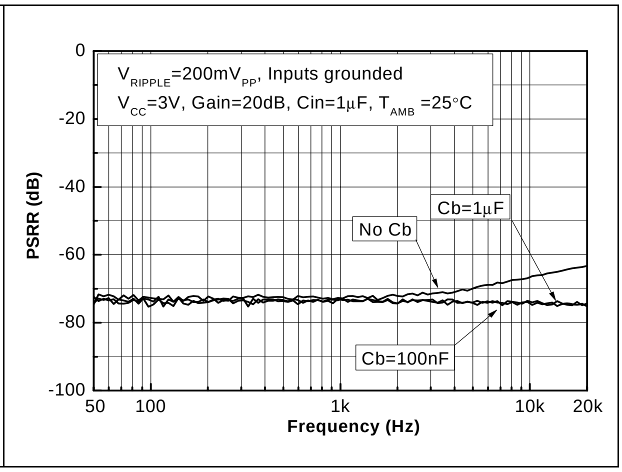


Figure 16. Single-ended output PSRR vs. frequency

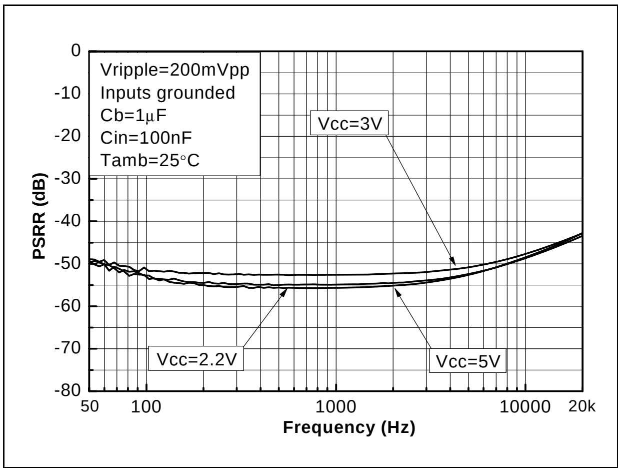


Figure 17. Equivalent input noise voltage density

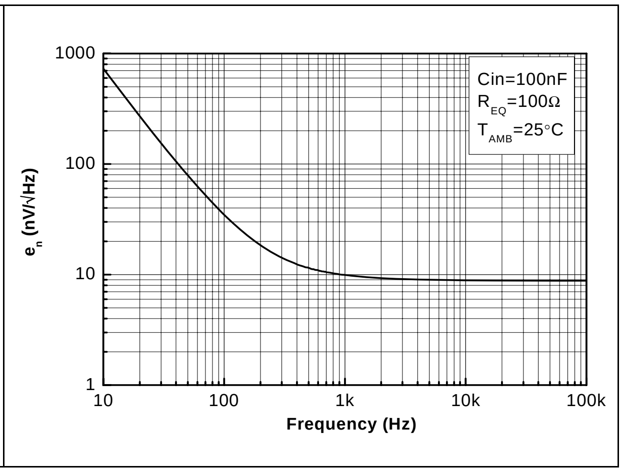


Figure 18. Δgain vs. power supply voltage

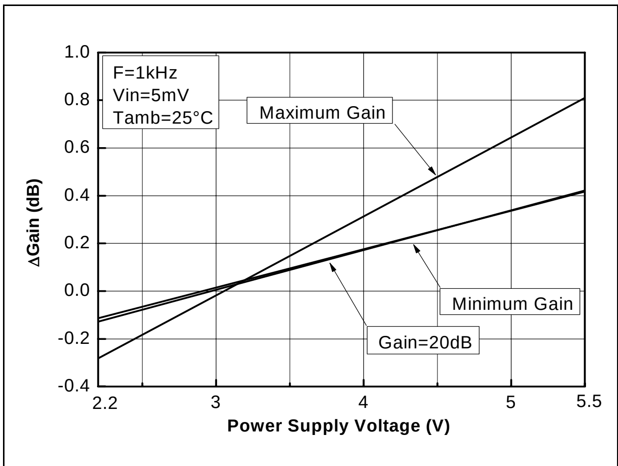


Figure 19. Δgain vs. ambient temperature

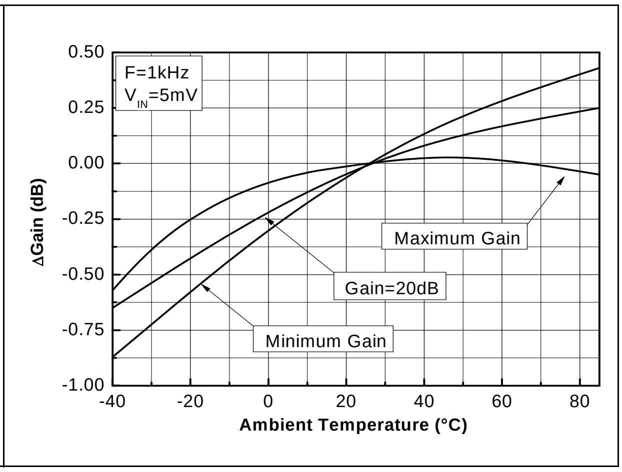


Figure 20. Maximum input voltage vs. gain, THD+N<1%

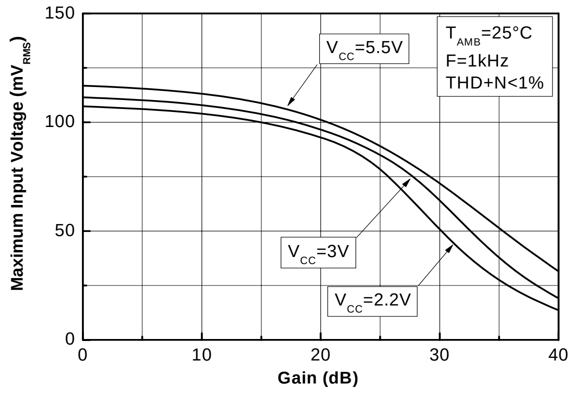


Figure 21. Maximum input voltage vs. power supply voltage, THD+N<1%

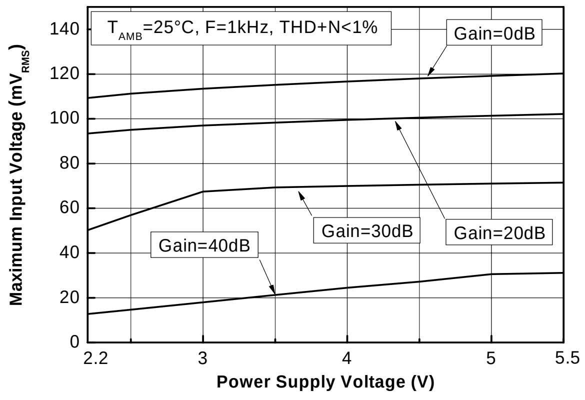


Figure 22. THD+N vs. input voltage

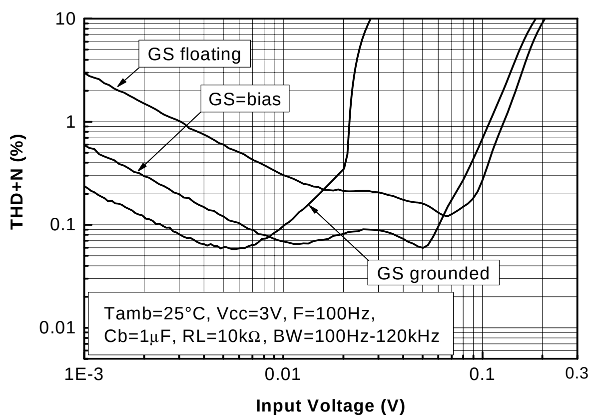


Figure 23. THD+N vs. input voltage

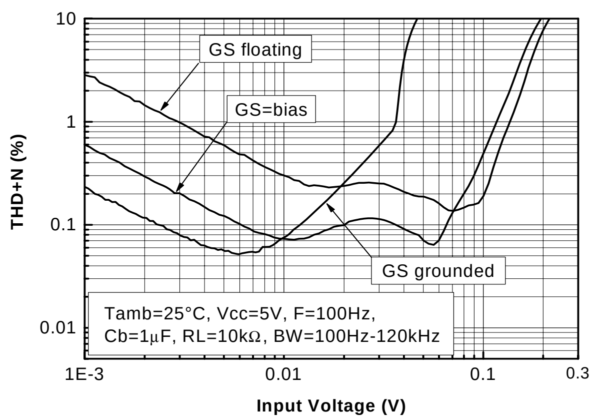


Figure 24. THD+N vs. input voltage

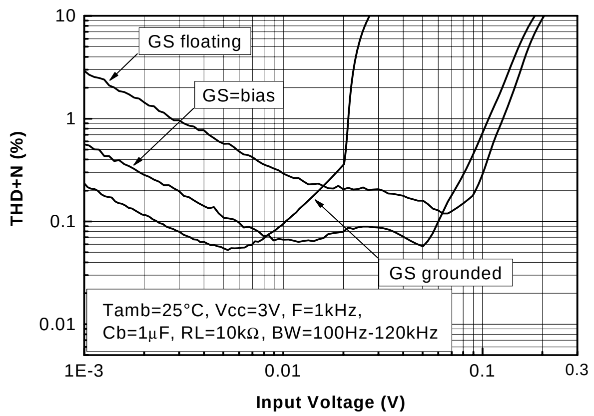


Figure 25. THD+N vs. input voltage

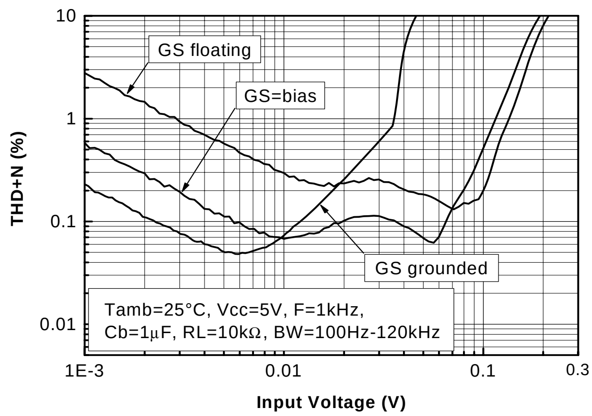


Figure 26. THD+N vs. input voltage

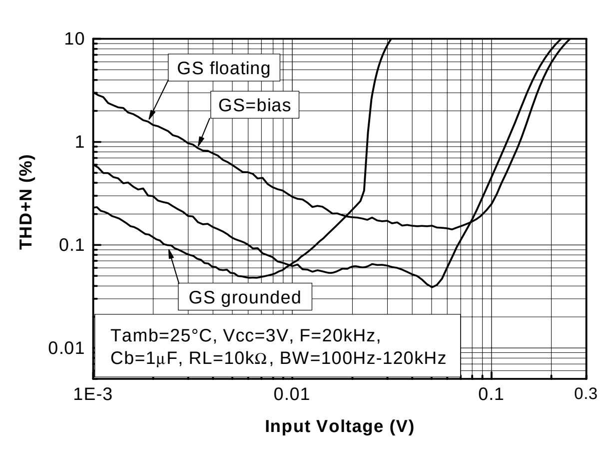


Figure 27. THD+N vs. input voltage

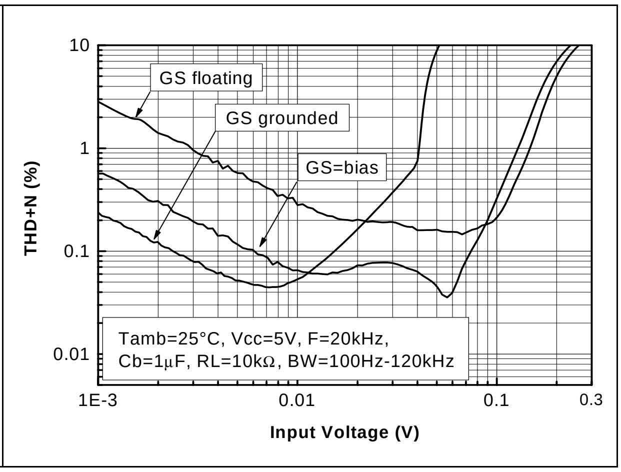


Figure 28. THD+N vs. frequency

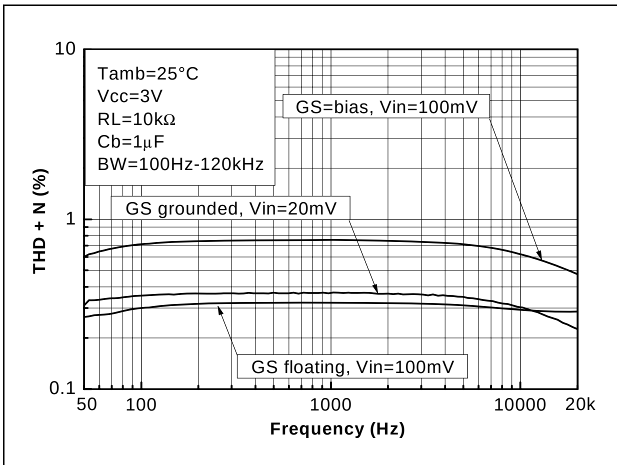


Figure 29. THD+N vs. frequency

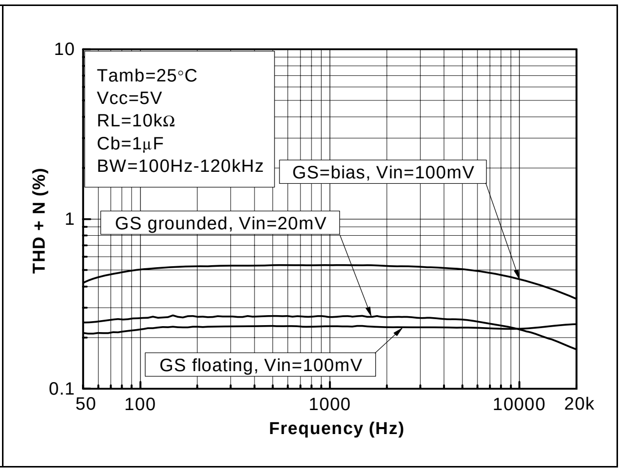


Figure 30. Transient response

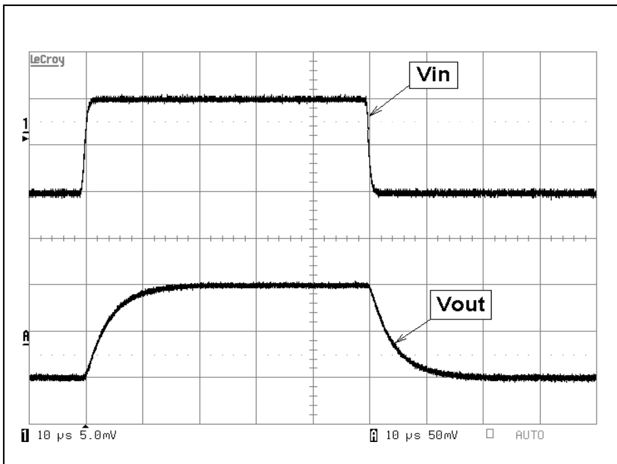
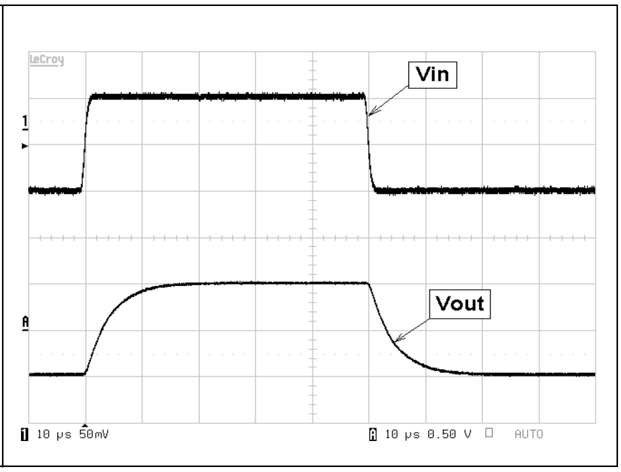


Figure 31. Transient response



5 Application information

5.1 Differential configuration principle

The TS472 is a full-differential input/output microphone preamplifier. The TS472 also includes a common mode feedback loop that controls the output bias value to average it at $V_{CC}/2$. This allows the device to always have a maximum output voltage swing, and by consequence, maximize the input dynamic voltage range.

The **advantages** of a full-differential amplifier are:

- Very high PSRR (power supply rejection ratio).
- High common mode noise rejection.
- In theory, the filtering of the internal bias by an external bypass capacitor is not necessary. But, to reach maximum performance in all tolerance situations, it is better to keep this option.

5.2 Higher cut-off frequency

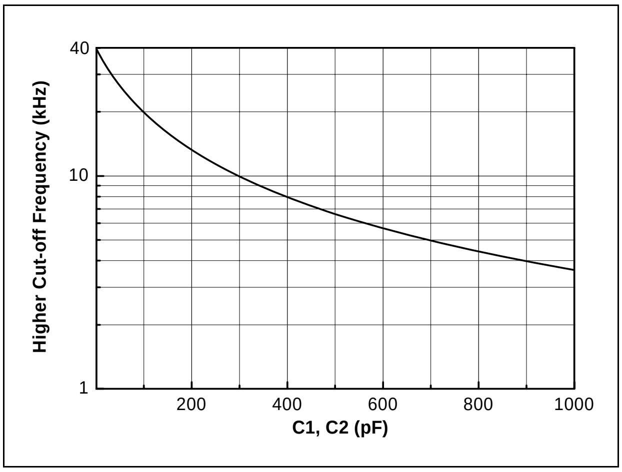
The higher cut-off frequency F_{CH} of the microphone preamplifier depends on the external capacitors C_1, C_2.

TS472 has an internal first order low pass filter (R=40kΩ, C=100pF) to limit the highest cut-off frequency on 40kHz (with a 3dB attenuation). By connecting C_1, C_2 you can decrease F_{CH} by applying the following formula:

$$F_{CH} = \frac{1}{2\pi \cdot 40 \times 10^3 \cdot (C_{1,2} + 100 \times 10^{-12})}$$

Figure 32 below indicates directly the higher cut-off frequency in Hz versus the value of the output capacitors C_1, C_2 in nF.

Figure 32. Higher cut-off frequency vs. output capacitors



For example, F_{CH} is almost 20kHz with $C_{1,2}$=100pF.

5.3 Lower cut-off frequency

The lower cut-off frequency F_{CL} of the microphone preamplifier depends on the input capacitors C_{in} and output capacitors C_{out}. These input and output capacitors are mandatory in an application because of DC voltage blocking.

The input capacitors C_{in} in series with the input impedance of the TS472 (100kΩ) are equivalent to a first order high pass filter. Assuming that F_{CL} is the lowest frequency to be amplified (with a 3dB attenuation), the minimum value of C_{in} is:

$$C_{in} = \frac{1}{2\pi \cdot F_{CL} \cdot 100 \times 10^{3}}$$

The capacitors C_{out} in series with the output resistors R_{out} (or an input impedance of the next stage) are also equivalent to a first order high pass filter. Assuming that F_{CL} is the lowest frequency to be amplified (with a 3dB attenuation), the minimum value of C_{out} is:

$$C_{out} = \frac{1}{2\pi \cdot F_{CL} \cdot R_{out}}$$

Figure 33. Lower cut-off frequency vs. input capacitors

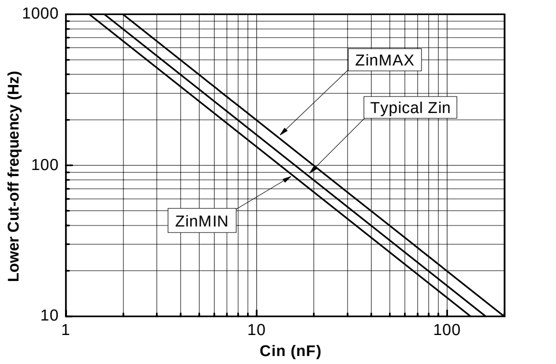


Figure 34. Lower cut-off frequency vs. output capacitors

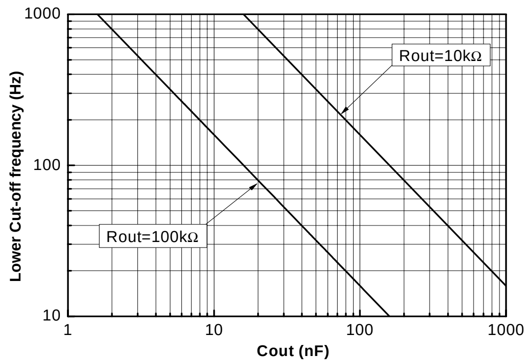


Figure 33 and *Figure 34* give directly the lower cut-off frequency (with 3dB attenuation) versus the value of the input or output capacitors

Note: In case F_{CL} is kept the same for calculation, take into account that the 1st order high-pass filter on the input and the 1st order high-pass filter on the output create a 2nd order high-pass filter in the audio signal path with an attenuation of 6dB on F_{CL} and a rolloff of 40dB/decade.

5.4 Low-noise microphone bias source

The TS472 provides a very low noise voltage and power supply rejection BIAS source designed for biasing an electret condenser microphone cartridge. The BIAS output is typically set at 2.0 V_{DC} (no load conditions), and can typically source 2mA with respect to drop-out, determined by the internal resistance 100Ω (for detailed load regulation curves see *Figure 8*).

5.5 Gain settings

The gain in the application depends mainly on:

- the sensitivity of the microphone
- the distance to the microphone
- the audio level of the sound
- the desired output level

The sensitivity of the microphone is generally expressed in dB/Pa, referenced to 1V/Pa. For example, the microphone used in testing had an output voltage of 6.3mV for a sound pressure of 1 Pa (where Pa is the pressure unit, Pascal). Expressed in dB, the sensitivity is:

$20Log(0.0063) = -44$ dB/Pa

To facilitate the first approach, *Table 11* below gives voltages and gains used with a low cost omnidirectional electret condenser microphone of -44dB/Pa.

Table 11. Typical TS472 gain vs. distance to the microphone (sensitivity -44dB/Pa)

Distance to microphone	Microphone output voltage	TS472 Gain
1cm	$30mV_{RMS}$	20
20cm	$3mV_{RMS}$	100

The gain of the TS472 microphone preamplifier can be set:

1. From -1.5 dB to 41 dB by connecting an external grounded resistor R_{GS} to the GS pin. It allows to adapt more precisely the gain to each application.

Table 12. Selected gain vs. gain select resistor

Gain (dB)	0	10	20	30	40
R_{GS} (Ω)	470k	27k	4k7	1k	68

Figure 35. Gain in dB vs. gain select resistor

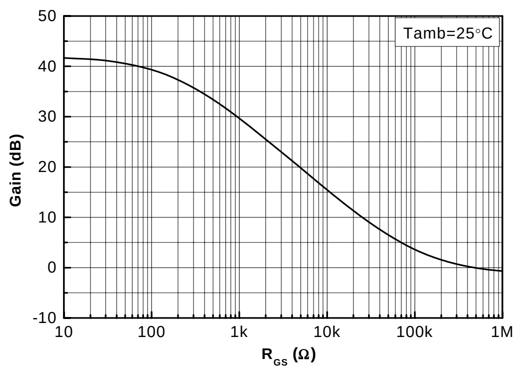
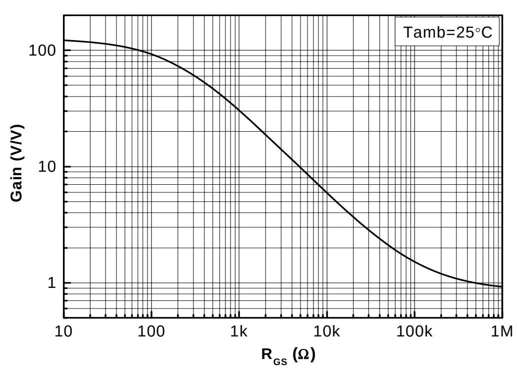


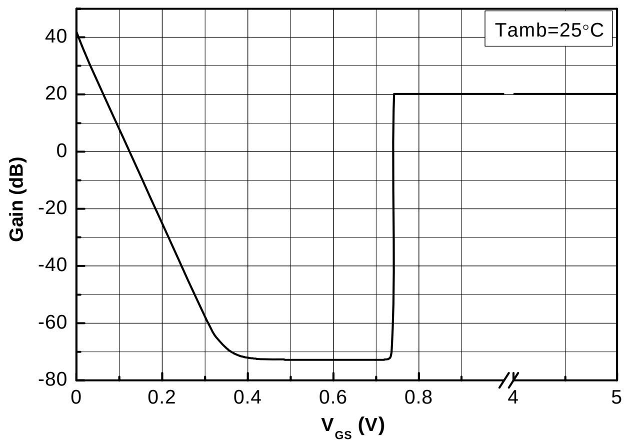
Figure 36. Gain in V/V vs. gain select resistor



2. To 20dB by applying $V_{GS} > 1V_{DC}$ on Gain Select (GS) pin. This setting can help to reduce a number of external components in an application, because 2.0 V_{DC} is provided by TS472 itself on BIAS pin.

Figure 37 below gives other values of the gain vs. voltage applied on GS pin.

Figure 37. Gain vs. gain select voltage

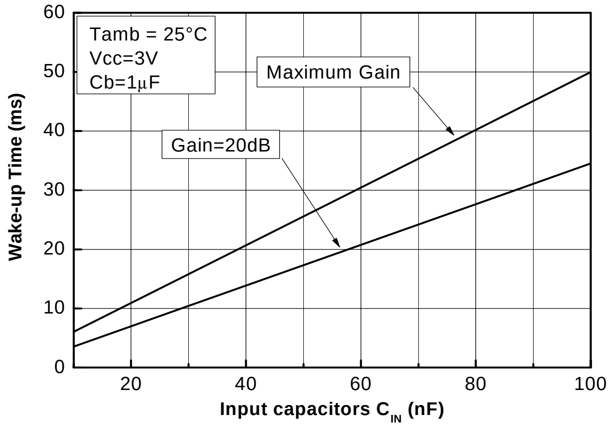


5.6 Wake-up time

When the standby is released to put the device ON, a signal appears on the output a few microseconds later, and the bypass capacitor C_b is charged in a few milliseconds. As C_b is directly linked to the bias of the amplifier, the bias will not work properly until the C_b voltage is correct.

In the typical application, when a biased microphone is connected to the differential input via the input capacitors (C_{in}), (and the output signal is in line with the specification), the wake-up time will depend upon the values of the input capacitors C_{in} and the gain. When gain is lower than 0dB, the wake-up time is determined only by the bypass capacitor C_b, as described above. For a gain superior to 0dB, see *Figure 38* below.

Figure 38. Wake-up time in the typical application vs. input capacitors



5.7 Standby mode

When the standby command is set, the time required to set the output stages (differential outputs and 2.0V bias output) in high impedance and the internal circuitry in shutdown mode is a few microseconds.

5.8 Layout considerations

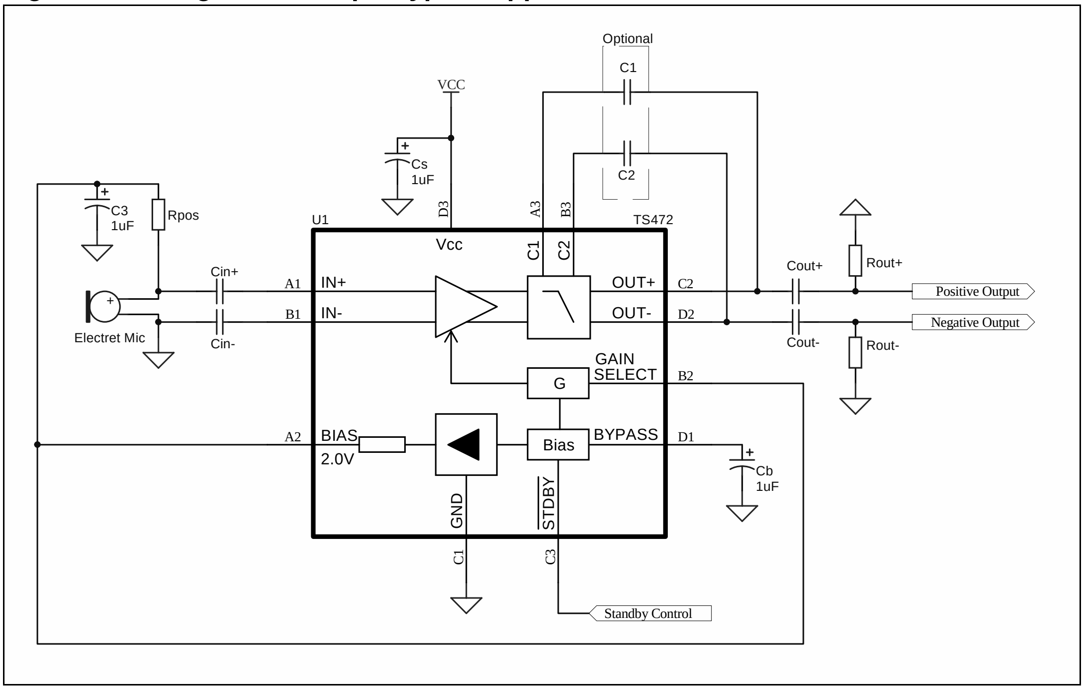
The TS472 has sensitive pins to connect C1, C2 and Rgs. To obtain high power supply rejection and low noise performance, it is mandatory that the layout track to these component is as short as possible.

Decoupling capacitors on V_{CC} and bypass pin are needed to eliminate power supply drops. In addition, the capacitor location for the dedicated pin should be as close to the device as possible.

5.9 Single-ended input configuration

It's possible to use the TS472 in a single-ended input configuration. The schematic in *Figure 39* provides an example of this configuration.

Figure 39. Single ended input typical application



5.10 Demo board

A demo board for the TS472 is available. For more information about this demo board, please refer to **Application Note AN2240**, which can be found on **www.st.com.**

Figure 40. PCB top layer

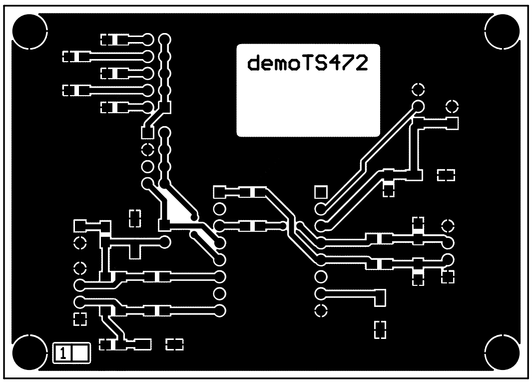


Figure 41. PCB bottom layer

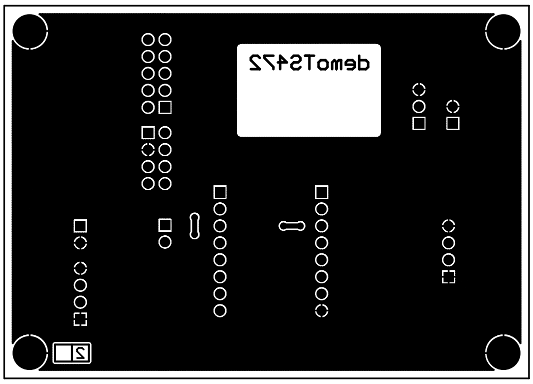
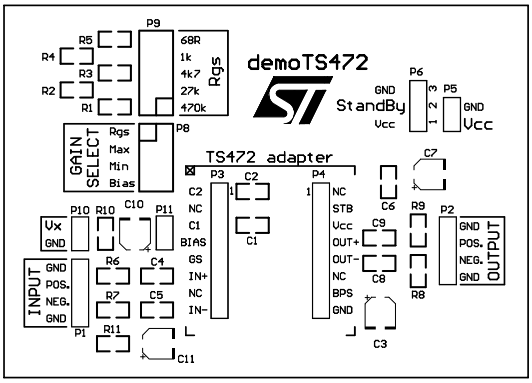


Figure 42. Component location



6 Package mechanical data

In order to meet environmental requirements, STMicroelectronics offers these devices in ECOPACK® packages. These packages have a Lead-free second level interconnect. The category of second level interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an STMicroelectronics trademark. ECOPACK specifications are available at: www.st.com.

6.1 Flip-chip package

Figure 43. TS472 footprint recommendation

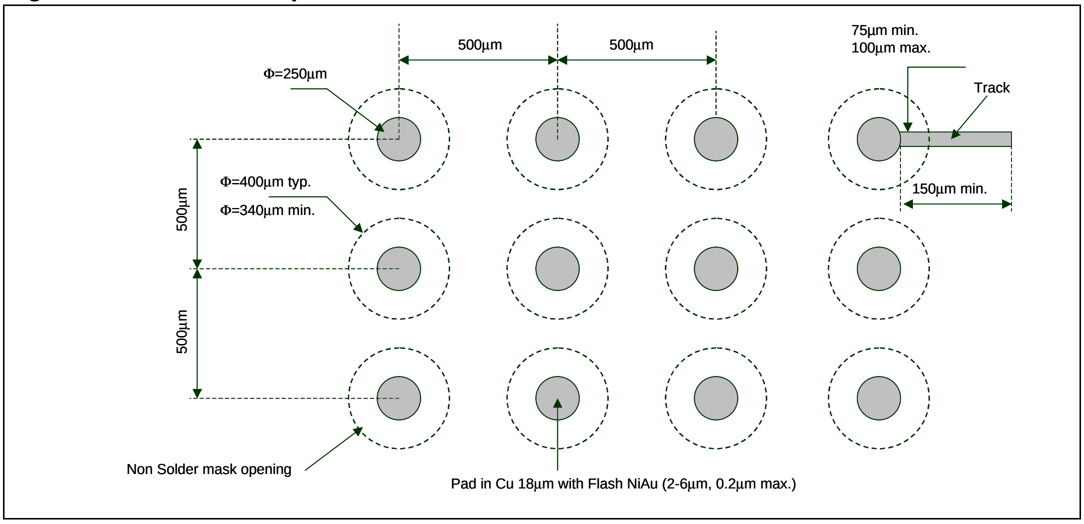


Figure 44. Pin-out (top view)

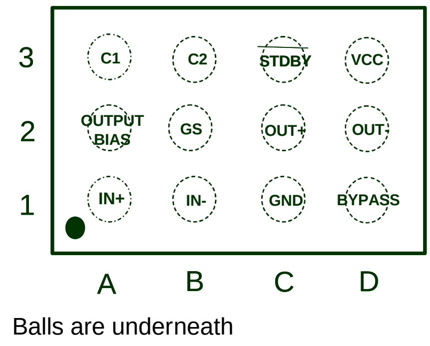


Figure 45. Marking (top view)

- ST logo
- Part number: 472
- E Lead free bumps
- Three digits datecode: YWW
- The dot indicates pin A1

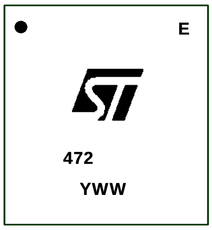
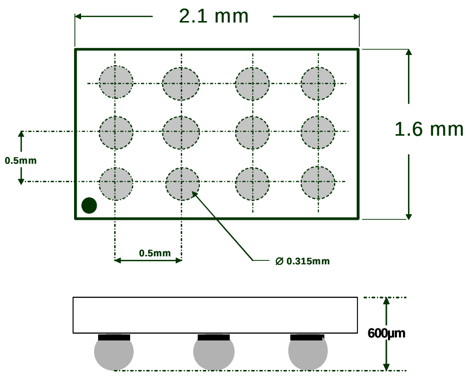
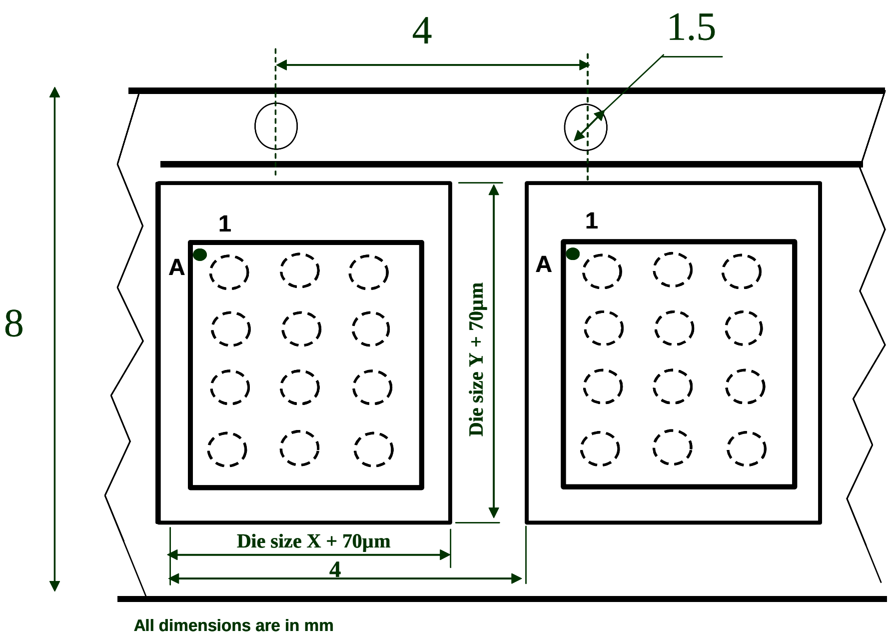


Figure 46. Flip-chip - 12 bumps



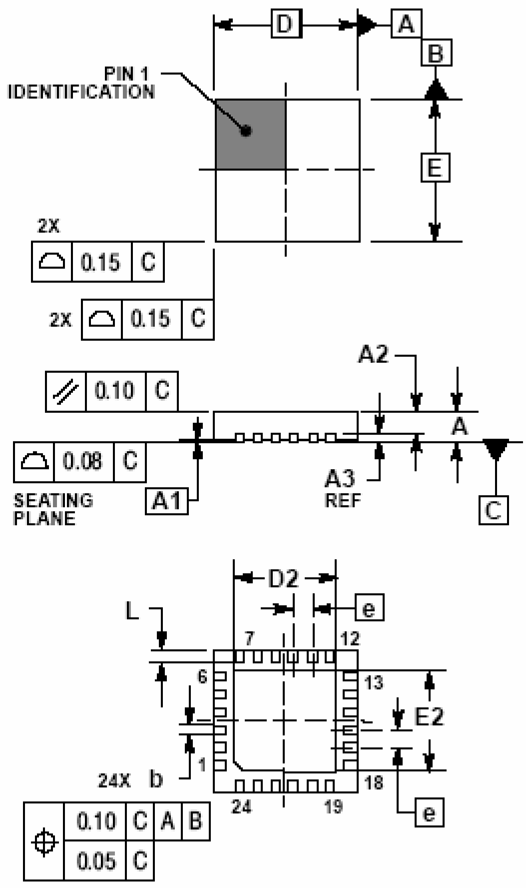
- Die size: **2.1mm x 1.6mm** ± 30µm
- Die height (including bumps): **600µm**
- Bumps diameter: **315µm** ±50µm
- Bump diameter before reflow: **300µm** ±10µm
- Bump height: **250µm** ±40µm
- Die height: **350µm** ±20µm
- Pitch: **500µm** ±50µm
- Coplanarity: **50µm max**

Figure 47. Tape & reel specification (top view)



6.2 QFN24 package

Figure 48. QFN24 package mechanical data



NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.25 AND 0.30 MM FROM TERMINAL.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

	MILLIMETERS	
DIM	MIN	MAX
A	0.80	1.00
A1	0.00	0.05
A2	0.60	0.80
A3	0.20 REF	
b	0.23	0.28
D	4.00 BSC	
D2	2.70	2.90
E	4.00 BSC	
E2	2.70	2.90
e	0.50 BSC	
L	0.35	0.45

7 Revision history

Table 13. Document revision history

Date	Revision	Changes
1-Jul-05	1	Initial release corresponding to product preview version.
1-Oct-05	2	First release of fully mature product datasheet.
1-Dec-05	3	Added single-ended input operation in *Section 5: Application information*.
12-Sep-2006	4	Added QFN package information. Updated curves, added new ones in *Section 4: Electrical characteristics*.