



PART NUMBER: VAT1-SMT series

DESCRIPTION: dc-dc converter

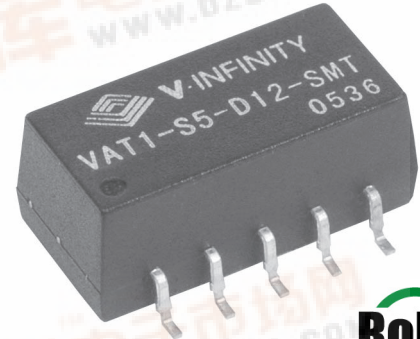
description

Designed to convert fixed voltages into an isolated voltage, the VAT1-SMT series is well suited for providing board-mount local supplies in a wide range of applications, including mixed analog/digital circuits, test & measurement equip., process/machine controls, datacom/telecom fields, etc...

The semi-regulated output can be followed by 3-terminal regulators to provide output protection, in addition to output regulation.

features

- isolated 1 W output
- temperature range: -40°C~+85°C
- unregulated
- high efficiency to 79%
- dual voltage output
- small footprint
- SMD package style
- industry standard pinout
- UL94-V0 package
- no heatsink required
- 1K Vdc isolation
- high power density
- no external component required
- low cost



model number	input voltage		output voltage	output current		efficiency	load regulation	UL60950-1
	nominal	range		max.	min.			
VAT1-S5-D5-SMT	5 Vdc	4.5~5.5 Vdc	±5 Vdc	±100 mA	±10 mA	72%	10~15%	YES
VAT1-S5-D9-SMT	5 Vdc	4.5~5.5 Vdc	±9 Vdc	±56 mA	±6 mA	75%	6.5~15%	YES
VAT1-S5-D12-SMT	5 Vdc	4.5~5.5 Vdc	±12 Vdc	±42 mA	±5 mA	78%	6~15%	YES
VAT1-S5-D15-SMT	5 Vdc	4.5~5.5 Vdc	±15 Vdc	±33 mA	±4 mA	79%	6~15%	YES
VAT1-S12-D5-SMT	12 Vdc	10.8~13.2 Vdc	±5 Vdc	±100 mA	±10 mA	74%	10~15%	YES
VAT1-S12-D9-SMT	12 Vdc	10.8~13.2 Vdc	±9 Vdc	±56 mA	±6 mA	76%	6.5~15%	YES
VAT1-S12-D12-SMT	12 Vdc	10.8~13.2 Vdc	±12 Vdc	±42 mA	±5 mA	78%	6~15%	YES
VAT1-S12-D15-SMT	12 Vdc	10.8~13.2 Vdc	±15 Vdc	±33 mA	±4 mA	79%	6~15%	YES
VAT1-S15-D5-SMT	15 Vdc	13.5~16.5 Vdc	±5 Vdc	±100 mA	±10 mA	74%	10~15%	NO
VAT1-S15-D9-SMT	15 Vdc	13.5~16.5 Vdc	±9 Vdc	±56 mA	±6A	75%	6.5~15%	NO
VAT1-S15-D12-SMT	15 Vdc	13.5~16.5 Vdc	±12 Vdc	±42 mA	±5 mA	79%	6~15%	NO
VAT1-S15-D15-SMT	15 Vdc	13.5~16.5 Vdc	±15 Vdc	±33 mA	±4 mA	79%	6~15%	NO
VAT1-S24-D5-SMT	24 Vdc	21.6~26.4 Vdc	±5 Vdc	±100 mA	±10 mA	72%	10~15%	NO
VAT1-S24-D9-SMT	24 Vdc	21.6~26.4 Vdc	±9 Vdc	±56 mA	±6 mA	74%	6.5~15%	NO
VAT1-S24-D12-SMT	24 Vdc	21.6~26.4 Vdc	±12 Vdc	±42 mA	±5 mA	76%	6~15%	NO
VAT1-S24-D15-SMT	24 Vdc	21.6~26.4 Vdc	±15 Vdc	±33 mA	±4 mA	77%	6~15%	NO
VAT1-S24-D24-SMT	24 Vdc	21.6~26.4 Vdc	±24 Vdc	±21 mA	±2 mA	78%	6~15%	NO

*VA(X)T1-Series with ALT PIN config. (see dimensions, page 2)

OUTPUT SPECIFICATIONS

item	test conditions	min.	typ.	max.	units
output power		0.1		1	W
line regulation	for Vin change of 1%			1.2	%
output voltage accuracy	see tolerance envelope graph				
temperature drift	@ 100% load			0.03	%/°C
output ripple	20 MHz bandwidth		50	75	mVp-p
noise	20 MHz bandwidth		75	150	
switching frequency	full load, nominal input		500		KHz

NOTE:

1. All specifications measured at TA=25°C, humidity <75%, nominal input voltage and rated output load unless otherwise specified.

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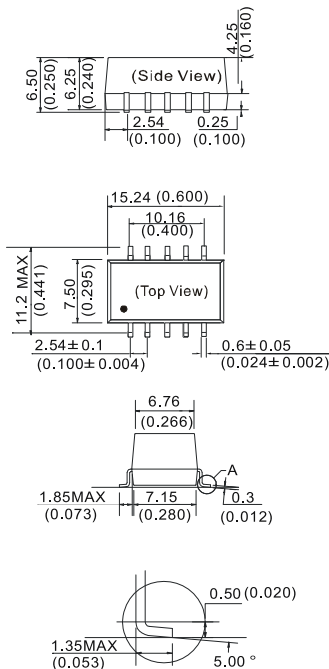
GENERAL SPECIFICATIONS

short circuit protection	<1 second
temperature rise at full load	25°C Max, 15°C typ.
cooling	free air convection
operating temperature range	-40°C to +85°C
storage temperature range	-55°C to +125°C
soldering temperature	260°C (1.5mm from case for 10 sec.)
storage humidity range	<95%
case material	plastic (UL94-V0)
safety	approved to UL60950-1 (E222736)
MTBF	>3,500,000 hrs.

ISOLATION SPECIFICATIONS

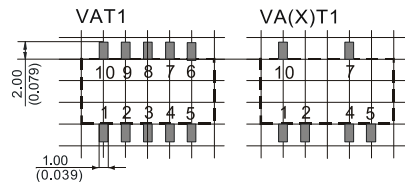
item	test conditions	min.	typ.	max.	units
isolation voltage	tested for 1 min.	1000			Vdc
insulation resistance	test at 500 Vdc	1000			M Ω

DIMENSIONS (mm)



First Angle Projection

RECOMMENDED FOOTPRINT
Top view, grid: 2.54mm (0.1 inch)



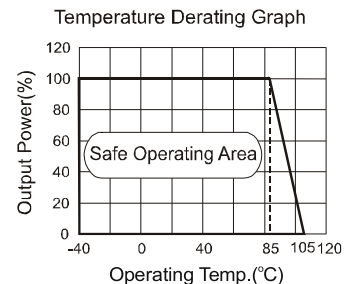
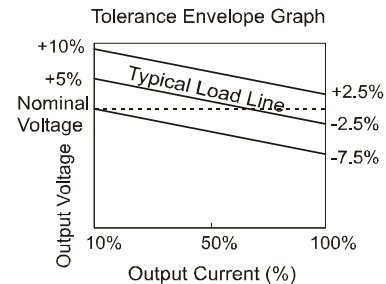
FOOTPRINT DETAILS

Pin	Single	ALT
1	GND	GND
2	Vin	Vin
4	0V	0V
5	-Vo	-Vo
7	+Vo	+Vo
10	NC	NC
3, 6, 8, 9	NC	NO Pin

NC: No Connection

Note:
Unit: mm (inch)
Pin section: 0.60*0.25mm (0.024*0.010 inch)
Pin tolerances: ±0.10mm (±0.004 inch)
General tolerances: ±0.15mm (±0.006 inch)

TYPICAL CHARACTERISTICS



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APPLICATION NOTES:

- Input filtering

To reduce the reflected ripple current and minimize EMI, especially when the converter input is more than 2" away from the DC source, it is recommended to connect a low ESR electrolytic capacitor between Vin and Gnd. The values suggested are as shown in Table 1. If additional filtering is required, the capacitance may be increased, or expanded to an LC network as shown in Figure 1.

TABLE 1

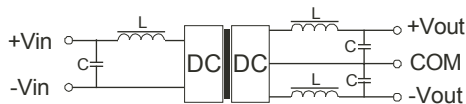
Input Voltage	External Input Capacitance
5 V	4.7 μ F
12 V	2.2 μ F
15 V	2.2 μ F
24 V	1.0 μ F

- Output filtering

An output capacitor is needed to meet output ripple requirements as shown in Table 2. Output capacitance may be increased for additional filtering, but should not exceed 10 μ F or expanded to an LC network as in Figure 1.

TABLE 2

Vout	External Output Capacitance
5 V	4.7 μ F
9 V	2.2 μ F
12 V	1.0 μ F
15 V	0.47 μ F
24 V	0.33 μ F



<Figure 1>

- Minimum loading

The converter needs a minimum of 10% loading to maintain output regulation. Operation under no-load conditions will not cause immediate damages but may reduce reliability, and cause performance not to meet specifications.

- Regulation

With a semi-regulated design, the converter's output voltage varies with load current and will change proportionally to the input voltage. If regulated output is needed, an external regulator can be used as shown in Figure 2.

- Protection

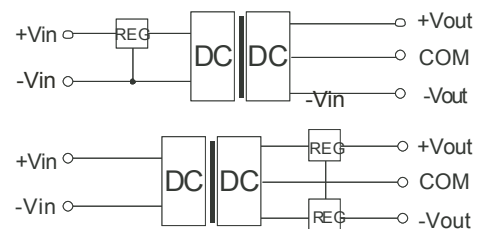
The converter has minimal protection against input over-voltage or output over-load, and may be permanently damaged if exposed to these conditions. An input clamping device can be used for input voltage limiting. An input fuse or an output fuse also be used to protect against over-loading.

- Dual outputs used as a single output

The +Vout and -Vout can be used to obtain a single output that is the sum of the two outputs. In this case, the COM pin shouldn't be used.

- External Regulator

An external 3-terminal regulator can be connected to the output of the converter to achieve full regulation. Make sure the converter's output voltage provides sufficient head room for the regulator. An additional benefit is that the built-in protection features in the regulator, such as OCP, OTP, etc, will protect the converter also. In a complimentary supply, a negative output regulator must be used to achieve the negative regulated output.



<Figure 2>