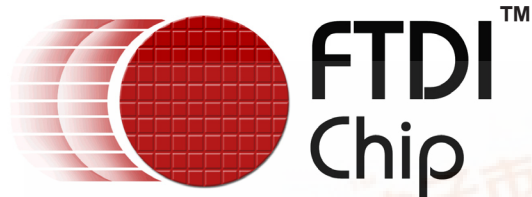
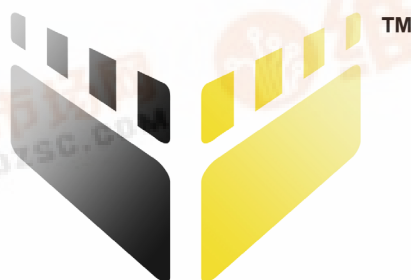


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VINCULUM

BINDING USB TECHNOLOGIES

VDIP1

Vinculum VNC1L Prototyping Module



<http://www.vinculum.com>

1. Introduction and Features

1.1 Introduction

The VDIP1 module is an MCU to embedded USB host controller development module for the VNC1L I.C. device. The VDIP1 is supplied on a PCB designed to fit into a 24 pin DIP socket, and provides access to the UART, parallel FIFO, and SPI interface pins on the VNC1L device, via its AD and AC bus pins. Not only is it ideal for developing and rapid prototyping of VNC1L designs, but also an attractive quantity discount structure makes this module suitable for incorporation into low and medium volume finished product designs.

The Vinculum VNC1L is the first of F.T.D.I.'s Vinculum family of Embedded USB host controller integrated circuit devices. Not only is it able to handle the USB Host Interface, and data transfer functions but owing to the inbuilt MCU and embedded Flash memory, Vinculum can encapsulate the USB device classes as well. When interfacing to mass storage devices such as USB Flash drives, Vinculum also transparently handles the FAT File structure communicating via UART, SPI or parallel FIFO interfaces via a simple to implement command set. Vinculum provides a new cost effective solution for providing USB Host capability into products that previously did not have the hardware resources available. The VNC1L is available in Pb-free (RoHS compliant) compact 48-Lead LQFP package.

1.2 Features

- Uses F.T.D.I.'s VNC1L embedded USB host controller I.C. device.
- USB 'A' type socket to interface with USB peripheral devices
- Second USB interface port available via module pins, if required.
- Jumper selectable UART, parallel FIFO, or SPI MCU interfaces.
- Single 5V supply input.
- Auxiliary 3.3 V / 200 mA power output to external logic.
- Power indicator, and USB traffic indicator LED's.
- Program or update firmware via USB Flash disk or via UART / parallel FIFO / SPI interface.
- VNC1L firmware programming control pins PROG# and RESET# brought out onto jumper interface
- VDIP1 is a Pb-free, RoHS complaint development module.
- VDIP1 module is supplied pre-loaded with Vinculum VDAP firmware.
- Schematics, and firmware files available for download from the [Vinculum website](#).

2. Pin Out and Signal Descriptions

2.1 Module Pin Out

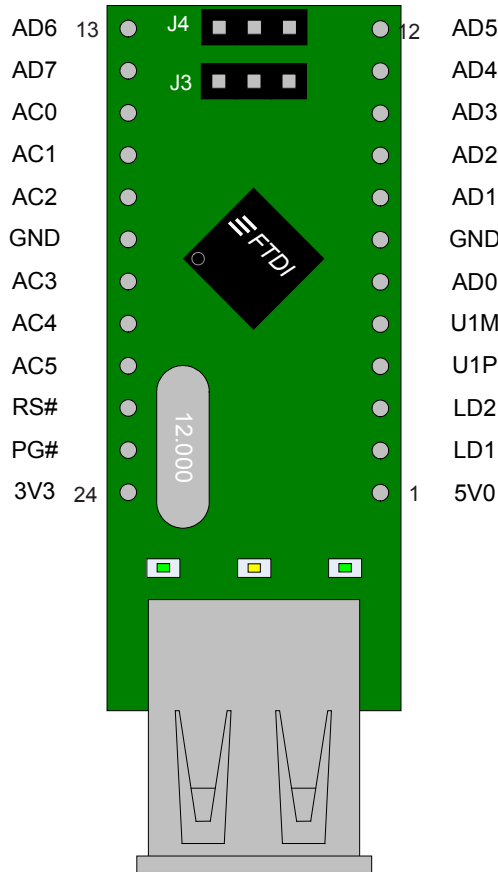


Figure 1 - VDIP1 Module Pin Out

2.2 Pin Signal Descriptions

Table 1 - VDIP1 module pin descriptions

Pin No.	Name	Pin Name on PCB	Type	Description
1	5V0	5V0	PWR Input	5.0 V module supply pin. This pin provides the 5.0V output on the USB 'A' type socket, and also the 3.3V supply to VNC1L, via an on-board 3.3 V L.D.O.
2	LED1	LD1	Output	USB port 1 traffic activity indicator LED. This pin is hard wired to a green LED on board the PCB. It is also brought out onto this pin which allows for the possibility of bringing out an additional LED traffic indicator out of the VDIP1 board. For example, if the VDIP1 USB connector is brought out onto an instrument front panel, an activity LED could be mounted along side it.
3	LED2	LD2	Output	USB port 2 traffic activity indicator LED. This pin is hard wired to a green LED on board the PCB. It is also brought out onto this pin which allows for the possibility of bringing out an additional LED traffic indicator out of the VDIP1 board. For example, if the VDIP1 USB connector is brought out onto an instrument front panel, an activity LED could be mounted along side it.
4	USBD1P	U1P	I/O	USB host / slave port 1 - USB Data Signal Plus with integrated pull up / pull down resistor. Module has on board 27 Ω USB series resistor. This pin can be brought out along with pin 5 to provide a second USB port, if required.
5	USBD1M	U1M	I/O	USB host / slave port 1 - USB Data Signal Minus with integrated pull up / pull down resistor. Module has on board 27 Ω USB series resistor. This pin can be brought out along with pin 4 to provide a second USB port, if required.
6	ADBUS0	AD0	I/O	5V safe bidirectional data / control bus, AD bit 0
7	GND	GND	PWR	Module ground supply pin
8	ADBUS1	AD1	I/O	5V safe bidirectional data / control bus, AD bit 1
9	ADBUS2	AD2	I/O	5V safe bidirectional data / control bus, AD bit 2
10	ADBUS3	AD3	I/O	5V safe bidirectional data / control bus, AD bit 3
11	ADBUS4	AD4	I/O	5V safe bidirectional data / control bus, AD bit 4
12	ADBUS5	AD5	I/O	5V safe bidirectional data / control bus, AD bit 5
13	ADBUS6	AD6	I/O	5V safe bidirectional data / control bus, AD bit 6
14	ADBUS7	AD7	I/O	5V safe bidirectional data / control bus, AD bit 7
15	ACBUS0	AC0	I/O	5V safe bidirectional data / control bus, AC bit 0
16	ACBUS1	AC1	I/O	5V safe bidirectional data / control bus, AC bit 1
17	ACBUS2	AC2	I/O	5V safe bidirectional data / control bus, AC bit 2
18	GND	GND	PWR	Module ground supply pin
19	ACBUS3	AC3	I/O	5V safe bidirectional data / control bus, AC bit 3
20	ACBUS4	AC4	I/O	5V safe bidirectional data / control bus, AC bit 4
21	ACBUS5	AC5	I/O	5V safe bidirectional data / control bus, AC bit 5
22	RESET#	RS#	Input	Can be used by an external device to reset the VNC1L. This pin can be used in combination with PROG# and the UART / parallel FIFO / SPI interface to program firmware into the VNC1L.
23	PROG#	PG#	Input	This pin is used in combination with the RESET# pin and the UART / parallel FIFO / SPI interface to program firmware into the VNC1L.
24	3V3	3V3	PWR Output	3.3V output from VDIP1's on board 3.3V L.D.O.

2.3 I/O Configuration Using The Jumper Pin Header

Two three way jumper pin headers are provided to allow for simple configuration of the I/O on data and control bus pins of the VDIP1. This is done by a combination of pulling up or pulling down the VNC1L's ACBUS5 (pin 46) and ACBUS6 (pin 47). The relevant portion of the VDIP1 module schematic is shown in figure 7, below.

Figure 2 - VDIP1 On-board jumper pin configuration.

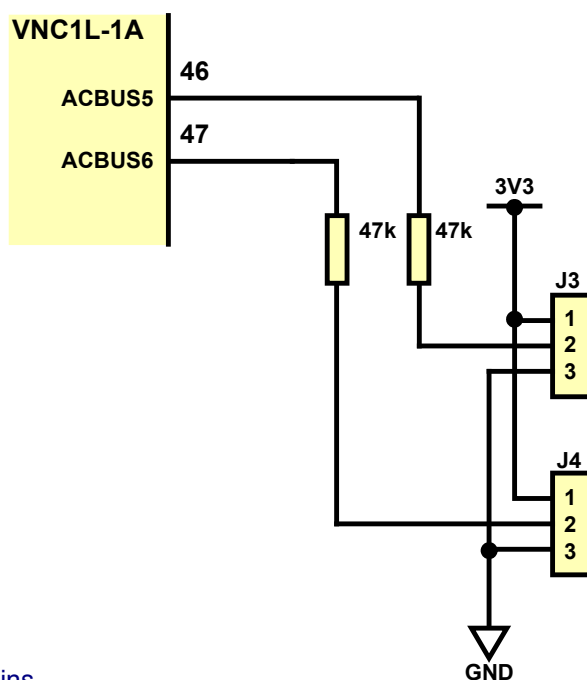


Table 2 - Port Selection Jumper Pins

ACBUS6 (VNC1L pin 47)	ACBUS5 (VNC1L pin 46)	I/O Mode
Pull-Up	Pull-Up	Serial UART
Pull-Up	Pull-Down	SPI
Pull-Down	Pull-Up	Parallel FIFO
Pull-Down	Pull-Down	Serial UART

Table 3 - Data and control bus configuration options

Pin No.	Name	Pin Name on PCB	Type	Description	Data and Control Bus Configuration Options			
					UART Interface	Parallel FIFO Interface	SPI Slave Interface	I/O Port
6	ADBUS0	AD0	I/O	5V safe bidirectional data / control bus, AD bit 0	TXD	D0	SCLK	PortAD0
8	ADBUS1	AD1	I/O	5V safe bidirectional data / control bus, AD bit 1	RXD	D1	SDI	PortAD1
9	ADBUS2	AD2	I/O	5V safe bidirectional data / control bus, AD bit 2	RTS#	D2	SDO	PortAD2
10	ADBUS3	AD3	I/O	5V safe bidirectional data / control bus, AD bit 3	CTS#	D3	CS	PortAD3
11	ADBUS4	AD4	I/O	5V safe bidirectional data / control bus, AD bit 4	DTR#	D4		PortAD4
12	ADBUS5	AD5	I/O	5V safe bidirectional data / control bus, AD bit 5	DSR#	D5		PortAD5
13	ADBUS6	AD6	I/O	5V safe bidirectional data / control bus, AD bit 6	DCD#	D6		PortAD6
14	ADBUS7	AD7	I/O	5V safe bidirectional data / control bus, AD bit 7	RI#	D7		PortAD7
15	ACBUS0	AC0	I/O	5V safe bidirectional data / control bus, AC bit 0	TXDEN#	RXF#		PortAC0
16	ACBUS1	AC1	I/O	5V safe bidirectional data / control bus, AC bit 1		TXE#		PortAC1
17	ACBUS2	AC2	I/O	5V safe bidirectional data / control bus, AC bit 2		RD#		PortAC2
19	ACBUS3	AC3	I/O	5V safe bidirectional data / control bus, AC bit 3		WR		PortAC3
20	ACBUS4	AC4	I/O	5V safe bidirectional data / control bus, AC bit 4				PortAC4

2.4 UART Interface Signal Descriptions

Table 4 - Data and Control Bus Signal Mode Options - UART Interface

Pin No.	Name	Type	Description
6	TXD	Output	Transmit asynchronous data output
8	RXD	Input	Receive asynchronous data input
9	RTS#	Output	Request To Send Control Output / Handshake signal
10	CTS#	Input	Clear To Send Control Input / Handshake signal
11	DTR#	Output	Data Terminal Ready Control Output / Handshake signal
12	DSR#	Input	Data Set Ready Control Input / Handshake signal
13	DCD#	Input	Data Carrier Detect Control Input
14	RI#	Input	Ring Indicator Control Input. When the Remote Wake up option is enabled in the EEPROM, taking RI# low can be used to resume the PC USB Host controller from suspend.
15	TXDEN#	Input	Enable Transmit Data for RS485 designs

2.5 Parallel FIFO Interface Signal Descriptions and Timing Diagrams

Table 5 - Data and Control Bus Signal Mode Options - Parallel FIFO Interface

Pin No.	Name	Type	Description
6	D0	I/O	FIFO Data Bus Bit 0
8	D1	I/O	FIFO Data Bus Bit 1
9	D2	I/O	FIFO Data Bus Bit 2
10	D3	I/O	FIFO Data Bus Bit 3
11	D4	I/O	FIFO Data Bus Bit 4
12	D5	I/O	FIFO Data Bus Bit 5
13	D6	I/O	FIFO Data Bus Bit 6
14	D7	I/O	FIFO Data Bus Bit 7
15	RXF#	OUTPUT	When high, do not read data from the FIFO. When low, there is data available in the FIFO which can be read by strobing RD# low, then high again.
16	TXE#	OUTPUT	When high, do not write data into the FIFO. When low, data can be written into the FIFO by strobing WR high, then low.
17	RD#	INPUT	Enables the current FIFO data byte on D0...D7 when low. Fetches the next FIFO data byte (if available) from the receive FIFO buffer when RD# goes from high to low.
19	WR	INPUT	Writes the data byte on the D0...D7 pins into the transmit FIFO buffer when WR goes from high to low.

Figure 3 - FIFO Read Cycle

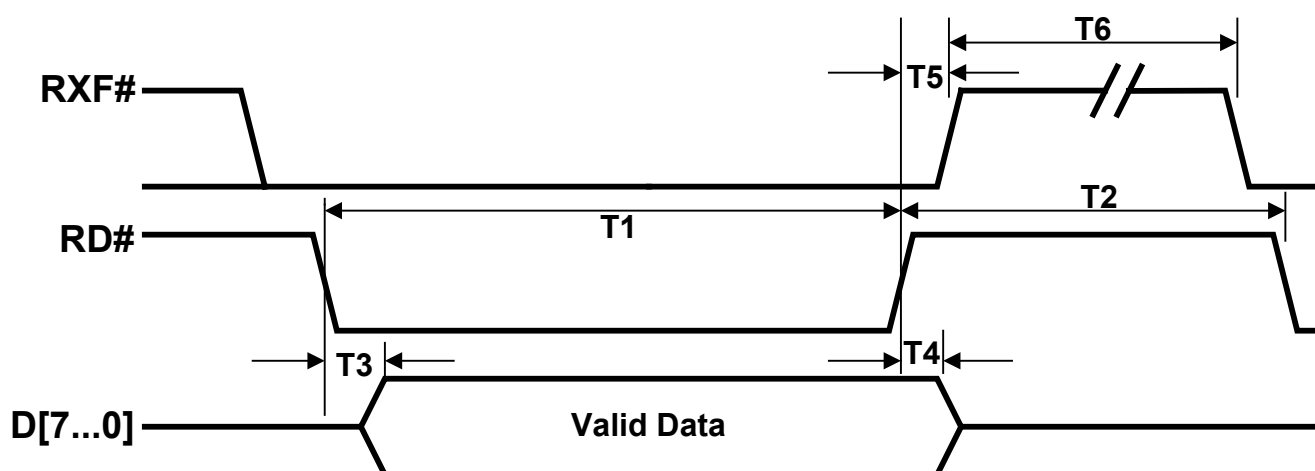


Table 6 - FIFO Read Cycle Timings

Time	Description	Min	Max	Unit
T1	RD Active Pulse Width	50	-	ns
T2	RD to RD Pre-Charge Time	50 + T6	-	ns
T3	RD Active to Valid Data*	20	50	ns
T4	Valid Data Hold Time from RD Inactive*	0	-	ns
T5	RD Inactive to RXF#	0	25	ns
T6	RXF Inactive After RD Cycle	80	-	ns

* Load = 30pF

Figure 4 - FIFO Write Cycle

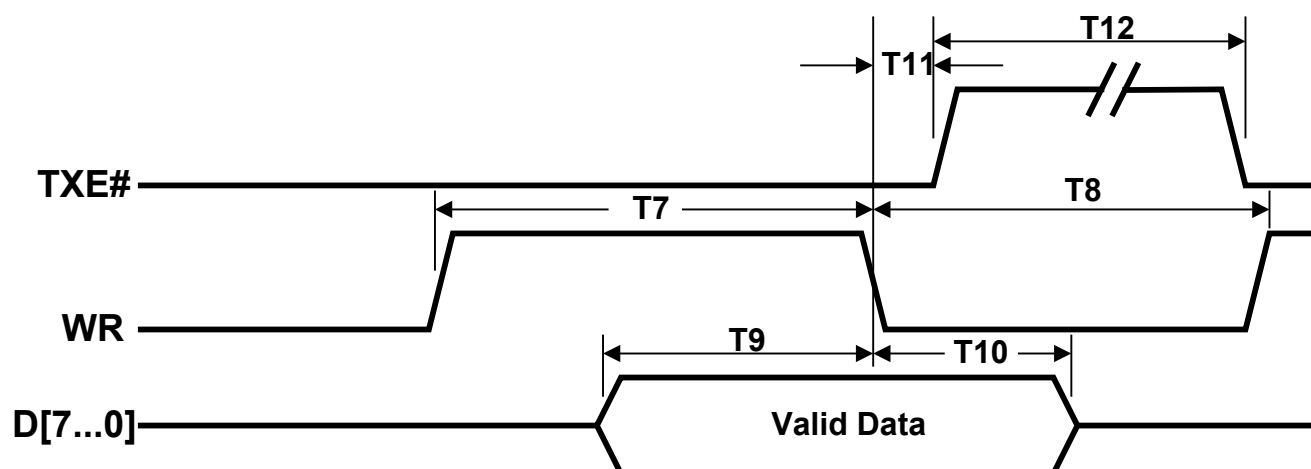


Table 7 - FIFO Write Cycle Timings

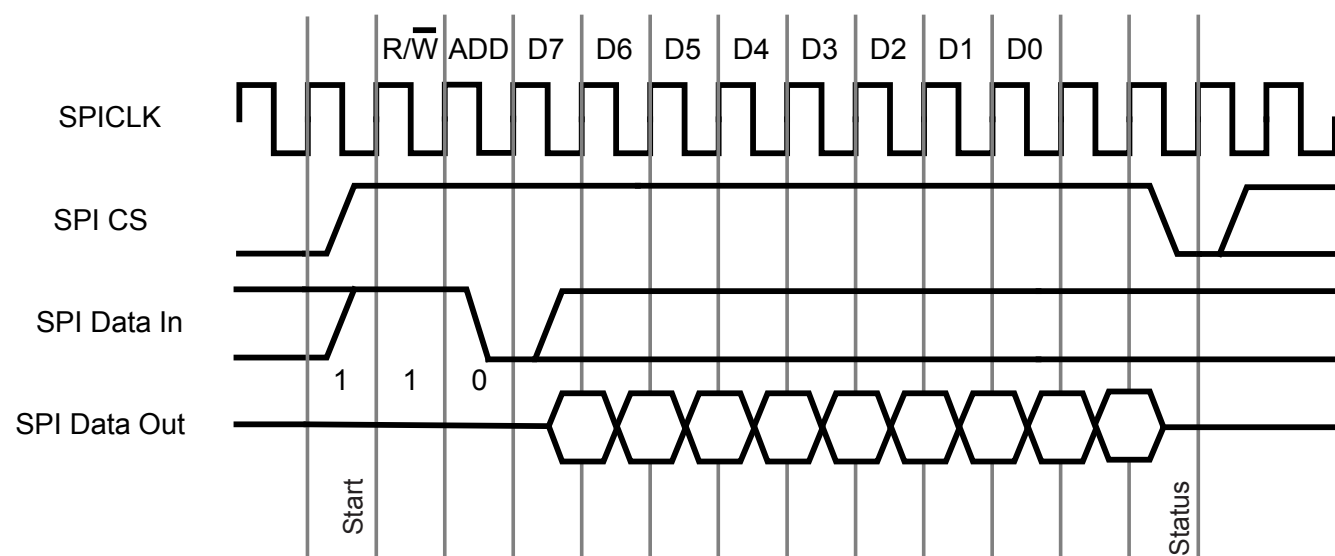
<i>Time</i>	<i>Description</i>	<i>Min</i>	<i>Max</i>	<i>Unit</i>
T7	WR Active Pulse Width	50	-	ns
T8	WR to RD Pre-Charge Time	50	-	ns
T9	Data Setup Time before WR Inactive	20	-	ns
T10	Data Hold Time from WR Inactive	0	-	ns
T11	WR Inactive to TXE#	5	25	ns
T12	TXE Inactive After WR Cycle	80	-	ns

2.6 SPI Interface Signal Descriptions and Timing Diagrams

Table 8 - Data and Control Bus Signal Mode Options - SPI Interface

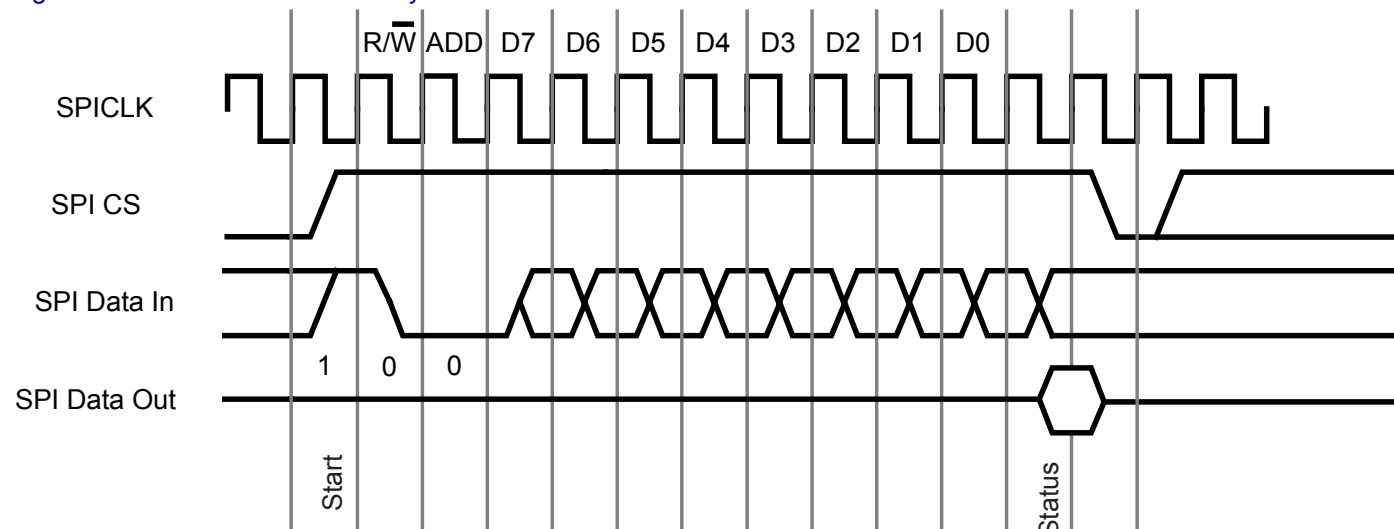
Pin No.	Name	Type	Description
6	SCLK	Input	SPI Clock input, 12MHz maximum.
8	SDI	Input	SPI Serial Data Input
9	SDO	Output	SPI Serial Data Output
10	CS	Input	SPI Chip Select Input

Figure 5 - SPI Slave Data Read Cycle



From Start - SPI CS must be held high for the entire read cycle, and must be taken low for at least one clock period after the read is completed. The first bit on SPI Data In is the R/W bit - inputting a '1' here allows data to be read from the chip. The next bit is the address bit, ADD, which is used to indicate whether the data register ('0') or the status register ('1') is read from. During the SPI read cycle a byte of data will start being output on SPI Data Out on the next clock cycle after the address bit, MSB first. After the data has been clocked out of the chip, the status of SPI Data Out should be checked to see if the data read is new data. A '0' level here on SPI Data Out means that the data read is new data. A '1' indicates that the data read is old data, and the read cycle should be repeated to get new data. Remember that CS must be held low for at least one clock period before being taken high again to continue with the next read or write cycle.

Figure 6 - SPI Slave Data Write Cycle



From Start - SPI CS must be held high for the entire write cycle, and must be taken low for at least one clock period after the write is completed. The first bit on SPI Data In is the R/W bit - inputting a '0' here allows data to be written to the chip. The next bit is the address bit, ADD, which is used to indicate whether the data register ('0') or the status

register ('1') is written to. During the SPI write cycle a byte of data can be input to SPI Data In on the next clock cycle after the address bit, MSB first. After the data has been clocked in to the chip, the status of SPI Data Out should be checked to see if the data read was accepted. A '0' level on SPI Data Out means that the data write was accepted. A '1' indicates that the internal buffer is full, and the write should be repeated. Remember that CS must be held low for at least one clock period before being taken high again to continue with the next read or write cycle.

Figure 7 - SPI Slave Data Timing Diagrams

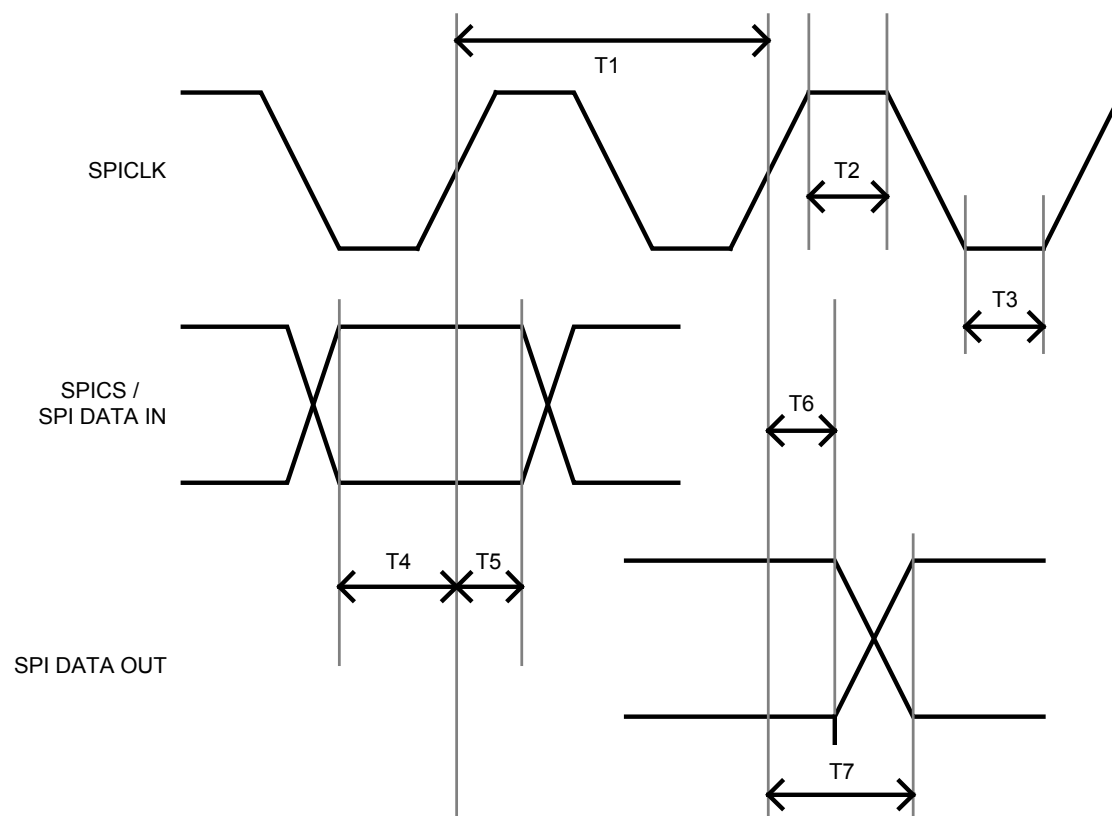


Table 9 - SPI Slave Data Timing

Time	Description	Min	Typical	Max	Unit
T1	SPICLK Period	83	-	-	ns
T2	SPICLK High	20	-	-	ns
T3	SPICLK Low	20	-	-	ns
T4	Input Setup Time	10	-	-	ns
T5	Input Hold Time	10	-	-	ns
T6	Output Hold Time	2	-	-	ns
T7	Output Valid Time	-	-	20	ns

Table 10 - Status Register (ADD = '1')

Bit	Description
0	RXF#
1	TXE#
2	-
3	-
4	RXF IRQEn
5	TXE IRQEn
6	-
7	-

3. Dimensions

3.1 VDIP1 Board Dimensions

The VDIP1 board dimensions are shown below.

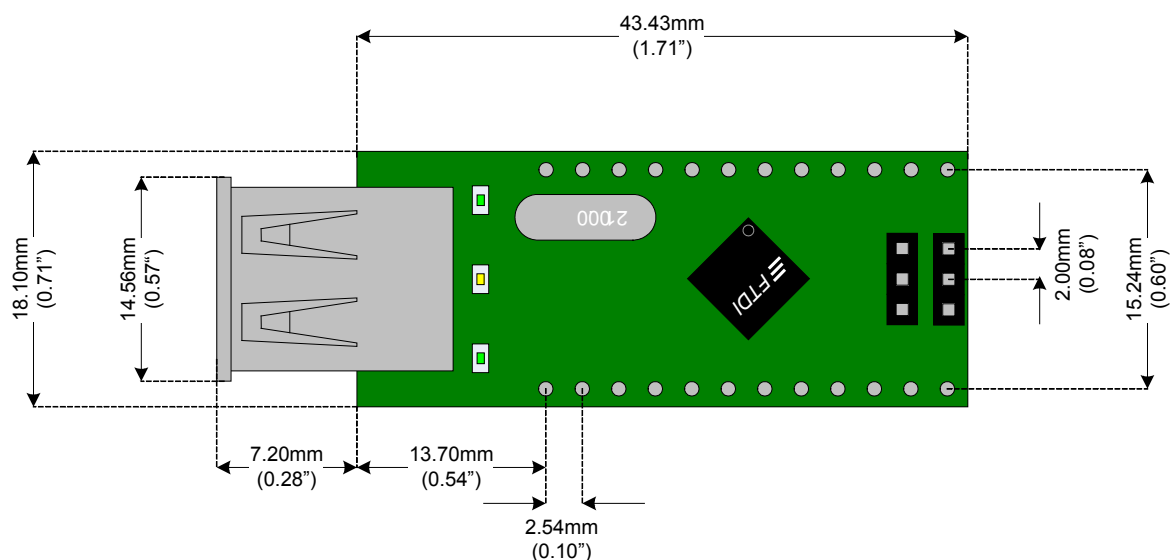


Figure 8 - VDIP1 dimensions, top view.

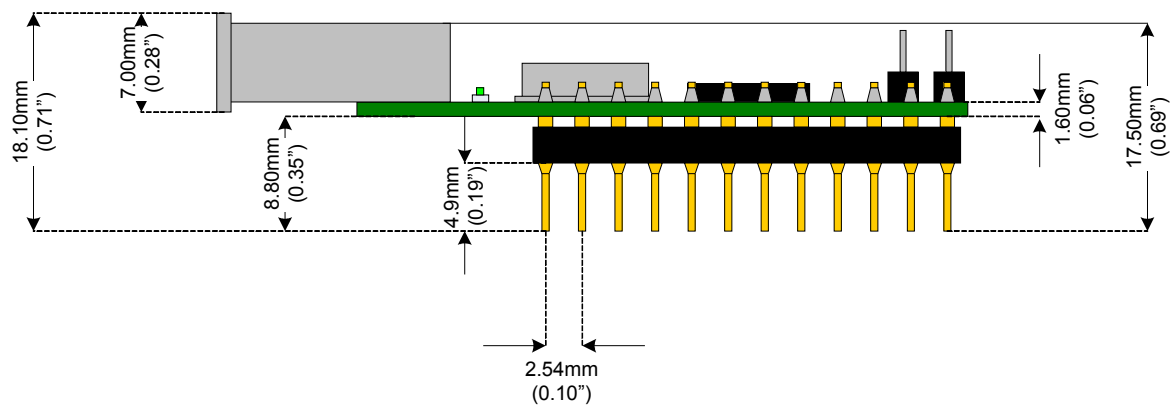


Figure 9 - VDIP1 dimensions , side view.

4. VDIP1 External Circuit Configuration

4.1 Adding a Second USB Port

The external circuit configuration for adding a second USB host port, with a USB activity LED, is shown below in figure 10.

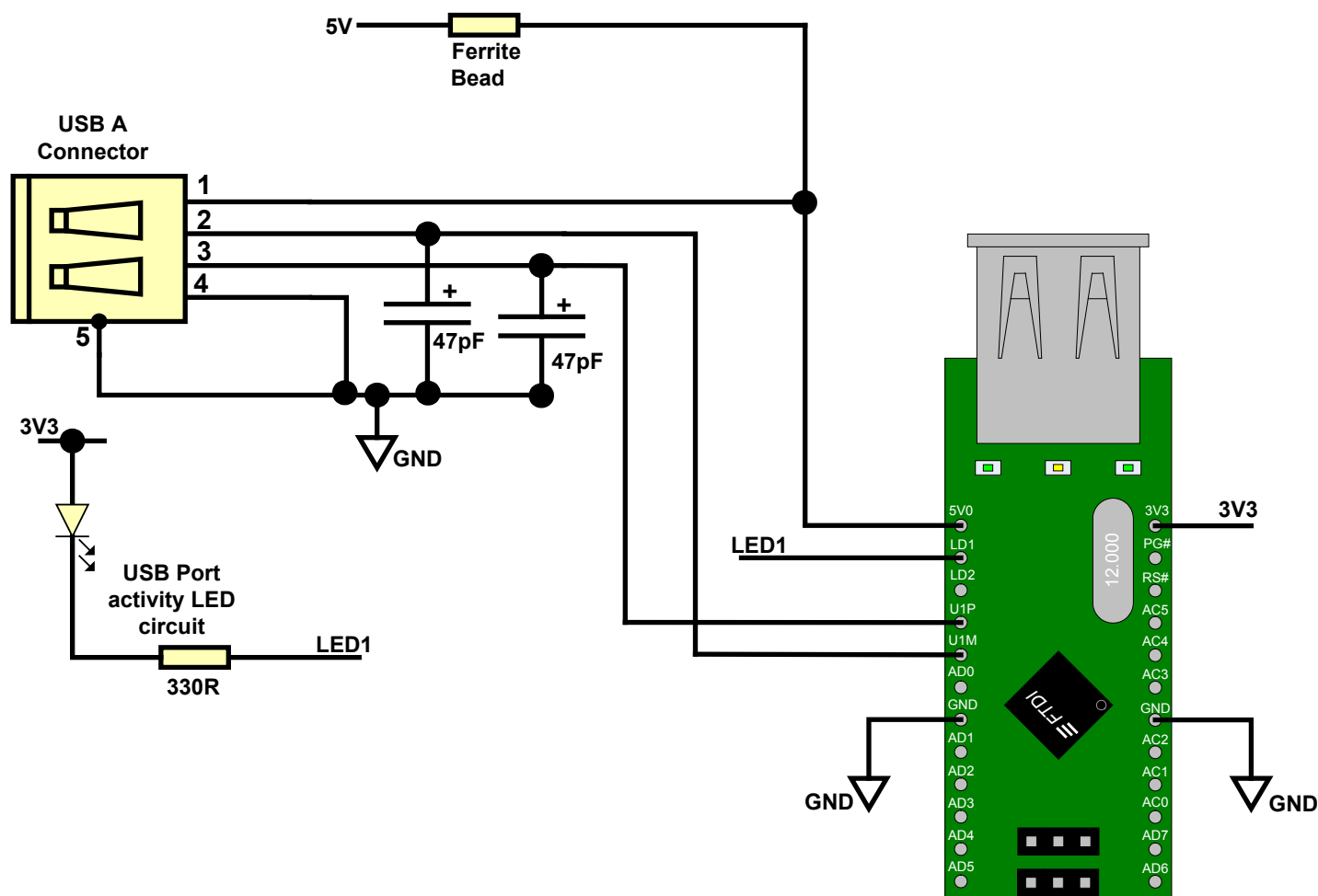


Figure 10 - Additional USB port configuration.

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