VND5E050J-E
VND5E050K-E

Double channel high side driver for automotive applications

Features

Max supply voltage	V_{CC}	41V
Operating voltage range	V_{CC}	4.5 to 28V
Max On-State resistance (per ch.)	R_{ON}	50 mΩ
Current limitation (typ)	I_{LIMH}	27 A
Off state supply current	I_S	2 μA(1)

(1) Typical value with all loads connected.

- General
  - Inrush current active management by power limitation
  - Very low stand-by current
  - 3.0V CMOS compatible inputs
  - Optimized electromagnetic emissions
  - Very low electromagnetic susceptibility
  - In compliance with the 2002/95/EC european directive
- Diagnostic functions
  - Open Drain status output
  - On-state open load detection
  - Off-state open load detection
  - Output short to Vcc detection
  - Overload and short to ground (power limitation) indication
  - Thermal shutdown indication
- Protections
  - Undervoltage shutdown
  - Overvoltage clamp
  - Load current limitation
  - Self limiting of fast thermal transients
  - Protection against loss of ground and loss of V_{CC}
  - Over-temperature shutdown with autorestart (thermal shutdown)
  - Reverse battery protected[a]
  - Electrostatic discharge protection

Application

- All types of resistive, inductive and capacitive loads

Description

The VND5E050J-E and VND5E050K-E are double channel high-side drivers manufactured in the ST proprietary VIPower M0-5 technology and housed in the tiny PowerSSO-12 and PowerSSO-24 packages.

The VND5E050J-E and VND5E050K-E are designed to drive automotive grounded loads delivering protection, diagnostics and easy 3V and 5V CMOS-compatible interface with any microcontroller.

The devices integrate advanced protective functions such as load current limitation, inrush and overload active management by power limitation, over-temperature shut-off with auto-restart and over-voltage active clamp.

A dedicated active low digital status pin is associated with every output channel in order to provide *Enhanced* diagnostic functions including fast detection of overload and short-circuit to ground, over-temperature indication, short-circuit to V_{CC} diagnosis and ON & OFF state open-load detection.

The diagnostic feedback of the whole device can be disabled by pulling the STAT_DIS pin up, thus allowing wired-ORing with other similar devices.

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[a] See *Application schematic on page 22*.

Contents

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1 Block diagram and pin description

Figure 1. Block diagram

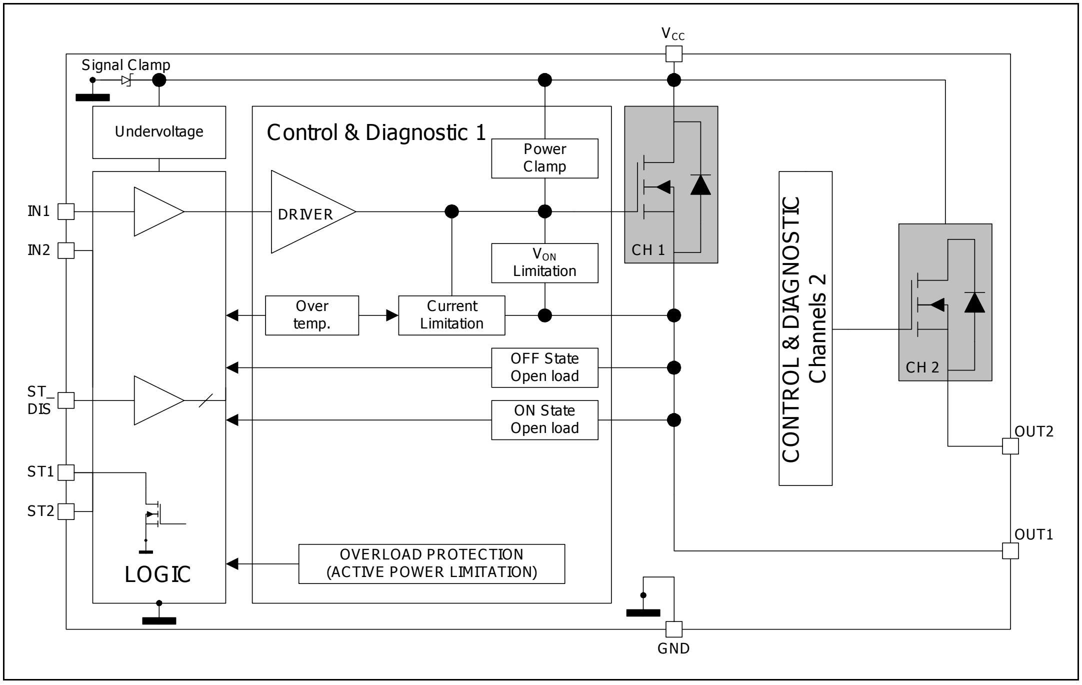


Table 1. Pin function

Name	Function
V_{CC}	Battery connection.
OUTPUTn	Power output.
GND	Ground connection. Must be reverse battery protected by an external diode/resistor network.
INPUTn	Voltage controlled input pin with hysteresis, CMOS compatible. Controls output switch state.
STATUSn	Open Drain digital diagnostic pin.
STAT_DIS	Active high CMOS compatible pin, to disable the STATUS pin.

Figure 2. Configuration diagram (top view)

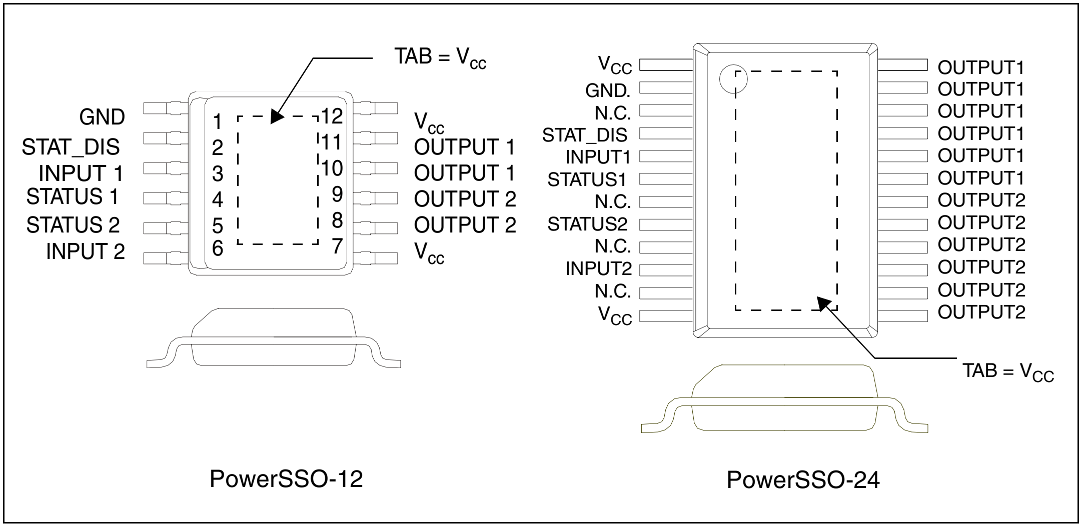
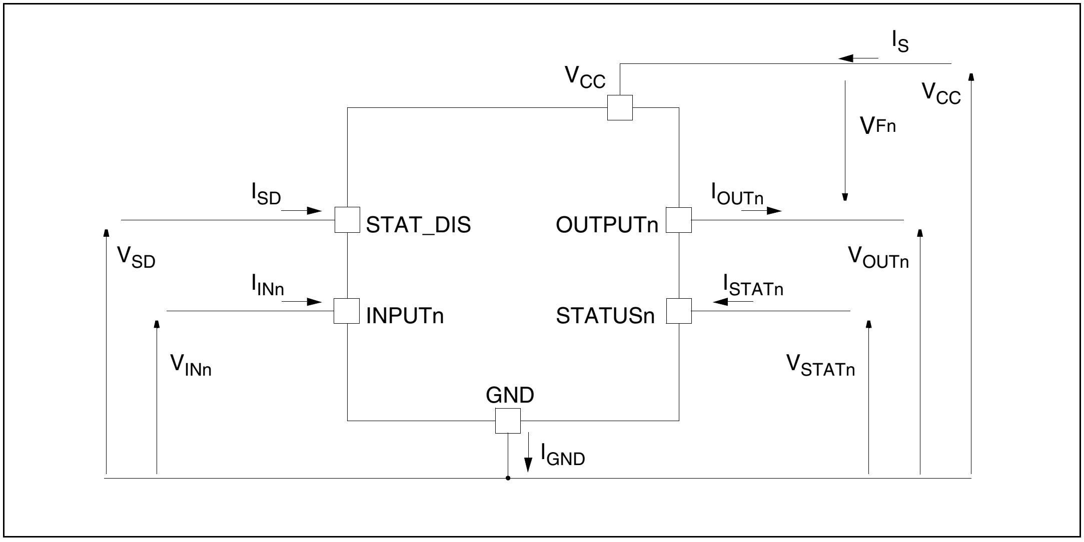


Table 2. Suggested connections for unused and not connected pins

Connection / pin	Status	N.C.	Output	Input	STAT_DIS
Floating	X	X	X	X	X
To ground	Not allowed	X	Not allowed	Through 10KΩ resistor	Through 10KΩ resistor

2 Electrical specifications

Figure 3. Current and voltage conventions



Note: $V_{Fn} = V_{OUTn} - V_{CC}$ *during reverse battery condition.*

2.1 Absolute maximum ratings

Stressing the device above the rating listed in the “Absolute maximum ratings” table may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the Operating sections of this specification is not implied. Exposure to the conditions in table below for extended periods may affect device reliability. Refer also to the STMicroelectronics SURE Program and other relevant quality document.

Table 3. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{CC}	DC supply voltage	41	V
$-V_{CC}$	Reverse DC supply voltage	0.3	V
$-I_{GND}$	DC reverse ground pin current	200	mA
I_{OUT}	DC output current	Internally limited	A
$-I_{OUT}$	Reverse DC output current	15	A
I_{IN}	DC input current	+10 / -1	mA
I_{STAT}	DC status current	+10 / -1	mA
I_{STAT_DIS}	DC status disable current	+10 / -1	mA
E_{MAX}	Maximum switching energy (L=3 mH; R_L=0Ω; V_{bat}=13.5V; T_{jstart}=150ºC; $I_{OUT} = I_{limL}$*(Typ.)*)	104	mJ

Table 3. Absolute maximum ratings (continued)

Symbol	Parameter	Value	Unit
V_{ESD}	Electrostatic discharge (Human Body Model: R=1.5KΩ; C=100pF) - INPUT - STATUS - STAT_DIS - OUTPUT - V_{CC}	 4000 4000 4000 5000 5000	 V V V V V
V_{ESD}	Charge device model (CDM-AEC-Q100-011)	750	V
T_j	Junction operating temperature	-40 to 150	°C
T_{stg}	Storage temperature	- 55 to 150	°C

2.2 Thermal data

Table 4. Thermal data

Symbol	Parameter	Value		Unit
		PowerSSO-12	PowerSSO-24	
$R_{thj\text{-}case}$	Thermal resistance junction-case (max.) (with one channel ON)	2.8	2.8	°C/W
$R_{thj\text{-}amb}$	Thermal resistance junction-ambient (max.)	See *Figure 36*	See *Figure 40*	°C/W

2.3 Electrical characteristics

Values specified in this section are for 8V<V_{CC}<28V; -40°C<T_j<150°C, unless otherwise stated.

Table 5. Power section

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{CC}	Operating supply voltage		4.5	13	28	V
V_{USD}	Undervoltage shutdown			3.5	4.5	V
$V_{USDhyst}$	Undervoltage shutdown hysteresis			0.5		V
R_{ON}	On state resistance(2)	I_{OUT}=2A; T_j=25°C I_{OUT}=2A; T_j=150°C I_{OUT}=2A; V_{CC}=5V; T_j=25°C			50 100 65	mΩ mΩ mΩ
V_{clamp}	Clamp voltage	I_S=20mA	41	46	52	V
I_S	Supply current	Off State; V_{CC}=13V; T_j=25°C; V_{IN}=V_{OUT}= 0V On State; V_{CC}=13V; V_{IN}=5V; I_{OUT}=0A		2(1) 3	5(1) 6	µA mA
$I_{L(off1)}$	Off state output current(2)	V_{IN}=V_{OUT}=0V; V_{CC}=13V; T_j=25°C V_{IN}=V_{OUT}=0V; V_{CC}=13V; T_j=125°C	0 0	0.01	3 5	µA
V_F	Output - V_{CC} diode voltage(2)	-I_{OUT}=2 A; T_j=150°C			0.7	V

(1) PowerMOS leakage included.

(2) For each channel.

Table 6. Switching (V_{CC} = 13V; T_j = 25°C)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn- On delay time	R_L= 6.5Ω (see *Figure 6*)		20		µs
$t_{d(off)}$	Turn- Off delay time	R_L= 6.5Ω (see *Figure 6*)		40		µs
$dV_{OUT}/dt_{(on)}$	Turn- On voltage slope	R_L= 6.5Ω		See *Figure 26*		V/ µs
$dV_{OUT}/dt_{(off)}$	Turn- Off voltage slope	R_L= 6.5Ω		See *Figure 28*		V/ µs
W_{ON}	Switching energy losses during t_{won}	R_L= 6.5Ω (see *Figure 6*)		0.21		mJ
W_{OFF}	Switching energy losses during t_{woff}	R_L= 6.5Ω (see *Figure 6*)		0.28		mJ

Table 7. Status pin (V_{SD}=0V)

Symbol	Parameter	Test conditions	Min.	Typ.	Max	Unit
V_{STAT}	Status low output voltage	I_{STAT}=1.6 mA, V_{SD}=0V			0.5	V
I_{LSTAT}	Status leakage current	Normal Operation or V_{SD}=5V, V_{STAT} = 5V			10	µA
C_{STAT}	Status pin input capacitance	Normal Operation or V_{SD}=5V, V_{STAT} = 5V			100	pF
V_{SCL}	Status clamp voltage	I_{STAT} = 1mA I_{STAT} = -1mA	5.5	 -0.7	7	V V

Table 8. Protections (1)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{limH}	DC short circuit current	V_{CC}=13V;5V<V_{CC}<28V	19	27	38 38	A A
I_{limL}	Short circuit current during thermal cycling	V_{CC}=13V T_R<T_j<T_{TSD}		7		A
T_{TSD}	Shutdown temperature		150	175	200	°C
T_R	Reset temperature		T_{RS} + 1	T_{RS} + 5		°C
T_{RS}	Thermal reset of STATUS		135			°C
T_{HYST}	Thermal hysteresis (T_{TSD}-T_R)			7		°C
t_{SDL}	Status delay in overload conditions	T_j>T_{TSD} (see *Figure 4*)			20	µs
V_{DEMAG}	Turn-off output voltage clamp	I_{OUT}=2A; V_{IN}=0; L=6mH	V_{CC}-41	V_{CC}-46	V_{CC}-52	V
V_{ON}	Output voltage drop limitation	I_{OUT}=0.1A; T_j= -40°C...+150°C		25		mV

(1) To ensure long term reliability under heavy overload or short circuit conditions, protection and related diagnostic signals must be used together with a proper software strategy. If the device is subjected to abnormal conditions, this software must limit the duration and number of activation cycles.

Table 9. Openload detection ($8V<V_{CC}<18V$)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{OL}	Openload ON state detection threshold	V_{IN} = 5V;	10		70	mA
$t_{DOL(on)}$	Openload ON state detection delay	I_{OUT} = 0A, V_{CC}=13V (see *Figure 4*)			200	µs
t_{POL}	Delay between INPUT falling edge and STATUS rising edge in open load condition	I_{OUT} = 0A (see *Figure 4*)	200	500	1200	µs
V_{OL}	Openload OFF state voltage detection threshold	V_{IN} = 0V;	2		4	V
t_{DSTKON}	Output short circuit to V_{CC} detection delay at turn Off	See *Figure 4*	180		t_{POL}	µs
$I_{L(off2)}$	Off state output current[1]	V_{IN}= 0V; V_{OUT}= 4V (see *Section 3.4: Open load detection in Off state*)	-75		0	µA
td_vol	Delay response from output rising edge to STATUS falling edge in open load	V_{IN}= 0V; V_{OUT}= 4V			20	µs

[1] For each channel.

Table 10. Logic input

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{IL}	Input low level				0.9	V
I_{IL}	Low level input current	V_{IN} =0.9 V	1			µA
V_{IH}	Input high level		2.1			V
I_{IH}	High level input current	V_{IN} = 2.1 V			10	µA
$V_{I(hyst)}$	Input hysteresis voltage		0.25			V
V_{ICL}	Input clamp voltage	I_{IN} = 1mA	5.5		7	V
		I_{IN} = -1mA		-0.7		V
V_{SDL}	STAT_DIS low level voltage				0.9	V
I_{SDL}	Low level STAT_DIS current	V_{SD} = 0.9 V	1			µA
V_{SDH}	STAT_DIS high level voltage		2.1			V
I_{SDH}	High level STAT_DIS current	V_{SD} = 2.1 V			10	µA
$V_{SD(hyst)}$	STAT_DIS hysteresis voltage		0.25			V
V_{SDCL}	STAT_DIS clamp voltage	I_{SD}=1mA	5.5		7	V
		I_{SD}=-1mA		-0.7		V

Figure 4. Status timings

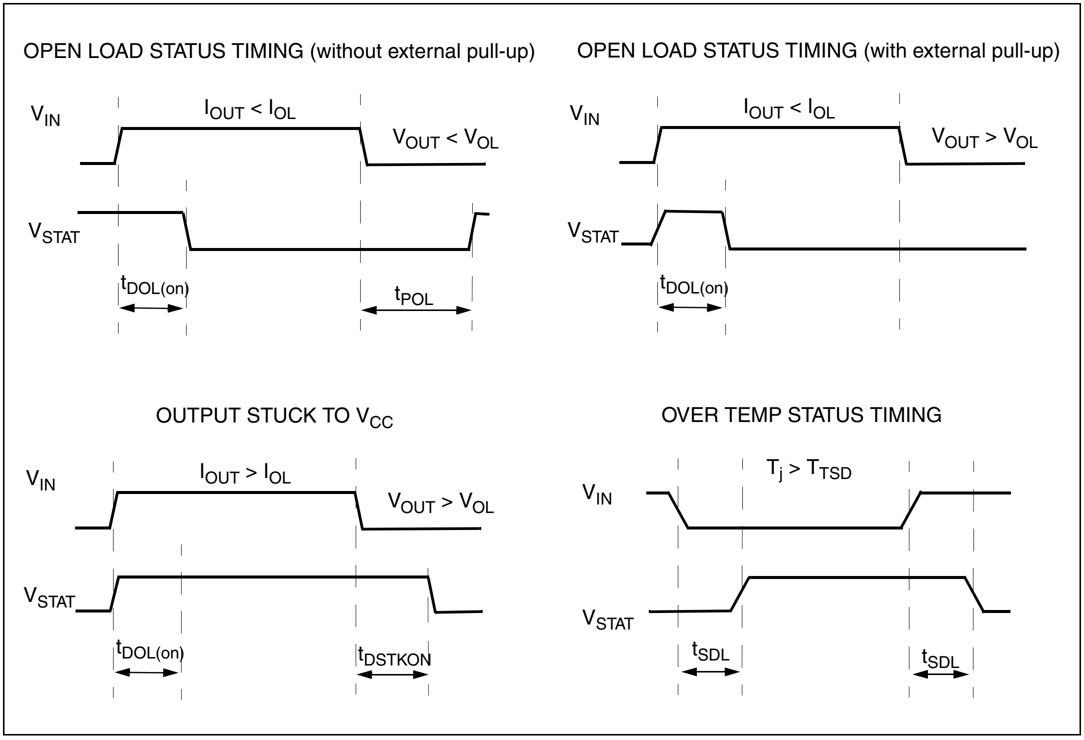


Figure 5. Output voltage drop limitation

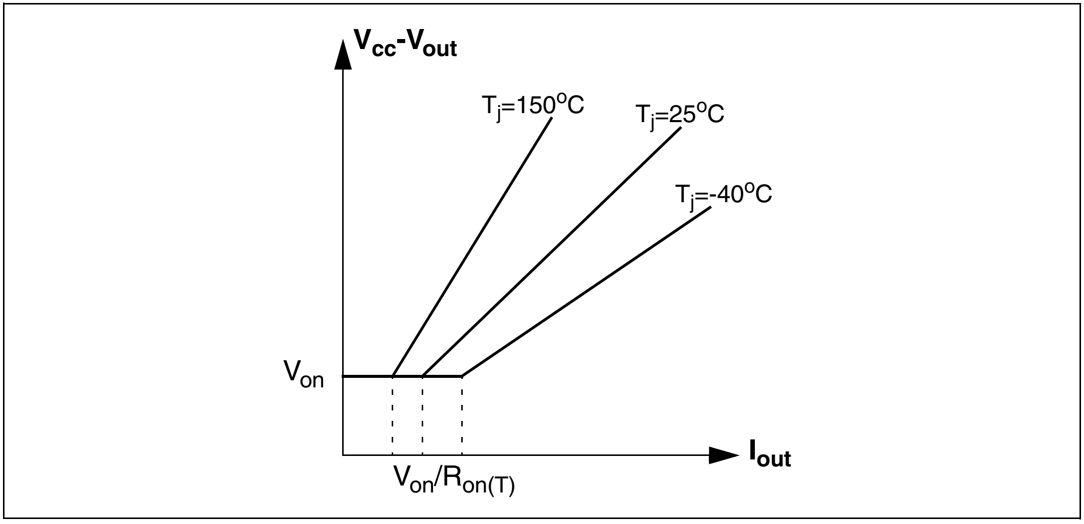


Figure 6. Switching characteristics

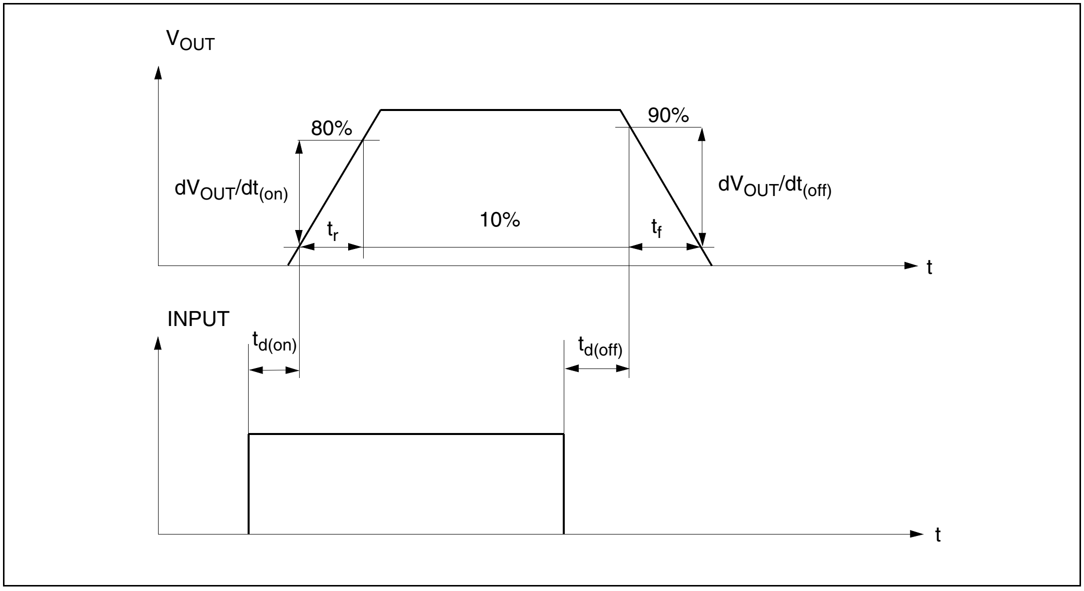


Table 11. Truth table

Conditions	Input	Output	Sense (V_{CSD}=0V)(1)
Normal operation	L H	L H	H H
Overtemperature	L H	L L	H L
Undervoltage	L H	L L	X X
Overload & Short circuit to GND	H H	X (no power limitation) Cycling (power limitation)	H L
Output voltage > V_{OL}	L H	H H	L(2) H
Output current < I_{OL}	L H	L H	H (3) L

(1) If the V_{CSD} is high, the SENSE output is at a high impedance, its potential depends on leakage currents and external circuit.

(2) The STATUS pin is low with a delay equal to t_{DSTKON} after INPUT falling edge.

(3) The STATUS pin becomes high with a delay equal to t_{POL} after INPUT falling edge.

Table 12. Electrical transient requirements

ISO 7637-2: 2004(E) Test pulse	Test levels		Number of pulses or test times	Burst cycle/pulse repetition time		Delays and Impedance
	III	IV				
1	-75V	-100V	5000 pulses	0.5 s	5 s	2 ms, 10 Ω
2a	+37V	+50V	5000 pulses	0.2 s	5 s	50 µs, 2 Ω
3a	-100V	-150V	1h	90 ms	100 ms	0.1 µs, 50 Ω
3b	+75V	+100V	1h	90 ms	100 ms	0.1 µs, 50 Ω
4	-6V	-7V	1 pulse			100 ms, 0.01 Ω
5b(2)	+65V	+87V	1 pulse			400 ms, 2 Ω

ISO 7637-2: 2004(E) Test pulse	Test level results(1)	
	III	IV
1	C	C
2a	C	C
3a	C	C
3b	C	C
4	C	C
5b(2)	C	C

(1) The above test levels must be considered referred to V_{CC} = 13.5V except for pulse 5b.

(2) Valid in case of external load dump clamp: 40V maximum referred to ground.

Class	Contents
C	All functions of the device are performed as designed after exposure to disturbance.
E	One or more functions of the device are not performed as designed after exposure to disturbance and cannot be returned to proper operation without replacing the device.

2.4 Waveforms

Figure 7. Normal operation

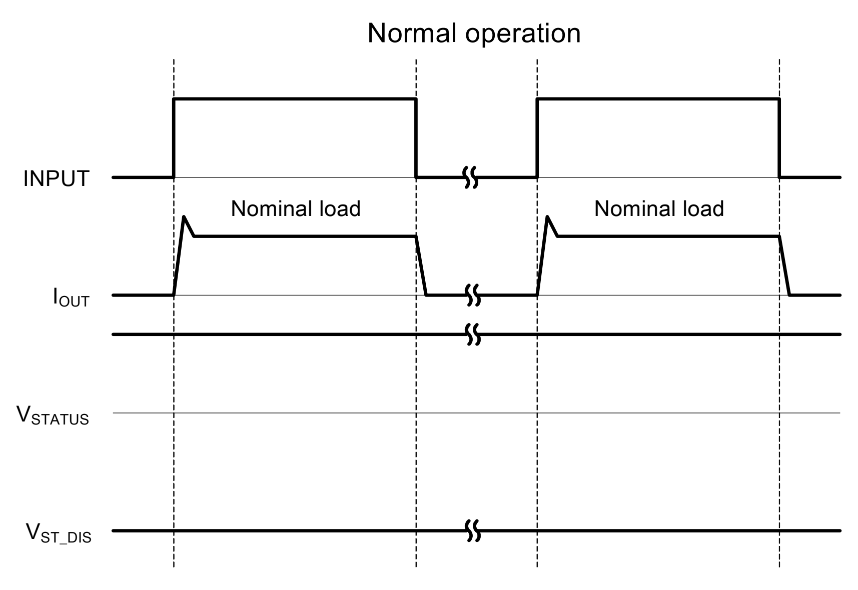


Figure 8. Undervoltage shutdown

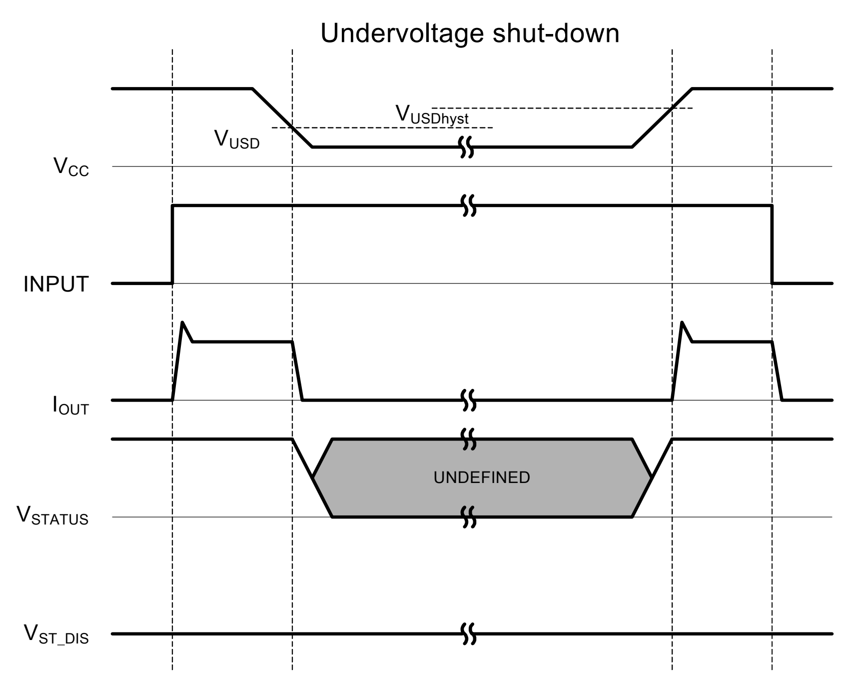


Figure 9. Overload or Short to GND

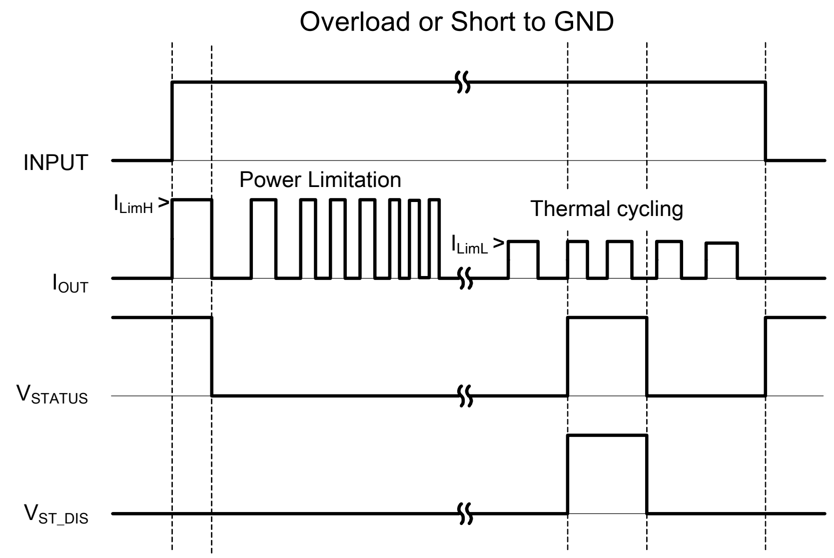


Figure 10. Intermittent Overload

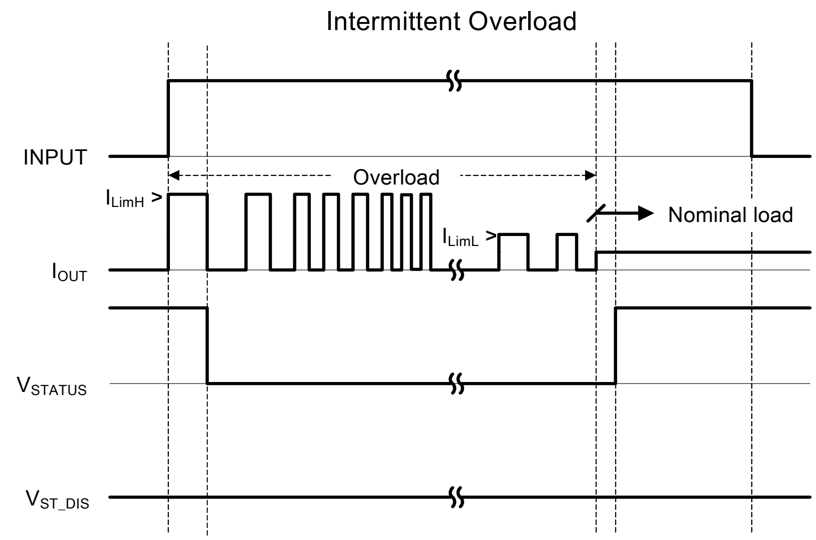


Figure 11. Open Load with external pull-up

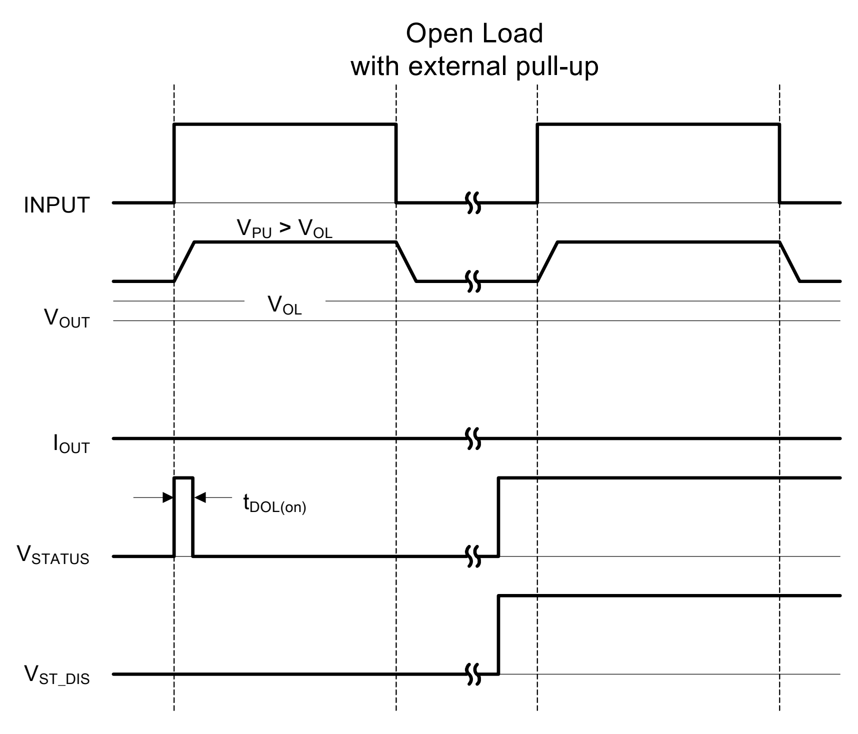


Figure 12. Open Load without external pull-up

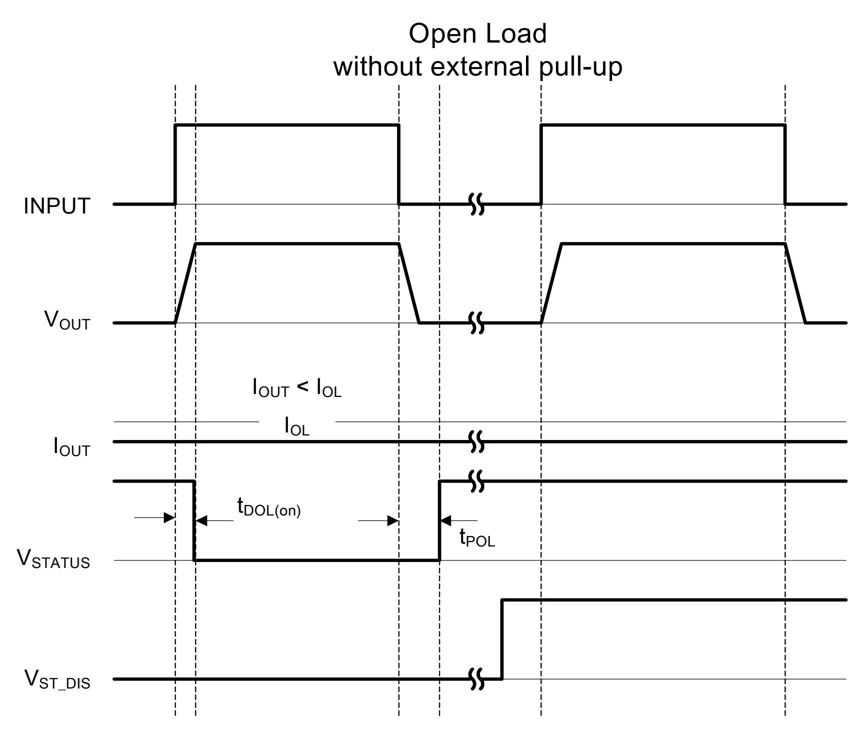


Figure 13. Short to V_{CC}

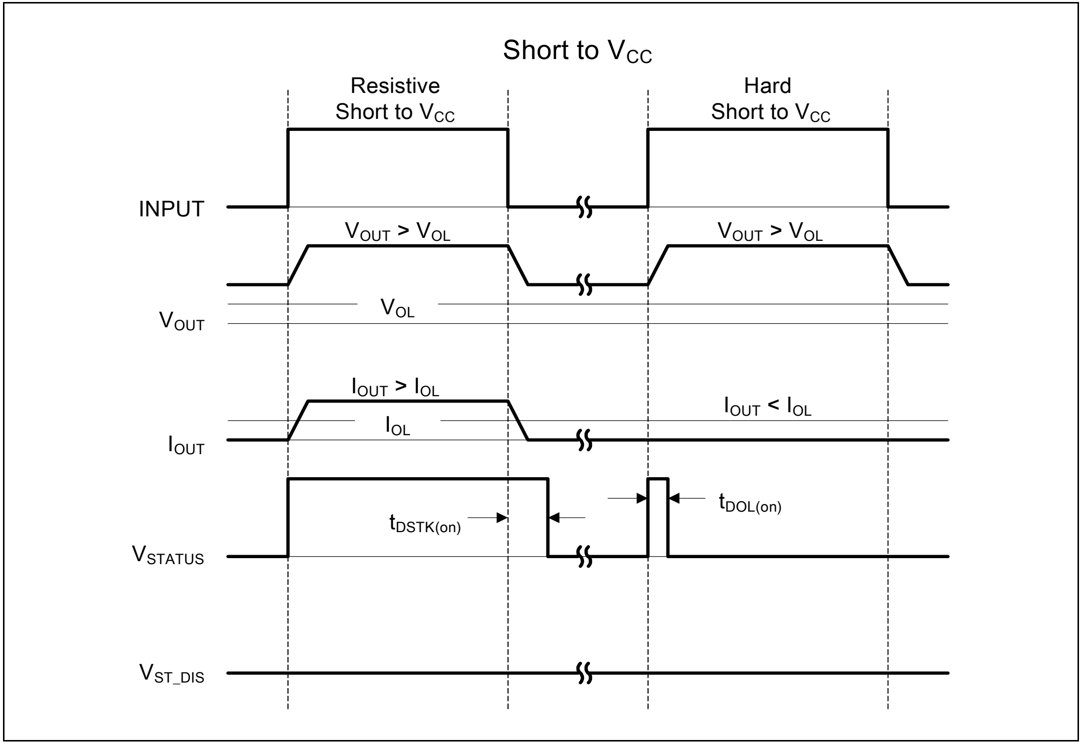
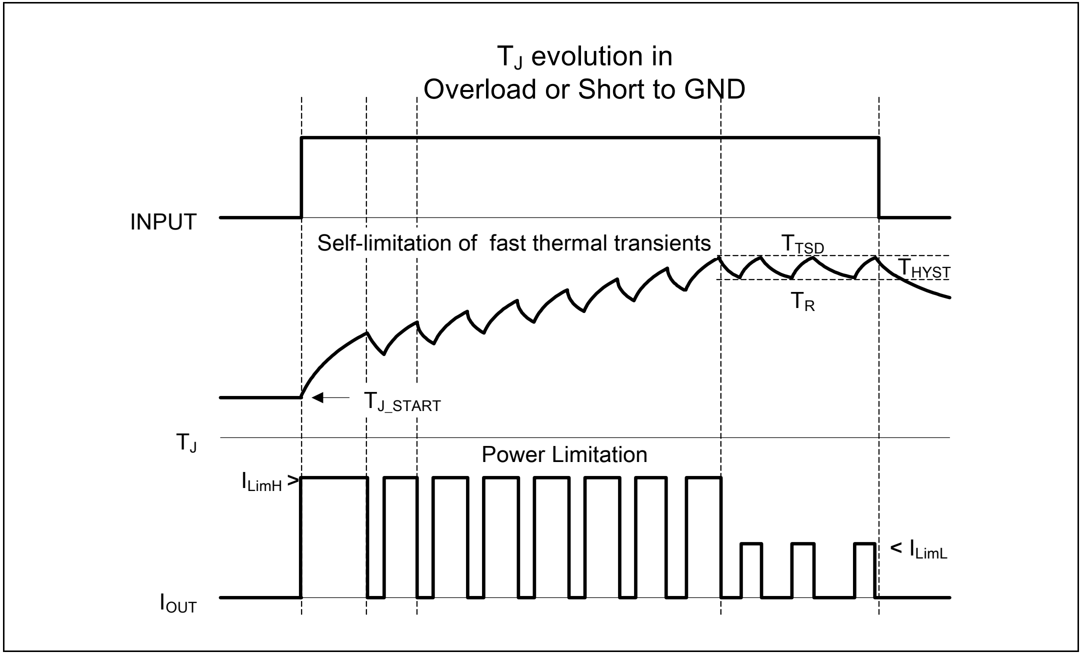


Figure 14. T_J evolution in Overload or Short to GND



2.5 Electrical characteristics curves

Figure 15. Off state output current

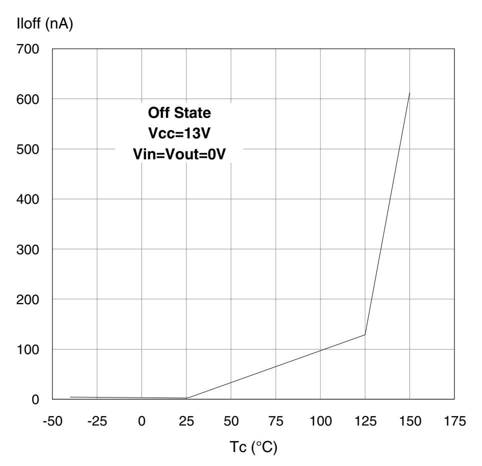


Figure 16. High level input current

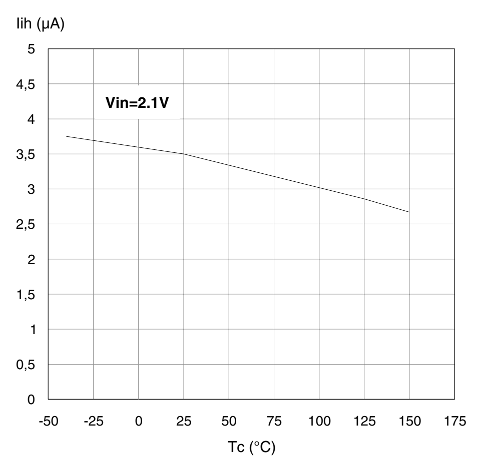


Figure 17. Input clamp voltage

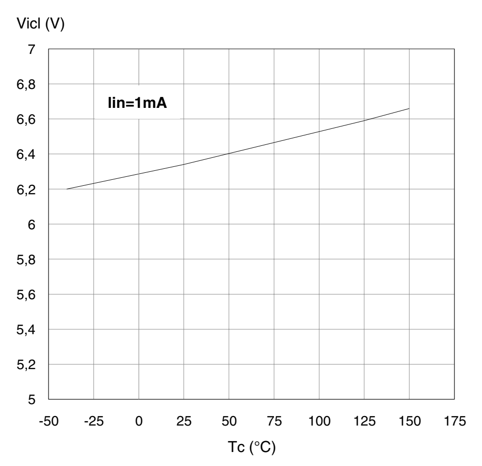


Figure 18. Input high level

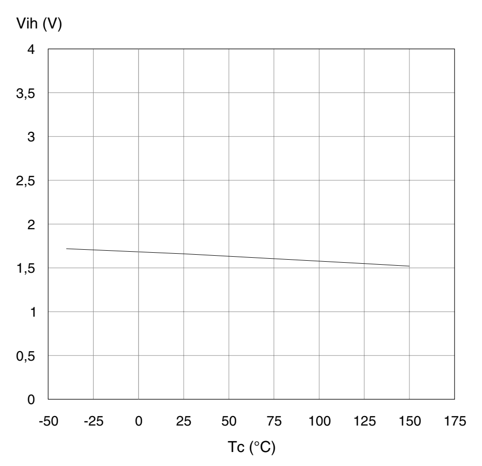


Figure 19. Input low level

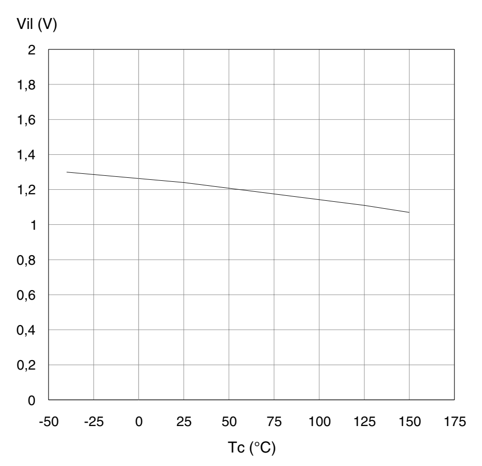


Figure 20. Low level STAT_DIS current

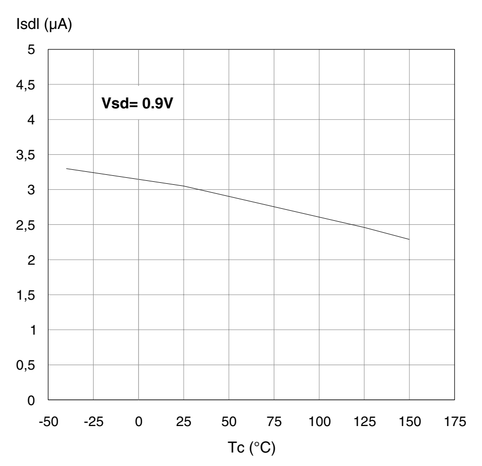


Figure 21. On state resistance vs T_{case}

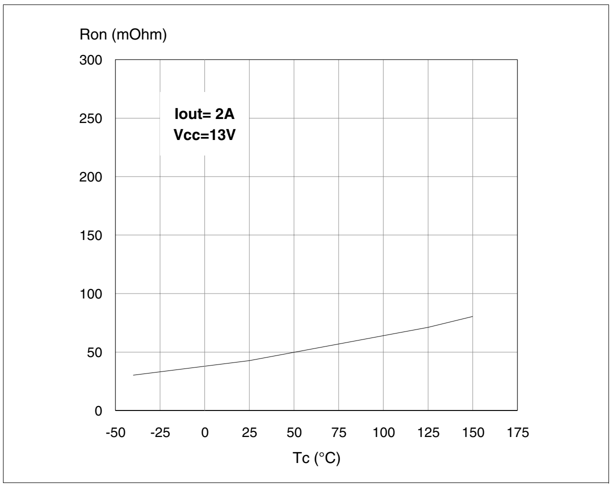


Figure 22. High level STAT_DIS current

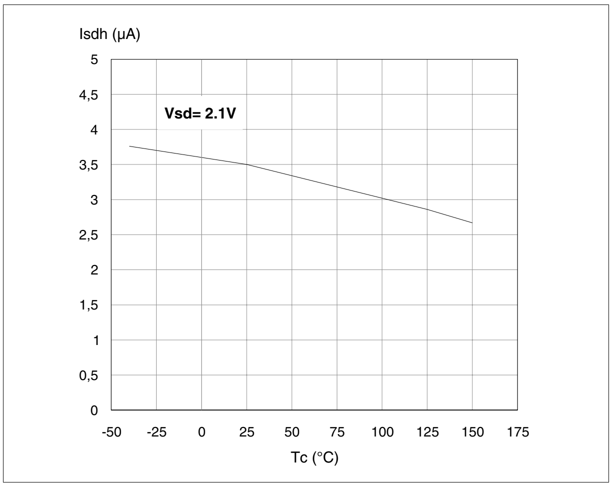


Figure 23. On state resistance vs V_{CC}

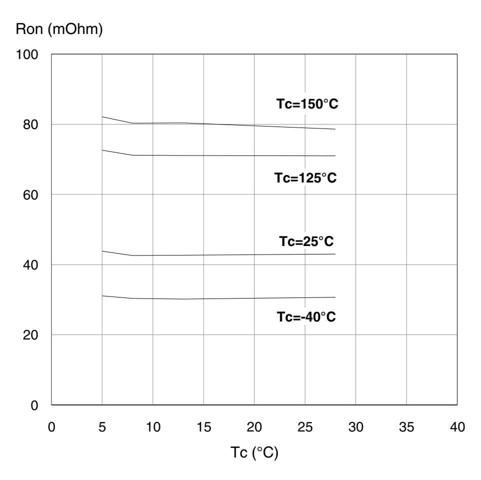


Figure 24. Low level input current

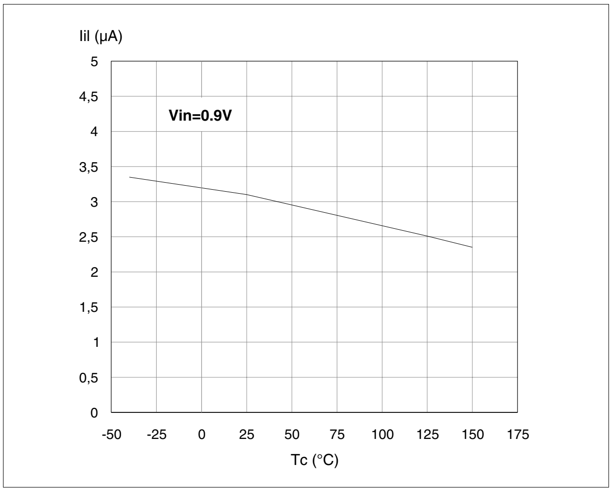


Figure 25. I_{LIM} vs T_{case}

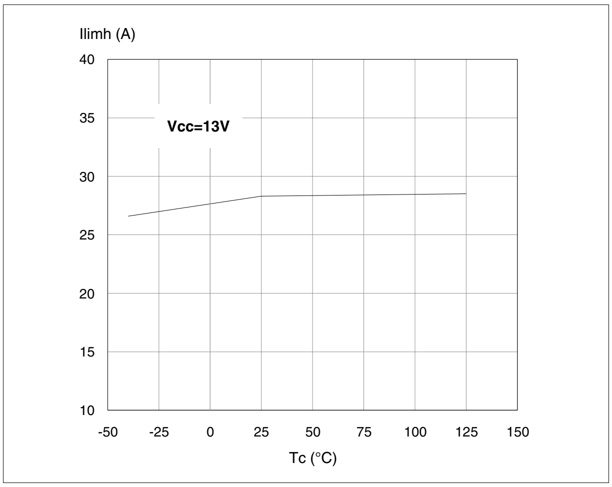


Figure 26. Turn-On voltage slope

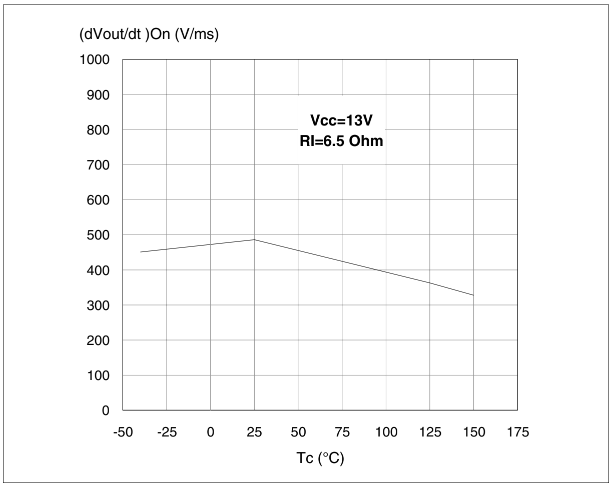


Figure 27. Undervoltage shutdown

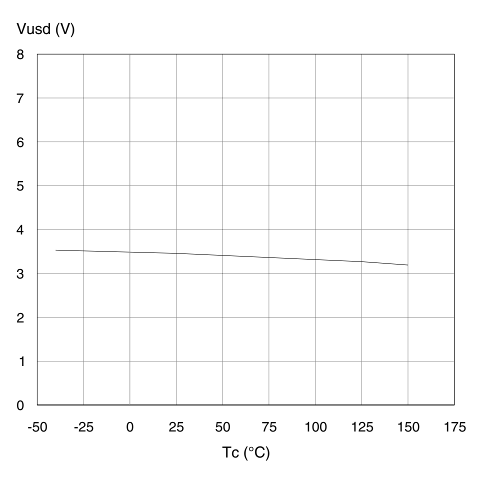


Figure 28. Turn-Off voltage slope

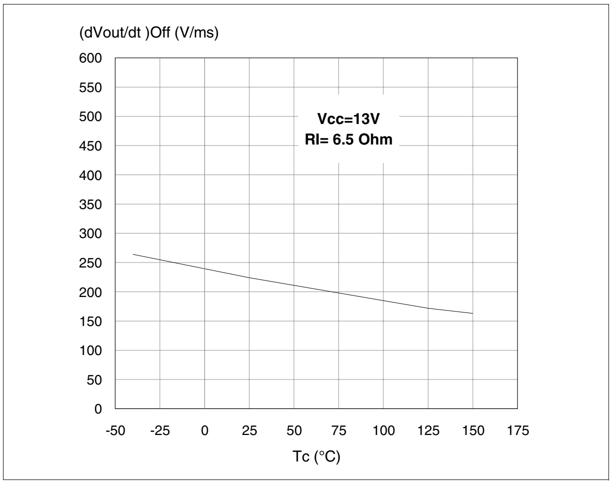


Figure 29. STAT_DIS clamp voltage

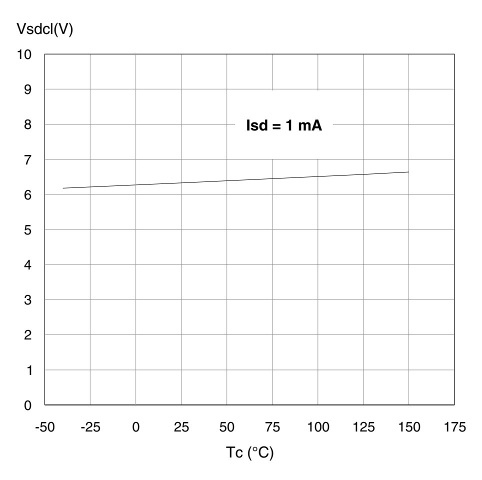


Figure 30. High level STAT_DIS voltage

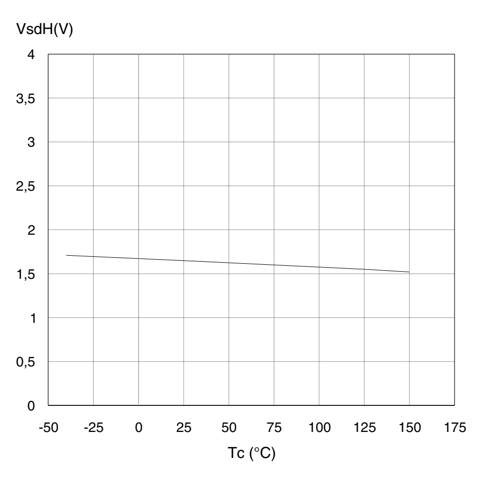
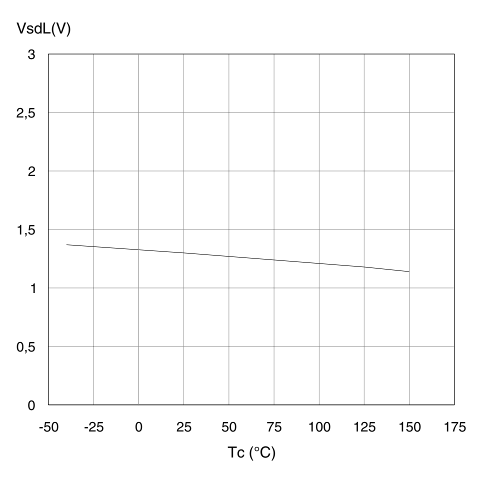
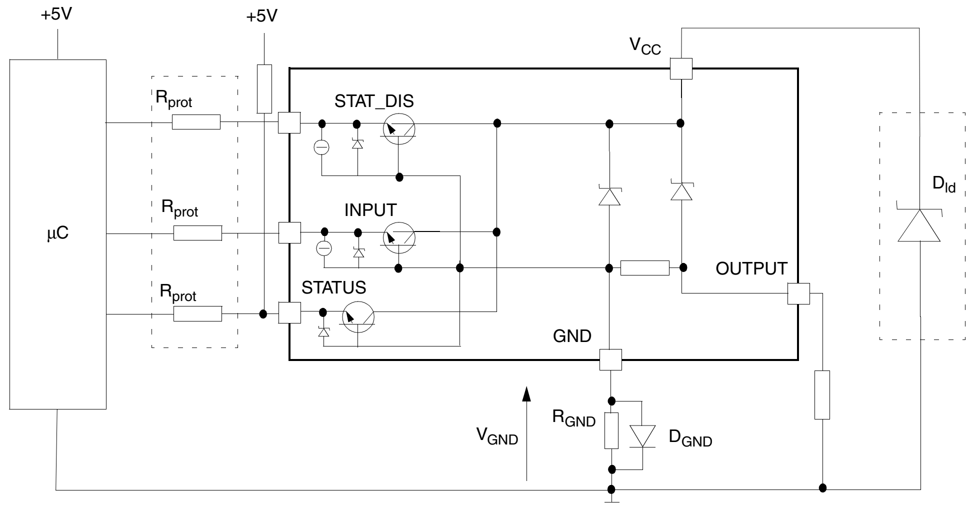


Figure 31. Low level STAT_DIS voltage



3 Application information

Figure 32. Application schematic



Note: Channel 2 has the same internal circuit as channel 1.

3.1 GND protection network against reverse battery

3.1.1 Solution 1: resistor in the ground line (R_{GND} only)

This can be used with any type of load.

The following is an indication on how to dimension the R_{GND} resistor.

1. $R_{GND} \leq 600mV / (I_{S(on)max})$.
2. $R_{GND} \geq (-V_{CC}) / (-I_{GND})$

where $-I_{GND}$ is the DC reverse ground pin current and can be found in the absolute maximum rating section of the device datasheet.

Power Dissipation in R_{GND} (when $V_{CC}<0$: during reverse battery situations) is:

$P_D = (-V_{CC})^2 / R_{GND}$

This resistor can be shared amongst several different HSDs. Please note that the value of this resistor should be calculated with formula (1) where $I_{S(on)max}$ becomes the sum of the maximum on-state currents of the different devices.

Please note that if the microprocessor ground is not shared by the device ground then the R_{GND} will produce a shift ($I_{S(on)max} * R_{GND}$) in the input thresholds and the status output values. This shift will vary depending on how many devices are ON in the case of several high side drivers sharing the same R_{GND}.

If the calculated power dissipation leads to a large resistor or several devices have to share the same resistor then ST suggests to utilize Solution 2 (see below).

3.1.2 Solution 2: diode (D_{GND}) in the ground line

A resistor (R_{GND}=1kΩ) should be inserted in parallel to D_{GND} if the device drives an inductive load.

This small signal diode can be safely shared amongst several different HSDs. Also in this case, the presence of the ground network will produce a shift (≈ 600mV) in the input threshold and in the status output values if the microprocessor ground is not common to the device ground. This shift will not vary if more than one HSD shares the same diode/resistor network.

3.2 Load dump protection

D_{ld} is necessary (Voltage Transient Suppressor) if the load dump peak voltage exceeds the V_{CC} max DC rating. The same applies if the device is subject to transients on the V_{CC} line that are greater than the ones shown in the ISO 7637-2: 2004(E) table.

3.3 MCU I/Os protection

If a ground protection network is used and negative transient are present on the V_{CC} line, the control pins will be pulled negative. ST suggests to insert a resistor (R_{prot}) in line to prevent the µC I/Os pins to latch-up.

The value of these resistors is a compromise between the leakage current of µC µand the current required by the HSD I/Os (Input levels compatibility) with the latch-up limit of µC I/Os.

$-V_{CCpeak}/I_{latchup} \leq R_{prot} \leq (V_{OH\mu C}-V_{IH}-V_{GND}) / I_{IHmax}$

Calculation example:

For V_{CCpeak}= - 100V and $I_{latchup} \geq$ 20mA; $V_{OH\mu C} \geq$ 4.5V

$5k\Omega \leq R_{prot} \leq 180k\Omega$

Recommended values: R_{prot} =10kΩ

3.4 Open load detection in Off state

Off state open load detection requires an external pull-up resistor (R_{PU}) connected between OUTPUT pin and a positive supply voltage (V_{PU}) like the +5V line used to supply the microprocessor.

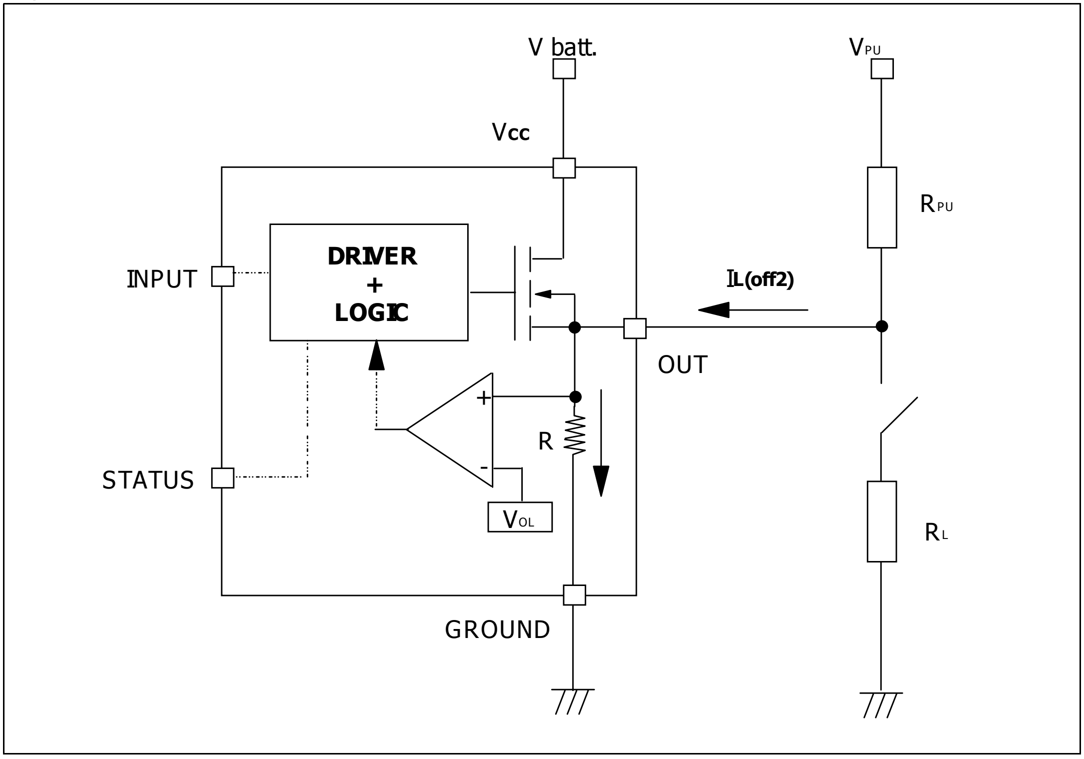
The external resistor has to be selected according to the following requirements:

1. no false open load indication when load is connected: in this case we have to avoid V_{OUT} to be higher than V_{Olmin}; this results in the following condition $V_{OUT}=(V_{PU}/(R_L+R_{PU}))R_L<V_{Olmin}$.
2. no misdetection when load is disconnected: in this case the V_{OUT} has to be higher than V_{OLmax}; this results in the following condition $R_{PU}<(V_{PU}–V_{OLmax})/I_{L(off2)}$.

Because $I_{s(OFF)}$ may significantly increase if V_{out} is pulled high (up to several mA), the pull-up resistor R_{PU} should be connected to a supply that is switched OFF when the module is in standby.

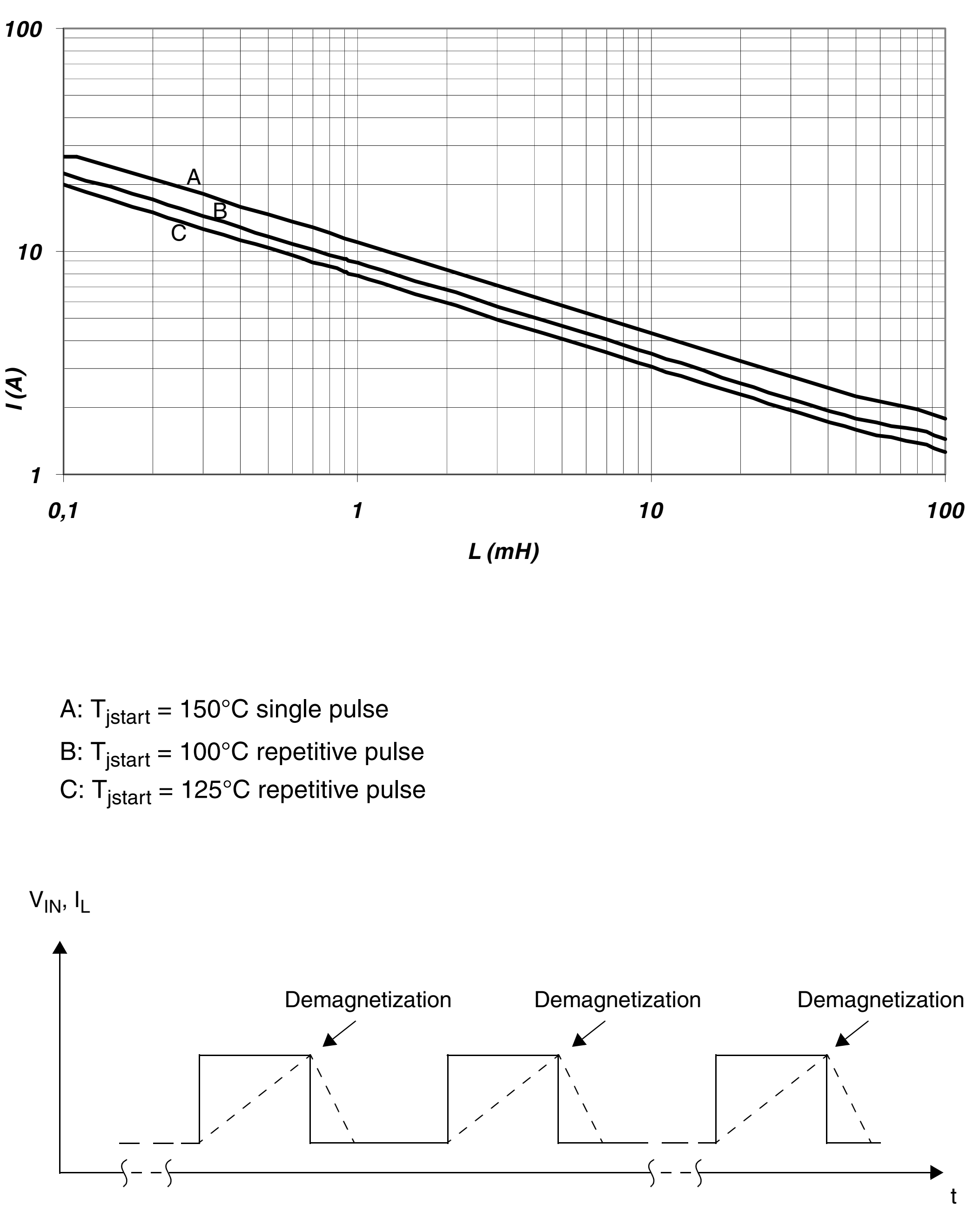
The values of V_{OLmin}, V_{OLmax} and $I_{L(off2)}$ are available in the Electrical Characteristics section.

Figure 33. Open load detection in Off state



3.5 Maximum demagnetization energy (V_{CC} = 13.5V)

Figure 34. Maximum turn-Off current versus inductance (for each channel)



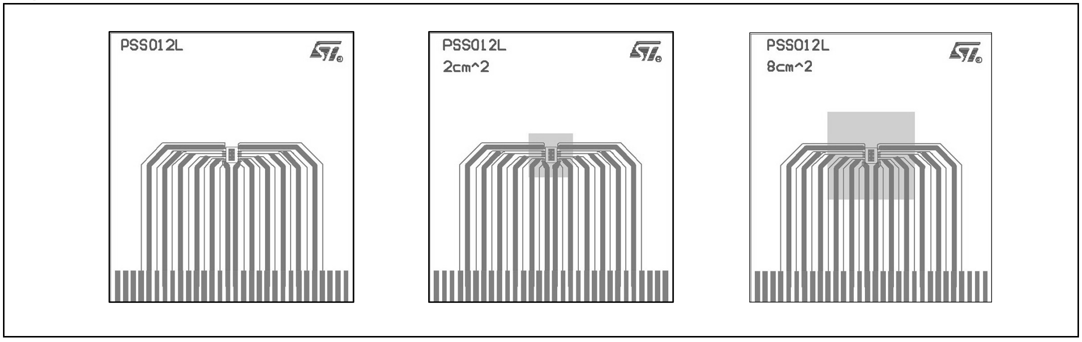
Note: *Values are generated with $R_L = 0\,\Omega$.*

In case of repetitive pulses, T_{jstart} (at beginning of each demagnetization) of every pulse must not exceed the temperature specified above for curves A and B.

4 Package and PCB thermal data

4.1 PowerSSO-12 thermal data

Figure 35. PowerSSO-12 PC board



Note: *Layout condition of R_{th} and Z_{th} measurements (PCB: Double layer, Thermal Vias, FR4 area= 77mm x 86mm,PCB thickness=1.6mm, Cu thickness=70µm (front and back side), Copper areas: from minimum pad lay-out to $8cm^2$).*

Figure 36. $R_{thj-amb}$ Vs. PCB copper area in open box free air condition (one channel ON)

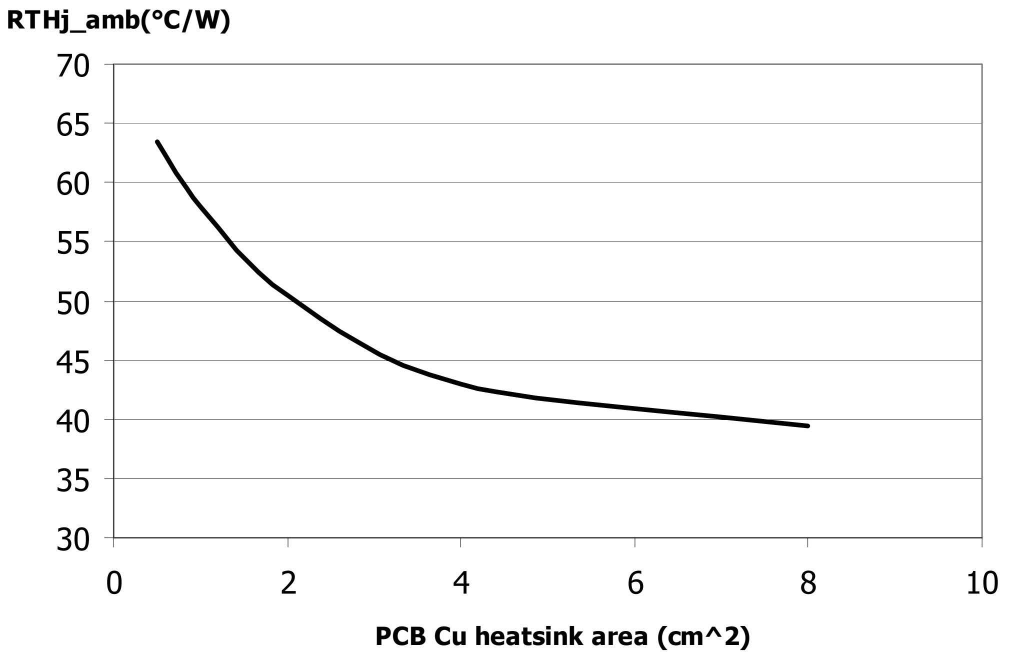
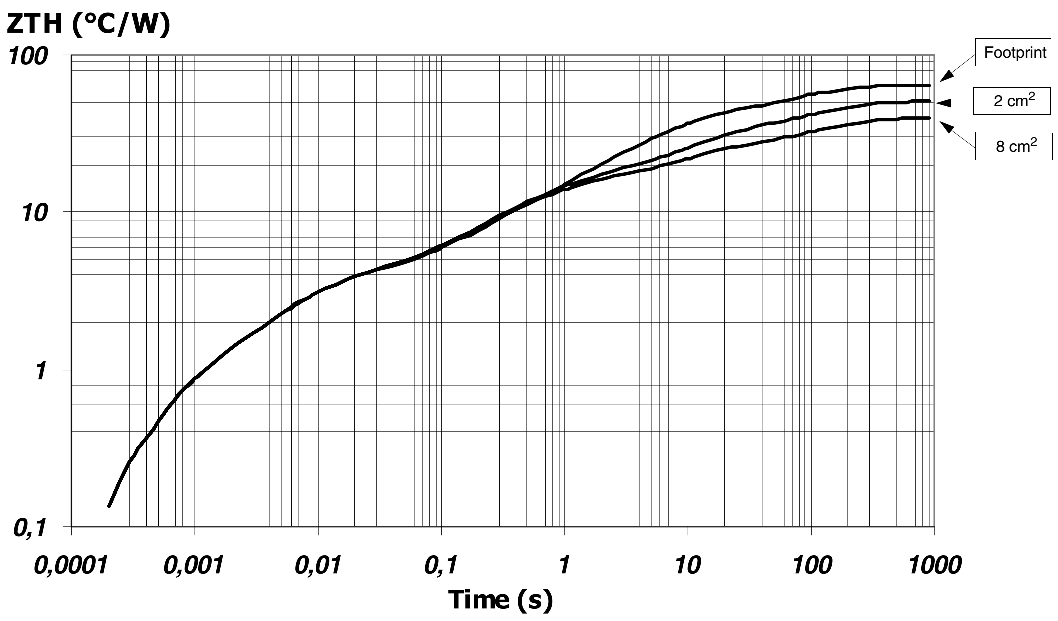


Figure 37. PowerSSO-12 thermal impedance junction ambient single pulse (one channel ON)

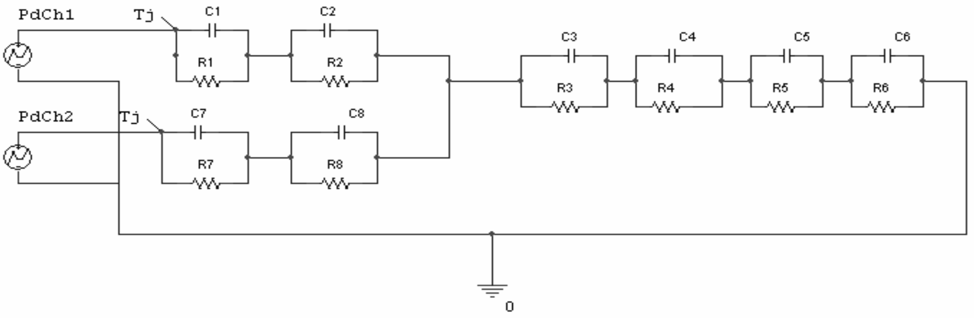


Equation 1: pulse calculation formula

$$Z_{TH\delta} = R_{TH} \cdot \delta + Z_{THtp}(1 - \delta)$$

where $\delta = t_P/T$

Figure 38. Thermal fitting model of a double channel HSD in PowerSSO-12 (b)



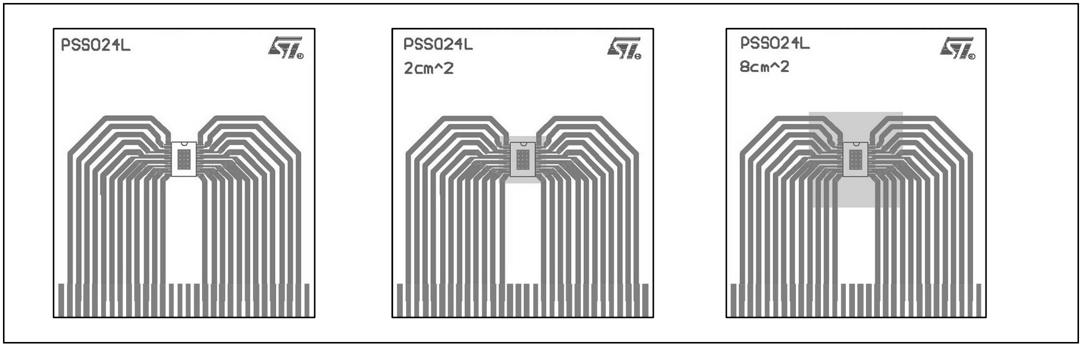
(b) The fitting model is a semplified thermal tool and is valid for transient evolutions where the embedded protections (power limitation or thermal cycling during thermal shutdown) are not triggered.

Table 13. PowerSSO-12 thermal parameters

Area/island (cm^2)	Footprint	2	8
R1= R7 (°C/W)	0.7		
R2= R8 (°C/W)	2.8		
R3 (°C/W)	4		
R4 (°C/W)	8	8	7
R5 (°C/W)	22	15	10
R6 (°C/W)	26	20	15
C1= C7 (W.s/°C)	0.001		
C2= C8 (W.s/°C)	0.0025		
C3 (W.s/°C)	0.05		
C4 (W.s/°C)	0.2	0.1	0.1
C5 (W.s/°C)	0.27	0.8	1
C6 (W.s/°C)	3	6	9

4.2 PowerSSO-24 thermal data

Figure 39. PowerSSO-24 PC board



Note: *Layout condition of R_{th} and Z_{th} measurements (PCB: Double layer, Thermal Vias, FR4 area= 77mm x 86mm, PCB thickness=1.6mm, Cu thickness=70µm (front and back side), Copper areas: from minimum pad lay-out to 8cm^2).*

Figure 40. $R_{thj-amb}$ Vs. PCB copper area in open box free air condition (one channel ON)

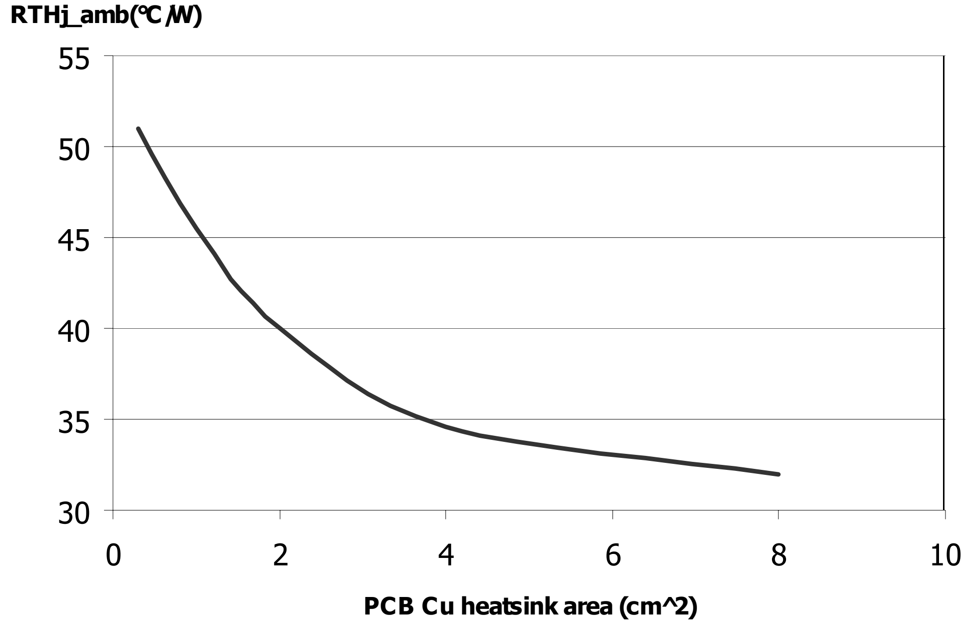
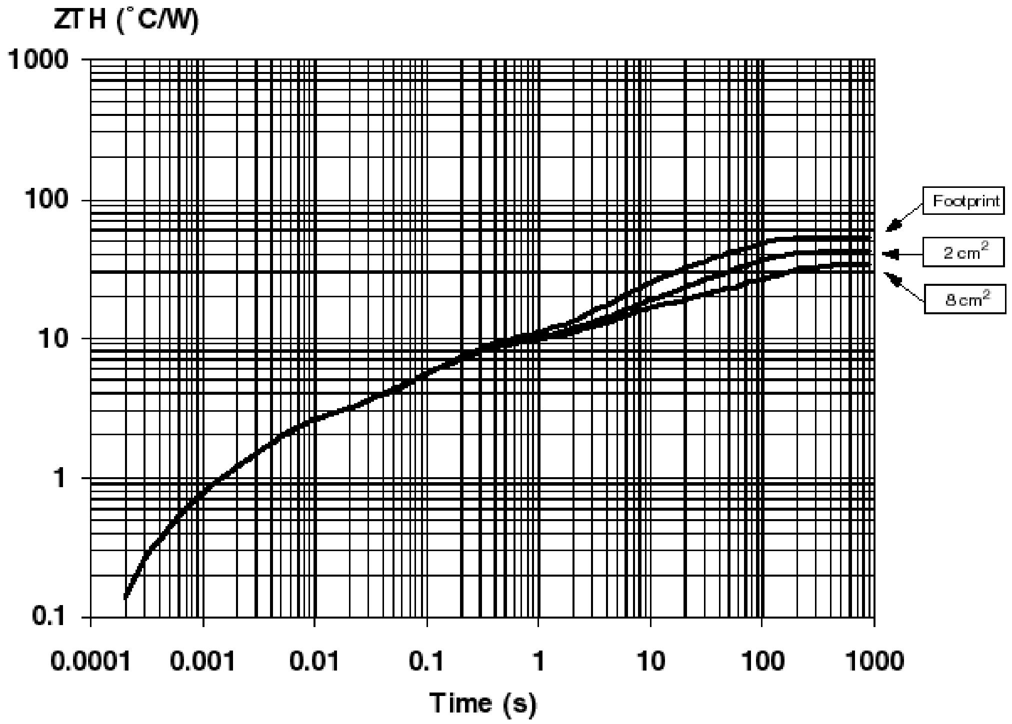


Figure 41. PowerSSO-24 thermal impedance junction ambient single pulse (one channel ON)

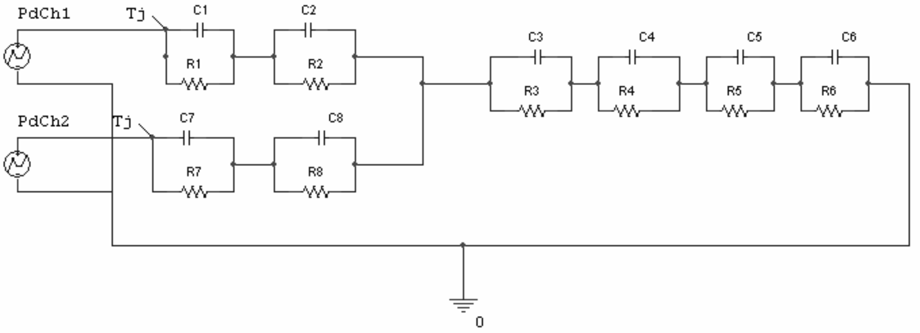


Equation 2: pulse calculation formula

$$Z_{TH\delta} = R_{TH} \cdot \delta + Z_{THtp}(1 - \delta)$$

where $\delta = t_P/T$

Figure 42. Thermal fitting model of a double channel HSD in PowerSSO-24 (c)



(c)The fitting model is a semplified thermal tool and is valid for transient evolutions where the embedded protections (power limitation or thermal cycling during thermal shutdown) are not triggered.

Table 14. PowerSSO-24 thermal parameters

Area/island (cm^2)	Footprint	2	8
R1=R7 (°C/W)	0.4		
R2=R8 (°C/W)	2		
R3 (°C/W)	6		
R4 (°C/W)	7.7		
R5 (°C/W)	9	9	8
R6 (°C/W)	28	17	10
C1=C7 (W.s/°C)	0.001		
C2=C8 (W.s/°C)	0.0022		
C3 (W.s/°C)	0.025		
C4 (W.s/°C)	0.75		
C5 (W.s/°C)	1	4	9
C6 (W.s/°C)	2.2	5	17

5 Package and packing information

5.1 ECOPACK® packages

In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a Lead-free second-level interconnect. The category of Second-Level Interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label.
ECOPACK is an ST trademark. ECOPACK specifications are available at: www.st.com.

5.2 PowerSSO-12 package information

Figure 43. PowerSSO-12 package dimensions

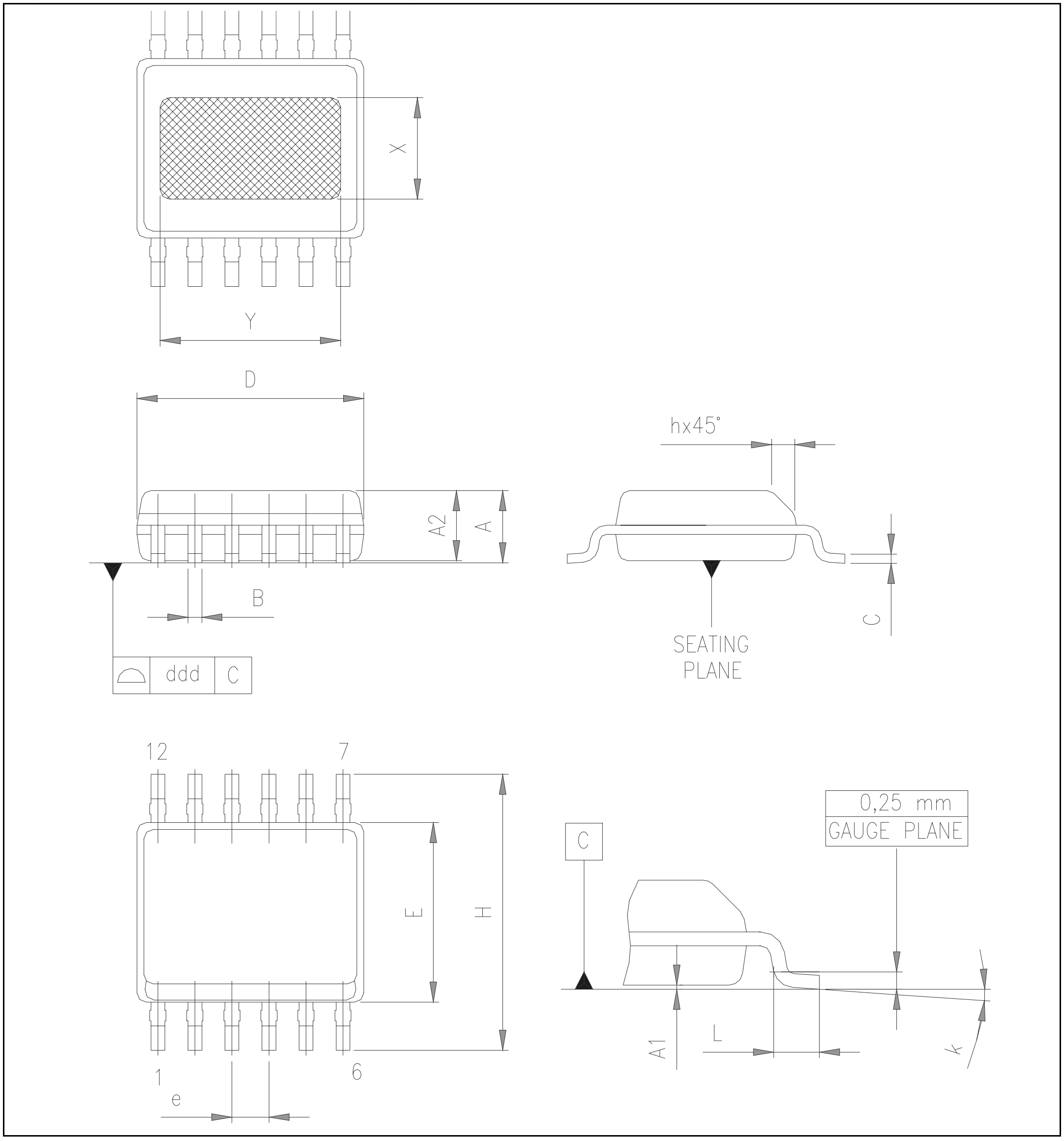


Table 15. PowerSSO-12 mechanical data

Symbol	Millimeters		
	Min.	Typ.	Max.
A	1.25		1.62
A1	0		0.1
A2	1.10		1.65
B	0.23		0.41
C	0.19		0.25
D	4.8		5.0
E	3.8		4.0
e		0.8	
H	5.8		6.2
h	0.25		0.5
L	0.4		1.27
k	0°		8°
X	1.9		2.5
Y	3.6		4.2
ddd			0.1

5.3 PowerSSO-24 package information

Figure 44. PowerSSO-24 package dimensions

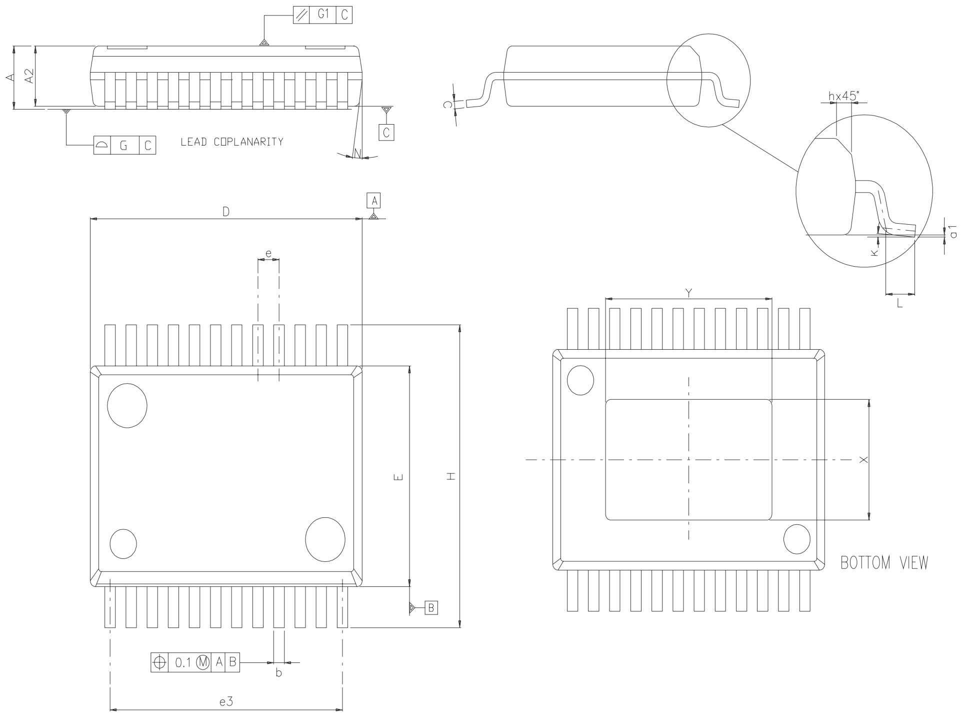


Table 16. PowerSSO-24 mechanical data

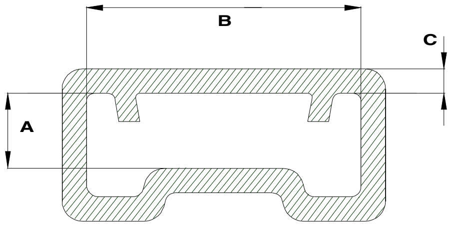
Symbol	Millimeters		
	Min.	Typ.	Max.
A	2.15		2.47
A2	2.15		2.40
a1	0		0.075
b	0.33		0.51
c	0.23		0.32
D	10.10		10.50
E	7.4		7.6
e		0.8	
e3		8.8	
G			0.1
G1			0.06

Table 16. PowerSSO-24 mechanical data (continued)

Symbol	Millimeters		
	Min.	Typ.	Max.
H	10.1		10.5
h			0.4
L	0.55		0.85
N			10deg
X	4.1		4.7
Y	6.5		7.1

5.4 PowerSSO-12 packing information

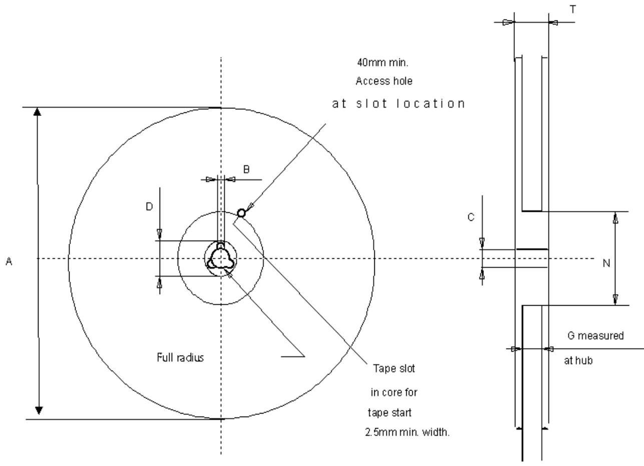
Figure 45. PowerSSO-12 tube shipment (no suffix)



Base Q.ty	100
Bulk Q.ty	2000
Tube length (± 0.5)	532
A	1.85
B	6.75
C (± 0.1)	0.6

All dimensions are in mm.

Figure 46. PowerSSO-12 tape and reel shipment (suffix “TR”)



REEL DIMENSIONS

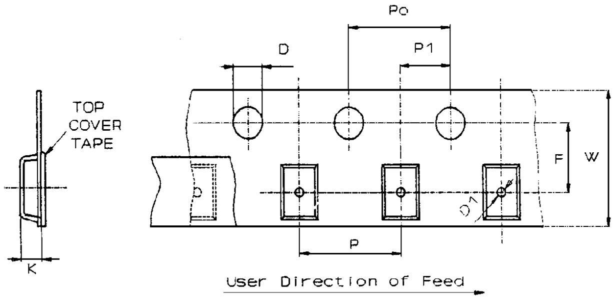
Base Q.ty	2500
Bulk Q.ty	2500
A (max)	330
B (min)	1.5
C (± 0.2)	13
F	20.2
G (+ 2 / -0)	12.4
N (min)	60
T (max)	18.4

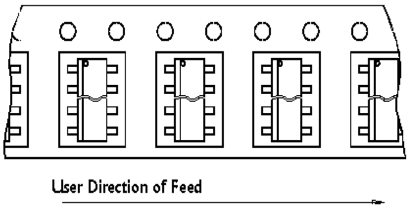
TAPE DIMENSIONS

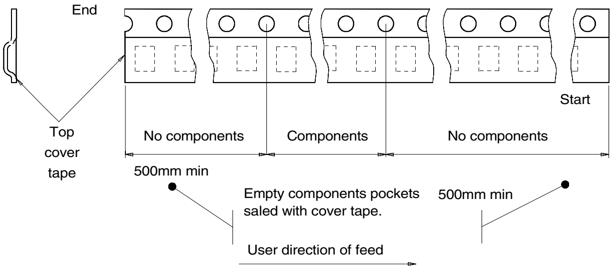
According to Electronic Industries Association (EIA) Standard 481 rev. A, Feb. 1986

Tape width	W	12
Tape Hole Spacing	P0 (± 0.1)	4
Component Spacing	P	8
Hole Diameter	D (± 0.05)	1.5
Hole Diameter	D1 (min)	1.5
Hole Position	F (± 0.1)	5.5
Compartment Depth	K (max)	4.5
Hole Spacing	P1 (± 0.1)	2

All dimensions are in mm.

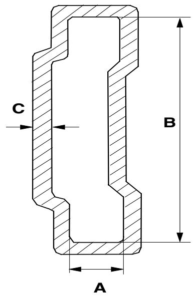






5.5 PowerSSO-24 packing information

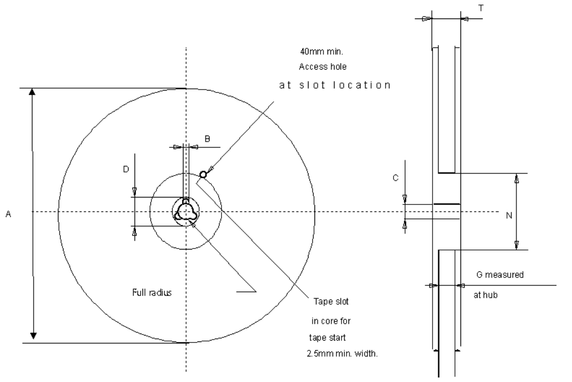
Figure 47. PowerSS0-24 tube shipment (no suffix)



Base Qty	49
Bulk Qty	1225
Tube length (±0.5)	532
A	3.5
B	13.8
C (±0.1)	0.6

All dimensions are in mm.

Figure 48. PowerSSO-24 tape and reel shipment (suffix “TR”)

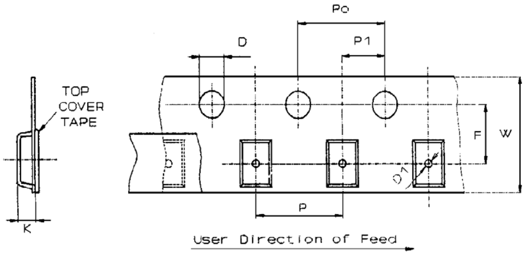


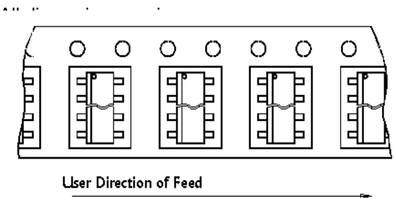
REEL DIMENSIONS

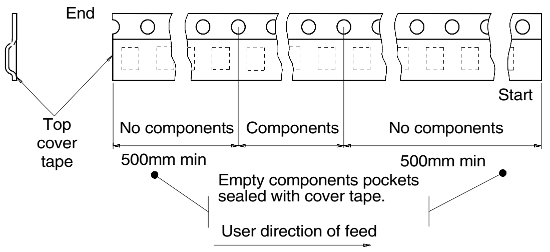
Base Qty	1000
Bulk Qty	1000
A (max)	330
B (min)	1.5
C (± 0.2)	13
F	20.2
G (+2 / -0)	24.4
N (min)	100
T (max)	30.4

TAPE DIMENSIONS
According to Electronic Industries Association (EIA) Standard 481 rev. A, Feb. 1986

Tape width	**W**	24
Tape Hole Spacing	**P0 (± 0.1)**	4
Component Spacing	**P**	12
Hole Diameter	**D (± 0.05)**	1.55
Hole Diameter	**D1 (min)**	1.5
Hole Position	**F (± 0.1)**	11.5
Compartment Depth	**K (max)**	2.85
Hole Spacing	**P1 (± 0.1)**	2







6 Order codes

Table 17. Device summary

Package	Order codes	
	Part number (Tube)	Part number (Tape & reel)
PowerSSO-12	VND5E050J-E	VND5E050JTR-E
PowerSSO-24	VND5E050K-E	VND5E050KTR-E

7 Revision history

Table 18. Document revision history

Date	Revision	Changes
04-Feb-2008	1	Initial release.

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