

SCAS738D-DECEMBER 2003-REVISED JUNE 2008

HEX BUFFER/DRIVER WITH OPEN-DRAIN OUTPUTS

FEATURES

- Operates From 1.65 V to 5 V
- Inputs and Open-Drain Outputs Accept Voltages up to 5.5 V
- Max t_{pd} of 3.6 ns at 5 V
- Latch-Up Performance Exceeds 250 mA Per JESD 17

SUPPORTS DEFENSE, AEROSPACE, AND MEDICAL APPLICATIONS

- Controlled Baseline
- One Assembly/Test Site
- One Fabrication Site
- Available in Military (-55°C/125°C), Industrial (-40°C/85°C) Temperature Ranges⁽¹⁾
- Extended Product Life Cycle
- Extended Product-Change Notification
- Product Traceability
- (1) Custom Temperature Ranges Available

DESCRIPTION/ORDERING INFORMATION

This hex buffer/driver is designed for 1.65-V to 5.5-V V_{CC} operation.

The outputs of the SN74LVC07A device are open drain and can be connected to other open-drain outputs to implement active-low wired-OR or active-high wired-AND functions. The maximum sink current is 24 mA.

Inputs can be driven from 1.8-V, 2.5-V, 3.3-V (LVTTL), or 5-V (CMOS) devices. This feature allows the use of this device as a translator in a mixed-system environment.

ORDERING INFORMATION

T _A	PACKAC	GE ⁽¹⁾	ORDERABLE PART NUMBER	TOP-SIDE MARKING		
-40°C to 85°C	TSSOP - PW	Reel of 2000	SN74LVC07AIPWREP	C07AEP		
–55°C to 125°C	TSSOP - PW	Reel of 2000	SN74LVC07AMPWREP	C07AMEP		

(1) Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

FUNCTION TABLE (each buffer/driver)

INPUT A	OUTPUT Y
Н	Н
L	L

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.



LOGIC DIAGRAM, EACH BUFFER/DRIVER (POSITIVE LOGIC)



Absolute Maximum Ratings(1)

over operating free-air temperature range (unless otherwise noted)

					MIN	MAX	UNIT
V_{CC}	Supply voltage range				-0.5	6.5	V
V_{I}	Input voltage range (2)				-0.5	6.5	V
Vo	Output voltage range				-0.5	6.5	V
I _{IK}	Input clamp current	V _I <)			-50	mA
I _{OK}	Output clamp current	V _O <	0			-50	mA
Io	Continuous output current					±50	mA
	Continuous current through each V _{CC} or	GND				±100	mA
θ_{JA}	Package thermal impedance (3)					113	°C/W
T _{stg}	Storage temperature range				-65	150	°C

⁽¹⁾ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

Recommended Operating Conditions⁽¹⁾

			MIN	MAX	UNIT	
V_{CC}	Supply voltage	1.65	5.5	٧		
		V _{CC} = 1.65 V to 1.95 V	0.65 × V _{CC}			
\ /		V _{CC} = 2.3 V to 2.7 V	1.7		V	
V _{IH}	High-level input voltage	V _{CC} =2.7 V to 3.6 V	2		V	
		V _{CC} = 4.5 V to 5.5 V	0.7 × V _{CC}			
		V _{CC} = 1.65 V to 1.95 V		0.35 × V _{CC}		
\/	Low-level input voltage	V _{CC} = 2.3 V to 2.7 V		0.7	V	
V _{IL}	Low-lover input voitage	$V_{CC} = 2.7 \text{ V to } 3.6 \text{ V}$		8.0	V	
		V _{CC} = 4.5 V to 5.5 V		$0.3 \times V_{CC}$		
VI	Input voltage		0	5.5	V	
V_{O}	Output voltage		0	5.5	V	
		V _{CC} = 1.65 V		4		
		$V_{CC} = 2.3 \text{ V}$		12		
I _{OL}	Low-level output current	V _{CC} = 2.7 V		12	mA	
		$V_{CC} = 3 V$		24		
		V _{CC} = 4.5 V		24		
т	Operating free-air temperature	SN74LVC07AIPWREP	-40	85	°C	
T _A	Operating nee-an temperature	SN74LVC07AMPWREP	-55	125	C	

All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, Implications of Slow or Floating CMOS Inputs, literature number SCBA004.

⁽²⁾ The input and output negative-voltage ratings may be exceeded if the input and output current ratings are observed.

⁽³⁾ The package thermal impedance is calculated in accordance with JESD 51-7.

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Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V _{cc}	MIN TYP ⁽¹⁾ MAX	UNIT
	$I_{OL} = 100 \mu A$	1.65 V to 5.5 V	0.2	
	I _{OL} = 4 mA	1.65 V	0.45	V
V_{OL}	1 12 m 1	2.3 V	0.7	
	I _{OL} = 12 mA	2.7 V	0.4	
	I _{OL} = 24 mA	3 V	0.55	
I _I	$V_I = 5.5 \text{ V or GND}$	3.6 V	±5	μΑ
I _{CC}	$V_I = V_{CC}$ or GND, $I_O = 0$	3.6 V	10	μΑ
ΔI_{CC}	One input at V_{CC} – 0.6 V, Other inputs at V_{CC} or GND	2.7 V to 3.6 V	500	μΑ
C _I	$V_I = V_{CC}$ or GND	3.3 V	5	pF

⁽¹⁾ All typical values are at $V_{CC} = 3.3 \text{ V}$, $T_A = 25^{\circ}\text{C}$.

Switching Characteristics

over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1 through 4)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC} = 1.8 V ± 0.15 V		V _{CC} = ± 0.2		V _{CC} = 2.7 V		$V_{CC} = 2.7 \text{ V}$ $V_{CC} = 3.3 \text{ V}$ $\pm 0.3 \text{ V}$		V _{CC} = 5 V ±0.5 V		UNIT
	(INFOT)	(0011-01)	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t _{pd}	Α	Υ	1	6.6	1	4.4		4.3	1	4.6	1	3.6	ns

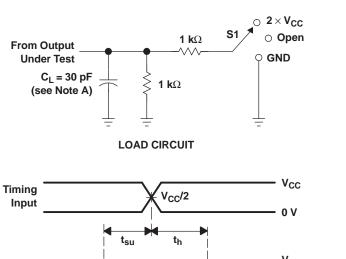
Operating Characteristics

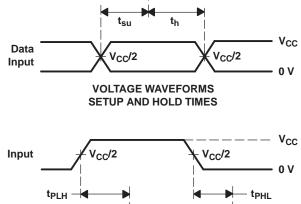
 $T_A = 25^{\circ}C$

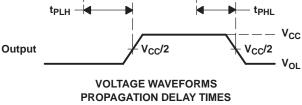
	PARAMETER	TEST CONDITIONS	V _{CC} = 1.8 V TYP	V _{CC} = 2.5 V TYP	V _{CC} = 3.3 V TYP	V _{CC} = 5 V TYP	UNIT
C _{pd}	Power dissipation capacitance	f = 10 MHz	1.8	2	2.5	3.78	pF

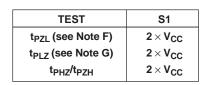


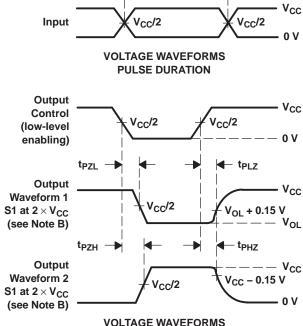
PARAMETER MEASUREMENT INFORMATION $V_{cc} = 1.8 \text{ V} \pm 0.15 \text{ V}$











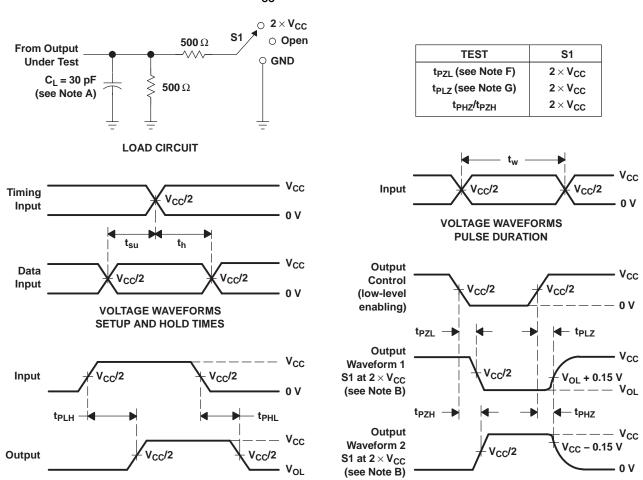
ENABLE AND DISABLE TIMES

NOTES: A. C_L includes probe and jig capacitance.

- B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, $Z_O = 50~\Omega$, $t_f \leq$ 2 ns, $t_f \leq$ 2 ns.
- D. The outputs are measured one at a time, with one transition per measurement.
- E. Since this device has open-drain outputs, t_{PLZ} and t_{PZL} are the same as t_{pd} .
- F. t_{PZL} is measured at $V_{CC}/2$.
- G. t_{PLZ} is measured at V_{OL} + 0.15 V.
- H. All parameters and waveforms are not applicable to all devices.

Figure 1. Load Circuit and Voltage Waveforms

PARAMETER MEASUREMENT INFORMATION $V_{CC} = 2.5 \text{ V} \pm 0.2 \text{ V}$



NOTES: A. C_L includes probe and jig capacitance.

VOLTAGE WAVEFORMS

PROPAGATION DELAY TIMES

- B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, $Z_O = 50~\Omega$, $t_f \leq$ 2 ns, $t_f \leq$ 2 ns.
- D. The outputs are measured one at a time, with one transition per measurement.
- E. Since this device has open-drain outputs, t_{PLZ} and t_{PZL} are the same as t_{pd}.
- F. t_{PZL} is measured at $V_{CC}/2$.
- G. t_{PLZ} is measured at V_{OL} + 0.15 V.
- H. All parameters and waveforms are not applicable to all devices.

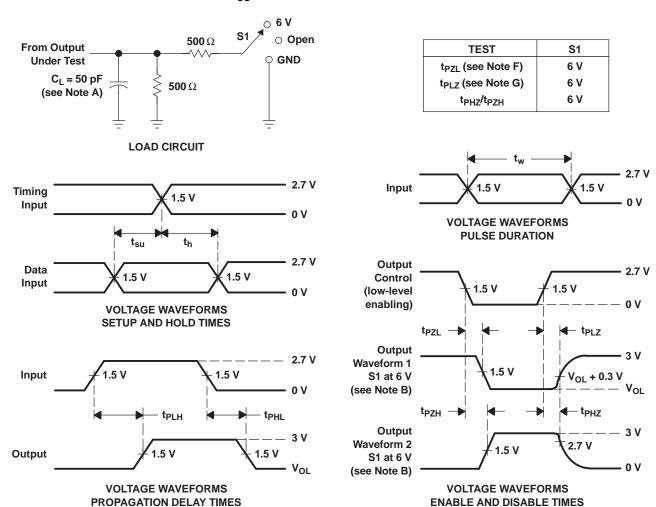
Figure 2. Load Circuit and Voltage Waveforms

VOLTAGE WAVEFORMS

ENABLE AND DISABLE TIMES



PARAMETER MEASUREMENT INFORMATION V_{CC} = 2.7 V AND 3.3 V ± 0.3 V



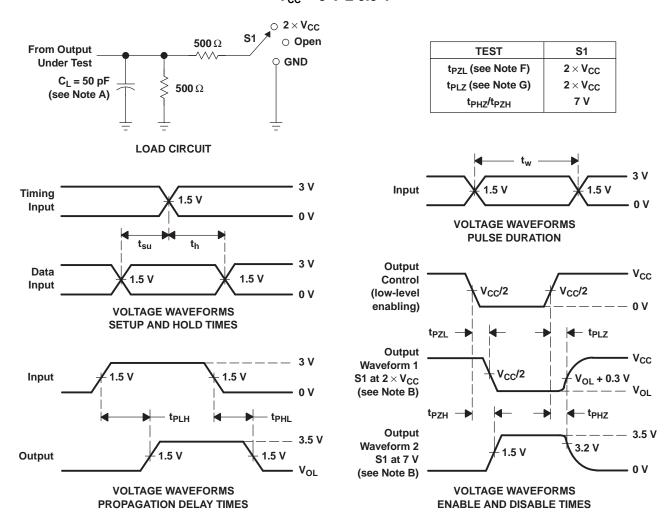
NOTES: A. C_L includes probe and jig capacitance.

- B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, Z_{O} = 50 Ω , $t_{f} \leq$ 2.5 ns. $t_{f} \leq$ 2.5 ns.
- D. The outputs are measured one at a time, with one transition per measurement.
- E. Since this device has open-drain outputs, t_{PLZ} and t_{PZL} are the same as t_{pd} .
- F. t_{PZL} is measured at 1.5 V.
- G. t_{PLZ} is measured at V_{OL} + 0.3 V.
- H. All parameters and waveforms are not applicable to all devices.

Figure 3. Load Circuit and Voltage Waveforms

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PARAMETER MEASUREMENT INFORMATION $V_{cc} = 5 \text{ V} \pm 0.5 \text{ V}$



- NOTES: A. C_L includes probe and jig capacitance.
 - B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
 - C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, Z_{Q} = 50 Ω , $t_{f} \leq$ 2.5 ns, $t_{f} \leq$ 2.5 ns.
 - D. The outputs are measured one at a time, with one transition per measurement.
 - E. Since this device has open-drain outputs, t_{PLZ} and t_{PZL} are the same as t_{pd}.
 - F. t_{PZL} is measured at $V_{CC}/2$.
 - G. t_{PLZ} is measured at $V_{OL} + 0.3 \text{ V}$.
 - H. All parameters and waveforms are not applicable to all devices.

Figure 4. Load Circuit and Voltage Waveforms



PACKAGE OPTION ADDENDUM

21-Jul-2008

PACKAGING INFORMATION

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	e Eco Plan ⁽²⁾	Lead/Ball Finish	MSL Peak Temp ⁽³⁾
SN74LVC07AIPWREP	ACTIVE	TSSOP	PW	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LVC07AMPWREP	ACTIVE	TSSOP	PW	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
V62/04654-01XE	ACTIVE	TSSOP	PW	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
V62/04654-02XE	ACTIVE	TSSOP	PW	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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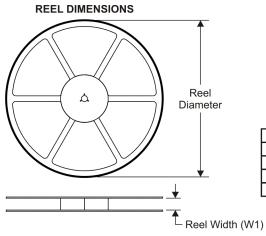
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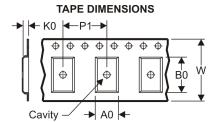


PACKAGE MATERIALS INFORMATION

5-Aug-2008

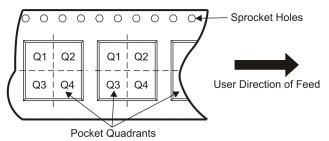
TAPE AND REEL INFORMATION





A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



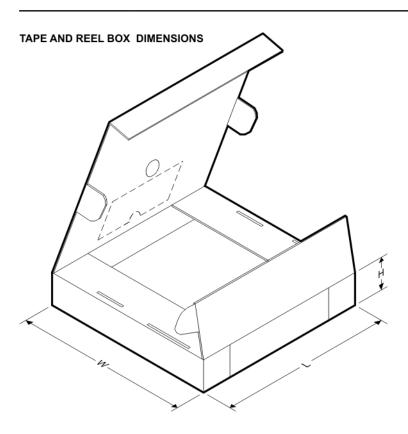
*All dimensions are nominal

Device	_	Package Drawing		SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74LVC07AIPWREP	TSSOP	PW	14	2000	330.0	12.4	7.0	5.6	1.6	8.0	12.0	Q1





5-Aug-2008



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)	
SN74LVC07AIPWREP	TSSOP	PW	14	2000	346.0	346.0	29.0	

PW (R-PDSO-G**)

14 PINS SHOWN

PLASTIC SMALL-OUTLINE PACKAGE



NOTES: A. All linear dimensions are in millimeters.

B. This drawing is subject to change without notice.

C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.

D. Falls within JEDEC MO-153

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