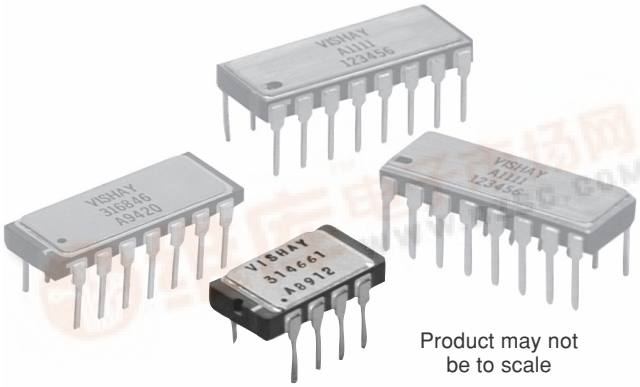
# Bulk Metal® Foil Technology
# Dual-In-Line Hermetic Resistor Networks





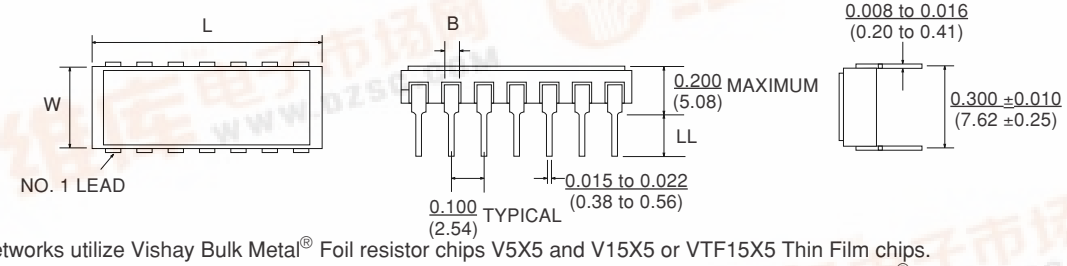
Product may not be to scale

Vishay Model 1442, 1445 and 1446 networks incorporate all the performance features of Vishay Bulk Metal® Foil technology. The 8, 14 and 16 pin side brazed DIPs are a ceramic package. Ceramic has the advantage of electrical isolation on the underside, and, in DIP form, a favorable pin arrangement when two networks are to be placed side by side and connected together.

Review data sheet "7 Technical Reasons to Specify Bulk Metal® Foil Resistor Networks."

Networks are built to your requirements. Send your schematic and electrical requirements to the Applications Engineering Department. (See data sheet "Network Worksheet.") A unique part number will be assigned which defines all aspects of your network.

## FIGURE 1 - PACKAGE SIZES AND CHARACTERISTICS



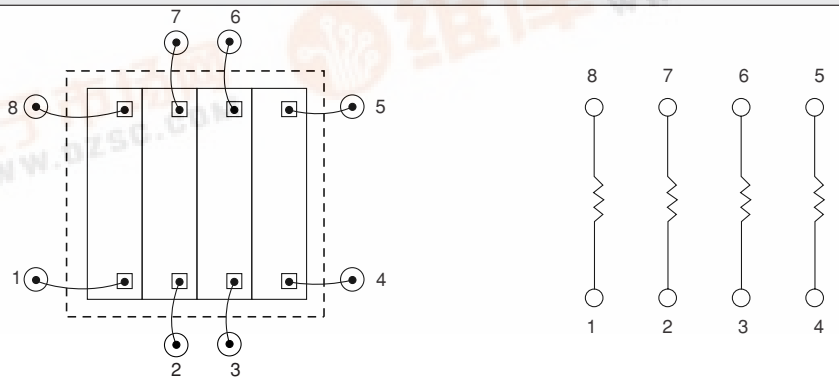

**NOTE:**

1. These networks utilize Vishay Bulk Metal® Foil resistor chips V5X5 and V15X5 or VTF15X5 Thin Film chips.
2. The V5X5 and V15X5 chips have maximum resistance values of 10K and 33K respectively in Bulk Metal® Foil and 500K in VTF15X5 Thin Film chips.
3. The V5X5 and V15X5 chip(s) can be intermixed in a package.

| VISHAY MODEL | NO. OF PINS | MAXIMUM DIMENSIONS in Inches (mm) | | | | CHIP CAPACITY | | MAXIMUM POWER RATING (WATTS) @ +70°C |
|---|---|---|---|---|---|---|---|---|
| | | L | W | B | LL | V5X5 | V15X5 | |
| 1442 | 8 | 0.520 ±0.020 (13.21 ±0.51) | 0.295 ±0.010 (7.49 ±0.025) | 0.054 (1.37) | 0.125 minimum (3.18) | 12 | 4 | 0.4 |
| 1445 | 14 | 0.740 ±0.045 (18.80 ±1.14) | 0.270 +0.035/–0.030 (6.86 +0.89/–0.76) | 0.046 (1.17) | 0.135 +0.015/–0.010 (3.43 +0.38/–0.25) | 30 | 10 | 1.2 |
| 1446 | 16 | 0.780 ±0.030 (19.81 ±0.76) | 0.290 ±0.008 (7.37 ±0.20) | 0.040 to 0.070 (1.01 to 1.78) | 0.135 +0.015/–0.010 (3.43 +0.38/–0.25) | 36 | 12 | 1.4 |

## FIGURE 2 - SAMPLE CIRCUIT DESIGN AND CHIP LAYOUT

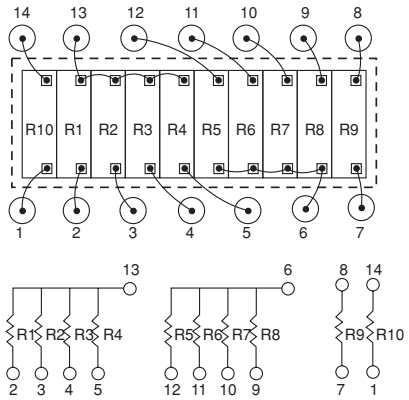
**NOTE:**
Usable area is represented by the dotted lines— a rectangle 0.150 Inches x 0.200 Inches. Illustrations not to scale. Chips shown undersize for clarity. Drawing view is from the top looking down into the package.



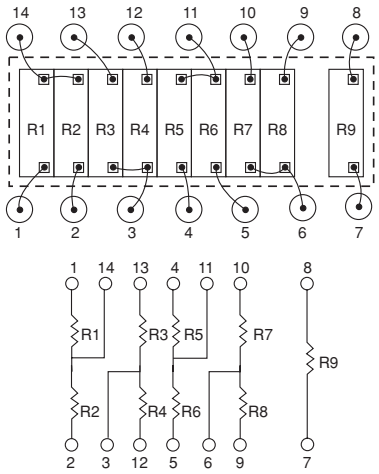
## FIGURE 3 - SAMPLE CIRCUIT DESIGNS AND CHIP LAYOUTS

**NOTE:**
Usable area is represented by the dotted lines— a rectangle 0.150 Inches x 0.500 Inches. Illustrations not to scale.
Chips shown undersize for clarity. Drawing view is from the top looking down into the package.

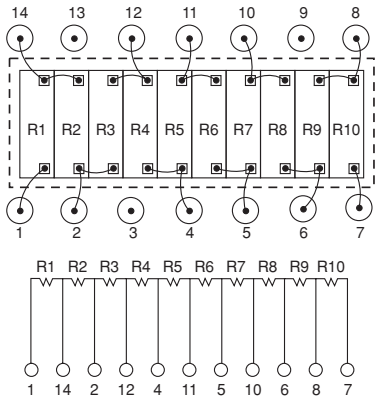
**TWO DECADES OF BCD LADDER PLUS TWO SCALING RESISTORS**




**FOUR DIVIDERS PLUS APPLICATION RESISTOR**




**TEN RESISTOR DIVIDER**

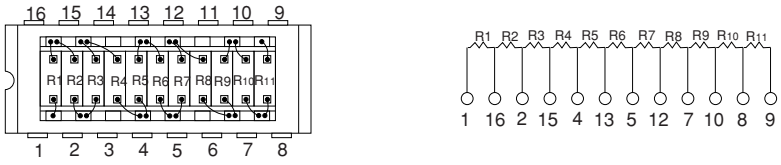



THROUGH HOLE

## FIGURE 4 - SAMPLE CIRCUIT DESIGNS AND CHIP LAYOUTS

**NOTE:** Usable area is represented by the dotted lines— a rectangle 0.150 Inches x 0.600 Inches. Illustrations not to scale. Chips shown undersize for clarity. Drawing view is from the top looking down into the package.

**ELEVEN RESISTOR DIVIDER**




**EIGHT RESISTOR PACKAGE**

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