



Model 335

DIFFERENTIAL LVPECL AND LVDS VCXO

FEATURES

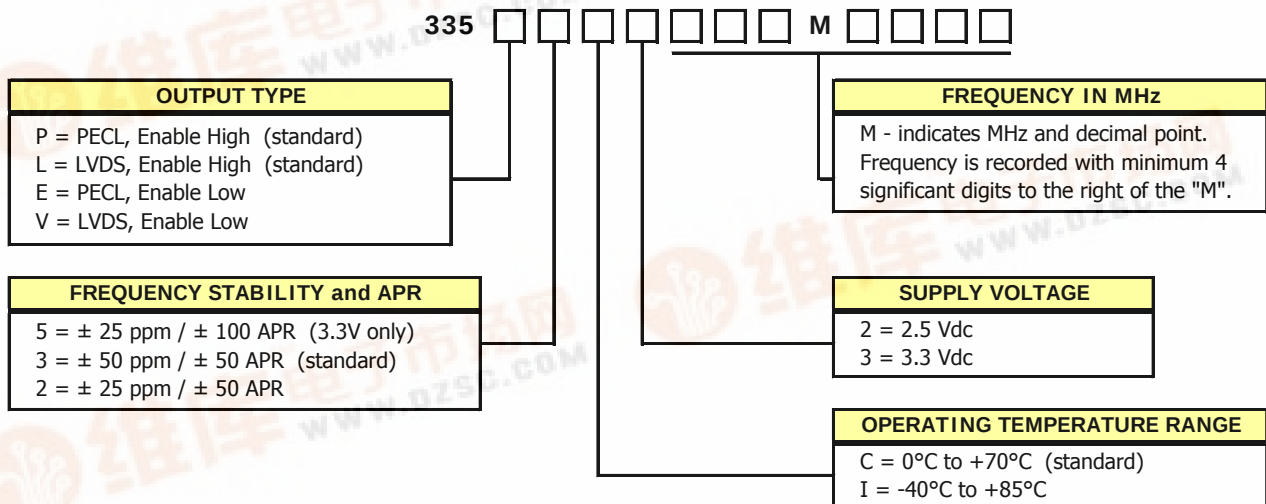
- Standard 7x5mm Surface Mount Footprint
- Differential LVPECL or LVDS Outputs
- Frequency Range 19.44 – 212.50 MHz
- Frequency Stability, ± 50 ppm Standard (± 25 ppm available)
- +2.5Vdc or +3.3Vdc Operation
- Operating Temperature to -40°C to $+85^{\circ}\text{C}$
- Output Enable Standard
- Low Phase Jitter, **NON-Multiplied**
- Tape & Reel Packaging
- **RoHS/Green Compliant**

DESCRIPTION

The Model 335 is a ceramic packaged Voltage Controlled oscillator offering reduced size and enhanced stability. The small size means it is perfect for any application. The enhanced stability means it is the perfect choice for today's communications applications that require tight frequency control.



ORDERING INFORMATION



Example Part Number: 335P3C3155M5200





Model 335
Differential LVPECL or LVDS
7x5mm VCXO

ELECTRICAL CHARACTERISTICS

	PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
Absolute Maximums	Maximum Supply Voltage	V_{CC}	-	-0.5	-	5.0	V
	Storage Temperature	T_{STG}	-	-55	-	125	°C
	Frequency Range LVPECL and LVDS	f_0	-	19.44	-	212.50	MHz
	Frequency Stability (See Note 1 and Ordering Information)	$\Delta f/f_0$	-	-	-	25, 50	± ppm
	Absolute Pull Range (See Note 2 and Ordering Information)	APR	-	50, 100	-	-	± ppm
	Operating Temperature Commercial	T_A	-	-20	25	70	°C
	Industrial			-40		85	
Electrical and Waveform Parameters	Supply Voltage	V_{CC}	± 5 %	2.38 3.14	2.5 3.3	2.63 3.47	V
	Supply Current LVPECL	I_{CC}	Maximum Load	-	50	75	mA
	LVDS			-	25	40	
	Control Voltage	V_C	$V_{CC} = 3.3V$	0.0	1.65	3.3	V
	Frequency Deviation	Δf	25°C at Time of Shipment	-	130	-	± ppm
	Linearity	L	Best Straight Line Fit	-15	10	15	%
	Input Impedance	Z_C	-	50	-	-	kOhms
	Transfer Function	-	-	-	Positive	-	-
	Start Up Time	T_S	Application of V_{CC}	-	5	10	ms
	Modulation Roll-off	-	@ -3dB	25	-	-	kHz
	Phase Jitter	t_{jms}	Bandwidth 12 kHz - 20 MHz	-	-	1	ps RMS
	Enable Function High						
	Enable Input Voltage	V_{IH}	Pin 2 Logic '1', Output Enabled	0.7* V_{CC}	-	-	V
	Disable Input Voltage	V_{IL}	Pin 2 Logic '0', Output Disabled	-	-	0.3* V_{CC}	
	Enable Function Low						
	Enable Input Voltage	V_{IH}	Pin 2 Logic '0', Output Enabled	0.3* V_{CC}			V
	Disable Input Voltage	V_{IL}	Pin 2 Logic '1', Output Disabled			0.7* V_{CC}	
	Disable Current	I_{IL}	Pin 1 or Pin 2 Logic '1', Output Disabled	-	-	20	µA
	Enable Time	T_{PLZ}	Pin 2 Logic '1' or Logic '0'	-	-	10	ms
	LVPECL WAVEFORM						
	Output Load	R_L	-	-	50	-	Ohms
	Output Duty Cycle	SYM	@ $V_{CC} - 1.3V$	45	-	55	%
	Output Voltage Levels						
	Logic '1' Level	V_{OH}	PECL Load	$V_{CC} - 1.025V$	-	-	V
	Logic '0' Level	V_{OL}	PECL Load	-	-	$V_{CC} - 1.62V$	
	Rise and Fall Time	T_R, T_F	@ 20% - 80% Levels		0.4	1.0	ns
	LVDS WAVEFORM						
	Output Load	R_L	-	-	100	-	Ohms
	Output Duty Cycle	SYM	@ 1.25V	45	-	55	%
	Differential Voltage	V_{OD}	$R_L = 100$ Ohms	250	350	450	mV
	Output Voltage Levels						
	Logic '1' Level	V_{OH}	LVDS Load	-	-	1.6	V
	Logic '0' Level	V_{OL}	LVDS Load	0.9	-	-	
	Rise and Fall Time	T_R, T_F	@ 20% - 80% Levels	-	0.4	1.0	ns

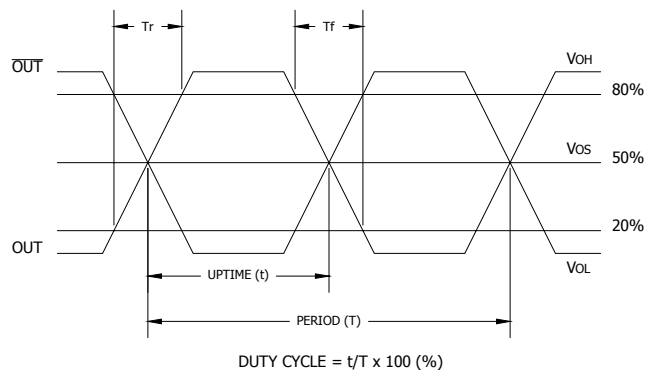
Notes:

1. Inclusive of initial tolerance at time of shipment, changes in supply voltage, load, temperature and 10 year aging at an average operating temperature of +40 °C.
2. Minimum guaranteed frequency shift from f_0 over variations in temperature, aging, power supply and load at an average operating temperature of +40°C for 10 years.

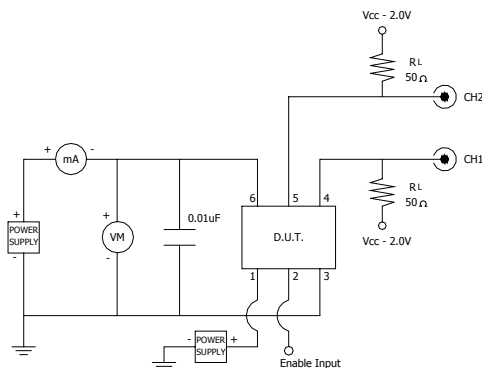


Model 335 **Differential LVPECL or LVDS** **7x5mm VCXO**

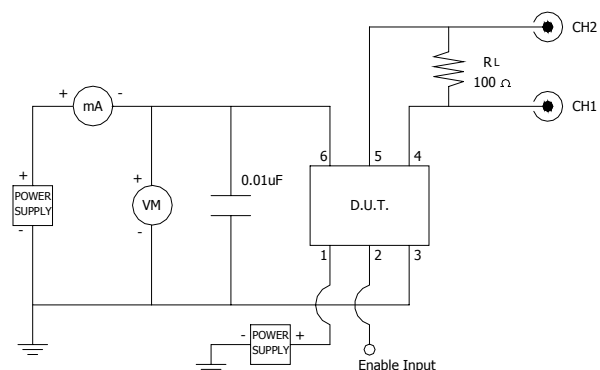
PECL/LVDS OUTPUT WAVEFORM



TEST CIRCUIT, PECL LOAD



TEST CIRCUIT, LVDS LOAD



D.U.T. PIN ASSIGNMENTS

PIN	SYMBOL	DESCRIPTION
1	V_C	Control Voltage
2	EOH	Enable
3	GND	Circuit & Package Ground
4	Output	RF Output
5	Output	Complimentary RF Output
6	V_{CC}	Supply Voltage

ENABLE HIGH **TRUTH TABLE**

PIN 2	PIN 4 / PIN 5
Logic '1'	Output
Open	Output
Logic '0'	High Imp.

ENABLE LOW **TRUTH TABLE**

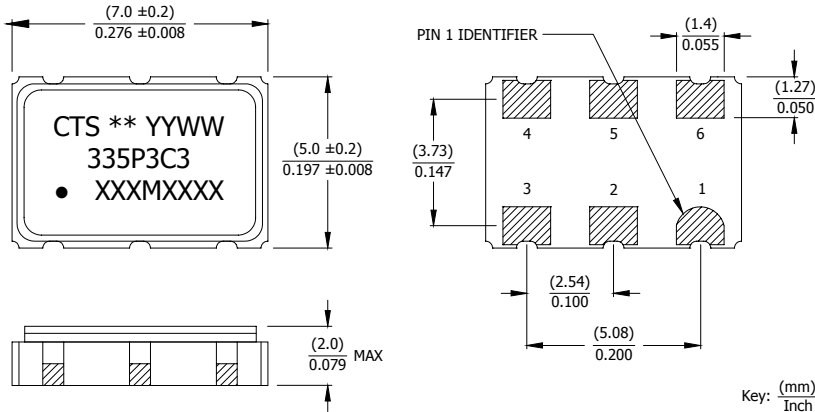
PIN 2	PIN 4 / PIN 5
Logic '1'	High Imp.
Open	Output
Logic '0'	Output



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MECHANICAL SPECIFICATIONS

PACKAGE DRAWING



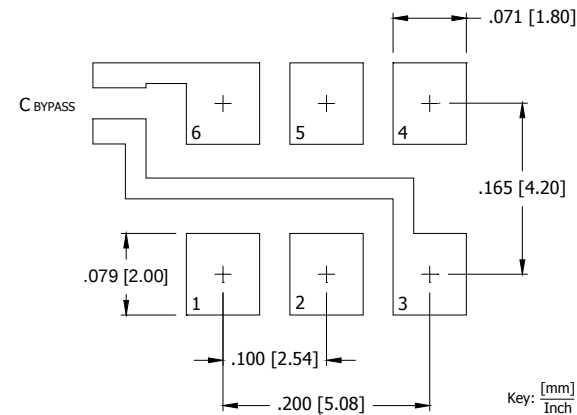
MARKING INFORMATION

1. ** - Manufacturing Site Code.
2. YYWW – Date code, YY – year, WW – week.
3. Truncated CTS part number.
4. XXXMXXXX - Frequency marked with 4 significant digits after the 'M'.

Notes

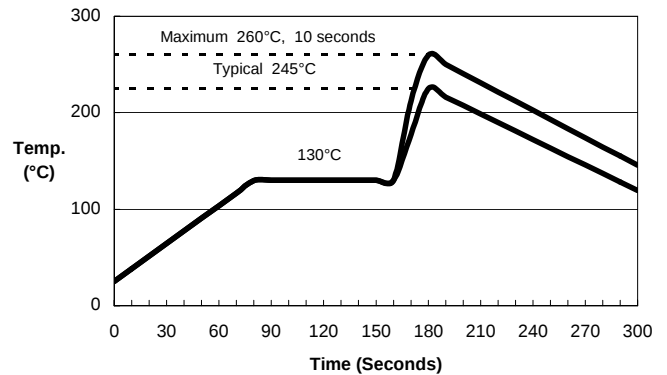
1. Termination pads (e4), barrier-plating is nickel (Ni) with gold (Au) flash plate.
2. Reflow conditions per JEDEC J-STD-020.

SUGGESTED SOLDER PAD GEOMETRY



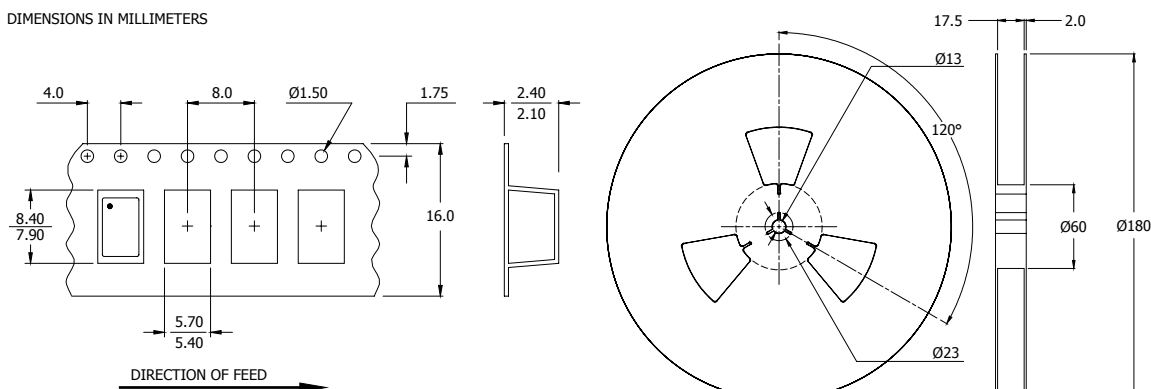
C_{BYPASS} should be ≥ 0.01 uF.

SUGGESTED REFLOW PROFILE



TAPE AND REEL INFORMATION

DIMENSIONS IN MILLIMETERS



Device quantity is 1,000 pieces per 180mm reel.

ENVIRONMENTAL SPECIFICATIONS

Temperature Cycle:	400 cycles from -55°C to +125°C, 10 minute dwell at each temperature, 1 minute transfer time between temperatures.
Mechanical Shock:	1,500g's, 0.5mS duration, ½ sinewave, 3 shocks each direction along 3 mutually perpendicular planes (18 total shocks).
Sinusoidal Vibration:	0.06 inches double amplitude, 10 to 55 Hz and 20g's, 55 to 2,000 Hz, 3 cycles each in 3 mutually perpendicular planes (9 times total).
Gross Leak:	No leak shall appear while immersed in an FC40 or equivalent liquid at +125°C for 20 seconds.
Fine Leak:	Mass spectrometer leak rates less than 2×10^{-8} ATM cc/sec air equivalent.
Resistance to Solder Heat:	Product must survive 3 reflows of +260°C peak, 10 seconds maximum.
High Temperature Operating Bias:	2,000 hours at +125°C, maximum bias, disregarding frequency shift.
Frequency Aging:	1,000 hours at +85°C, full bias, less than ± 5 ppm shift.
Moisture Sensitivity Level:	Level 1 per JEDEC J-STD-020.

QUALITY AND RELIABILITY

Quality systems meet or exceed the requirements of ISO 9000:2000 standards.