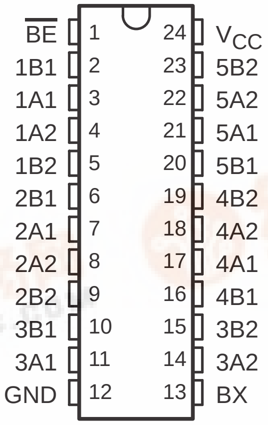
SN74CB3T3383
10-BIT FET BUS-EXCHANGE SWITCH
2.5-V/3.3-V LOW-VOLTAGE BUS SWITCH WITH 5-V-TOLERANT LEVEL SHIFTER

SCDS158A − OCTOBER 2003 − REVISED DECEMBER 2004

- **Output Voltage Translation Tracks V_{CC}**
- **Supports Mixed-Mode Signal Operation On All Data I/O Ports**
  - **5-V Input Down To 3.3-V Output Level Shift With 3.3-V V_{CC}**
  - **5-V/3.3-V Input Down To 2.5-V Output Level Shift With 2.5-V V_{CC}**
- **5-Tolerant I/Os With Device Powered Up or Powered Down**
- **Bidirectional Data Flow, With Near-Zero Propagation Delay**
- **Low ON-State Resistance (r_{on}) Characteristics (r_{on} = 5 Ω Typical)**
- **Low Input/Output Capacitance Minimizes Loading ($C_{io(OFF)}$ = 8 pF Typical)**
- **Data and Control Inputs Provide Undershoot Clamp Diodes**
- **Low Power Consumption (I_{CC} = 20 µA Max)**
- **V_{CC} Operating Range From 2.3 V to 3.6 V**
- **Data I/Os Support 0- to 5-V Signaling Levels (0.8 V, 1.2 V, 1.5 V, 1.8 V, 2.5 V, 3.3 V, 5 V)**
- **Control Inputs Can Be Driven by TTL or 5-V/3.3-V CMOS Outputs**
- **I_{off} Supports Partial-Power-Down Mode Operation**
- **Latch-Up Performance Exceeds 250 mA Per JESD 17**
- **ESD Performance Tested Per JESD 22**
  - **2000-V Human-Body Model (A114-B, Class II)**
  - **1000-V Charged-Device Model (C101)**
- **Supports Digital Applications: Level Translation, Memory Interleaving, Bus Isolation**
- **Ideal for Low-Power Portable Equipment**

DBQ, DGV, DW, OR PW PACKAGE
(TOP VIEW)



description/ordering information

ORDERING INFORMATION

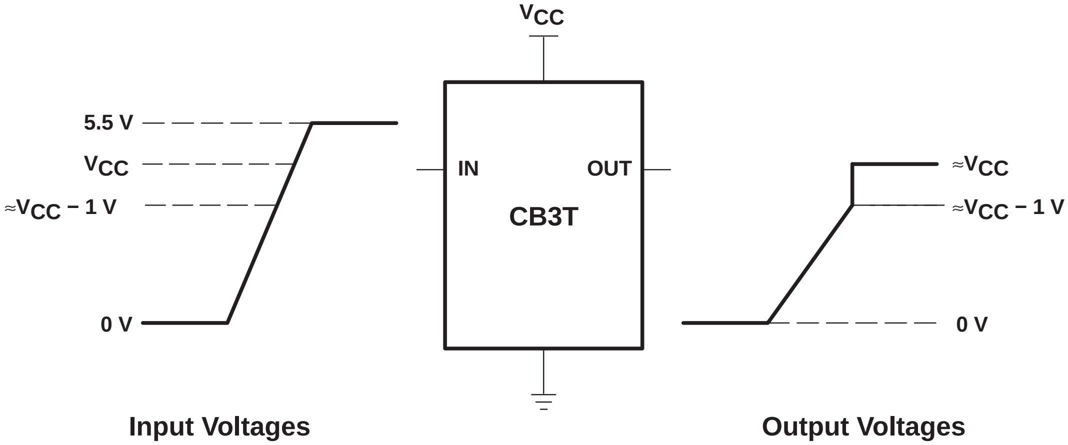
T_A	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
−40°C to 85°C	SOIC − DW	Tube	SN74CB3T3383DW	CB3T3383
		Tape and reel	SN74CB3T3383DWR	
	SSOP (QSOP) − DBQ	Tape and reel	SN74CB3T3383DBQR	CB3T3383
	TSSOP − PW	Tube	SN74CB3T3383PW	KS383
		Tape and reel	SN74CB3T3383PWR	
	TVSOP − DGV	Tape and reel	SN74CB3T3383DGVR	KS383

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

description/ordering information (continued)

The SN74CB3T3383 is a high-speed TTL-compatible FET bus-exchange switch with low ON-state resistance (r_{on}), allowing for minimal propagation delay. The device fully supports mixed-mode signal operation on all data I/O ports by providing voltage translation that tracks V_{CC}. The SN74CB3T3383 supports systems using 5-V TTL, 3.3-V LVTTL, and 2.5-V CMOS switching standards, as well as user-defined switching levels (see Figure 1).



NOTE A: If the input high voltage (V_{IH}) level is greater than or equal to V_{CC} − 1 V, and less than or equal to 5.5 V, then the output high voltage (V_{OH}) level will be equal to approximately the V_{CC} voltage level.

Figure 1. Typical DC Voltage Translation Characteristics

The SN74CB3T3383 is organized as a 10-bit bus switch or as a 5-bit bus-exchange with enable ($\overline{BE}$) input. When used as a 5-bit bus-exchange, the device provides data exchanging between four signal ports. When $\overline{BE}$ is low, the bus-exchange switch is ON, and the select input (BX) controls the data path. When $\overline{BE}$ is high, the bus-exchange switch is OFF, and a high-impedance state exists between the A and B ports.

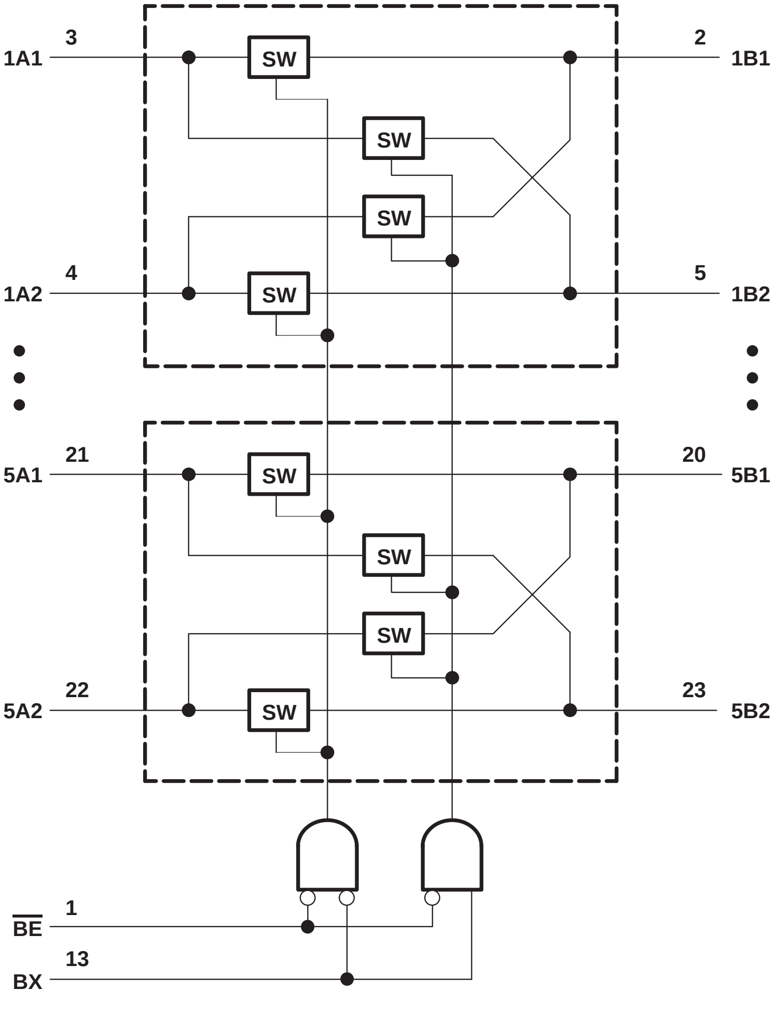
This device is fully specified for partial-power-down applications using I_{off}. The I_{off} feature ensures that damaging current will not backflow through the device when it is powered down. The device has isolation during power off.

To ensure the high-impedance state during power up or power down, $\overline{BE}$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

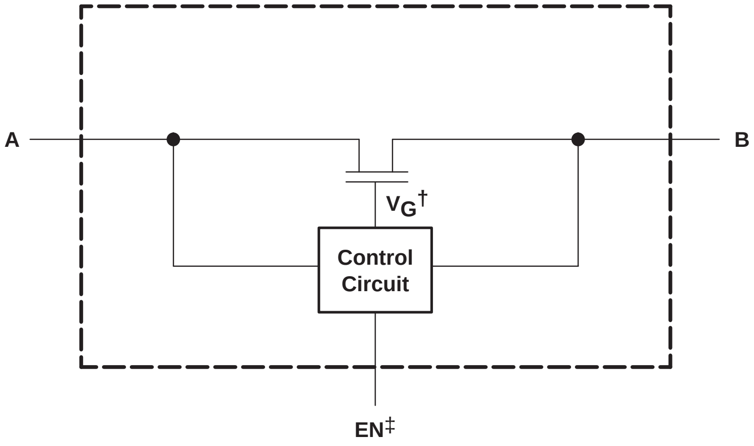
**FUNCTION TABLE
(each 5-bit switch)**

INPUTS		INPUTS/OUTPUTS		FUNCTION
$\overline{BE}$	BX	A1	A2	
L	L	B1	B2	A1 port = B1 port A2 port = B2 port
L	H	B2	B1	A1 port = B2 port A2 port = B1 port
H	X	Z	Z	Disconnect

logic diagram (positive logic)



simplified schematic, each FET switch (SW)



† Gate Voltage (V_G) is approximately equal to $V_{CC} + V_T$ when the switch is ON and $V_I > V_{CC} + V_T$.
‡ EN is the internal enable signal applied to the switch.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)§

Supply voltage range, V_{CC} (see Note 1)		−0.5 V to 7 V
Control input voltage range, V_{IN} (see Notes 1 and 2)		−0.5 V to 7 V
Switch I/O voltage range, $V_{I/O}$ (see Notes 1, 2, and 3)		−0.5 V to 7 V
Control input clamp current, I_{IK} ($V_{IN} < 0$)		−50 mA
I/O port clamp current, $I_{I/OK}$ ($V_{I/O} < 0$)		−50 mA
ON-state switch current, $I_{I/O}$ (see Note 4)		±128 mA
Continuous current through V_{CC} or GND terminals		±100 mA
Package thermal impedance, θ_{JA} (see Note 5):	DBQ package	61°C/W
	DGV package	86°C/W
	DW package	46°C/W
	PW package	88°C/W
Storage temperature range, T_{stg}		−65°C to 150°C

§ Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES:
1. All voltages are with respect to ground unless otherwise specified.
2. The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
3. V_I and V_O are used to denote specific conditions for $V_{I/O}$.
4. I_I and I_O are used to denote specific conditions for $I_{I/O}$.
5. The package thermal impedance is calculated in accordance with JESD 51-7.

recommended operating conditions (see Note 6)

			MIN	MAX	UNIT
V_{CC}	Supply voltage		2.3	3.6	V
V_{IH}	High-level control input voltage	V_{CC} = 2.3 V to 2.7 V	1.7	5.5	V
		V_{CC} = 2.7 V to 3.6 V	2	5.5	
V_{IL}	Low-level control input voltage	V_{CC} = 2.3 V to 2.7 V	0	0.7	V
		V_{CC} = 2.7 V to 3.6 V	0	0.8	
$V_{I/O}$	Data input/output voltage		0	5.5	V
T_A	Operating free-air temperature		−40	85	°C

NOTE 6: All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP[†]	MAX	UNIT
V_{IK}		V_{CC} = 3 V, I_I = −18 mA				−1.2	V
V_{OH}		See Figures 3 and 4					
I_{IN}[‡]	Control inputs	V_{CC} = 3.6 V, V_{IN}[‡] = 3.6 V to 5.5 V or GND				±10	μA
I_I		V_{CC} = 3.6 V, Switch ON, V_{IN} = V_{CC} or GND	V_I = V_{CC} − 0.7 V to 5.5 V			±20	μA
			V_I = 0.7 V to V_{CC} − 0.7 V			−40	
			V_I = 0 to 0.7 V			±5	
I_{OZ}[§]		V_{CC} = 3.6 V, V_O = 0 to 5.5 V, V_I = 0, Switch OFF, V_{IN} = V_{CC} or GND				±10	μA
I_{off}		V_{CC} = 0, V_O = 0 to 5.5 V, V_I = 0,				10	μA
I_{CC}		V_{CC} = 3.6 V, $I_{I/O}$ = 0, Switch ON or OFF, V_{IN} = V_{CC} or GND	V_I = V_{CC} or GND			20	μA
			V_I = 5.5 V			20	
ΔI_{CC}[¶]	Control inputs	V_{CC} = 3 V to 3.6 V, One input at V_{CC} − 0.6 V, Other inputs at V_{CC} or GND				300	μA
C_{in}	Control inputs	V_{CC} = 3.3 V, V_{IN} = V_{CC} or GND			4		pF
$C_{io(OFF)}$		V_{CC} = 3.3 V, $V_{I/O}$ = 5.5 V, 3.3 V, or GND, Switch OFF, V_{IN} = V_{CC} or GND			8		pF
$C_{io(ON)}$		V_{CC} = 3.3 V, Switch ON, V_{IN} = V_{CC} or GND	$V_{I/O}$ = 5.5 V or 3.3 V		7		pF
			$V_{I/O}$ = GND		21		
r_{on}[#]		V_{CC} = 2.3 V, TYP at V_{CC} = 2.5 V, V_I = 0	I_O = 24 mA		5	9	Ω
			I_O = 16 mA		5	9	
		V_{CC} = 3 V, V_I = 0	I_O = 64 mA		5	8	
			I_O = 32 mA		5	8	

[†] All typical values are at V_{CC} = 3.3 V (unless otherwise noted), T_A = 25°C.

[‡] V_{IN} and I_{IN} refer to control inputs. V_I, V_O, I_I, and I_O refer to data pins.

[§] For I/O ports, the parameter I_{OZ} includes the input leakage current.

[¶] This is the increase in supply current for each input that is at the specified TTL voltage level, rather than V_{CC} or GND.

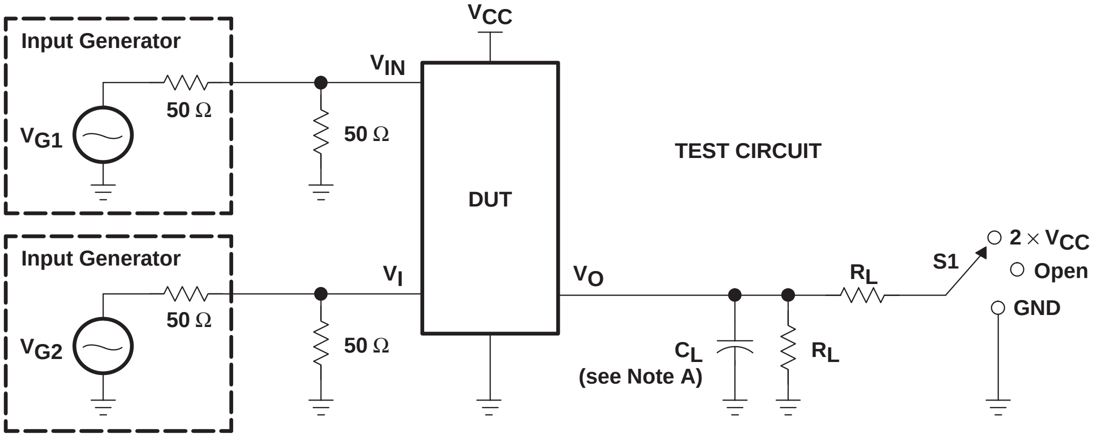
[#] Measured by the voltage drop between A and B terminals at the indicated current through the switch. ON-state resistance is determined by the lower of the voltages of the two (A or B) terminals.

switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figure 2)

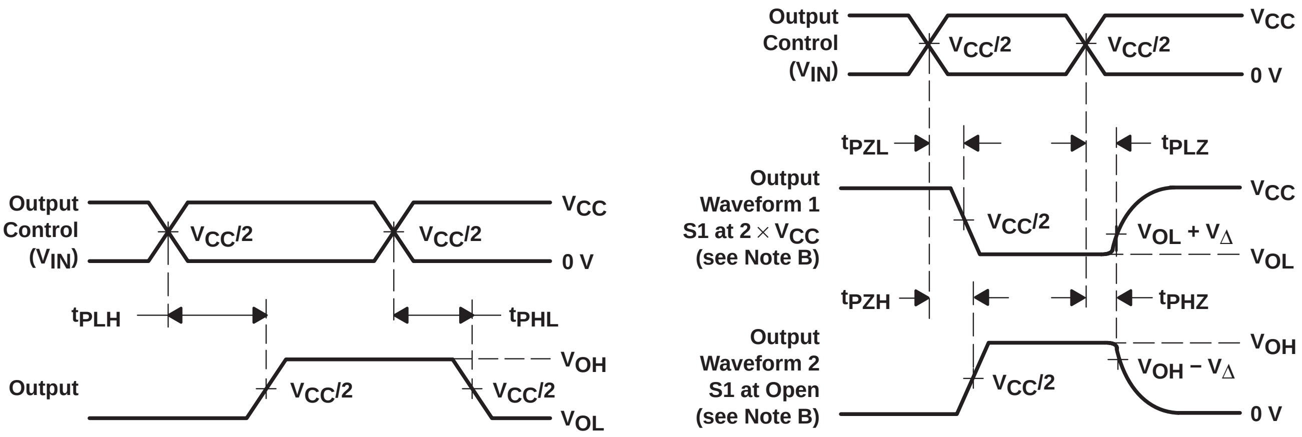
PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 2.5 V ± 0.2 V		V_{CC} = 3.3 V ± 0.3 V		UNIT
			MIN	MAX	MIN	MAX	
t_{pd}[†]	A or B	B or A		0.15		0.25	ns
$t_{pd(s)}$	BX	A or B	1	15	1	10	
t_{en}	$\overline{BE}$	A or B	1	13.5	1	9	ns
t_{dis}	$\overline{BE}$	A or B	1	7	1	8.5	ns

[†] The propagation delay is the calculated RC time constant of the typical ON-state resistance of the switch and the specified load capacitance, when driven by an ideal voltage source (zero output impedance).

PARAMETER MEASUREMENT INFORMATION



TEST	V_{CC}	S1	R_L	V_I	C_L	V_Δ
$t_{pd(s)}$	2.5 V ± 0.2 V 3.3 V ± 0.3 V	Open Open	500 Ω 500 Ω	3.6 V or GND 5.5 V or GND	30 pF 50 pF	
t_{PLZ}/t_{PZL}	2.5 V ± 0.2 V 3.3 V ± 0.3 V	2 × V_{CC} 2 × V_{CC}	500 Ω 500 Ω	GND GND	30 pF 50 pF	0.15 V 0.3 V
t_{PHZ}/t_{PZH}	2.5 V ± 0.2 V 3.3 V ± 0.3 V	Open Open	500 Ω 500 Ω	3.6 V 5.5 V	30 pF 50 pF	0.15 V 0.3 V



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES ($t_{pd(s)}$)

VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

NOTES:
- A. C_L includes probe and jig capacitance.
- B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, $t_r \le 2.5$ ns, $t_f \le 2.5$ ns.
- D. The outputs are measured one at a time, with one transition per measurement.
- E. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
- F. t_{PZL} and t_{PZH} are the same as t_{en}.
- G. t_{PLH} and t_{PHL} are the same as $t_{pd(s)}$. The t_{pd} propagation delay is the calculated RC time constant of the typical ON-state resistance of the switch and the specified load capacitance, when driven by an ideal voltage source (zero output impedance).
- H. All parameters and waveforms are not applicable to all devices.

Figure 2. Test Circuit and Voltage Waveforms

TYPICAL CHARACTERISTICS

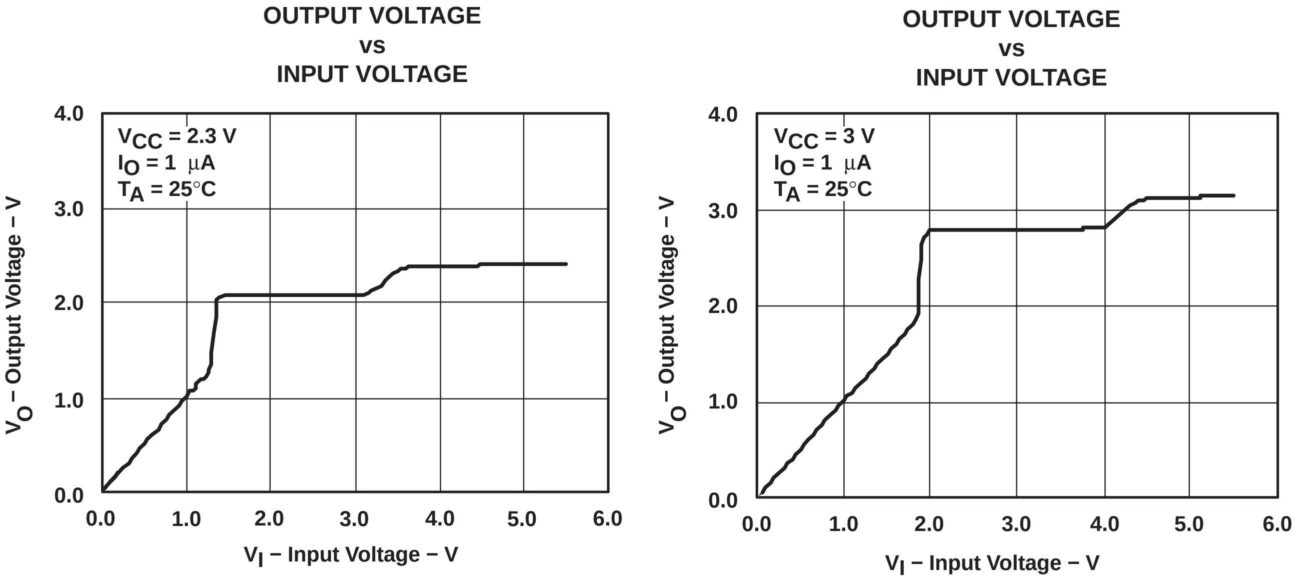
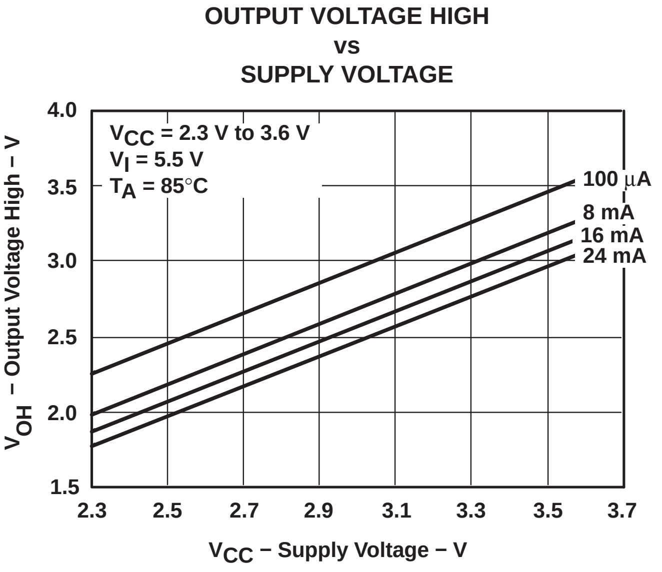
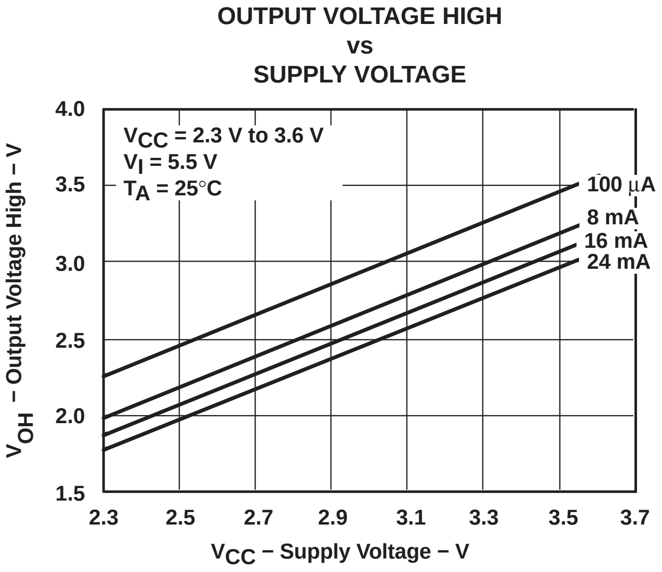


Figure 3. Data Output Voltage vs Data Input Voltage

TYPICAL CHARACTERISTICS (continued)





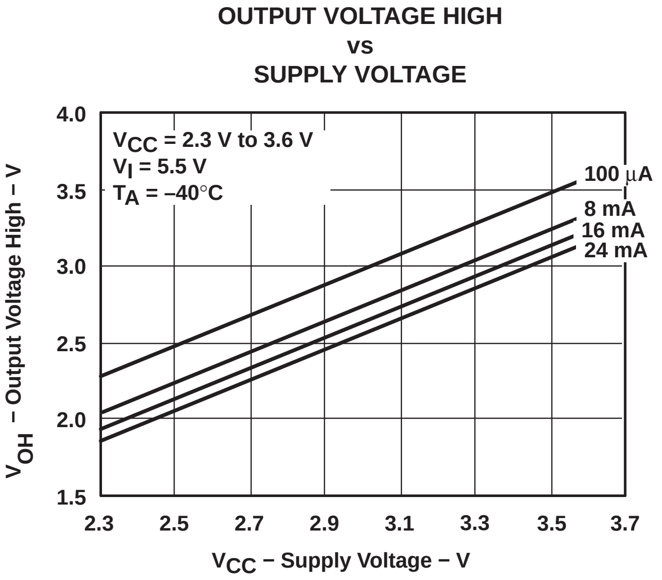


Figure 4. V_{OH} Values

PACKAGE OPTION ADDENDUM

PACKAGING INFORMATION

Orderable Device	Status [1]	Package Type	Package Drawing	Pins	Package Qty	Eco Plan [2]	Lead/Ball Finish	MSL Peak Temp [3]
74CB3T3383DBQRE4	ACTIVE	SSOP/ QSOP	DBQ	24	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
74CB3T3383DBQRG4	ACTIVE	SSOP/ QSOP	DBQ	24	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
74CB3T3383DGVRE4	ACTIVE	TVSOP	DGV	24	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
74CB3T3383DGVRG4	ACTIVE	TVSOP	DGV	24	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74CB3T3383DBQR	ACTIVE	SSOP/ QSOP	DBQ	24	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
SN74CB3T3383DGVR	ACTIVE	TVSOP	DGV	24	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74CB3T3383DW	ACTIVE	SOIC	DW	24	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74CB3T3383DWE4	ACTIVE	SOIC	DW	24	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74CB3T3383DWG4	ACTIVE	SOIC	DW	24	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74CB3T3383DWR	ACTIVE	SOIC	DW	24	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74CB3T3383DWRE4	ACTIVE	SOIC	DW	24	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74CB3T3383DWRG4	ACTIVE	SOIC	DW	24	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74CB3T3383PW	ACTIVE	TSSOP	PW	24	60	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74CB3T3383PWE4	ACTIVE	TSSOP	PW	24	60	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74CB3T3383PWG4	ACTIVE	TSSOP	PW	24	60	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74CB3T3383PWR	ACTIVE	TSSOP	PW	24	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74CB3T3383PWRE4	ACTIVE	TSSOP	PW	24	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74CB3T3383PWRG4	ACTIVE	TSSOP	PW	24	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and

PACKAGE OPTION ADDENDUM

package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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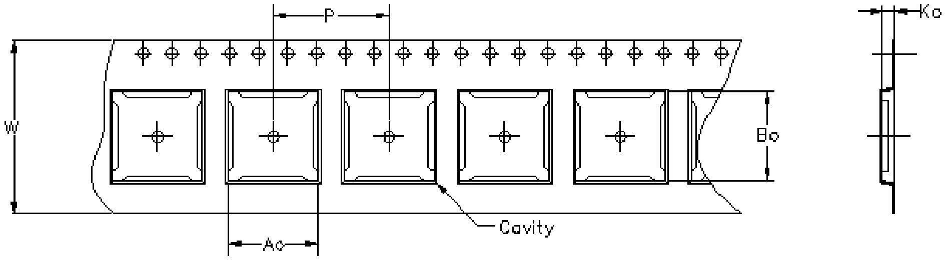
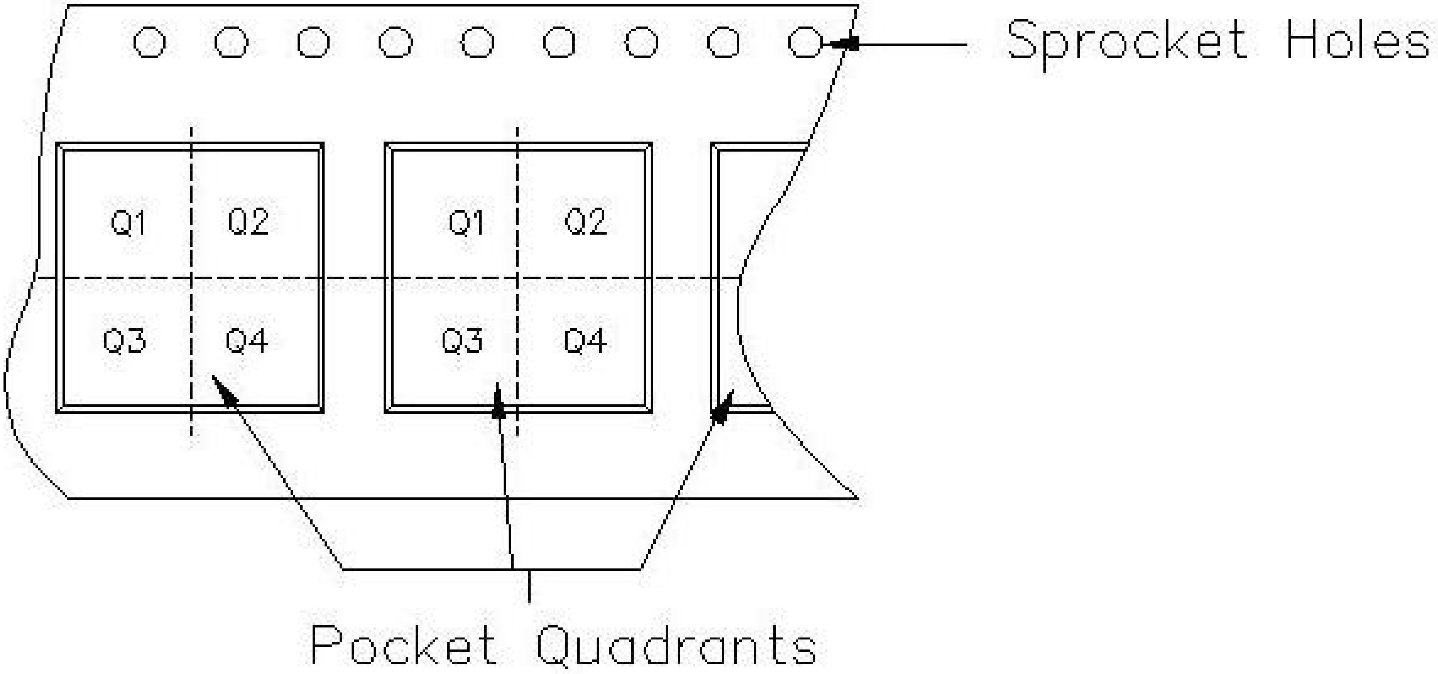


Carrier tape design is defined largely by the component lentgh, width, and thickness.

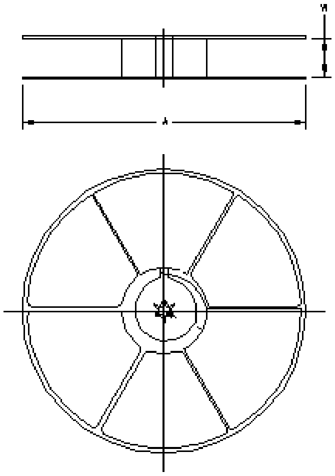
Ao = Dimension designed to accommodate the component width.
Bo = Dimension designed to accommodate the component length.
Ko = Dimension designed to accommodate the component thickness.
W = Overall width of the carrier tape.
P = Pitch between successive cavity centers.



TAPE AND REEL INFORMATION

PACKAGE MATERIALS INFORMATION

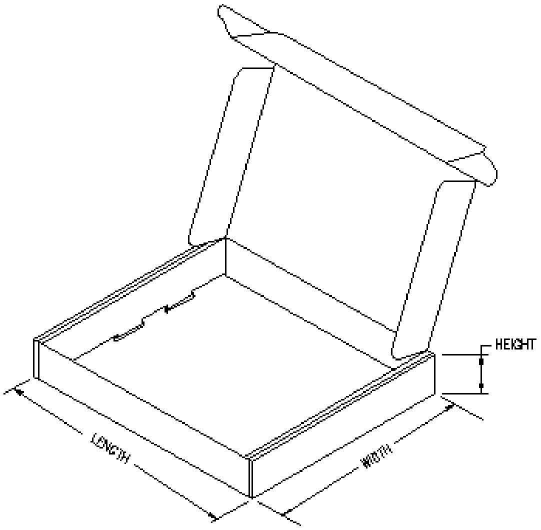
Device	Package	Pins	Site	Reel Diameter (mm)	Reel Width (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74CB3T3383DBQR	DBQ	24	MLA	330	16	6.5	9.0	2.1	8	16	Q1
SN74CB3T3383DGVR	DGV	24	MLA	330	12	7.0	5.6	1.6	8	12	Q1
SN74CB3T3383DWR	DW	24	TAI	330	24	10.75	15.7	2.7	12	24	Q1
SN74CB3T3383PWR	PW	24	MLA	330	16	6.95	8.3	1.6	8	16	Q1



TAPE AND REEL BOX INFORMATION

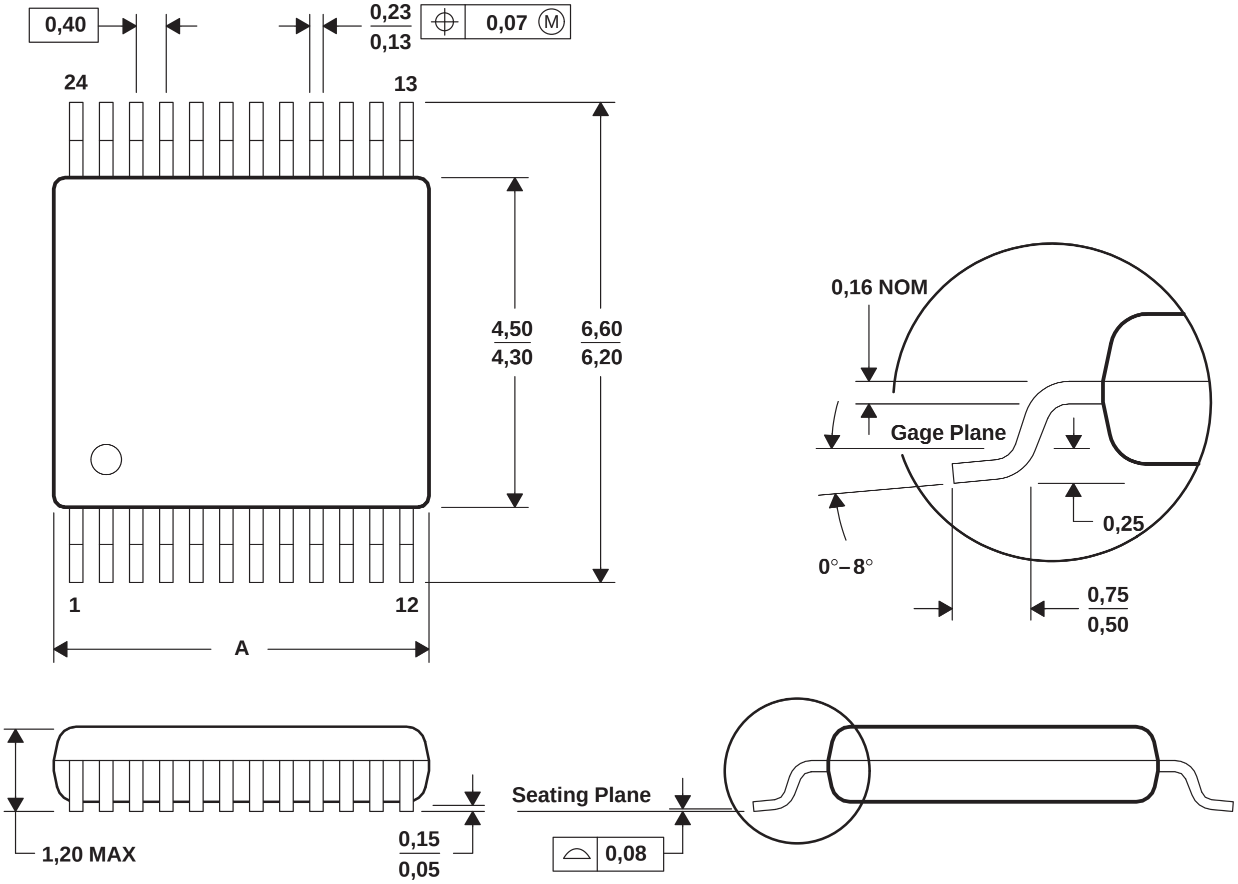
Device	Package	Pins	Site	Length (mm)	Width (mm)	Height (mm)
SN74CB3T3383DBQR	DBQ	24	MLA	346.0	346.0	33.0
SN74CB3T3383DGVR	DGV	24	MLA	346.0	346.0	29.0
SN74CB3T3383DWR	DW	24	TAI	346.0	346.0	41.0
SN74CB3T3383PWR	PW	24	MLA	346.0	346.0	33.0

PACKAGE MATERIALS INFORMATION



DGV (R-PDSO-G**) PLASTIC SMALL-OUTLINE

24 PINS SHOWN



PINS ** DIM	14	16	20	24	38	48	56
A MAX	3,70	3,70	5,10	5,10	7,90	9,80	11,40
A MIN	3,50	3,50	4,90	4,90	7,70	9,60	11,20

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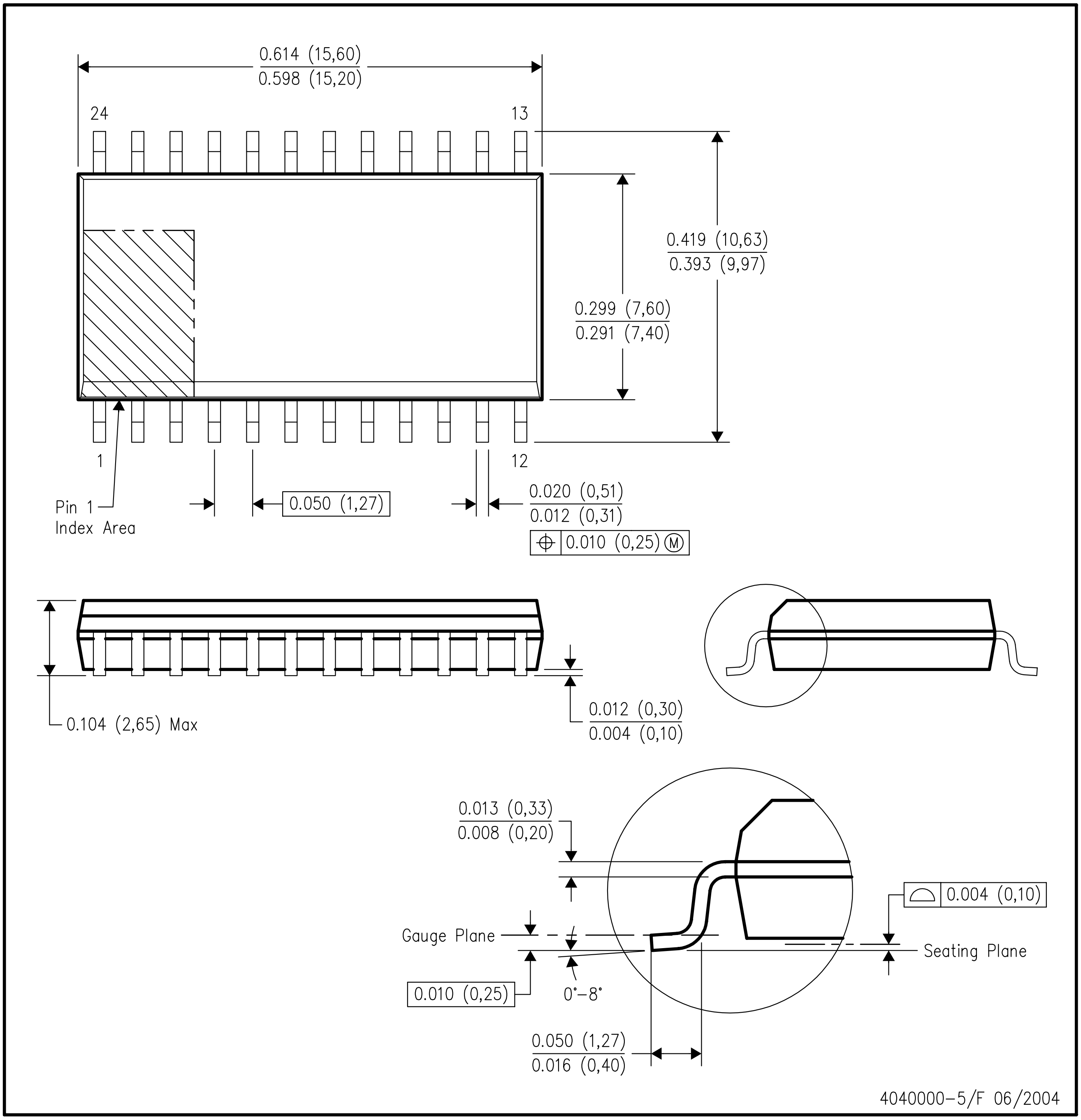
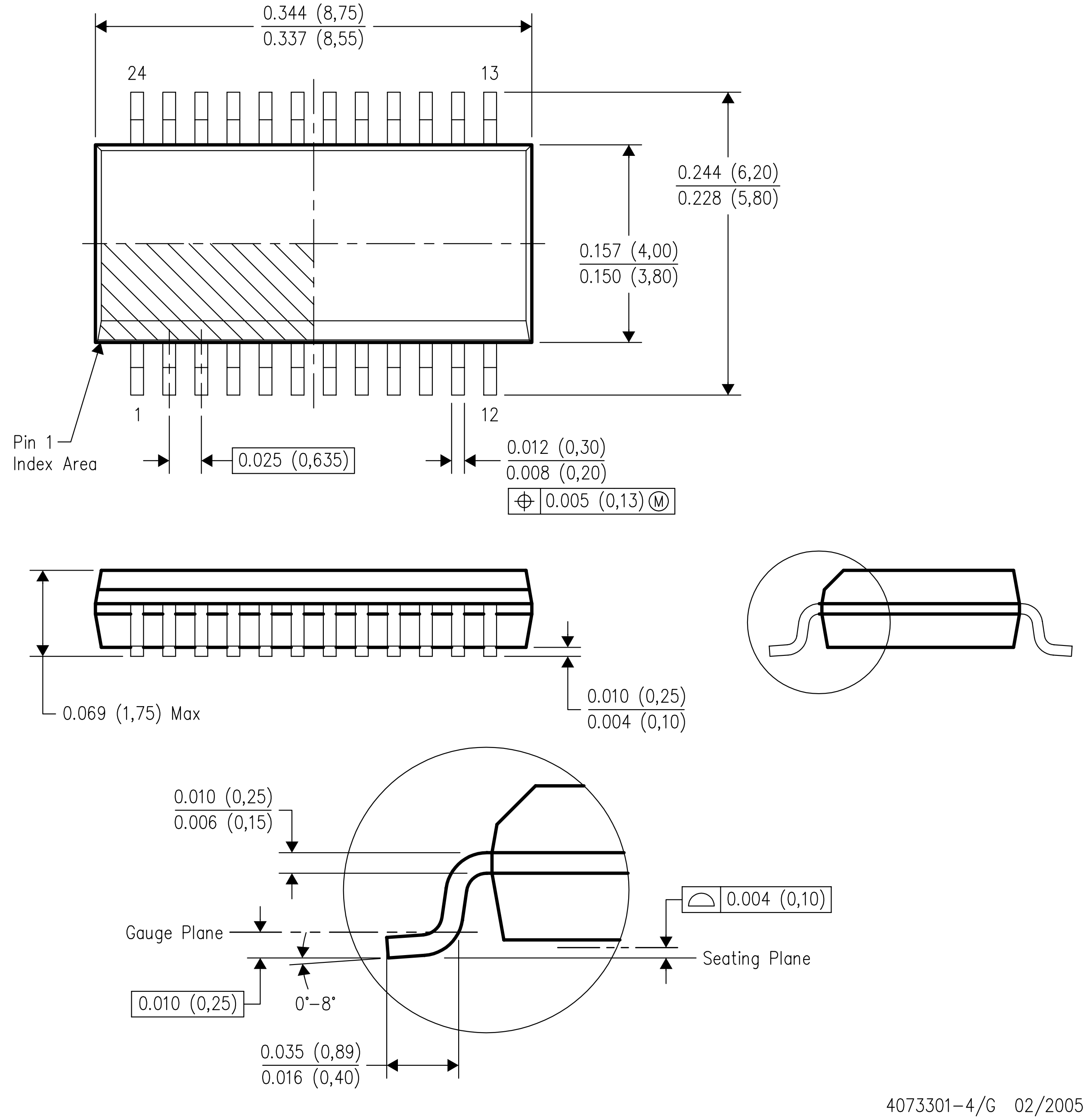
NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15 per side.
- D. Falls within JEDEC: 24/48 Pins – MO-153
  14/16/20/56 Pins – MO-194

DW (R-PDSO-G24) PLASTIC SMALL-OUTLINE PACKAGE



NOTES:
- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
- D. Falls within JEDEC MS-013 variation AD.

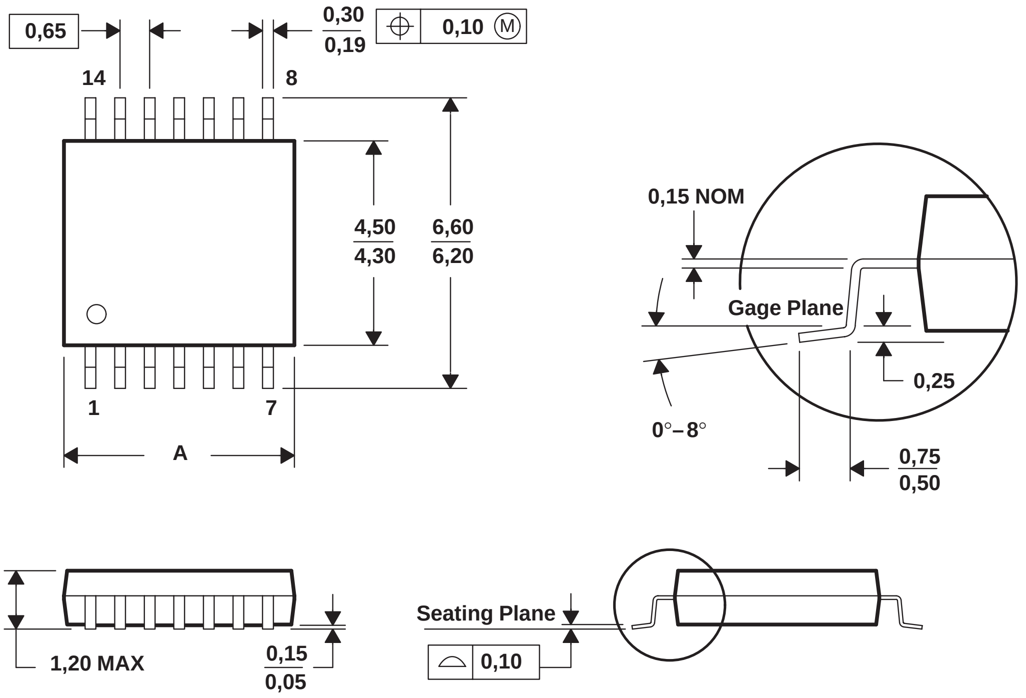
DBQ (R–PDSO–G24) PLASTIC SMALL–OUTLINE PACKAGE



NOTES:
- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15) per side.
- D. Falls within JEDEC MO–137 variation AE.

PW (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

14 PINS SHOWN



PINS ** / DIM	8	14	16	20	24	28
A MAX	3,10	5,10	5,10	6,60	7,90	9,80
A MIN	2,90	4,90	4,90	6,40	7,70	9,60

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NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
- D. Falls within JEDEC MO-153

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