

SN54CBT16244, SN74CBT16244 16-BIT FET BUS SWITCHES

SCDS031I – MAY 1996 – REVISED OCTOBER 2000

- **Members of Texas Instruments' Widebus™ Family**
- **Standard '16244-Type Pinout**
- **5-Ω Switch Connection Between Two Ports**
- **TTL-Compatible Input Levels**

description

The 'CBT16244 devices provide 16 bits of high-speed TTL-compatible bus switching in a standard '16244 device pinout. The low on-state resistance of the switch allows connections to be made with minimal propagation delay.

These devices are organized as four 4-bit low-impedance switches with separate output-enable ($\overline{OE}$) inputs. When $\overline{OE}$ is low, the switch is on, and data can flow from port A to port B, or vice versa. When $\overline{OE}$ is high, the switch is open, and the high-impedance state exists between the two ports.

SN54CBT16244 ... WD PACKAGE SN74CBT16244 ... DGG, DGV, OR DL PACKAGE (TOP VIEW)

$\overline{1OE}$	1	48	$\overline{2OE}$
1B1	2	47	1A1
1B2	3	46	1A2
GND	4	45	GND
1B3	5	44	1A3
1B4	6	43	1A4
V _{CC}	7	42	V _{CC}
2B1	8	41	2A1
2B2	9	40	2A2
GND	10	39	GND
2B3	11	38	2A3
2B4	12	37	2A4
3B1	13	36	3A1
3B2	14	35	3A2
GND	15	34	GND
3B3	16	33	3A3
3B4	17	32	3A4
V _{CC}	18	31	V _{CC}
4B1	19	30	4A1
4B2	20	29	4A2
GND	21	28	GND
4B3	22	27	4A3
4B4	23	26	4A4
$\overline{4OE}$	24	25	$\overline{3OE}$

ORDERING INFORMATION

T _A	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
–40°C to 85°C	SSOP – DL	Tube	SN74CBT16244DL	CBT16244
		Tape and reel	SN74CBT16244DLR	
	TSSOP – DGG	Tape and reel	SN74CBT16244DGGR	CBT16244
–55°C to 125°C	TVSOP – DGV	Tape and reel	SN74CBT16244DGV	CY244
	CFP – WD	Tube	SNJ54CBT16244WD	SNJ54CBT16244WD

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

FUNCTION TABLE (each 4-bit bus switch)

INPUT $\overline{OE}$	OUTPUTS A, B
L	A port = B port
H	Disconnect

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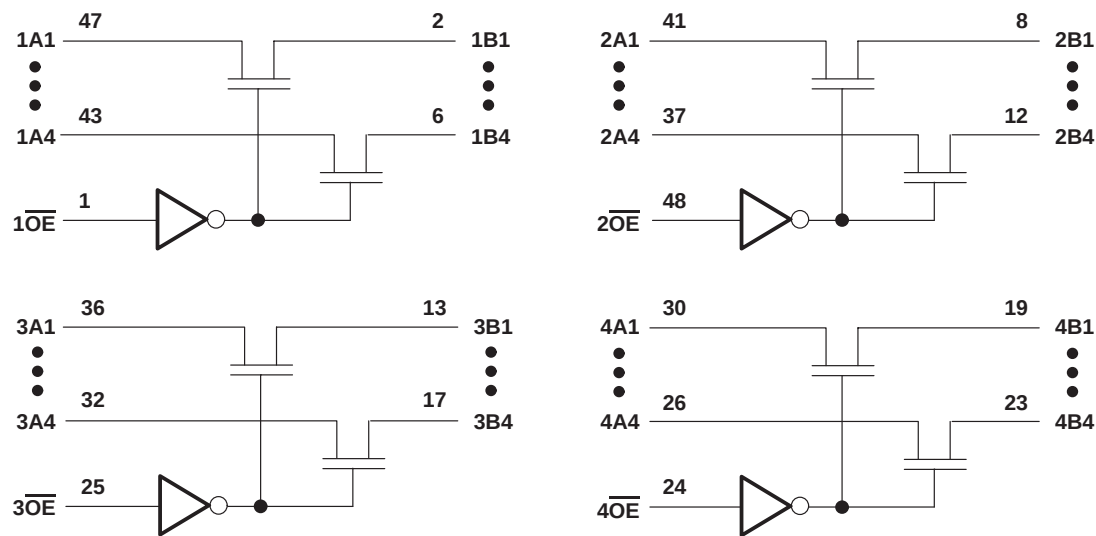


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On products compliant to MIL-PRF-38535, all parameters are tested unless otherwise noted. On all other products, production processing does not necessarily include testing of all parameters.

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16-BIT FET BUS SWITCHES

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logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

Supply voltage range, V_{CC}	–0.5 V to 7 V
Input voltage range, V_I (see Note 1)	–0.5 V to 7 V
Continuous channel current	128 mA
Input clamp current, I_{IK} ($V_{I/O} < 0$)	–50 mA
Package thermal impedance, θ_{JA} (see Note 2): DGG package	70°C/W
DGV package	58°C/W
DL package	63°C/W
Storage temperature range, T_{stg}	–65°C to 150°C

[†] Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. The package thermal impedance is calculated in accordance with JESD 51-7.

recommended operating conditions (see Note 3)

		SN54CBT16244		SN74CBT16244		UNIT
		MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage	4	5.5	4	5.5	V
V_{IH}	High-level control input voltage	2		2		V
V_{IL}	Low-level control input voltage		0.8		0.8	V
T_A	Operating free-air temperature	–55	125	–40	85	°C

NOTE 3: All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	SN54CBT16244			SN74CBT16244			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}		$V_{CC} = 4.5\text{ V}$, $I_I = -18\text{ mA}$			-1.2			-1.2	V
I_I		$V_{CC} = 0$, $V_I = 5.5\text{ V}$			10			10	μA
		$V_{CC} = 5.5\text{ V}$, $V_I = 5.5\text{ V or GND}$			± 1			± 1	
I_{CC}		$V_{CC} = 5.5\text{ V}$, $V_I = V_{CC}\text{ or GND}$, $I_O = 0$			3.2			3	μA
$\Delta I_{CC}^\ddagger$	Control inputs	$V_{CC} = 5.5\text{ V}$, Other inputs at $V_{CC}\text{ or GND}$, One input at 3.4 V			2.5			2.5	mA
C_i	Control inputs	$V_I = 3\text{ V or } 0$			2.5			2.5	pF
$C_{io(OFF)}$		$V_O = 3\text{ V or } 0$, $\overline{OE} = V_{CC}$			4.5			4.5	pF
$r_{on}^\S$		$V_{CC} = 4\text{ V}$, $V_I = 2.4\text{ V}$, $I_I = 15\text{ mA}$			20			20	Ω
		$V_{CC} = 4.5\text{ V}$, $V_I = 0$, $I_I = 64\text{ mA}$			5 10			5 7	
		$V_{CC} = 4.5\text{ V}$, $V_I = 0$, $I_I = 30\text{ mA}$			5 10			5 7	
		$V_{CC} = 4.5\text{ V}$, $V_I = 2.4\text{ V}$, $I_I = 15\text{ mA}$			8 14			8 12	

† All typical values are at $V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}$.

‡ This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.

§ Measured by the voltage drop between the A and B terminals at the indicated current through the switch. On-state resistance is determined by the lower of the voltages of the two (A or B) terminals.

switching characteristics over recommended operating free-air temperature range, $C_L = 50\text{ pF}$ (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	SN54CBT16244				SN74CBT16244				UNIT
			V _{CC} = 4 V		V _{CC} = 5 V ± 0.5 V		V _{CC} = 4 V		V _{CC} = 5 V ± 0.5 V		
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t _{pd} [¶]	A or B	B or A				0.8*		0.35		0.25	ns
t _{en}	$\overline{OE}$	A or B		10.3	1	9.2		5.5	1	5.1	ns
t _{dis}	$\overline{OE}$	A or B		9.7	1	8.2		5.2	1	5.4	ns

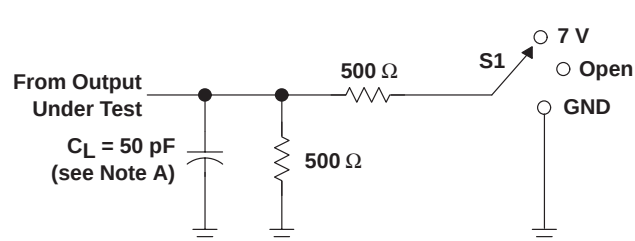
* On products compliant to MIL-PRF-38535, this parameter is not production tested.

† The propagation delay is the calculated RC time constant of the typical on-state resistance of the switch and the specified load capacitance, when driven by an ideal voltage source (zero output impedance).

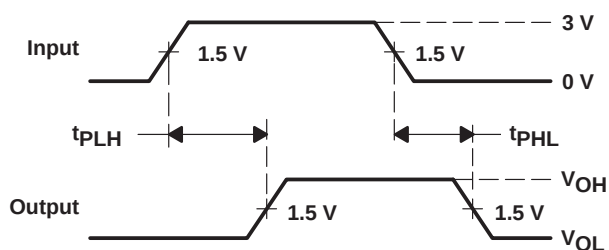
SN54CBT16244, SN74CBT16244 16-BIT FET BUS SWITCHES

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PARAMETER MEASUREMENT INFORMATION

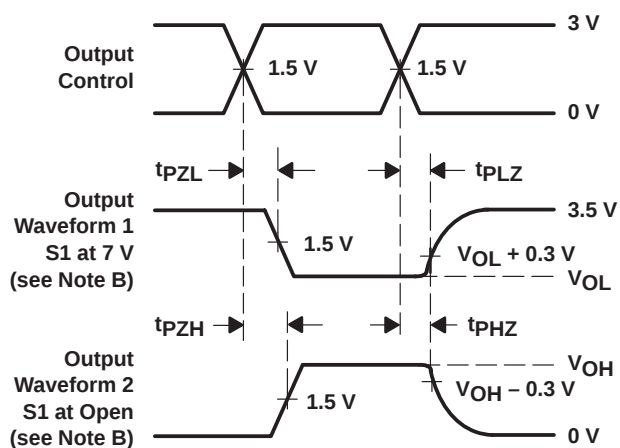


LOAD CIRCUIT



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES

TEST	S1
t_{pd}	Open
t_{PLZ}/t_{PZL}	7 V
t_{PHZ}/t_{PZH}	Open



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

- NOTES:
- A. C_L includes probe and jig capacitance.
 - B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 - C. All input pulses are supplied by generators having the following characteristics: $PRR \leq 10 \text{ MHz}$, $Z_O = 50 \Omega$, $t_r \leq 2.5 \text{ ns}$, $t_f \leq 2.5 \text{ ns}$.
 - D. The outputs are measured one at a time with one transition per measurement.
 - E. t_{PLZ} and t_{PHZ} are the same as t_{dis} .
 - F. t_{PZL} and t_{PZH} are the same as t_{en} .
 - G. t_{PLH} and t_{PHL} are the same as t_{pd} .

Figure 1. Load Circuit and Voltage Waveforms

PACKAGING INFORMATION

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/Ball Finish	MSL Peak Temp ⁽³⁾
5962-9855301QXA	ACTIVE	CFP	WD	48	1	TBD	A42 SNPB	N / A for Pkg Type
74CBT16244DGGRE4	ACTIVE	TSSOP	DGG	48	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
74CBT16244DGVRE4	ACTIVE	TVSOP	DGV	48	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
74CBT16244DGVRG4	ACTIVE	TVSOP	DGV	48	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74CBT16244DGGR	ACTIVE	TSSOP	DGG	48	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74CBT16244DGVR	ACTIVE	TVSOP	DGV	48	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74CBT16244DL	ACTIVE	SSOP	DL	48	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74CBT16244DLG4	ACTIVE	SSOP	DL	48	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74CBT16244DLR	ACTIVE	SSOP	DL	48	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74CBT16244DLRG4	ACTIVE	SSOP	DL	48	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SNJ54CBT16244WD	ACTIVE	CFP	WD	48	1	TBD	A42 SNPB	N / A for Pkg Type

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBsolete: TI has discontinued the production of the device.

⁽²⁾ Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

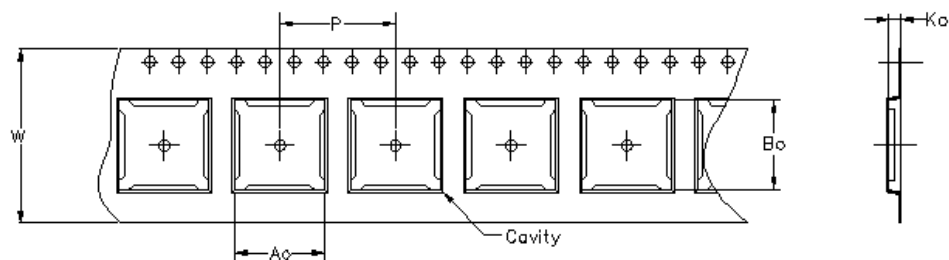
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

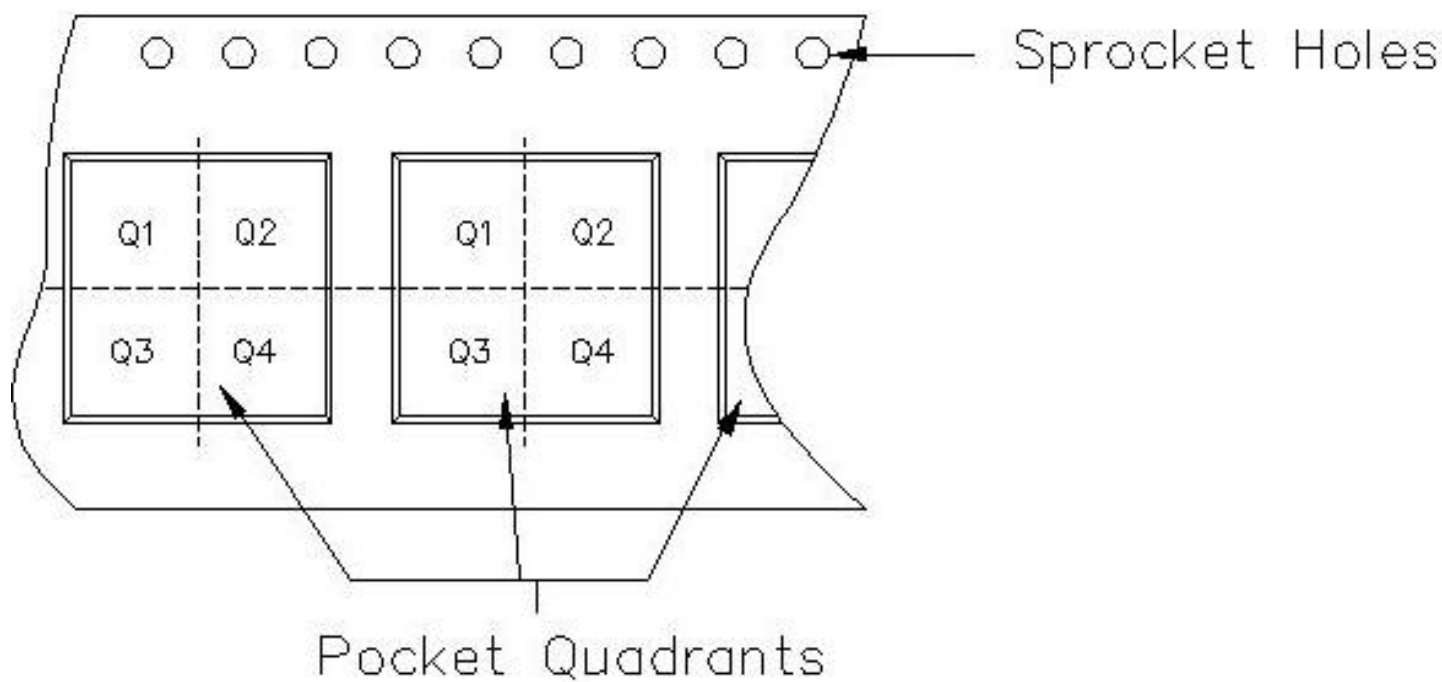
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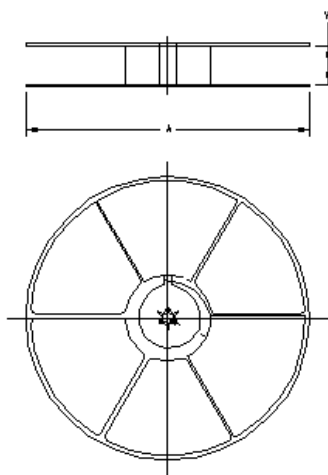
Carrier tape design is defined largely by the component length, width, and thickness.

A_0 = Dimension designed to accommodate the component width.
B_0 = Dimension designed to accommodate the component length.
K_0 = Dimension designed to accommodate the component thickness.
W = Overall width of the carrier tape.
P = Pitch between successive cavity centers.



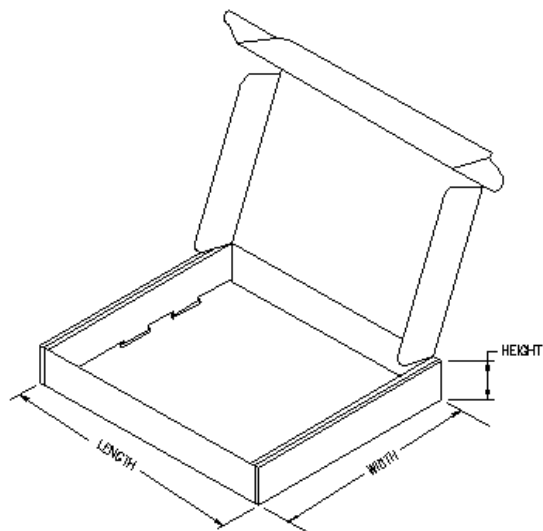
TAPE AND REEL INFORMATION

Device	Package	Pins	Site	Reel Diameter (mm)	Reel Width (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74CBT16244DGGR	DGG	48	MLA	330	24	8.6	15.8	1.8	12	24	Q1
SN74CBT16244DGVR	DGV	48	MLA	330	24	6.8	10.1	1.6	12	24	Q1
SN74CBT16244DLR	DL	48	MLA	330	32	11.35	16.2	3.1	16	32	Q1



TAPE AND REEL BOX INFORMATION

Device	Package	Pins	Site	Length (mm)	Width (mm)	Height (mm)
SN74CBT16244DGGR	DGG	48	MLA	333.2	333.2	31.75
SN74CBT16244DGVR	DGV	48	MLA	333.2	333.2	31.75
SN74CBT16244DLR	DL	48	MLA	346.0	346.0	49.0



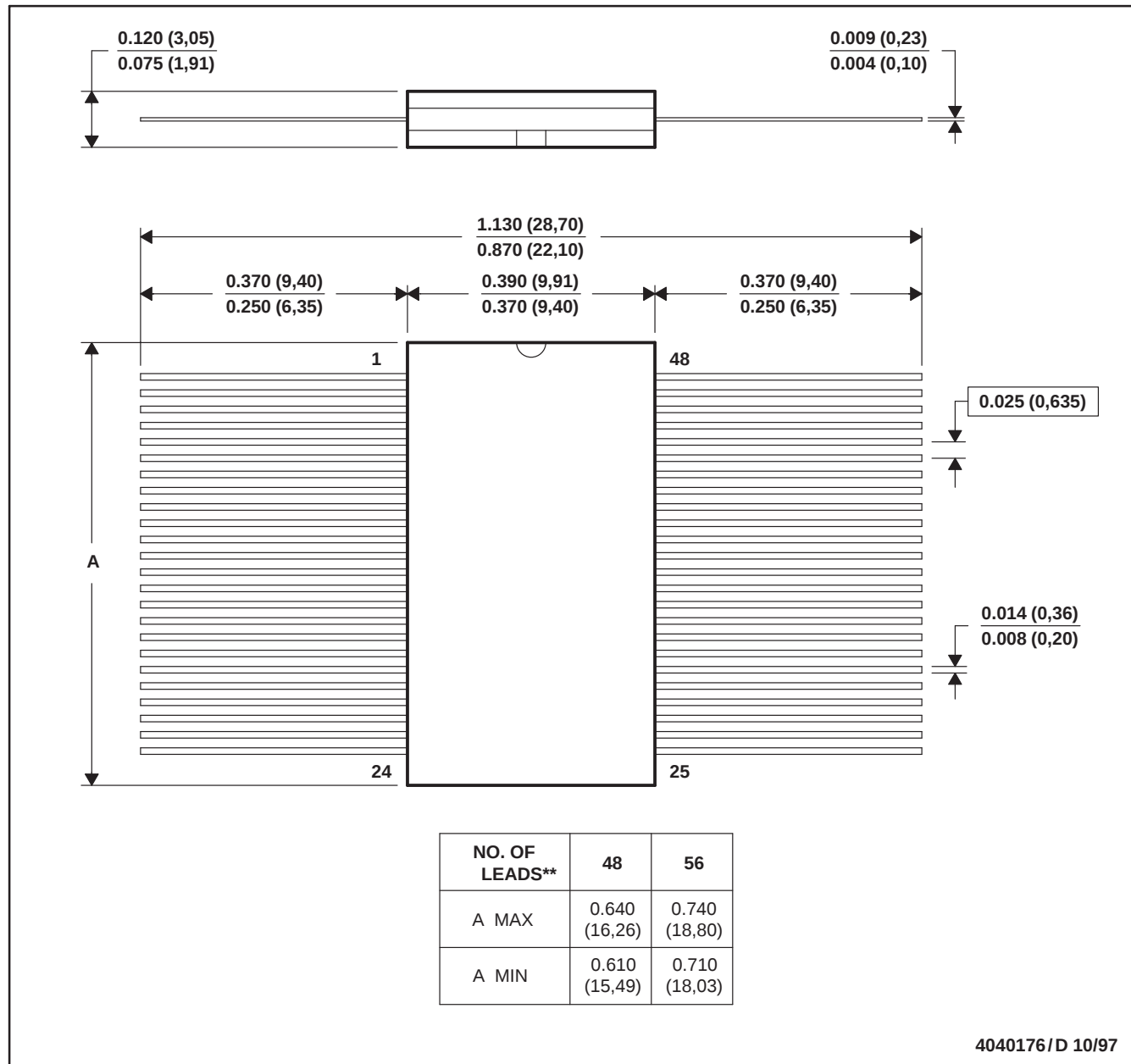
MECHANICAL DATA

MCFP010B – JANUARY 1995 – REVISED NOVEMBER 1997

WD (R-GDFP-F**)

CERAMIC DUAL FLATPACK

48 LEADS SHOWN



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. This package can be hermetically sealed with a ceramic lid using glass frit.
 - D. Index point is provided on cap for terminal identification only
 - E. Falls within MIL STD 1835: GDFP1-F48 and JEDEC MO-146AA
GDFP1-F56 and JEDEC MO-146AB

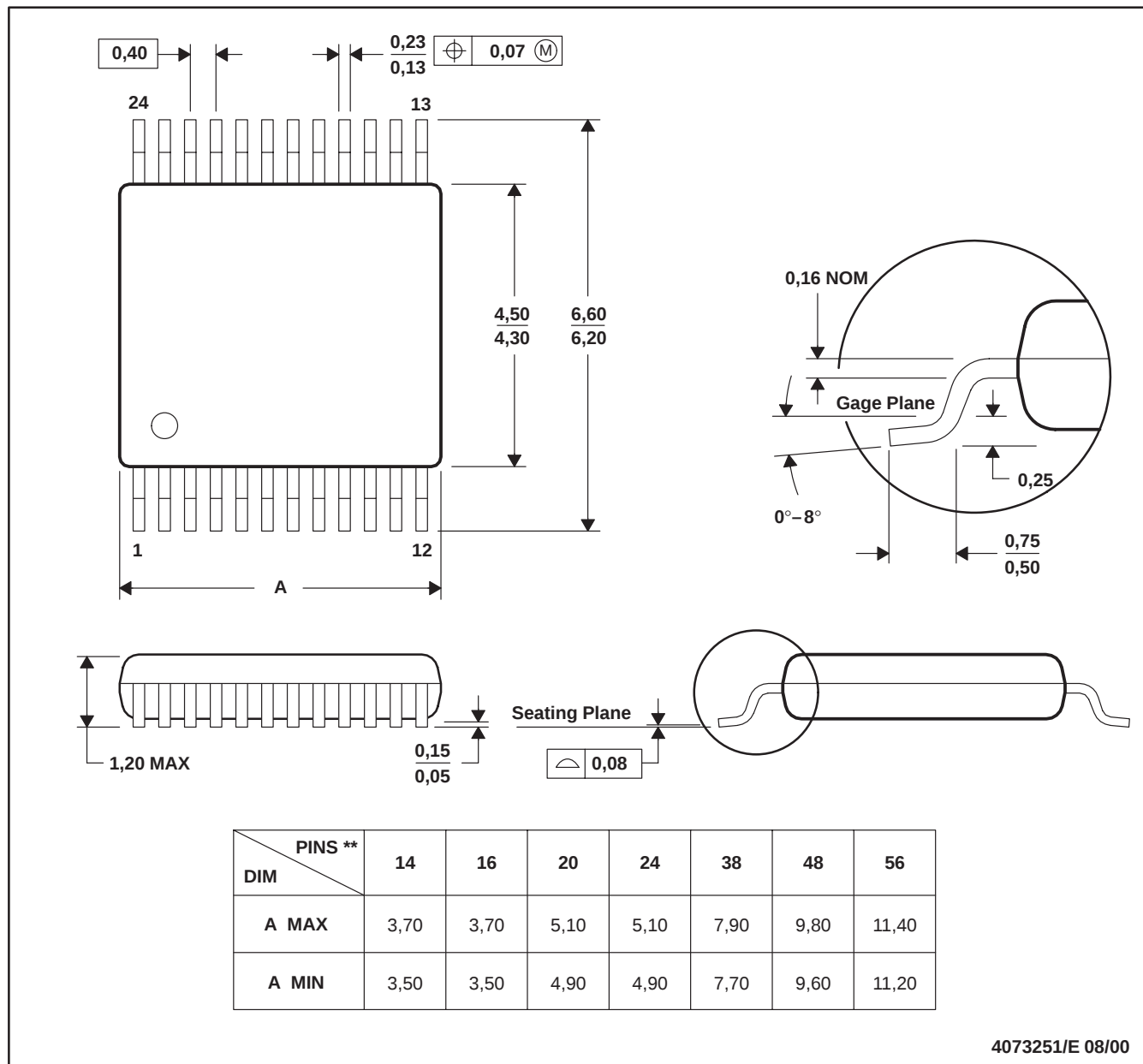
MECHANICAL DATA

MPDS006C – FEBRUARY 1996 – REVISED AUGUST 2000

DGV (R-PDSO-G**)

PLASTIC SMALL-OUTLINE

24 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15 per side.
 D. Falls within JEDEC: 24/48 Pins – MO-153
 14/16/20/56 Pins – MO-194

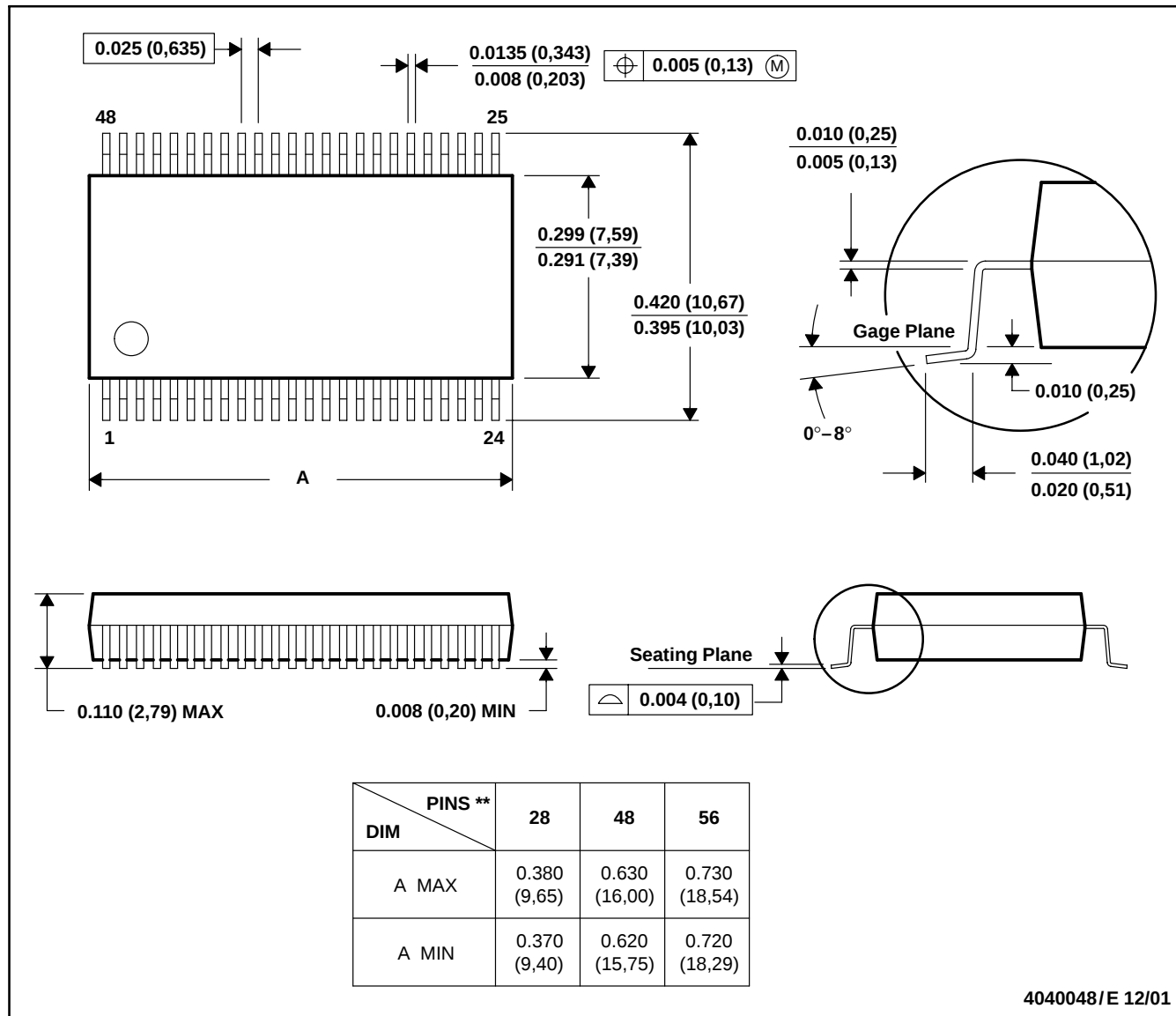
MECHANICAL DATA

MSS0001C – JANUARY 1995 – REVISED DECEMBER 2001

DL (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

48 PINS SHOWN



- NOTES: A. All linear dimensions are in inches (millimeters).
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
 D. Falls within JEDEC MO-118

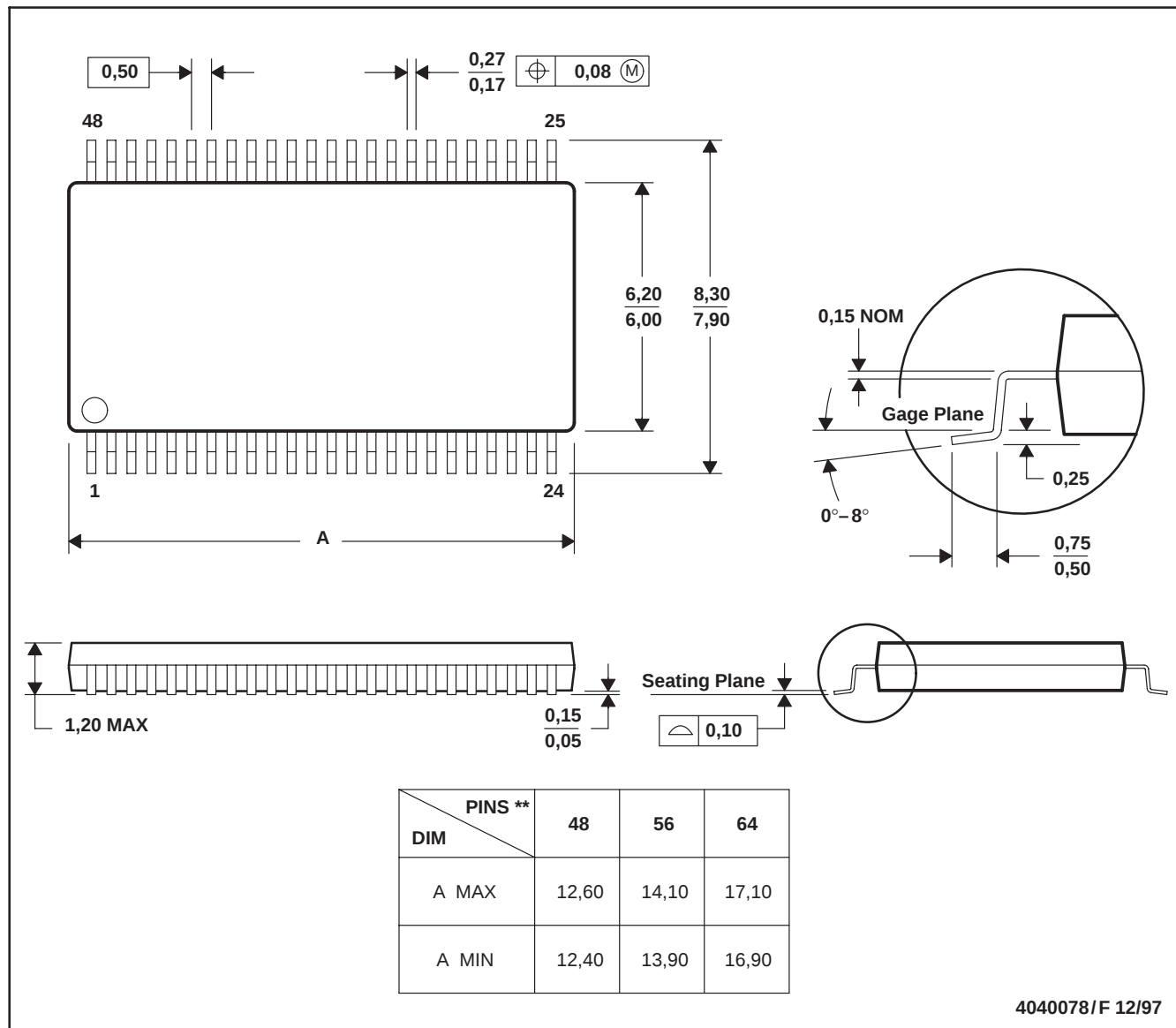
MECHANICAL DATA

MTSS003D – JANUARY 1995 – REVISED JANUARY 1998

DGG (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

48 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold protrusion not to exceed 0,15.
 D. Falls within JEDEC MO-153

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