



SCCS055 - August 1994 - Revised March 2000

CY74FCT16374T CY74FCT162374T

16-Bit Registers

Features

- FCT-E speed at 3.7 ns
- Power-off disable outputs permits live insertion
- Edge-rate control circuitry for significantly improved noise characteristics
- Typical output skew < 250 ps
- ESD > 2000V
- TSSOP (19.6-mil pitch) and SSOP (25-mil pitch) packages
- Industrial temperature range of -40°C to +85°C
- V_{CC} = 5V ± 10%

CY74FCT16374T Features:

- 64 mA sink current, 32 mA source current
- Typical V_{OLP} (ground bounce) < 1.0V at V_{CC} = 5V, T_A = 25°C

CY74FCT162374T Features:

- Balanced 24 mA output drivers
- Reduced system switching noise
- Typical V_{OLP} (ground bounce) < 0.6V at V_{CC} = 5V, T_A = 25°C

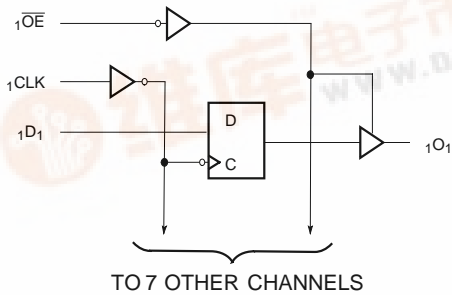
Functional Description

CY74FCT16374T and CY74FCT162374T are 16-bit D-type registers designed for use as buffered registers in high-speed, low power bus applications. These devices can be used as two independent 8-bit registers or as a single 16-bit register by connecting the output Enable (OE) and Clock (CLK) inputs. Flow-through pinout and small shrink packaging aid in simplifying board layout. The output buffers are designed with power-off disable feature that allows live insertion of boards.

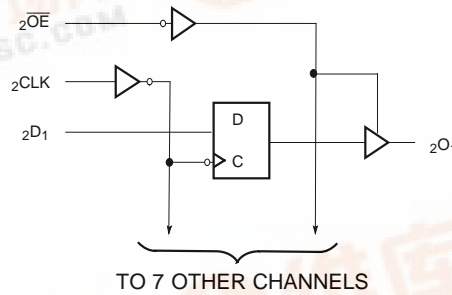
The CY74FCT16374T is ideally suited for driving high-capacitance loads and low-impedance backplanes.

The CY74FCT162374T has 24-mA balanced output drivers with current limiting resistors in the outputs. This reduces the need for external terminating resistors and provides for minimal undershoot and reduced ground bounce. The CY74FCT162374T is ideal for driving transmission lines.

Logic Block Diagrams



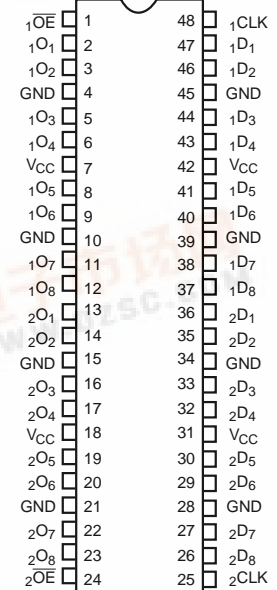
FCT162374-1



FCT162374-2

Pin Configuration

SSOP/TSSOP Top View



FCT162374-3



Function Table^[1]

Inputs			Outputs	Function
D	CLK	\overline{OE}	O	
X	L	H	Z	High-Z
X	H	H	Z	
L	\lrcorner	L	L	Load Register
H	\lrcorner	L	H	
L	\lrcorner	H	Z	
H	\lrcorner	H	Z	

Pin Description

Name	Description
D	Data Inputs
CLK	Clock Inputs
\overline{OE}	Three-State Output Enable Inputs (Active LOW)
O	Three-State Outputs

Maximum Ratings^[2, 3]

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature	-55°C to +125°C
Ambient Temperature with Power Applied	-55°C to +125°C
DC Input Voltage.....	-0.5V to +7.0V
DC Output Voltage.....	-0.5V to +7.0V
DC Output Current (Maximum Sink Current/Pin).....	-60 to +120 mA
Power Dissipation	1.0W
Static Discharge Voltage.....	>2001V (per MIL-STD-883, Method 3015)

Operating Range

Range	Ambient Temperature	V _{CC}
Industrial	-40°C to +85°C	5V ± 10%

Electrical Characteristics Over the Operating Range

Parameter	Description	Test Conditions	Min.	Typ. ^[4]	Max.	Unit
V _{IH}	Input HIGH Voltage		2.0			V
V _{IL}	Input LOW Voltage				0.8	V
V _H	Input Hysteresis ^[5]			100		mV
V _{IK}	Input Clamp Diode Voltage	V _{CC} =Min., I _{IN} =-18 mA		-0.7	-1.2	V
I _{IH}	Input HIGH Current	V _{CC} =Max., V _I =V _{CC}			±1	µA
I _{IL}	Input LOW Current	V _{CC} =Max., V _I =GND			±1	µA
I _{OZH}	High Impedance Output Current (Three-State Output pins)	V _{CC} =Max., V _{OUT} =2.7V			±1	µA
I _{OZL}	High Impedance Output Current (Three-State Output pins)	V _{CC} =Max., V _{OUT} =0.5V			±1	µA
I _{OS}	Short Circuit Current ^[6]	V _{CC} =Max., V _{OUT} =GND	-80	-140	-200	mA
I _O	Output Drive Current ^[6]	V _{CC} =Max., V _{OUT} =2.5V	-50		-180	mA
I _{OFF}	Power-Off Disable	V _{CC} =0V, V _{OUT} ≤4.5V ^[7]			±1	µA

Output Drive Characteristics for CY74FCT16374T

Parameter	Description	Test Conditions	Min.	Typ. ^[4]	Max.	Unit
V _{OH}	Output HIGH Voltage	V _{CC} =Min., I _{OH} =-3 mA	2.5	3.5		V
		V _{CC} =Min., I _{OH} =-15 mA	2.4	3.5		V
		V _{CC} =Min., I _{OH} =-32 mA	2.0	3.0		V
V _{OL}	Output LOW Voltage	V _{CC} =Min., I _{OL} =64 mA		0.2	0.55	V

Notes:

- H = HIGH Voltage Level. L = LOW Voltage Level. X = Don't Care. Z = HIGH Impedance. \lrcorner = LOW-to-HIGH Transition.
- Operation beyond the limits set forth may impair the useful life of the device. Unless otherwise noted, these limits are over the operating free-air temperature range.
- Unused inputs must always be connected to an appropriate logic voltage level, preferably either V_{CC} or ground.
- Typical values are at V_{CC}= 5.0V, T_A= +25°C ambient.
- This parameter is specified but not tested.
- Not more than one output should be shorted at a time. Duration of short should not exceed one second. The use of high-speed test apparatus and/or sample and hold techniques are preferable in order to minimize internal chip heating and more accurately reflect operational values. Otherwise prolonged shorting of a high output may raise the chip temperature well above normal and thereby cause invalid readings in other parametric tests. In any sequence of parameter tests, I_{OS} tests should be performed last.
- Tested at +25°C.

Output Drive Characteristics for CY74FCT162374T

Parameter	Description	Test Conditions	Min.	Typ. ^[4]	Max.	Unit
I _{ODL}	Output LOW Current ^[6]	V _{CC} =5V, V _{IN} =V _{IH} or V _{IL} , V _{OUT} =1.5V	60	115	150	mA
I _{ODH}	Output HIGH Current ^[6]	V _{CC} =5V, V _{IN} =V _{IH} or V _{IL} , V _{OUT} =1.5V	-60	-115	-150	mA
V _{OH}	Output HIGH Voltage	V _{CC} =Min., I _{OH} =-24 mA	2.4	3.3		V
V _{OL}	Output LOW Voltage	V _{CC} =Min., I _{OL} =24 mA		0.3	0.55	V

Capacitance^[5] (T_A = +25°C, f = 1.0 MHz)

Parameter	Description	Test Conditions	Typ. ^[4]	Max.	Unit
C _{IN}	Input Capacitance	V _{IN} = 0V	4.5	6.0	pF
C _{OUT}	Output Capacitance	V _{OUT} = 0V	5.5	8.0	pF

Power Supply Characteristics

Parameter	Description	Test Conditions	Typ. ^[4]	Max.	Unit	
I _{CC}	Quiescent Power Supply Current	V _{CC} =Max. V _{IN} ≤0.2V, V _{IN} ≥V _{CC} -0.2V	5	500	μA	
ΔI _{CC}	Quiescent Power Supply Current (TTL inputs HIGH)	V _{CC} =Max. V _{IN} =3.4V ^[8]	0.5	1.5	mA	
I _{CCD}	Dynamic Power Supply Current ^[9]	V _{CC} =Max., One Input Toggling, 50% Duty Cycle, Outputs Open, \overline{OE} =GND	60	100	μA/MHz	
I _C	Total Power Supply Current ^[10]	V _{CC} =Max., f ₀ =10 MHz, f ₁ =5 MHz, 50% Duty Cycle, Outputs Open, One Bit Toggling, \overline{OE} =GND	V _{IN} =V _{CC} or V _{IN} =GND	0.6	1.5	mA
			V _{IN} =3.4V or V _{IN} =GND	1.1	3.0	mA
		V _{CC} =Max., f ₀ =10 MHz, f ₁ =2.5 MHz, 50% Duty Cycle, Outputs Open, Sixteen Bits Toggling, \overline{OE} =GND	V _{IN} =V _{CC} or V _{IN} =GND	3.0	5.5 ^[11]	mA
			V _{IN} =3.4V or V _{IN} =GND	7.5	19.0 ^[11]	mA

Note:

8. Per TTL driven input (V_{IN}=3.4V); all other inputs at V_{CC} or GND.
9. This parameter is not directly testable, but is derived for use in Total Power Supply calculations.
10. I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}
I_C = I_{CC} + ΔI_{CC}D_HN_T + I_{CCD}(f₀/2 + f₁N₁)
I_{CC} = Quiescent Current with CMOS input levels
ΔI_{CC} = Power Supply Current for a TTL HIGH input (V_{IN}=3.4V)
D_H = Duty Cycle for TTL inputs HIGH
N_T = Number of TTL inputs at D_H
I_{CCD} = Dynamic Current caused by an input transition pair (HLH or LHL)
f₀ = Clock frequency for registered devices, otherwise zero
f₁ = Input signal frequency
N₁ = Number of inputs changing at f₁
All currents are in milliamps and all frequencies are in megahertz.
11. Values for these conditions are examples of the I_{CC} formula. These limits are specified but not tested.

Switching Characteristics Over the Operating Range^[12]

Parameter	Description	CY74FCT16374T CY74FCT162374T		CY74FCT16374AT CY74FCT162374AT		Unit	Fig. No. ^[13]
		Min.	Max.	Min.	Max.		
t _{PLH} t _{PHL}	Propagation Delay CLK to O	2.0	10.0	2.0	6.5	ns	1, 5
t _{PZH} t _{PZL}	Output Enable Time	1.5	12.5	1.5	6.5	ns	1, 7, 8
t _{PHZ} t _{PLZ}	Output Disable Time	1.5	8.0	1.5	5.5	ns	1, 7, 8
t _{SU}	Set-Up Time HIGH or LOW, D to CLK	2.0		2.0		ns	4
t _H	Hold Time HIGH or LOW, D to CLK	1.5		1.5		ns	4
t _W	CLK Pulse Width HIGH or LOW	5.0		5.0		ns	5
t _{SK(O)}	Output Skew ^[14]		0.5		0.5	ns	

Parameter	Description	CY74FCT16374CT CY74FCT162374CT		CY74FCT16374ET CY74FCT162374ET		Unit	Fig. No. ^[13]
		Min.	Max.	Min.	Max.		
t _{PLH} t _{PHL}	Propagation Delay CLK to O	2.0	5.2	2.0	3.7	ns	1, 5
t _{PZH} t _{PZL}	Output Enable Time	1.5	5.5	1.5	4.4	ns	1, 7, 8
t _{PHZ} t _{PLZ}	Output Disable Time	1.5	5.0	1.5	3.6	ns	1, 7, 8
t _{SU}	Set-Up Time HIGH or LOW, D to CLK	2.0		1.5		ns	4
t _H	Hold Time HIGH or LOW, D to CLK	1.5		0.0		ns	4
t _W	CLK Pulse Width HIGH or LOW	3.3		3.0		ns	5
t _{SK(O)}	Output Skew ^[14]		0.5		0.5	ns	

Notes:

12. Minimum limits are specified but not tested on Propagation Delays.

13. See "Parameter Measurement Information" in the General Information section.

14. Skew between any two outputs of the same package switching in the same direction. This parameter is ensured by design.

Ordering Information CY74FCT16374T

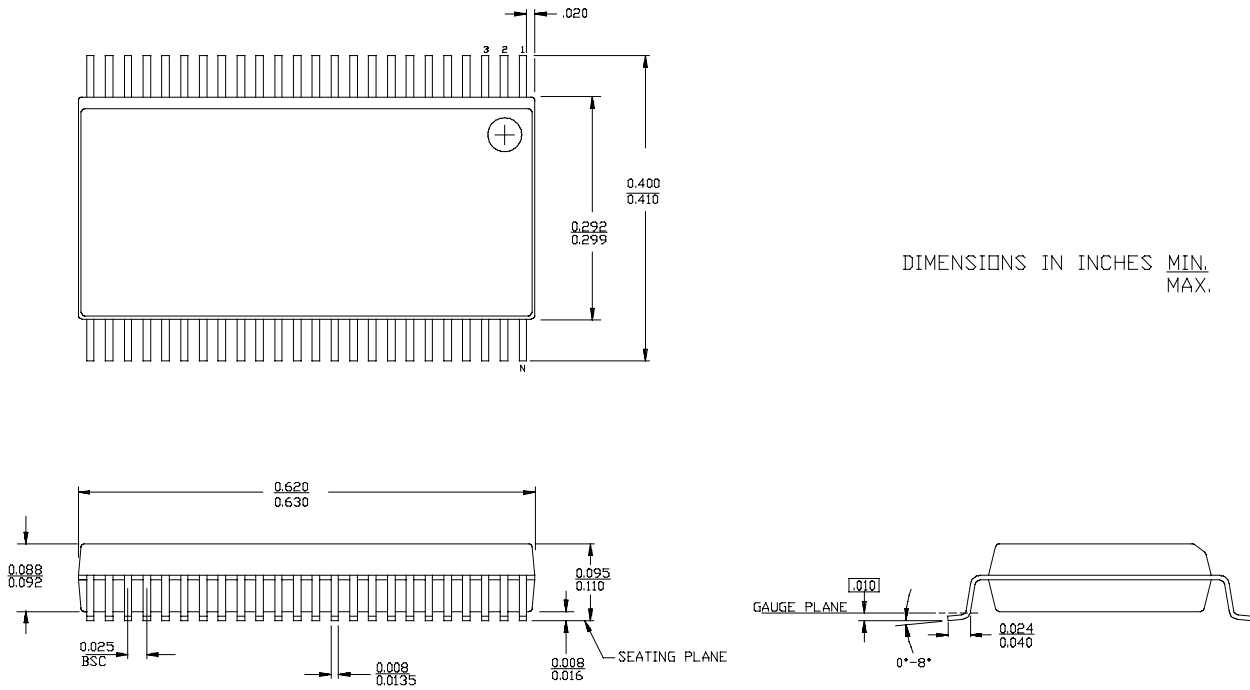
Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
3.7	CY74FCT16374ETPACT	Z48	48-Lead (240-Mil) TSSOP	Industrial
	CY74FCT16374ETPVC/PVCT	O48	48-Lead (300-Mil) SSOP	
5.2	CY74FCT16374CTPACT	Z48	48-Lead (240-Mil) TSSOP	Industrial
	CY74FCT16374CTPVC/PVCT	O48	48-Lead (300-Mil) SSOP	
6.5	CY74FCT16374ATPACT	Z48	48-Lead (240-Mil) TSSOP	Industrial
	CY74FCT16374ATPVC/PVCT	O48	48-Lead (300-Mil) SSOP	
10.0	CY74FCT16374TPVC/PVCT	O48	48-Lead (300-Mil) SSOP	Industrial

Ordering Information CY74FCT162374T

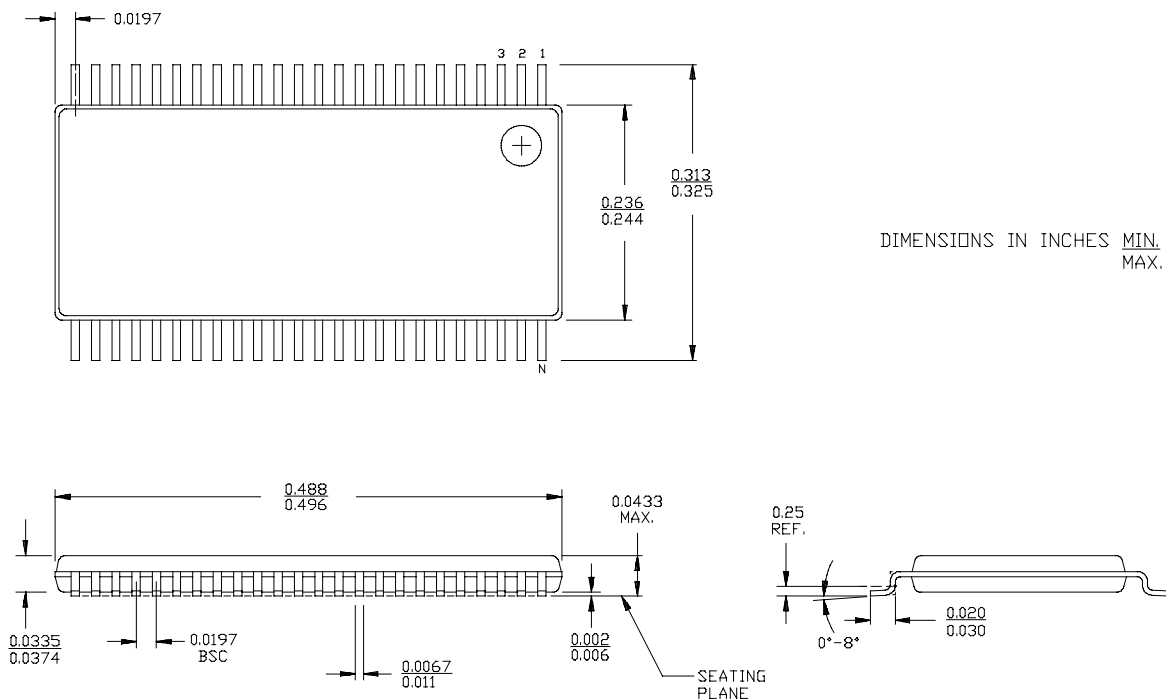
Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
3.7	74FCT162374ETPACT	Z48	48-Lead (240-Mil) TSSOP	Industrial
	CY74FCT162374ETPVC	O48	48-Lead (300-Mil) SSOP	
	74FCT162374ETPVCT	O48	48-Lead (300-Mil) SSOP	
5.2	74FCT162374CTPACT	Z48	48-Lead (240-Mil) TSSOP	Industrial
	CY74FCT162374CTPVC	O48	48-Lead (300-Mil) SSOP	
	74FCT162374CTPVCT	O48	48-Lead (300-Mil) SSOP	
6.5	74FCT162374ATPACT	Z48	48-Lead (240-Mil) TSSOP	Industrial
	CY74FCT162374ATPVC	O48	48-Lead (300-Mil) SSOP	
	74FCT162374ATPVCT	O48	48-Lead (300-Mil) SSOP	
10.0	CY74FCT162374TPVC/PVCT	O48	48-Lead (300-Mil) SSOP	Industrial

Package Diagrams

48-Lead Shrunk Small Outline Package O48



48-Lead Thin Shrunk Small Outline Package Z48



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