T-52-33-05

5100
Peripheral Interface Controller

The 5100 is a high performance CMOS device that integrates a level-sensitive interrupt sharing controller, Programmable Option Select Logic, an IBM compatible timer, and glue logic into a single 144-pin flat pack. The 5100 is one of four devices in the 85000 chip set designed to provide 100% PS/2 Model 50/60 compatibility and greater flexibility in building a distinctive high performance Model 50/60 compatible system.

Features

- 100% hardware and software compatible with IBM PS/2 Model 50/60
- 100% implementation of Programmable Option Select (POS) logic
- 100% implementation of Model 50/60 compatible system control registers
- Two IBM compatible interrupt controllers
- IBM compatible system timer
- Watchdog timer logic
- System board I/O decode logic
- Peripheral device control logic
- NMI generator
- Clock generation logic for the 80287 and 8042 keyboard controller
- Supports external CMOS RAM for configuration registers
- Built-in 74LS245 compatible video buffers
- 1.5 micron high performance CMOS technology
- 144-pin PFP package

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ACC Micro 5100 Block Diagram