REVISIONS

LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
A	Technical changes to 1.4 and table I. Convert to one-part one-part number frmat. Editorial changes throughout.	91-07-01	W. K. HECKMAN
B	Add case outline "M". Technical changes to 1.3, 1.4, 1.6, and table I. Delete fault coverage requirement for classes B and S. Editorial changes throughout.	92-03-04	

THE ORIGINAL FIRST PAGE OF THIS DRAWING HAS BEEN REPLACED.

REV																			
SHEET																			
REV	B	B	B	B	B	B	B	B	B	B	B								
SHEET	15	16	17	18	19	20	21	22	23	24	25								

REV STATUS OF SHEETS	REV	B	B	B	B	B	B	B	B	B	B	B	B	B
	SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14

PMIC N/A

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DRAWING APPROVAL DATE: 90-02-01

REVISION LEVEL: B

DEFENSE ELECTRONICS SUPPLY CENTER
DAYTON, OHIO 45444

STANDARDIZED MILITARY DRAWING

THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE

AMSC N/A

MICROCIRCUITS, DIGITAL, CMOS, I/O EXPANDED MICROCONTROLLER, MONOLITHIC SILICON

SIZE	CAGE CODE	5962-89726
A	67268	

SHEET 1 OF 25

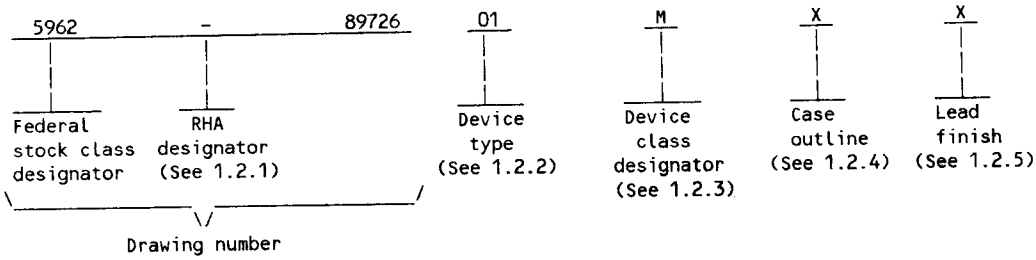
DESC FORM 193
JUL 91

5962-E403

1. SCOPE

1.1 Scope. This drawing forms a part of a one part - one part number documentation system (see 6.6 herein). Two product assurance classes consisting of military high reliability (device classes B, Q, and M) and space application (device classes S and V), and a choice of case outlines and lead finishes are available and are reflected in the Part or Identifying Number (PIN). Device class M microcircuits represent non-JAN class B microcircuits in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices". When available, a choice of radiation hardness assurance (RHA) levels are reflected in the PIN.

1.2 PIN. The PIN shall be as shown in the following example:



1.2.1 Radiation hardness assurance (RHA) designator. Device classes M, B, and S RHA marked devices shall meet the MIL-M-38510 specified RHA levels and shall be marked with the appropriate RHA designator. Device classes Q and V RHA marked devices shall meet the MIL-I-38535 specified RHA levels and shall be marked with the appropriate RHA designator. A dash (-) indicates a non-RHA device.

1.2.2 Device type(s). The device type(s) shall identify the circuit function as follows:

Device type	Generic number	Circuit function
01	80C451	CMOS I/O expanded microcontroller
02	83C451	CMOS I/O expanded microcontroller with a one time programmable EPROM.

1.2.3 Device class designator. The device class designator shall be a single letter identifying the product assurance level as follows:

Device class	Device requirements documentation
M	Vendor self-certification to the requirements for non-JAN class B microcircuits in accordance with 1.2.1 of MIL-STD-883
B or S	Certification and qualification to MIL-M-38510
Q or V	Certification and qualification to MIL-I-38535

1.2.4 Case outline(s). For device classes M, B, and S, case outline(s) shall meet the requirements in appendix C of MIL-M-38510 and as listed below. For device classes Q and V, case outline(s) shall meet the requirements of MIL-I-38535, appendix C of MIL-M-38510, and as listed below.

Outline letter	Case outline
X	D-13 (64-lead, 3.240" x 0.920" x 0.225"), dual-in-line package
U	C-7 (68-terminal, 0.962" x 0.962" x 0.120"), square chip carrier
M	C-J2 (68-terminal, 0.958" x 0.958" x 0.190"), square leaded chip carrier

1.2.5 Lead finish. The lead finish shall be as specified in MIL-M-38510 for classes M, B, and S or MIL-I-38535 for classes Q and V. Finish letter "X" shall not be marked on the microcircuit or its packaging. The "X" designation is for use in specifications when lead finishes A, B, and C are considered acceptable and interchangeable without preference.

1.3 Absolute maximum ratings. 1/

Maximum power dissipation	200 mW
Voltage range from V_{CC} to V_{SS}	-0.5 V dc to +6.5 V dc
Voltage range from any pin to V_{SS}	-0.5 V dc to V_{CC} + 0.5 V dc
Storage temperature range	-65°C to +150°C
Lead temperature (soldering, 5 seconds)	+300°C
Maximum junction temperature (T_J)	200°C
Thermal resistance, junction-to-case (Θ_{JC})	See MIL-M-38510, appendix C
Data retention for device type 02	10 years minimum

1.4 Recommended operating conditions.

Supply voltage range (V_{CC})	4.5 V dc to 5.5 V dc
Case operating temperature range (T_C)	-55°C to +125°C
Maximum low level input voltage (except EA)	0.2 V_{CC} - 0.25 V dc
Maximum low level input voltage (EA)	0.2 V_{CC} - 0.45 V dc
Minimum high level input voltage (except XTAL1, RST)	0.2 V_{CC} + 1.1 V dc
Minimum high level input voltage (XTAL1, RST)	0.7 V_{CC} dc +0.2 V dc

1.5 Logic testing for device classes Q and V.

Fault coverage measurement of manufacturing logic tests (MIL-STD-883, test method 5012)	XX percent 2/

2. APPLICABLE DOCUMENTS

2.1 Government specifications, standards, bulletin, and handbook. Unless otherwise specified, the following specifications, standards, bulletin, and handbook of the issue listed in that issue of the Department of Defense Index of Specifications and Standards specified in the solicitation, form a part of this drawing to the extent specified herein.

SPECIFICATIONS

MILITARY

MIL-M-38510 - Microcircuits, General Specification for.
MIL-I-38535 - Integrated Circuits, Manufacturing, General Specification for.

STANDARDS

MILITARY

MIL-STD-480 - Configuration Control-Engineering Changes, Deviations and Waivers.
MIL-STD-883 - Test Methods and Procedures for Microelectronics.

BULLETIN

MILITARY

MIL-BUL-103 - List of Standardized Military Drawings (SMD's).

HANDBOOK

MILITARY

MIL-HDBK-780 - Standardized Military Drawings.

1/ Stresses above the absolute maximum rating may cause permanent damage to the device. Extended operation at the maximum levels may degrade performance and affect reliability.
2/ Values will be added when they become available.

(Copies of the specifications, standards, bulletin, and handbook required by manufacturers in connection with specific acquisition functions should be obtained from the contracting activity or as directed by the contracting activity.)

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing shall take precedence.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements for device class M shall be in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices" and as specified herein. The individual item requirements for device classes B and S shall be in accordance with MIL-M-38510 and as specified herein. This is a fully characterized military detail specification and is suitable for qualification of device classes B and S to the requirements of MIL-M-38510. The individual item requirements for device classes Q and V shall be in accordance with MIL-I-38535, the device manufacturer's Quality Management (QM) plan, and as specified herein.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-M-38510 for device classes M, B, and S and MIL-I-38535 for device classes Q and V and herein.

3.2.1 Case outline(s). The case outline(s) shall be in accordance with 1.2.4 herein.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 1.

3.2.3 Block or logic diagram. The block or logic diagram shall be as specified on figure 2.

3.2.4 Radiation exposure circuit. The radiation exposure circuit shall be specified when available.

3.3 Electrical performance characteristics and postirradiation parameter limits. Unless otherwise specified herein, the electrical performance characteristics and postirradiation parameter limits are as specified in table I and shall apply over the full case operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table IIA. The electrical tests for each subgroup are defined in table I.

3.5 Marking. The part shall be marked with the PIN listed in 1.2 herein. Marking for device class M shall be in accordance with MIL-STD-883 (see 3.1 herein). In addition, the manufacturer's PIN may also be marked as listed in MIL-BUL-103. Marking for device classes B and S shall be in accordance with MIL-M-38510. Marking for device classes Q and V shall be in accordance with MIL-I-38535.

3.5.1 Certification/compliance mark. The compliance mark for device class M shall be a "C" as required in MIL-STD-883 (see 3.1 herein). The certification mark for device classes B and S shall be a "J" or "JAN" as required in MIL-M-38510. The certification mark for device classes Q and V shall be a "QML" as required in MIL-I-38535.

3.6 Certificate of compliance. For device class M, a certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-BUL-103 (see 6.7.3 herein). For device classes Q and V, a certificate of compliance shall be required from a QML-38535 listed manufacturer in order to supply to the requirements of this drawing (see 6.7.2 herein). The certificate of compliance submitted to DESC-ECC prior to listing as an approved source of supply for this drawing shall affirm that the manufacturer's product meets, for device class M the requirements of MIL-STD-883 (see 3.1 herein), or for device classes Q and V, the requirements of MIL-I-38535 and the requirements herein.

3.7 Certificate of conformance. A certificate of conformance as required for device class M in MIL-STD-883 (see 3.1 herein) or device classes B and S in MIL-M-38510 or for device classes Q and V in MIL-I-38535 shall be provided with each lot of microcircuits delivered to this drawing.

3.8 Notification of change for device class M. For device class M, notification to DESC-ECC of change of product (see 6.2 herein) involving devices acquired to this drawing is required for any change as defined in MIL-STD-480.

3.9 Verification and review for device class M. For device class M, DESC, DESC's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$, $4.5\ V \le V_{CC} \le 5.5\ V$ unless otherwise specified		Group A subgroups	Device type	Limits		Unit
						Min	Max	
Output low voltage port 1-6, AFLAG, BFLAG 1/	V_{OL}	I_{OL} = 1.6 mA	V_{CC} = 4.5 V, 5.5 V; $V_{IN} = V_{IL}$ max, V_{IH} min	1,2,3	All		0.45	V
Output low voltage Port 0, ALE, PSEN 1/	V_{OL1}	I_{OL} = 3.2 mA		1,2,3	All		0.45	V
Output high voltage ports 1-6, AFLAG, BFLAG	V_{OH}	I_{OH} = -60 µA		1,2,3	All	2.4		V
		I_{OH} = -25 µA				0.75 V_{CC}		
		I_{OH} = -10 µA				0.90 V_{CC}		
Output high voltage port 0 in external bus mode, ALE, PSEN 2/	V_{OH}	I_{OH} = -400 µA		1,2,3	All	2.4		V
		I_{OH} = -150 µA				0.75 V_{CC}		
		I_{OH} = -40 µA				0.9 V_{CC}		
Logic 0 input current, ports 1-6 AFLAG, BFLAG	I_{IL}	V_{IN} = 0.45 V, V_{CC} = 5.5 V		1,2,3	All	0.0	-75	µA
Logic 0 to 1 transition current ports 1-6, AFLAG, BFLAG	I_{TL}	V_{IN} = 2.0 V, V_{CC} = 5.5 V				0.0	-750	
Input leakage current port 0, EA, IDS, ODS	I_{LI}	$V_{IN} = V_{CC}$	V_{CC} = 4.5 V			0	10	
			V_{CC} = 5.0 V					
		V_{IN} = 0.45 V	V_{CC} = 5.5 V			0	-10	
Reset pull down resistor	R_{RST}			1,2,3	All	50	150	kΩ

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ $4.5\ V \le V_{CC} \le 5.5\ V$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Pin capacitance	C_{IO}	Test freq - 1 MHz, (see 4.4.1c)	4	All		10	pF
Power down current 3/	I_{PD}	V_{CC} = 2 V to 6 V	1,2,3	All		75	µA
Supply current operating 4/	I_{CC1}	Freq. = 3.5 MHz	1,2,3	All			mA
		V_{CC} = 4.5 V 5/				8	
		V_{CC} = 5 V 5/				10	
		V_{CC} = 5.5 V 5/				12	
		Freq. = 8 MHz					
		V_{CC} = 4.5 V 5/				13	
		V_{CC} = 5 V 5/				19	
		V_{CC} = 5.5 V 5/				21	
		Freq. = 12 MHz					
		V_{CC} = 4.5 V				20	
		V_{CC} = 5 V				25	
		V_{CC} = 5.5 V				30	
Supply current idle 6/	I_{CC2}	Freq = 3.5 MHz	1,2,3	All			mA
		V_{CC} = 4.5 V 5/				2.5	
		V_{CC} = 5 V 5/				2.5	
		V_{CC} = 5.5 V 5/				3.5	
		Freq. = 8 MHz					
		V_{CC} = 4.5 V 5/				3.0	
		V_{CC} = 5 V 5/				3.5	
		V_{CC} = 5.5 V 5/				4.5	
		Freq. = 12 MHz					
		V_{CC} = 4.5 V				3.5	
		V_{CC} = 5 V				4.0	
		V_{CC} = 5.5 V				5.0	
Functional test		See 4.4.1d, VCC = 4.5 V	7,8	All			

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ $4.5\ V \le V_{CC} \le 5.5\ V$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
AC ELECTRICAL CHARACTERISTICS							
Oscillator frequency	t_{CLCL} 1/	See figure 3 C_L = 100 pF for port 0, ALE, PSEN. C_L = 80 pF for all other outputs. V_{CC} = 4.5 V	9,10,11	All	3.5	12	MHz
ALE pulse width	t_{LHLL}		9,10,11	All	$2t_{CLCL}$ -40		ns
Address valid to ALE low	t_{AVLL}		9,10,11	All	t_{CLCL} -55		ns
Address hold after ALE low	t_{LLAX}		9,10,11	All	t_{CLCL} -35		ns
ALE low to valid instr in	t_{LLIV}		9,10,11	All		$4t_{CLCL}$ -100	ns
ALE low to $\overline{PSEN}$ low	t_{LLPL}		9,10,11	All	t_{CLCL} -40		ns
$\overline{PSEN}$ pulse width	t_{PLPH}		9,10,11	All	$3t_{CLCL}$ -45		ns
$\overline{PSEN}$ low to valid instr in	t_{PLIV}		9,10,11	All		$3t_{CLCL}$ -105	ns
Input instr hold after PSEN	t_{PXIX}		9,10,11	All	0		ns
Input instr float after PSEN	t_{PXIZ}		9,10,11	All		t_{CLCL} -25	ns
Address to valid instr in	t_{AVIV}		9,10,11	All		$5t_{CLCL}$ -105	ns
$\overline{PSEN}$ low to address float	t_{PLAZ}		9,10,11	All		25	ns
$\overline{RD}$ pulse width	t_{RLRH}		9,10,11	All	$6t_{CLCL}$ -100		ns

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$, $4.5\ V \le V_{CC} \le 5.5\ V$ unless otherwise specified	Group A subgroups	Device type	Limits Min	Limits Max	Unit
$\overline{WR}$ pulse width	t_{WLWH}	See figure 3 C_L = 100 pF for port 0, ALE, $\overline{PSEN}$. C_L = 80 pF for all other outputs. V_{CC} = 4.5 V	9,10,11	All	$6t_{CLCL}$ -100		ns
$\overline{RD}$ low to valid data in	t_{RLDV}		9,10,11	All		$5t_{CLCL}$ -165	ns
Data hold after $\overline{RD}$	t_{RHDX}		9,10,11	All	0		ns
Data float after $\overline{RD}$	t_{RHDZ}		9,10,11	All		$2t_{CLCL}$ -70	ns
ALE low to valid data in	t_{LLDV}		9,10,11	All		$8t_{CLCL}$ -150	ns
Address to valid data in	t_{AVDV}		9,10,11	All		$9t_{CLCL}$ -165	ns
ALE low to $\overline{RD}$ or or $\overline{WR}$ low	t_{LLWL}		9,10,11	All	$3t_{CLCL}$ -50	$3t_{CLCL}$ +50	ns
Data valid to $\overline{WR}$ transition	t_{QVWX}		9,10,11	All	t_{CLCL} -60		
Data hold after $\overline{WR}$	t_{WHQX}		9,10,11	All	t_{CLCL} -50		ns
$\overline{RD}$ low to address float	t_{RLAZ}		9,10,11	All		0	ns
$\overline{RD}$ or $\overline{WR}$ high to ALE high	t_{WHLH}		9,10,11	All	t_{CLCL} -40	t_{CLCL} +40	ns

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ $4.5\ V \le V_{CC} \le 5.5\ V$ unless otherwise specified	Group A sub-groups	Device type	Limits Min	Limits Max	Unit
$\overline{IDS}$ width	t_{ILIH}	C_L = 100 pF for port 0, ALE, $\overline{PSEN}$. C_L = 80 pF for all other outputs. See figure 3. Port 6 input (input rise and fall times 5 ns). V_{CC} =4.5 V	9,10,11	All	$3t_{CLCL}$ +20		ns
Data setup to $\overline{IDS}$ high	t_{DVIH}				10		
Data hold after $\overline{IDS}$	t_{IHDX}				30		
PE to $\overline{IDS}$	t_{FLIL}				25		
$\overline{IDS}$ to IBF(BFLAG) delay	t_{IVFV}					130	
$\overline{ODS}$ width	t_{OLOH}	C_L = 100 pF for port 0, ALE, $\overline{PSEN}$. C_L = 80 pF for all other outputs. See figure 3. Port 6 output. V_{CC} = 4.5 V	9,10,11	All	$3t_{CLCL}$ +20		ns
SEL to data out delay	t_{FVDV}					85	
$\overline{ODS}$ to data out delay	t_{OLDV}					80	
$\overline{ODS}$ to data float delay	t_{OHDZ}					35	ns
$\overline{ODS}$ to OBF(AFLAG) delay	t_{OVFD}					100	
PE(BFLAG) to data out delay	t_{FLDV}					120	
$\overline{ODS}$ high to SEL (AFLAG) delay	t_{OHFH}				100		

1/ Capacitive loading on ports 0 and 2 can cause spurious noise to be superimposed on the V_{OLS} of ALE and ports 1 and 3. The noise is caused by external bus capacitance discharging into port 0 and port 2 pins when these pins make 1-to-0 transitions during bus operations in the worst cases it could be desirable to qualify ALE with a Schmitt trigger, or use an address latch with a Schmitt trigger STROBE input.

2/ Capacitive loading on ports 0 and 2 can cause the V_{OH} on ALE and PSEN to momentarily fall before the 0.9 V_{CC} specification when the address bits are stabilizing.

3/ I_{PD} is measured with all output pins disconnected; EA = port 0 = V_{CC}; XTAL2 = NC; RST = V_{SS}; V_{CC} = 2 V to 6 V is allowed for power down current test.

4/ I_{CC1} is measured with all output pins disconnected; XTAL1 driven with $t_{CLCH} = t_{CHCL}$ = 5 ns, $V_{IL} = V_{SS}$ + 0.5 V, $V_{IH} = V_{CC}$ - 0.5 V; XTAL1 = NC; EA = RST = port 0 = V_{CC}. I_{CC} will be slightly higher if a crystal oscillator is used.

5/ This parameter is guaranteed, if not tested, to the limits specified.

6/ Idle I_{CC2} is measured with all output pins disconnected; XTAL1 driven with t_{CLCH}, t_{CHCL} = 5 ns, $V_{IL} = V_{SS}$ + 0.5 V, $V_{IH} = V_{CC}$ - 0.5 V; XTAL = NC; port 0 = V_{CC}; EA = RST = V_{SS}.

Device types	01 and 02	
Case outlines	X	M and U
Terminal number	Terminal symbol	Terminal symbol
1	$\overline{EA}$	$\overline{EA}$
2	P2.0/A8	P2.0/A8
3	P2.1/A9	P2.1/A9
4	P2.2/A10	P2.2/A10
5	P2.3/A11	P2.3/A11
6	P2.4/A12	P2.4/A12
7	P2.5/A13	P2.5/A13
8	P2.6/A14	P2.6/A14
9	P2.7/A15	P2.7/A15
10	P0.7/AD7	P0.7/AD7
11	P0.6/AD6	P0.6/AD6
12	P0.5/AD5	P0.5/AD5
13	P0.4/AD4	P0.4/AD4
14	P0.3/AD3	P0.3/AD3
15	P0.2/AD2	P0.2/AD2
16	P0.1/AD1	P0.1/AD1
17	P0.0/AD0	P0.0/AD0
18	V_{CC}	V_{CC}
19	P4.3	P4.7
20	P4.2	P4.6
21	P4.1	P4.5
22	P4.0	P4.4
23	P1.0	P4.3
24	P1.1	P4.2
25	P1.2	P4.1
26	P1.3	P4.0
27	P1.4	P1.0
28	P1.5	P1.1
29	P1.6	P1.2
30	P1.7	P1.3
31	RST	P1.4
32	P3.0/RxD	P1.5
33	P3.1/$\underline{TxD}$	P1.6
34	P3.2/INT0	P1.7

Device types	01 and 02	
Case outlines	X	M and U
Terminal number	Terminal symbol	Terminal symbol
35	P3.3/$\overline{INT1}$	RST
36	P3.4/T0	P3.0/RxD
37	P3.5/$\underline{T1}$	P3.1/$\underline{TxD}$
38	P3.6/$\underline{WR}$	P3.2/$\underline{INT0}$
39	P3.7/$\overline{RD}$	P3.3/INT1
40	P5.0	P3.4/T0
41	P5.1	P3.5/$\underline{T1}$
42	P5.2	P3.6/$\underline{WR}$
43	P5.3	P3.7/$\overline{RD}$
44	P5.4	P5.0
45	P5.5	P5.1
46	P5.6	P5.2
47	P5.7	P5.3
48	XAL2	P5.4
49	XAL1	P5.5
50	V_{SS}	P5.6
51	$\underline{ODS}$	P5.7
52	IDS	XAL2
53	BFLAG	XAL1
54	AFLAG	V_{SS}
55	P6.0	$\underline{ODS}$
56	P6.1	IDS
57	P6.2	BFLAG
58	P6.3	AFLAG
59	P6.4	P6.0
60	P6.5	P6.1
61	P6.6	P6.2
62	$\underline{P6.7}$	P6.3
63	PSEN	P6.4
64	ALE	P6.5
65	---	P6.6
66	---	$\underline{P6.7}$
67	---	PSEN
68	---	ALE

FIGURE 1. Terminal connections.

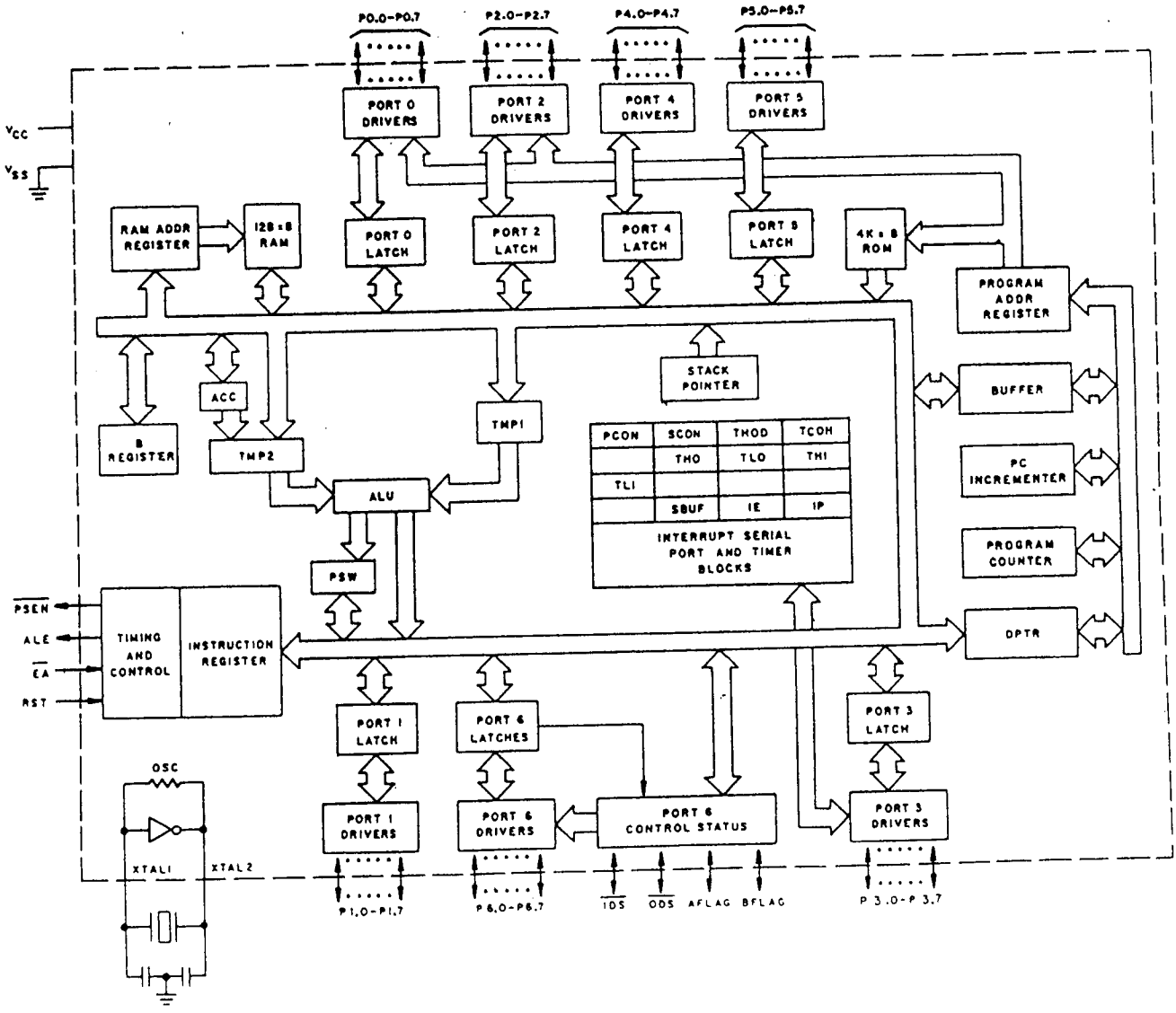
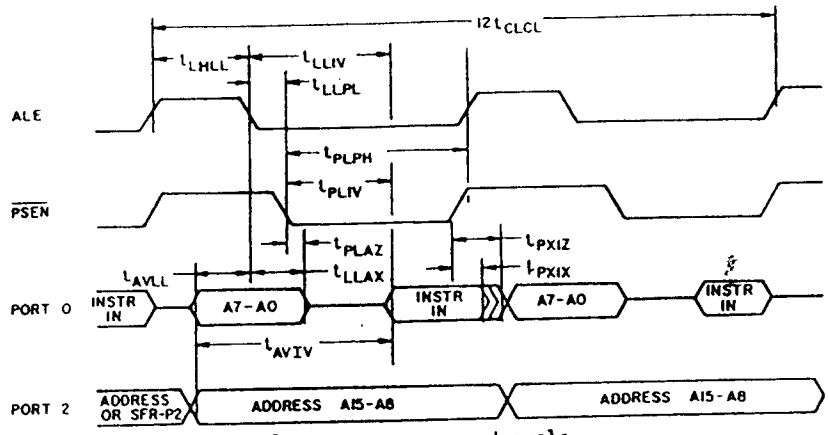
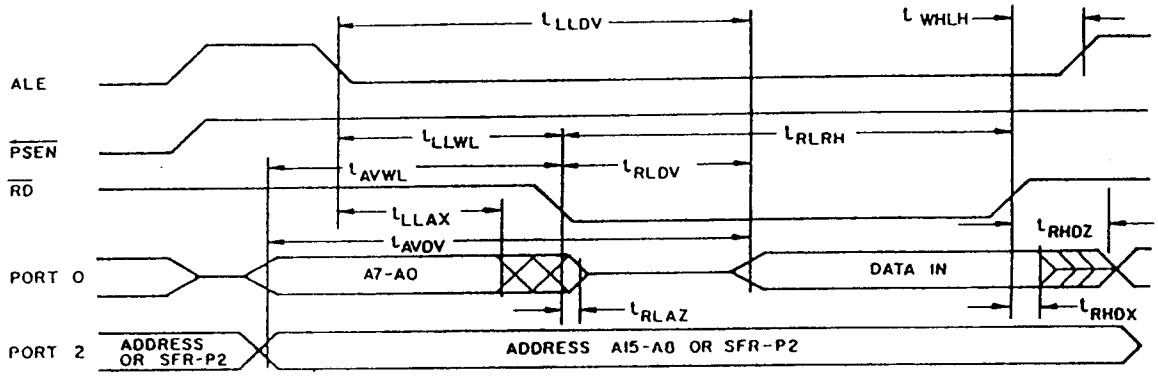


FIGURE 2. Block diagram.

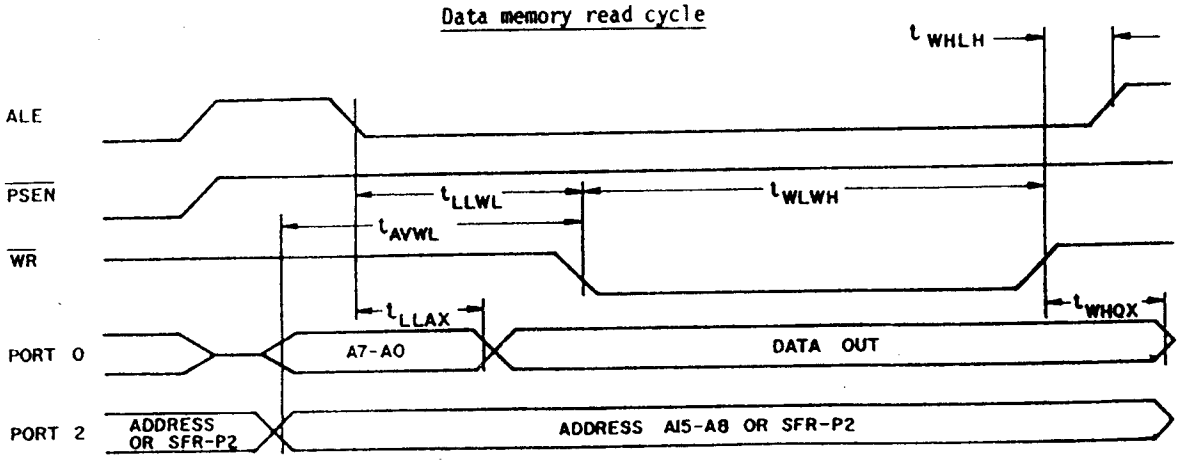
STANDARDIZED MILITARY DRAWING DEFENSE ELECTRONICS SUPPLY CENTER DAYTON, OHIO 45444	SIZE A		5962-89726
		REVISION LEVEL B	SHEET 11



Program memory read cycle

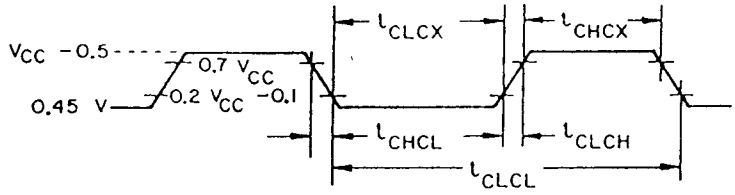


Data memory read cycle

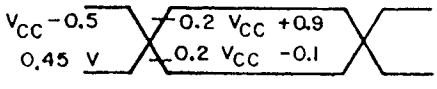


Data memory write cycle

FIGURE 3. Switching waveforms and test circuit.

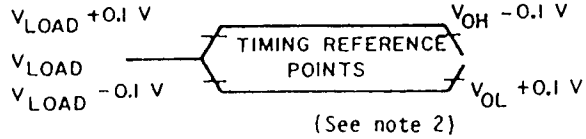


External clock drive waveform



(See note 1)

AC testing input, output waveforms

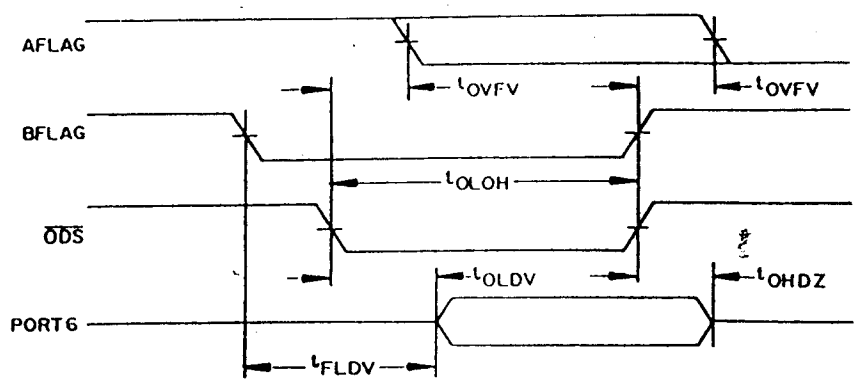


(See note 2)

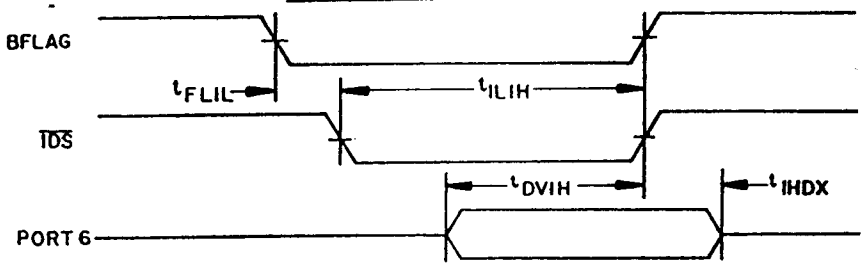
Float waveforms

NOTES:
1. AC inputs during testing are driven at V_{CC} -0.5 V for a logic "1" and 0.45 V for a logic "0". Timing measurements are made at V_{IH} minimum for a logic "1" and V_{IL} maximum for a logic "0".
2. For timing purposes, a port pin is no longer floating when a 100 mV change from load voltage occurs, and begins to float when a 100 mV change from the loaded V_{OH}/V_{OL} level occurs. $I_{OL}/I_{O\,H} > \pm 20$ mA.
3. External clock: $t_{CHCL} = t_{CLCH} = 5$ ns.

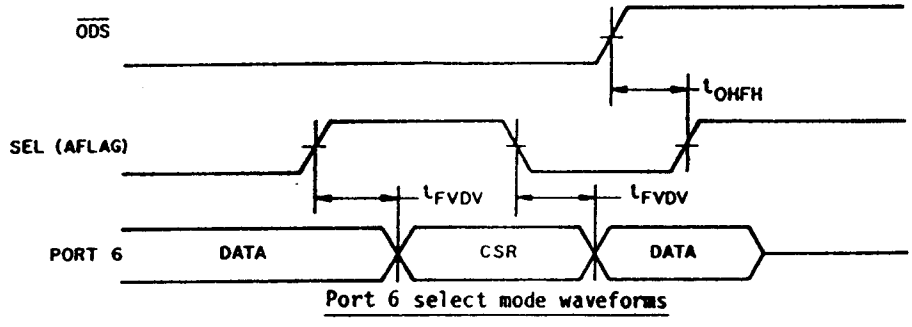
FIGURE 3. Switching waveforms and test circuit - Continued.



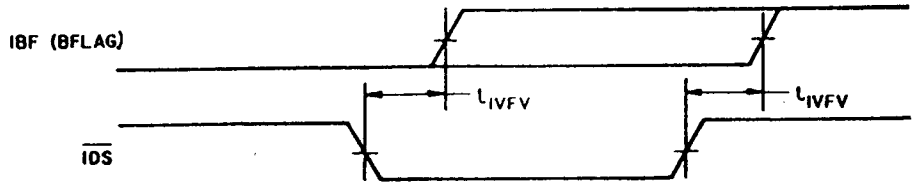
Port 6 output waveforms



Port 6 input waveforms



Port 6 select mode waveforms



IBF flag output waveforms

FIGURE 3. Switching waveforms and test circuit - Continued.

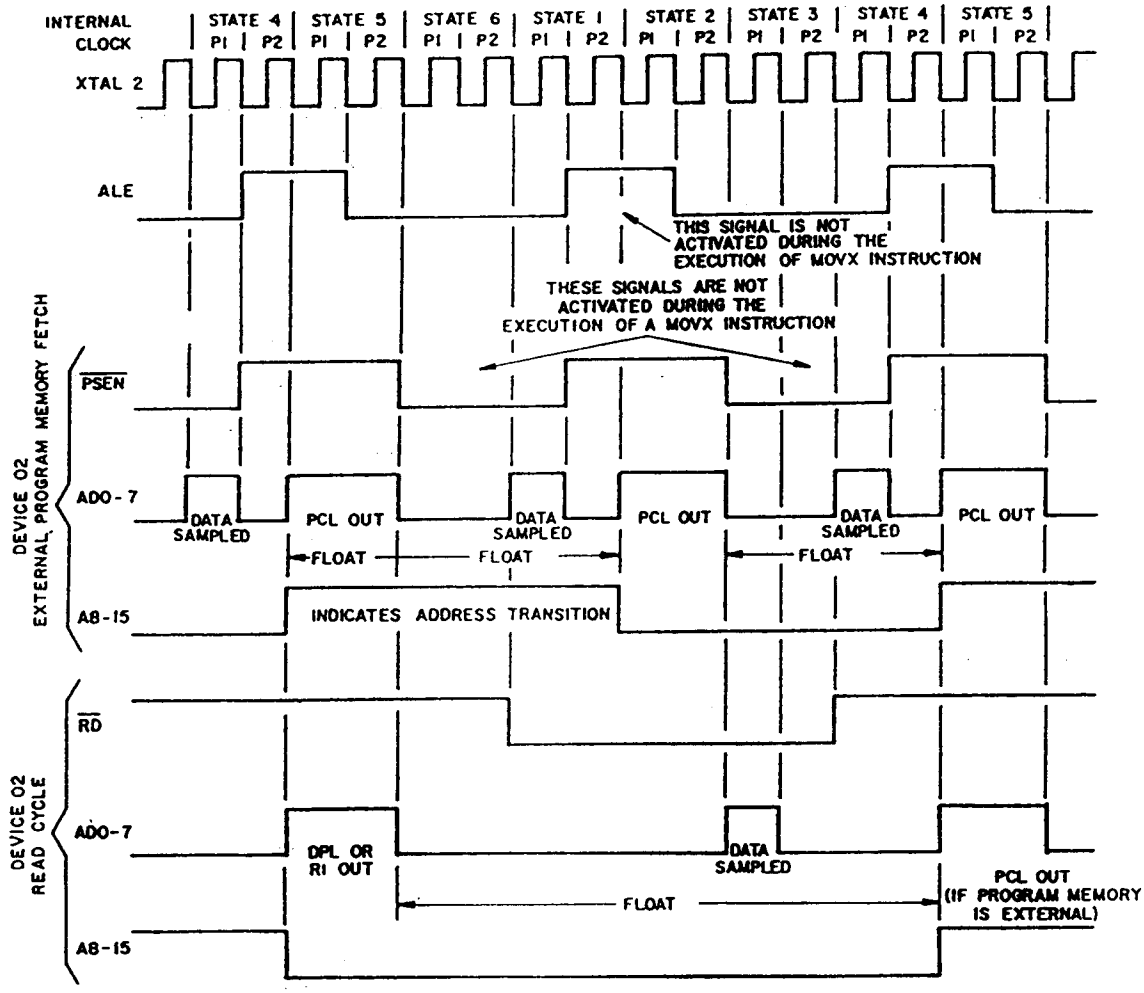
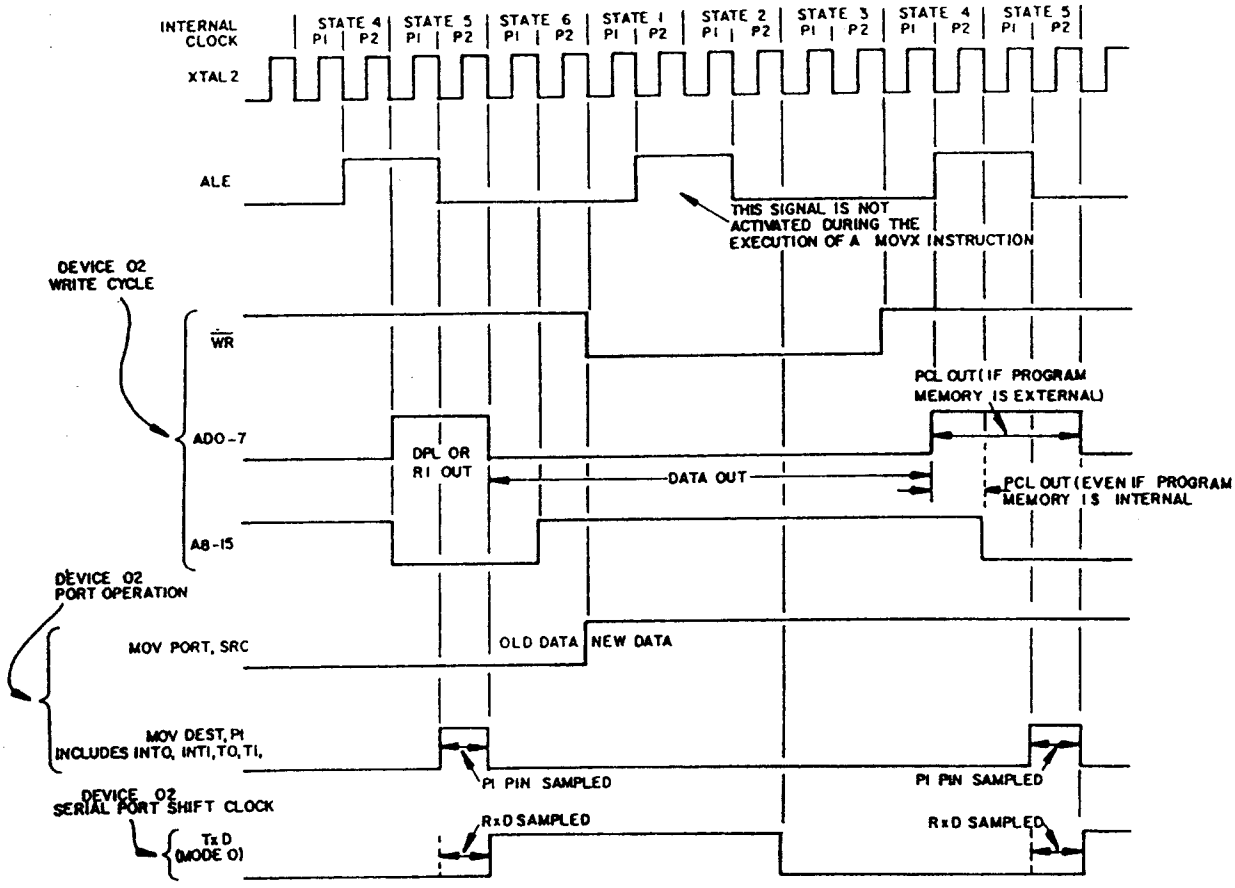
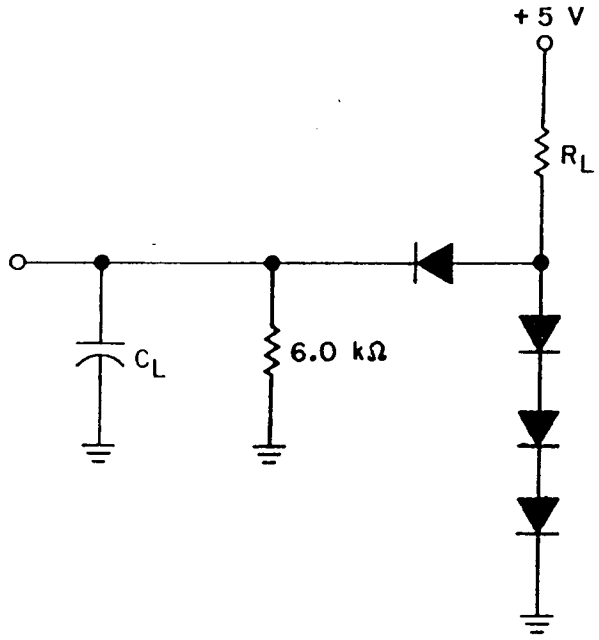


FIGURE 3. Switching waveforms and test circuit - Continued.



NOTE: This diagram indicates when signals are clocked internally, however, the time it takes the signals to propagate to the pin range from 25 ns to 125 ns. This propagation delay is dependent on variables such as temperature and pin loading. Propagation also varies from output to output and component to component. Typically (T_A = 25°C fully loaded), RD and WR propagation delays are approximately 50 ns; propagation delays for other signals are approximately 85 ns. These timing delays are incorporated in the ac specifications.

FIGURE 3. Switching waveforms and test circuit - Continued.



Output	R_L	C_L
Port 0, ALE, PSEN	1.2 kΩ	100 pF
All other outputs	2.4 kΩ	80 pF

TEST CIRCUIT

NOTES:
1. All diodes are IN914 or equivalent.
2. C_L includes tester and fixture capacitance.

FIGURE 3. Switching waveforms and test circuit - Continued.

3.10 Microcircuit group assignment for device classes M, B, and S. Device classes M, B, and S devices covered by this drawing shall be in microcircuit group number 105 (see MIL-M-38510, appendix E).

3.11 Serialization for device class S. All device class S devices shall be serialized in accordance with MIL-M-38510.

3.12 PIN supersession information. The PIN supersession information shall be as specified in appendix A.

4. QUALITY ASSURANCE PROVISIONS

4.1 Sampling and inspection. For device class M, sampling and inspection procedures shall be in accordance with section 4 of MIL-M-38510 to the extent specified in MIL-STD-883 (see 3.1 herein). For device classes B and S, sampling and inspection procedures shall be in accordance with MIL-M-38510 and method 5005 of MIL-STD-883, except as modified herein. For device classes Q and V, sampling and inspection procedures shall be in accordance with MIL-I-38535 and the device manufacturer's QM plan.

4.2 Screening. For device class M, screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection. For device classes B and S, screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to qualification and quality conformance inspection. For device classes Q and V, screening shall be in accordance with MIL-I-38535, and shall be conducted on all devices prior to qualification and technology conformance inspection.

4.2.1 Additional criteria for device classes M, B, and S.

a. Burn-in test, method 1015 of MIL-STD-883.

(1) Test condition A, B, C, or D. For device class M, the test circuit shall be submitted to DESC-ECC for review with the certificate of compliance. For device classes B and S, the test circuit shall be submitted to the qualifying activity.

(2) T_A = +125°C, minimum.

b. Interim and final electrical test parameters shall be as specified in table IIA herein.

c. For device 02, all devices shall be mask programmed to the requirements of the altered item drawing prior to the initiation of any testing.

4.2.2 Additional criteria for device classes Q and V.

a. The burn-in test duration, test condition and test temperature or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-I-38535. The burn-in test circuit shall be submitted to DESC-ECC with the certificate of compliance and shall be under the control of the device manufacturer's Technology Review Board (TRB) in accordance with MIL-I-38535.

b. Interim and final electrical test parameters shall be as specified in table IIA herein.

c. Additional screening for device class V beyond the requirements of device class Q shall be as specified in appendix B of MIL-I-38535 and as detailed in table IIB herein.

4.3 Qualification inspection.

4.3.1 Qualification inspection for device classes B and S. Qualification inspection for device classes B and S shall be in accordance with MIL-M-38510. Inspections to be performed shall be those specified in method 5005 of MIL-STD-883 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.5).

4.3.2 Qualification inspection for device classes Q and V. Qualification inspection for device classes Q and V shall be in accordance with MIL-I-38535. Inspections to be performed shall be those specified in MIL-I-38535 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.5).

4.4 Conformance inspection. Quality conformance inspection for device class M shall be in accordance with MIL-STD-883 (see 3.1 herein) and as specified herein. Quality conformance inspection for device classes B and S shall be in accordance with MIL-M-38510 and as specified herein. Inspections to be performed for device classes M, B, and S shall be those specified in method 5005 of MIL-STD-883 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.5). Technology conformance inspection for classes Q and V shall be in accordance with MIL-I-38535 including groups A, B, C, D, and E inspections and as specified herein except where option 2 of MIL-I-38535 permits alternate in-line control testing.

4.4.1 Group A inspection.

a. Tests shall be as specified in table IIA herein.

b. Subgroups 5 and 6 in table I, method 5005 of MIL-STD-883 shall be omitted.

c. Subgroup 4 (C_{IO} measurement) shall be measured only for the intial test and after process or design changes which may affect capacitance. A minimum sample size of 5 devices with zero rejects shall be required.

d. For device class M, subgroups 7 and 8 tests shall include verification of the device functionality. These tests shall be maintained and availble from the approved source of supply upon request. For device classes B and S, subgroups 7 and 8 tests shall include verification of the device functionality as approved by the qualifying activity. For device classes Q and V, subgroups 7 and 8 shall include verifying the functionality of the device; these tests shall have been fault graded in accordance with MIL-STD-883, test method 5012 (see 1.5 herein).

TABLE IIA. Electrical test requirements.

Test requirements	Subgroups (per method 5005, table I)			Subgroups (per MIL-I-38535, table III)	
	Device class M	Device class B	Device class S	Device class Q	Device class V
Interim electrical parameters (see 4.2)	---	---	1,7,9	---	1,7,9
Final electrical parameters (see 4.2)	1,2,3,7, 1/ 8,9,10,11	1,2,3,7, 2/ 8,9,10,11	1,2,3,7, 2/ 8,9,10,11	1,2,3,7 1/ 8,9,10,11	1,2,3,7, 1/ 8,9,10,11
Group A test requirements (see 4.4)	1,2,3,4,7 8,9,10,11	1,2,3,4,7 8,9,10,11	1,2,3,4,7 8,9,10,11	1,2,3,4,7 8,9,10,11	1,2,3,4,7 8,9,10,11
Group B end-point electrical parameters (see 4.4)	---	---	2,8A,10	---	2,8A,10
Group C end-point electrical parameters (see 4.4)	2,8A,10	2,8A,10	---	2,8A,10	---
Group D end-point electrical parameters (see 4.4)	2,8A,10	2,8A,10	2,8A,10	2,8A,10	2,8A,10
Group E end-point electrical parameters (see 4.4)	1,7,9	1,7,9	1,7,9	1,7,9	1,7,9

1/ PDA applies to subgroup 1.
2/ PDA aoplies to subgroups 1 and 7.

4.4.2 Group B inspection. The group B inspection end-point electrical parameters shall be as specified in table IIA herein.

4.4.3 Group C inspection. The group C inspection end-point electrical parameters shall be as specified in table IIA herein.

4.4.3.1 Additional criteria for device classes M, B, and S. Steady-state life test conditions, method 1005 of MIL-STD-883:

a. Test condition A, B, C, or D. For device class M, the test circuit shall be submitted to DESC-ECC for review with the certificate of compliance. For device classes B and S, the test circuit shall be submitted to the qualifying activity.

b. T_A = +125°C, minimum.

c. Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

4.4.3.2 Additional criteria for device classes Q and V. The steady-state life test duration, test condition and test temperature or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-I-38535. The steady-state life test circuit shall be submitted to DESC-ECC with the certificate of compliance and shall be under the control of the device manufacturer's TRB in accordance with MIL-I-38535.

TABLE IIB. Additional screening for device class V.

Test	MIL-STD-883, test method	Lot requirement
Particle impact noise detection	2020	100%
Internal visual	2010, condition A or approved alternate	100%
Nondestructive bond pull	2023 or approved alternate	100%
Reverse bias burn-in	1015	100%
Burn-in	1015, total of 240 hours at +125°C	100%
Radiographic	2012	100%

4.4.4 Group D inspection. The group D inspection end-point electrical parameters shall be as specified in table IIA herein.

4.4.5 Group E inspection. Group E inspection is required only for parts intended to be marked as radiation hardness assured (see 3.5 herein). RHA levels for device classes B, S, Q, and V shall be M, D, R, and H and for device class M shall be M and D. RHA quality conformance inspection sample tests shall be performed at the RHA level specified in the acquisition document.

a. RHA tests for device classes B and S for levels M, D, R, and H or for device class M for levels M and D shall be performed through each level to determine at what levels the devices meet the RHA requirements. These RHA tests shall be performed for initial qualification and after design or process changes which may affect the RHA performance of the device.

b. End-point electrical parameters shall be as specified in table IIA herein.

c. Prior to total dose irradiation, each selected sample shall be assembled in its qualified package. It shall pass the specified group A electrical parameters in table I for subgroups specified in table IIA herein.

d. For device classes M, B, and S, the devices shall be subjected to radiation hardness assured tests as specified in MIL-M-38510 for RHA level being tested, and meet the postirradiation end-point electrical parameter limits as defined in table I at T_A = +25°C ±5 percent, after exposure.

e. Prior to and during total dose irradiation testing, the devices shall be biased to establish a worst case condition as specified in the radiation exposure circuit.

f. For device classes M, B, and S, subgroups 1 and 2 in table V, method 5005 of MIL-STD-883 shall be tested as appropriate for device construction.

g. When specified in the purchase order or contract, a copy of the RHA delta limits shall be supplied.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-M-38510 for device classes M, B, and S and MIL-I-38535 for device classes Q and V.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.1.1 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.1.2 Substitutability. Device classes B and Q devices will replace device class M devices.

6.2 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished in accordance with MIL-STD-481 using DD Form 1693, Engineering Change Proposal (Short Form).

6.3 Record of users. Military and industrial users shall inform Defense Electronics Supply Center when a system application requires configuration control and which SMD's are applicable to that system. DESC will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronic devices (FSC 5962) should contact DESC-ECC, telephone (513) 296-6022.

6.4 Comments. Comments on this drawing should be directed to DESC-ECC, Dayton, Ohio 45444, or telephone (513) 296-8526.

6.5 Symbols, definitions, and functional descriptions.

Mnemonic	Type	Name and function
V_{SS}		GROUND: 0 V reference
V_{CC}		Power supply: + 5 V
P0.0-P0.7	I/O	Port 0: An 8-bit open drain, bidirectional I/O port. Port 0 is also the multiplexed low-order address and data bus during accesses to external memory and outputs instruction bytes during program verification. External pull-ups are required during program verification. Port 0 can sink/source eight LS TTL inputs.
P1.0-P1.7	I/O	Port 1. Port 1 is an 8-bit bidirectional I/O port with internal pullups. Port 1 receives the low-order address bytes during program verification. In device 02, port 1 can sink/source three LS TTL inputs, and drive CMOS inputs without external pull-ups.
P2.0-P2.7	I/O	Port 2: An 8-bit bidirectional I/O port with internal pull-ups. Port 2 emits the high-order address bytes during accesses to external memory and receives the high-order address bits and control signals during program verification in device 02. Port 2 can sin/source three LS TTL inputs and drive CMOS inputs without external pull-ups.
P3.0-P3.7	I/O	Port 3: An 8-bit bidirectional I/O port with internal pull-ups. Port 3 can sink/source three LS TTL inputs and drive CMOS input without external pull-ups. Port 3 also serves the device 02 special functions listed as follows:
	I	P3.0 RXD (serial input port)
	O	P3.1 TXD (Serial input port)
	I	P3.2 INTO (external interrupt 0)
	I	P3.3 INT1 (external interrupt 1)
	I	P3.4 TO (Timer 0 external input)
	I	P3.5 T1 (Timer 1 external input)
	O	P3.6 WR (external data memory with write strobe)
	O	P3.7 RD (external data memory read strobe)
P4.0-P4.3	I/O	Port 4: A 4 or 8-bit bidirectional
P4.0-P4.7	I/O	port with internal pull-ups. Port 4 can sink/source three LS TTL inputs and drive CMOS inputs without external pull-ups.
P5.0-P5.7	I/O	Port 5: An 8-bit I/O port with internal pull-ups. Port 5 can sink/source three LS TTL inputs and drive CMOS inputs without external pull-ups.
P6.0-6.7	I/O	Port 6: A specialized 8-bit bidirectional I/O port with internal pull-ups. This special port can sink/source three LS TTL inputs and drive CMOS inputs without external pull-ups. Port 6 can be used in strobed or nonstrobed mode of operation and in conjunction with four control pins that serve the functions listed below.
		Port 6 control lines:
$\overline{ODS}$	I	$\overline{ODS}$: Output data strobe
IDS	I	IDS: Input data strobe
BFLAG	I/O	BFLAG: A bidirectional I/O pin with internal pull-ups.
AFLAG	I/O	AFLAG: A bidirectional I/O pin with internal pull-ups.

Mnemonic	Type	Name and function
RST	I	Reset: A high level on this pin for two machine cycles while the oscillator is running resets the device. An internal pull-down resistor permits power-on reset using only a capacitor connected to the V_{CC}.
ALE	O	Address latch enable: An output for latching the low byte of the address during accesses to external memory. ALE is activated at a constant rate of 1/6 the oscillator frequency except during an external data memory access, at which time one ALE is skipped. ALE can sink/source eight LS TTL inputs and drive CMOS inputs without an external pull-up.
$\overline{\text{PSEN}}$	O	Program store enable: This output is the read strobe to external program memory, PSEN is activated twice each machine cycle during fetches from external program memory; however, when executing out of external program memory, two activations of PSEN are skipped during each access to external data memory, PSEN is not activated during fetches from internal program memory, PSEN can sink/source eight LS TTL inputs and drive CMOS/COMOS inputs without an external pull-up.
$\overline{\text{EA}}$	I	Instruction execution control: When $\overline{\text{EA}}$ is held high, the CPU executes out of internal program memory, unless the program counter exceeds 0FFH. When $\overline{\text{EA}}$ is held low, the CPU executes out of external program memory. $\overline{\text{EA}}$ must never be allowed to float.
XTAL1	I	Crystal 1: An input to the inverting amplifier that forms the oscillator. This input receives the external oscillator when an external oscillator is used.
XTAL2	O	Crystal 2: An output of the inverting amplifier that forms the oscillator. This pin should be floated when an external oscillator is used.

6.6 One part - one part number system. The one part - one part number system described below has been developed to allow for transitions between identical generic devices covered by the four major microcircuit requirements documents (MIL-M-38510, MIL-H-38534, MIL-I-38535, and 1.2.1 of MIL-STD-883) without the necessity for the generation of unique PIN's. The four military requirements documents represent different class levels, and previously when a device manufacturer upgraded military product from one class level to another, the benefits of the upgraded product were unavailable to the Original Equipment Manufacturer (OEM), that was contractually locked into the original unique PIN. By establishing a one part number system covering all four documents, the OEM can acquire to the highest class level available for a given generic device to meet system needs without modifying the original contract parts selection criteria.

Military documentation format	Example PIN under new system	Manufacturing source listing	Document listing
New MIL-M-38510 Military Detail Specifications (in the SMD format)	5962-XXXXXZZ(B or S)YY	QPL-38510 (Part 1 or 2)	MIL-BUL-103
New MIL-H-38534 Standardized Military Drawings	5962-XXXXXZZ(H or K)YY	QML-38534	MIL-BUL-103
New MIL-I-38535 Standardized Military Drawings	5962-XXXXXZZ(Q or V)YY	QML-38535	MIL-BUL-103
New 1.2.1 of MIL-STD-883 Standardized Military Drawings	5962-XXXXXZZ(M)YY	MIL-BUL-103	MIL-BUL-103

6.7 Sources of supply.

6.7.1 Sources of supply for device classes B and S. Sources of supply for device classes B and S are listed in QPL-38510.

6.7.2 Sources of supply for device classes Q and V. Sources of supply for device classes Q and V are listed in QML-38535. The vendors listed in QML-38535 have submitted a certificate of compliance (see 3.6 herein) to DESC-ECC and have agreed to this drawing.

6.7.3 Approved sources of supply for device class M. Approved sources of supply for class M are listed in MIL-BUL-103. The vendors listed in MIL-BUL-103 have agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to and accepted by DESC-ECC.

APPENDIX A

PIN SUPERSESSION INFORMATION

10. SCOPE

10.1 Scope. This appendix contains the PIN supersession information to support the one part-one part number system. For new system designs, after the date of this document the NEW PIN shall be used in lieu of the OLD PIN. For existing system designs prior to the date of this document the NEW PIN can be used in lieu of the OLD PIN. This is a mandatory part of the specification. The information contained herein is intended for compliance. The PIN supersession data shall be as follows:

20. APPLICABLE DOCUMENTS This section is not applicable to this appendix.

30. SUPERSESSION DATA

NEW PIN	OLD PIN
5962-8972601MXX	5962-8972601XX
5962-8972601MUX	5962-8972601UX
5962-8972602MXX	5962-8972602XX
5962-8972602MUX	5962-8972602UX