

18-bit universal bus transceiver (3-State)

74ABT16500C
74ABTH16500C

FEATURES

- 18-bit bidirectional bus interface
- 3-State buffers
- 74ABTH16500C incorporates bus-hold data inputs which eliminate the need for external pull-up resistors to hold unused inputs
- Output capability: +64mA/-32mA
- TTL input and output switching levels
- Live insertion/extraction permitted
- Power-up reset
- Power-up 3-State
- Negative edge-triggered clock inputs
- Latch-up protection exceeds 500mA per JEDEC Std 17
- ESD protection exceeds 2000V per MIL STD 883 Method 3015 and 200V per Machine Model
- Flexible operation permits 18 embedded D-type latches or flip-flops to operate in clocked, transparent, or latched modes.

DESCRIPTION

The 74ABT16500C is a high-performance BiCMOS Device which combines low static and dynamic power dissipation with high speed and high output drive.

This device is an 18-bit universal transceiver featuring non-inverting 3-State bus compatible outputs in both send and receive directions. Data flow in each direction is controlled by output enable ($\overline{\text{OEAB}}$ and $\overline{\text{OEBA}}$), latch enable ($\overline{\text{LEAB}}$ and $\overline{\text{LEBA}}$), and clock ($\overline{\text{CPAB}}$ and $\overline{\text{CPBA}}$) inputs. For A-to-B data flow, the device operates in the transparent mode when $\overline{\text{LEAB}}$ is High. When $\overline{\text{LEAB}}$ is Low, the A data is latched if $\overline{\text{CPAB}}$ is held at a High or Low logic level. If $\overline{\text{LEAB}}$ is Low, the A-bus data is stored in the latch/flip-flop on the High-to-Low transition of $\overline{\text{CPAB}}$. When $\overline{\text{OEAB}}$ is High, the outputs are active. When $\overline{\text{OEAB}}$ is Low, the outputs are in the high-impedance state.

Data flow for B-to-A is similar to that of A-to-B but uses $\overline{\text{OEBA}}$, $\overline{\text{LEBA}}$ and $\overline{\text{CPBA}}$. The output enables are complimentary ($\overline{\text{OEAB}}$ is active High, and $\overline{\text{OEBA}}$ is active Low).

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

Two options are available, 74ABT16500C which does not have the bus-hold feature and 74ABTH16500C which incorporates the bus-hold feature.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS $T_{\text{amb}} = 25^{\circ}\text{C}$; $\text{GND} = 0\text{V}$	TYPICAL	UNIT
t_{PLH} t_{PHL}	Propagation delay An to Bn or Bn to An	$C_L = 50\text{pF}$; $V_{\text{CC}} = 5\text{V}$	2.1 1.7	ns
C_{IN}	Input capacitance (Control pins)	$V_I = 0\text{V}$ or V_{CC}	3	pF
$C_{\text{I/O}}$	I/O pin capacitance	Outputs disabled; $V_{\text{I/O}} = 0\text{V}$ or V_{CC}	7	pF
I_{CCZ}	Quiescent supply current	Outputs disabled; $V_{\text{CC}} = 5.5\text{V}$	500	μA
I_{CCL}		Outputs low; $V_{\text{CC}} = 5.5\text{V}$	8	mA

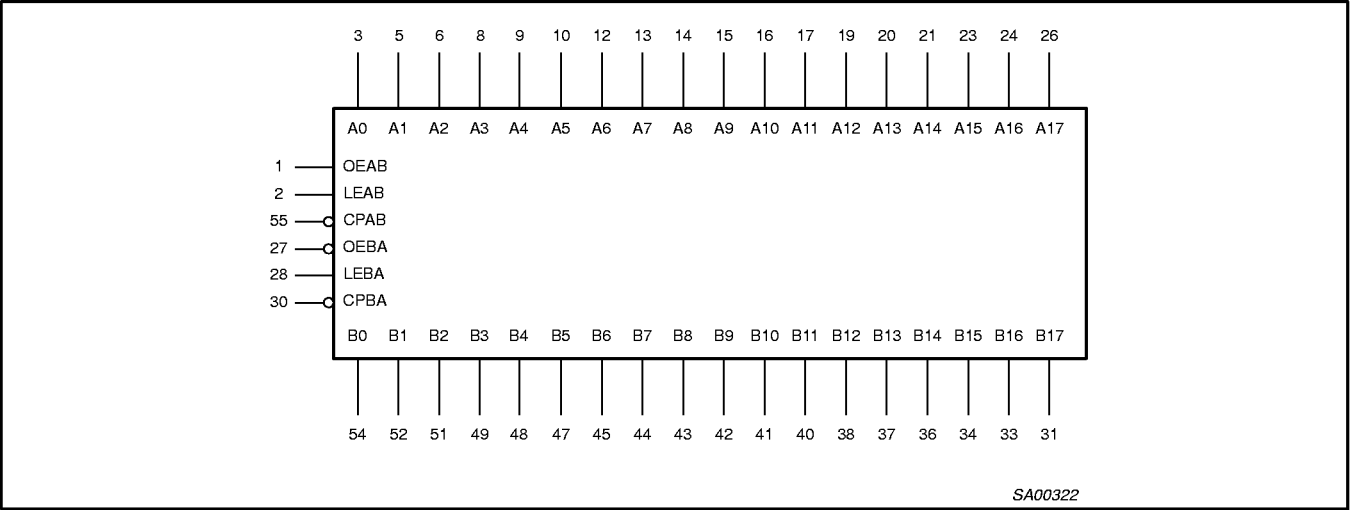
ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	OUTSIDE NORTH AMERICA	NORTH AMERICA	DWG NUMBER
56-Pin Plastic SSOP Type III	-40°C to $+85^{\circ}\text{C}$	74ABT16500C DL	BT16500C DL	SOT371-1
56-Pin Plastic TSSOP Type II	-40°C to $+85^{\circ}\text{C}$	74ABT16500C DGG	BT16500C DGG	SOT364-1
56-Pin Plastic SSOP Type III	-40°C to $+85^{\circ}\text{C}$	74ABTH16500C DL	BH16500C DL	SOT371-1
56-Pin Plastic TSSOP Type II	-40°C to $+85^{\circ}\text{C}$	74ABTH16500C DGG	BH16500C DGG	SOT364-1

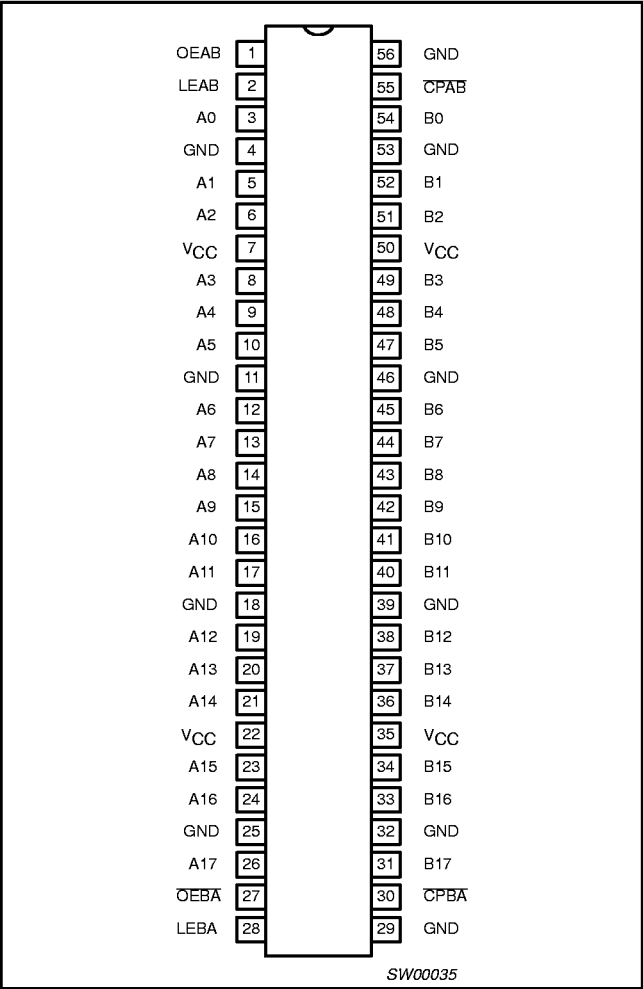
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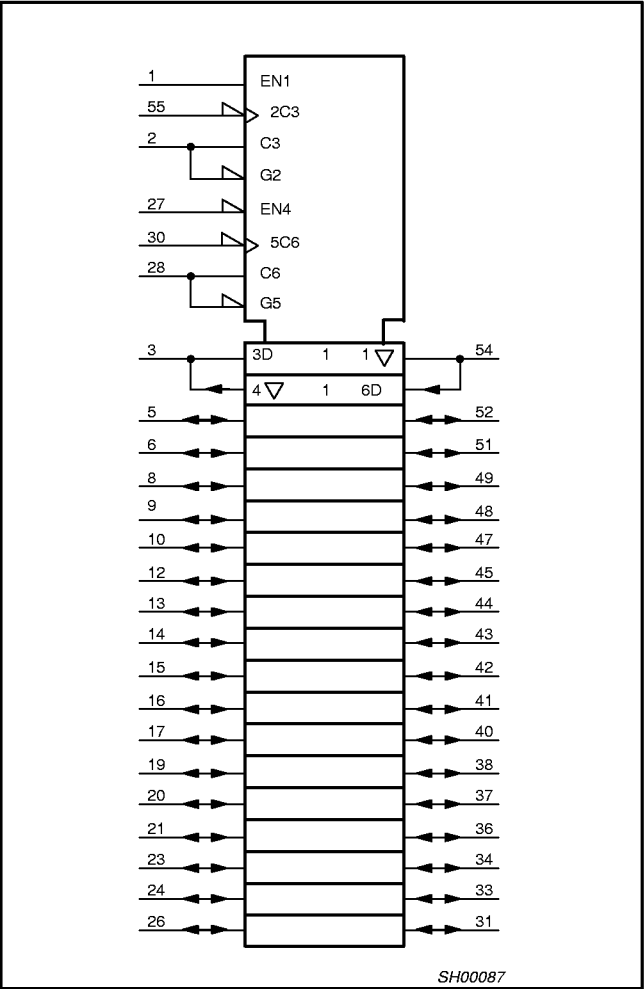
LOGIC SYMBOL



PIN CONFIGURATION



LOGIC SYMBOL (IEEE/IEC)



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PIN DESCRIPTION

PIN NUMBER	SYMBOL	NAME AND FUNCTION
1	OEAB	A-to-B Output enable input
27	$\overline{\text{OEBA}}$	B-to-A Output enable input (active low)
2, 28	LEAB/LEBA	A-to-B/B-to-A Latch enable input
55, 30	$\overline{\text{CPAB/CPBA}}$	A-to-B/B-to-A Clock input (active falling edge)
3, 5, 6, 8, 9, 10, 12, 13, 14, 15, 16, 17, 19, 20, 21, 23, 24, 26	A0-A17	Data inputs/outputs (A side)
54, 52, 51, 49, 48, 47, 45, 44, 43, 42, 41, 40, 38, 37, 36, 34, 33, 31	B0-B17	Data inputs/outputs (B side)
4, 11, 18, 25, 32, 39, 46, 53	GND	Ground (0V)
7, 22, 35, 50	V _{CC}	Positive supply voltage

FUNCTION TABLE

INPUTS				Internal Registers	OUTPUTS	OPERATING MODE
OEAB	LEAB	CPAB	A _n		B _n	
L	H	X	X	X	Z	Disabled
L	↓	X	h	H	Z	Disabled, Latch data
L	↓	X	l	L	Z	
L	L	H or L	X	NC	Z	Disabled, Hold data
L	L	↓	h	H	Z	Disabled, Clock data
L	L	↓	l	L	Z	
H	H	X	H	H	H	Transparent
H	H	X	L	L	L	
H	↓	X	h	H	H	Latch data & display
H	↓	X	l	L	L	
H	L	↓	h	H	H	Clock data & display
H	L	↓	l	L	L	
H	L	H or L	X	H	H	Hold data & display
H	L	H or L	X	L	L	

NOTE: A-to-B data flow is shown; B-to-A flow is similar but uses $\overline{\text{OEBA}}$, LEBA, and $\overline{\text{CPBA}}$.

H = High voltage level

h = High voltage level one set-up time prior to the Enable or Clock transition

L = Low voltage level

l = Low voltage level one set-up time prior to the Enable or Clock transition

NC= No Change

X = Don't care

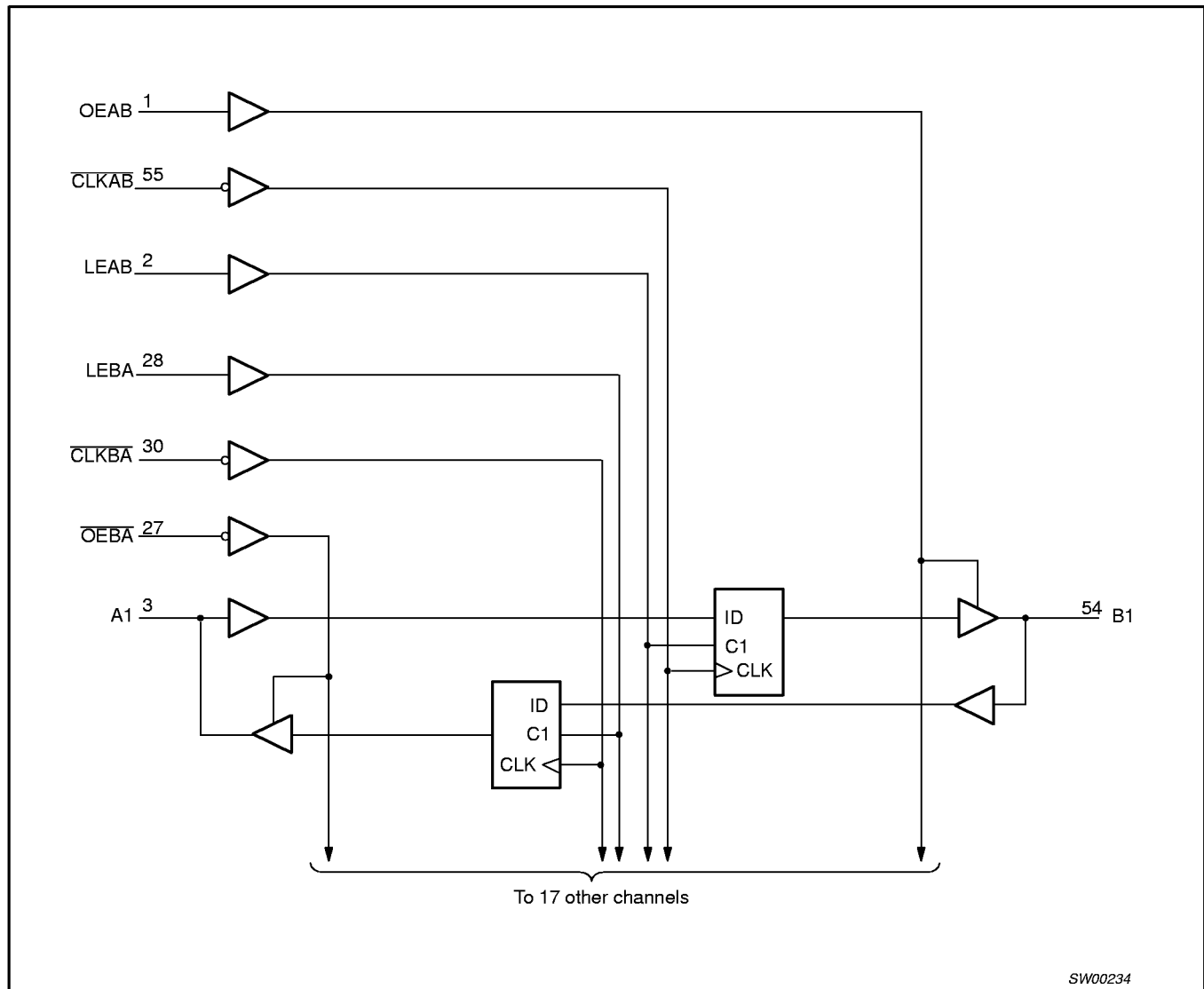
Z = High Impedance "off" state

↓ = High-to-Low Enable or Clock transition

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LOGIC DIAGRAM



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ABSOLUTE MAXIMUM RATINGS^{1, 2}

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		-0.5 to +7.0	V
I_{IK}	DC input diode current	$V_I < 0$	-18	mA
V_I	DC input voltage ³		-1.2 to +7.0	V
I_{OK}	DC output diode current	$V_O < 0$	-50	mA
V_{OUT}	DC output voltage ³	Output in Off or High state	-0.5 to +5.5	V
I_{OUT}	DC output current	Output in Low state	128	mA
		Output in High state	-64	
T_{stg}	Storage temperature range		-65 to +150	°C

NOTES:

1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability. The maximum junction temperature of this integrated circuit should not exceed 150°C.
3. The input and output negative voltage ratings may be exceeded if the input and output clamp current ratings are observed.

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS		UNIT
		MIN	MAX	
V_{CC}	DC supply voltage	4.5	5.5	V
V_I	Input voltage	0	V_{CC}	V
V_{IH}	High-level input voltage	2.0		V
V_{IL}	Input voltage		0.8	V
I_{OH}	High-level output current		-32	mA
I_{OL}	Low-level output current		64	mA
$\Delta t/\Delta v$	Input transition rise or fall rate; Outputs enabled		10	ns/V
T_{amb}	Operating free-air temperature range	-40	+85	°C

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DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS		LIMITS					UNIT
				T _{amb} = +25°C			T _{amb} = -40°C to +85°C		
				MIN	TYP	MAX	MIN	MAX	
V _{IK}	Input clamp voltage	V _{CC} = 4.5V; I _{IK} = -18mA			-0.8	-1.2		-1.2	V
V _{OH}	High-level output voltage	V _{CC} = 4.5V; I _{OH} = -3mA; V _I = V _{IL} or V _{IH}		2.5	2.9		2.5		V
		V _{CC} = 5.0V; I _{OH} = -3mA; V _I = V _{IL} or V _{IH}		3.0	4.0		3.0		V
		V _{CC} = 4.5V; I _{OH} = -32mA; V _I = V _{IL} or V _{IH}		2.0	2.4		2.0		V
V _{OL}	Low-level output voltage	V _{CC} = 4.5V; I _{OL} = 64mA; V _I = V _{IL} or V _{IH}			0.35	0.55		0.55	V
V _{RST}	Power-up output voltage ³	V _{CC} = 5.5V; I _O = 1mA; V _I = GND or V _{CC}			0.13	0.55		0.55	V
I _I	Input leakage current	V _{CC} = 5.5V; V _I = GND or 5.5V	Control pins		±0.01	±1.0		±1.0	μA
I _{HOLD}	Bus Hold current A and B Ports ⁶ 74ABTH16500C	V _{CC} = 4.5V; V _I = 0.8V		35			35		μA
		V _{CC} = 4.5V; V _I = 2.0V		-75			-75		
		V _{CC} = 5.5V; V _I = 0 to 5.5V		±800					
I _{OFF}	Power-off leakage current	V _{CC} = 0.0V; V _O or V _I ≤ 4.5V			±2	±100		±100	μA
I _{PU/PD}	Power-up/down 3-State output current ⁴	V _{CC} = 2.1V; V _O = 0.0V or V _{CC} ; V _{OE} = Don't care			±2	±50		±50	μA
I _{IH} + I _{OZH}	3-State output High current	V _{CC} = 5.5V; V _O = 5.5V; V _I = V _{IL} or V _{IH}			1.0	10		10	μA
I _{IL} + I _{OZL}	3-State output Low current	V _{CC} = 5.5V; V _O = 0.0V; V _I = V _{IL} or V _{IH}			-1.0	-10		-10	μA
I _{CEX}	Output High leakage current	V _{CC} = 5.5V; V _O = 5.5V; V _I = GND or V _{CC}			2	50		50	μA
I _O	Output current ¹	V _{CC} = 5.5V; V _O = 2.5V		-50	-80	-180	-50	-180	mA
I _{CCH}	Quiescent supply current	V _{CC} = 5.5V; Outputs High, V _I = GND or V _{CC}			0.5	2		2	mA
I _{CCL}		V _{CC} = 5.5V; Outputs Low, V _I = GND or V _{CC}			8	19		19	mA
I _{CCZ}		V _{CC} = 5.5V; Outputs 3-State; V _I = GND or V _{CC}			0.5	2		2	mA
ΔI _{CC}	Additional supply current per input pin ² 74ABT16500C	V _{CC} = 5.5V; one input at 3.4V, other inputs at V _{CC} or GND			5.0	50		50	μA
ΔI _{CC}	Additional supply current per input pin ² 74ABTH16500C	V _{CC} = 5.5V; one input at 3.4V, other inputs at V _{CC} or GND			200	500		500	μA

NOTES:

- Not more than one output should be tested at a time, and the duration of the test should not exceed one second.
- This is the increase in supply current for each input at 3.4V.
- For valid test results, data must not be loaded into the flip-flops (or latches) after applying the power.
- This parameter is valid for any V_{CC} between 0V and 2.1V, with a transition time of up to 10msec. From V_{CC} = 2.1V to V_{CC} = 5V ± 10% a transition time of up to 100μsec is permitted.
- Unused pins at V_{CC} or GND.
- This is the bus hold overdrive current required to force the input to the opposite logic state.

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AC CHARACTERISTICS

GND = 0V, $t_R = t_F = 2.5\text{ns}$, $C_L = 50\text{pF}$, $R_L = 500\Omega$

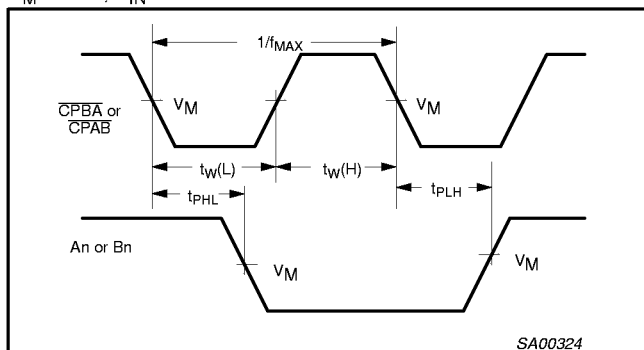
SYMBOL	PARAMETER	WAVEFORM	LIMITS					UNIT
			T _{amb} = +25°C V _{CC} = +5.0V			T _{amb} = −40 to +85°C V _{CC} = +5.0V ±0.5V		
			MIN	TYP	MAX	MIN	MAX	
f _{max}	Maximum clock frequency	1	150	225		150		MHz
t _{PLH} t _{PHL}	Propagation delay An to Bn or Bn to An	2	1.0 1.0	2.1 1.7	3.0 2.5	1.0 1.0	3.4 3.0	ns
t _{PLH} t _{PHL}	Propagation delay LEAB to Bn or LEBA to An	3	1.0 1.0	3.2 2.8	4.3 3.7	1.0 1.0	4.9 4.0	ns
t _{PLH} t _{PHL}	Propagation delay CPAB to Bn or CPBA to An	1	1.0 1.0	3.4 2.6	4.5 3.5	1.0 1.0	5.3 4.6	ns
t _{PZH} t _{PZL}	Output enable time to HIGH and LOW level	5 6	1.0 1.5	3.3 2.4	4.4 3.2	1.0 1.5	5.0 3.9	ns
t _{PHZ} t _{PLZ}	Output disable time from HIGH and LOW level	5 6	1.5 1.4	3.3 2.5	4.3 3.3	1.5 1.4	5.3 3.9	ns

AC SETUP REQUIREMENTS

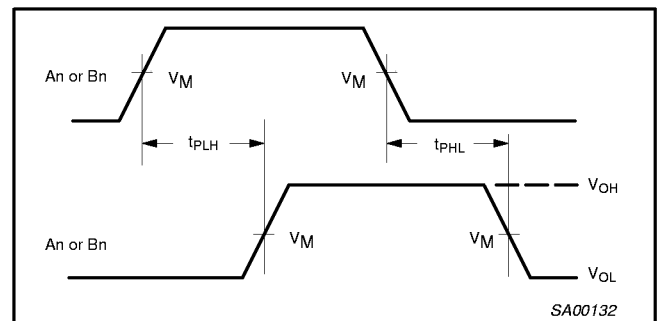
GND = 0V, $t_R = t_F = 2.5\text{ns}$, $C_L = 50\text{pF}$, $R_L = 500\Omega$

SYMBOL	PARAMETER	WAVEFORM	LIMITS			UNIT
			$T_{\text{amb}} = +25^\circ\text{C}$ $V_{\text{CC}} = +5.0\text{V}$		$T_{\text{amb}} = -40 \text{ to } +85^\circ\text{C}$ $V_{\text{CC}} = +5.0\text{V} \pm 0.5\text{V}$	
			MIN	TYP	MIN	
$t_s(\text{H})$ $t_s(\text{L})$	Setup time, HIGH or LOW An to $\overline{\text{CPAB}}$ or Bn to $\overline{\text{CPBA}}$	4	2.0 2.0	0.7 0.6	2.0 2.0	ns
$t_h(\text{H})$ $t_h(\text{L})$	Hold time, HIGH or LOW An to $\overline{\text{CPAB}}$ or Bn to $\overline{\text{CPBA}}$	4	0.7 0.7	-0.5 -0.8	0.7 0.7	ns
$t_s(\text{H})$ $t_s(\text{L})$	Setup time, HIGH or LOW An to LEAB or Bn to LEBA	4	2.0 2.0	0.1 0.1	2.0 2.0	ns
$t_h(\text{H})$ $t_h(\text{L})$	Hold time HIGH or LOW An to LEAB or Bn to LEBA	4	0.7 0.7	-0.1 -0.1	0.7 0.7	ns
t_w	Pulse width, HIGH or LOW $\overline{\text{CPAB}}$ or $\overline{\text{CPBA}}$	1	3	1.2	3	ns
$t_w(\text{H})$	Pulse width, HIGH LEAB or LEBA	3	3	1.2	3	ns

AC WAVEFORMS

 $V_M = 1.5\text{V}$, $V_{\text{IN}} = \text{GND to } 3.0\text{V}$ 

Waveform 1. Propagation Delay, Clock Input to Output, Clock Pulse Width, and Maximum Clock Frequency



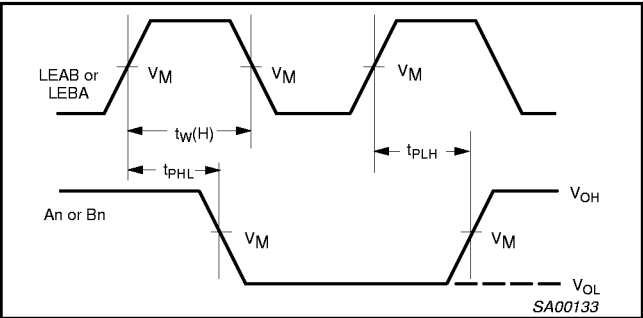
Waveform 2. Propagation Delay, Transparent Mode

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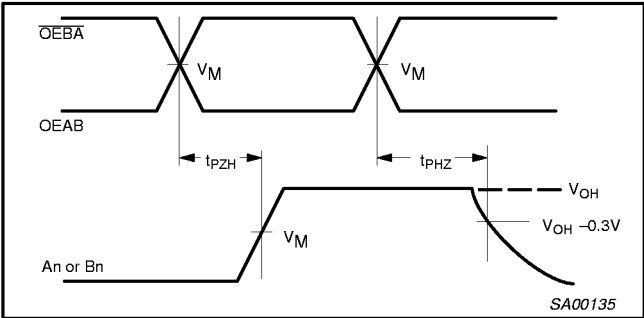
74ABT16500C
74ABTH16500C

AC WAVEFORMS (Continued)

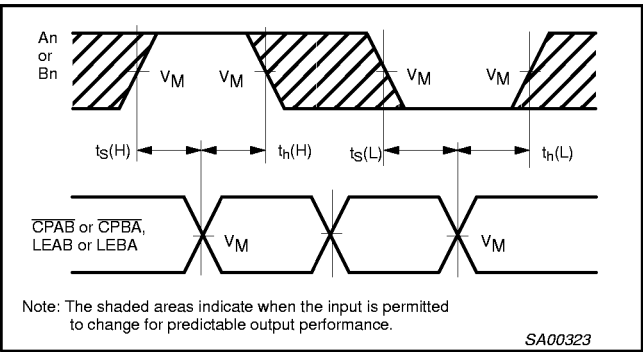
$V_M = 1.5V$, $V_{IN} = GND$ to $3.0V$



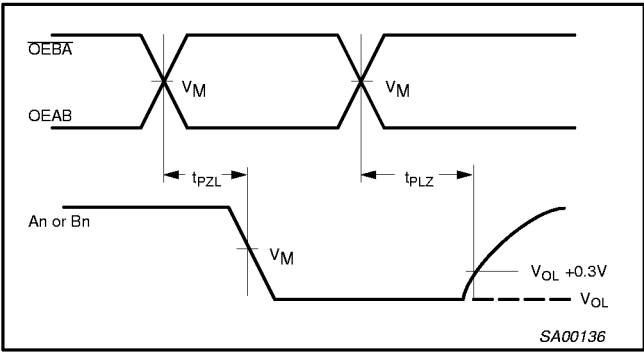
Waveform 3. Propagation Delay, Enable to Output, and Enable Pulse Width



Waveform 5. 3-State Output Enable Time to High Level and Output Disable Time from High Level



Waveform 4. Data Setup and Hold Times



Waveform 6. 3-State Output Enable Time to Low Level and Output Disable Time from Low Level

TEST CIRCUIT AND WAVEFORMS

Test Circuit for 3-State Outputs

SWITCH POSITION

TEST	SWITCH
t_{PLZ}	closed
t_{PZL}	closed
All other	open

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

Input Pulse Definition

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_R	t_F
74ABT/H16	3.0V	1MHz	500ns	2.5ns	2.5ns

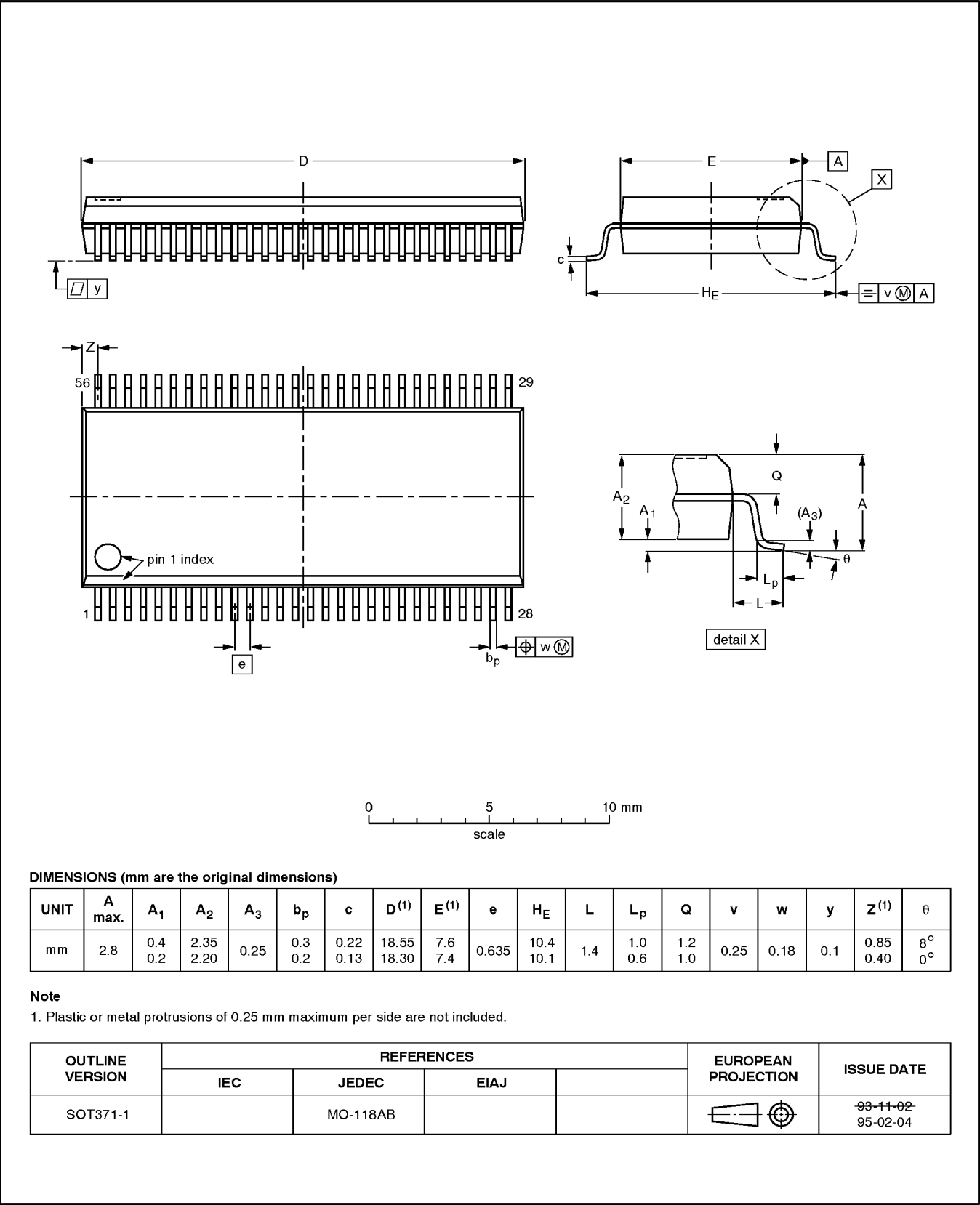
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SSOP56: plastic shrink small outline package; 56 leads; body width 7.5 mm

SOT371-1



18-bit universal bus transceiver (3-State)

74ABT16500C
74ABTH16500C

TSSOP56: plastic thin shrink small outline package; 56 leads; body width 6.1mm

SOT364-1

