



## 54ACQ/74ACQ574 • 54ACTQ/74ACTQ574

### Quiet Series Octal D Flip-Flop with TRI-STATE® Outputs

#### General Description

The 'ACQ/'ACTQ574 is a high-speed, low-power octal D-type flip-flop with a buffered Common Clock (CP) and a buffered common Output Enable ( $\overline{OE}$ ). The information presented to the D inputs is stored in the flip-flops on the LOW-to-HIGH clock (CP) transition.

'ACQ/'ACTQ574 utilizes Quiet Series technology to guarantee quiet output switching and improve dynamic threshold performance. FACT Quiet Series™ features GTO™ output control and undershoot corrector in addition to a split ground bus for superior performance.

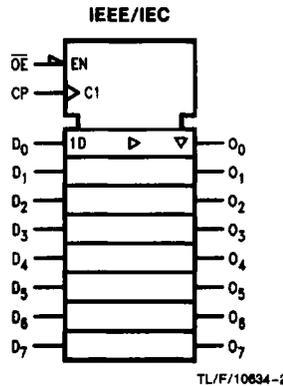
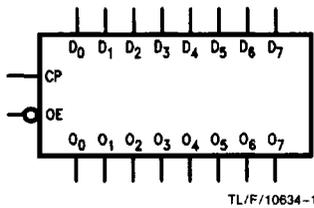
The 'ACQ/'ACTQ574 is functionally identical to the 'ACTQ374 but with different pin-out.

#### Features

- Guaranteed simultaneous switching noise level and dynamic threshold performance
- Guaranteed pin-to-pin skew AC performance
- Inputs and outputs on opposite sides of the package allowing easy interface with microprocessors
- Functionally identical to the 'ACQ/ACTQ374
- TRI-STATE outputs drive bus lines or buffer memory address registers
- Outputs source/sink 24 mA
- Faster prop delays than the standard 'AC/'ACT574
- 4 kV minimum ESD immunity

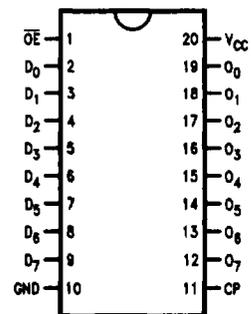
**Ordering Code:** See Section 8

#### Logic Symbols



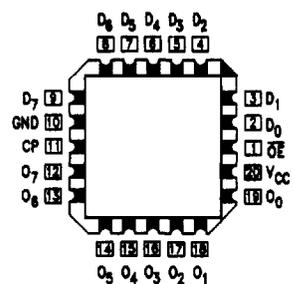
#### Connection Diagrams

##### Pin Assignment for DIP, Flatpak and SOIC



Pin Names	Description
D <sub>0</sub> -D <sub>7</sub>	Data Inputs
CP	Clock Pulse Input
$\overline{OE}$	TRI-STATE Output Enable Input
$\overline{O}_0$ - $\overline{O}_7$	TRI-STATE Outputs

##### Pin Assignment for LCC and PCC



## Functional Description

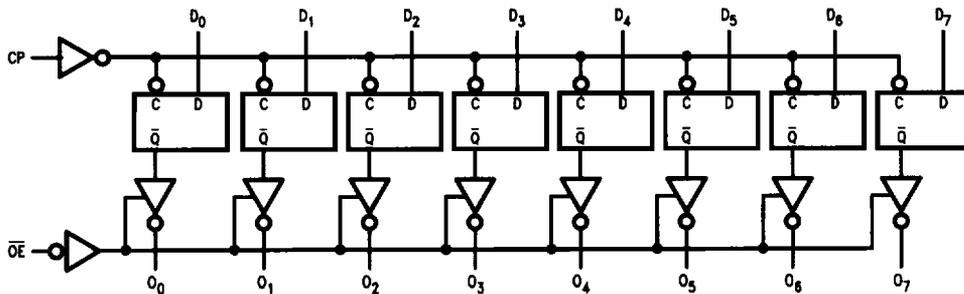
The 'ACQ/'ACTQ574 consists of eight edge-triggered flip-flops with individual D-type inputs and TRI-STATE true outputs. The buffered clock and buffered Output Enable are common to all flip-flops. The eight flip-flops will store the state of their individual D inputs that meet the setup and hold time requirements on the LOW-to-HIGH Clock (CP) transition. With the Output Enable ( $\overline{OE}$ ) LOW, the contents of the eight flip-flops are available at the outputs. When  $\overline{OE}$  is HIGH, the outputs go to the high impedance state. Operation of the  $\overline{OE}$  input does not affect the state of the flip-flops.

### Function Table

Inputs			Internal	Outputs	Function
$\overline{OE}$	CP	D	Q	$O_N$	
H	H	L	NC	Z	Hold
H	H	H	NC	Z	Hold
H	↗	L	L	Z	Load
H	↗	H	H	Z	Load
L	↗	L	L	L	Data Available
L	↗	H	H	H	Data Available
L	H	L	NC	NC	No Change in Data
L	H	H	NC	NC	No Change in Data

H = HIGH Voltage Level  
 L = LOW Voltage Level  
 X = Immaterial  
 Z = High Impedance  
 ↗ = LOW-to-HIGH Transition  
 NC = No Change

## Logic Diagram



TL/F/10634-5

Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

## Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage ( $V_{CC}$ )	-0.5V to +7.0V
DC Input Diode Current ( $I_{IK}$ )	
$V_I = -0.5V$	-20 mA
$V_I = V_{CC} + 0.5V$	+20 mA
DC Input Voltage ( $V_I$ )	-0.5V to $V_{CC} + 0.5V$
DC Output Diode Current ( $I_{OK}$ )	
$V_O = -0.5V$	-20 mA
$V_O = V_{CC} + 0.5V$	+20 mA
DC Output Voltage ( $V_O$ )	-0.5V to $V_{CC} + 0.5V$
DC Output Source or Sink Current ( $I_O$ )	±50 mA
DC $V_{CC}$ or Ground Current per Output Pin ( $I_{CC}$ or $I_{GND}$ )	±50 mA
Storage Temperature ( $T_{STG}$ )	-65°C to +150°C
DC Latch-Up Source or Sink Current	±300 mA
Junction Temperature ( $T_J$ )	
CDIP	175°C
PDIP	140°C

**Note 1:** Absolute maximum ratings are those values beyond which damage to the device may occur. The databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables. National does not recommend operation of FACT™ circuits outside databook specifications.

## Recommended Operating Conditions

Supply Voltage ( $V_{CC}$ )		2.0V to 6.0V
'ACQ		4.5V to 5.5V
'ACTQ		
Input Voltage ( $V_I$ )		0V to $V_{CC}$
Output Voltage ( $V_O$ )		0V to $V_{CC}$
Operating Temperature ( $T_A$ )		
74ACQ/ACTQ		-40°C to +85°C
54ACQ/ACTQ		-55°C to +125°C
Minimum Input Edge Rate $\Delta V/\Delta t$		
'ACQ Devices		
$V_{IN}$ from 30% to 70% of $V_{CC}$		
$V_{CC}$ @ 3.0V, 4.5V, 5.5V		125 mV/ns
Minimum Input Edge Rate $\Delta V/\Delta t$		
'ACTQ Devices		
$V_{IN}$ from 0.8V to 2.0V		
$V_{CC}$ @ 4.5V, 5.5V		125 mV/ns

## DC Electrical Characteristics for 'ACQ Family Devices

Symbol	Parameter	$V_{CC}$ (V)	74ACQ		54ACQ	74ACQ	Units	Conditions	
			$T_A = +25^\circ\text{C}$		$T_A =$ -55°C to +125°C	$T_A =$ -40°C to +85°C			
			Typ	Guaranteed Limits					
$V_{IH}$	Minimum High Level Input Voltage	3.0	1.5	2.1	2.1	2.1	V	$V_{OUT} = 0.1V$ or $V_{CC} - 0.1V$	
		4.5	2.25	3.15	3.15	3.15			
		5.5	2.75	3.85	3.85	3.85			
$V_{IL}$	Maximum Low Level Input Voltage	3.0	1.5	0.9	0.9	0.9	V	$V_{OUT} = 0.1V$ or $V_{CC} - 0.1V$	
		4.5	2.25	1.35	1.35	1.35			
		5.5	2.75	1.65	1.65	1.65			
$V_{OH}$	Minimum High Level Output Voltage	3.0	2.99	2.9	2.9	2.9	V	$I_{OUT} = -50 \mu\text{A}$	
		4.5	4.49	4.4	4.4	4.4			
		5.5	5.49	5.4	5.4	5.4			
		3.0		2.56	2.4	2.46	V		* $V_{IN} = V_{IL}$ or $V_{IH}$ -12 mA $I_{OH}$ -24 mA -24 mA
		4.5		3.86	3.7	3.76			
		5.5		4.86	4.7	4.76			
$V_{OL}$	Maximum Low Level Output Voltage	3.0	0.002	0.1	0.1	0.1	V	$I_{OUT} = 50 \mu\text{A}$	
		4.5	0.001	0.1	0.1	0.1			
		5.5	0.001	0.1	0.1	0.1			
		3.0		0.36	0.50	0.44	V		* $V_{IN} = V_{IL}$ or $V_{IH}$ 12 mA $I_{OL}$ 24 mA 24 mA
		4.5		0.36	0.50	0.44			
		5.5		0.36	0.50	0.44			

\*All outputs loaded; thresholds on input associated with output under test.

†Maximum test duration 2.0 ms, one output loaded at a time.

### DC Electrical Characteristics for 'ACQ Family Devices (Continued)

Symbol	Parameter	V <sub>CC</sub> (V)	74ACQ		54ACQ	74ACQ	Units	Conditions
			T <sub>A</sub> = +25°C		T <sub>A</sub> = -55°C to +125°C	T <sub>A</sub> = -40°C to +85°C		
			Typ	Guaranteed Limits				
I <sub>IN</sub>	Maximum Input Leakage Current	5.5		±0.1	±1.0	±1.0	μA	V <sub>I</sub> = V <sub>CC</sub> , GND (Note 1)
I <sub>OLD</sub>	†Minimum Dynamic Output Current	5.5			50	75	mA	V <sub>OLD</sub> = 1.65V Max
I <sub>OHD</sub>		5.5			-50	-75	mA	V <sub>OHD</sub> = 3.85V Min
I <sub>CC</sub>	Maximum Quiescent Supply Current	5.5		8.0	160.0	80.0	μA	V <sub>IN</sub> = V <sub>CC</sub> or GND (Note 1)
I <sub>OZ</sub>	Maximum TRI-STATE Leakage Current	5.5		±0.5	±10.0	±5.0	μA	V <sub>I(OE)</sub> = V <sub>IL</sub> , V <sub>IH</sub> V <sub>I</sub> = V <sub>CC</sub> , GND V <sub>O</sub> = V <sub>CC</sub> , GND
V <sub>OLP</sub>	Quiet Output Maximum Dynamic V <sub>OL</sub>	5.0	1.1	1.5			V	Figures 1, 2 (Notes 2, 3)
V <sub>OLV</sub>	Quiet Output Minimum Dynamic V <sub>OL</sub>	5.0	-0.6	-1.2			V	Figures 1, 2 (Notes 2, 3)
V <sub>IHD</sub>	Minimum High Level Dynamic Input Voltage	5.0	3.1	3.5			V	(Notes 2, 4)
V <sub>ILD</sub>	Maximum Low Level Dynamic Input Voltage	5.0	1.9	1.5			V	(Notes 2, 4)

\*All outputs loaded; thresholds on input associated with output under test.

†Maximum test duration 2.0 ms, one output loaded at a time.

**Note 1:** I<sub>IN</sub> and I<sub>CC</sub> @ 3.0V are guaranteed to be less than or equal to the respective limit @ 5.5V V<sub>CC</sub>. I<sub>CC</sub> for 54ACQ @ 25°C is identical to 74ACQ @ 25°C

**Note 2:** Worst case package

**Note 3:** Max number of outputs defined as (n). Data inputs are driven 0V to 5V. One output @ GND.

**Note 4:** Maximum number of data inputs (n) switching. (n - 1) inputs switching 0V to 5V ('ACQ). Input-under-test switching: 5V to threshold (V<sub>ILD</sub>), 0V to threshold (V<sub>IHD</sub>). f = 1 MHz.

## DC Electrical Characteristics for 'ACTQ Family Devices

Symbol	Parameter	V <sub>CC</sub> (V)	74ACTQ		54ACTQ		74ACTQ		Units	Conditions
			T <sub>A</sub> = +25°C		T <sub>A</sub> = -55°C to +125°C		T <sub>A</sub> = -40°C to +85°C			
			Typ	Guaranteed Limits						
V <sub>IH</sub>	Minimum High Level Input Voltage	4.5	1.5	2.0	2.0	2.0	2.0	2.0	V	V <sub>OUT</sub> = 0.1V or V <sub>CC</sub> - 0.1V
		5.5	1.5	2.0	2.0	2.0	2.0	2.0		
V <sub>IL</sub>	Maximum Low Level Input Voltage	4.5	1.5	0.8	0.8	0.8	0.8	0.8	V	V <sub>OUT</sub> = 0.1V or V <sub>CC</sub> - 0.1V
		5.5	1.5	0.8	0.8	0.8	0.8	0.8		
V <sub>OH</sub>	Minimum High Level Output Voltage	4.5	4.49	4.4	4.4	4.4	4.4	4.4	V	I <sub>OUT</sub> = -50 μA
		5.5	5.49	5.4	5.4	5.4	5.4	5.4		
		4.5		3.85	3.70	3.76	3.76	3.76	V	*V <sub>IN</sub> = V <sub>IL</sub> or V <sub>IH</sub> I <sub>OH</sub> = -24 mA -24 mA
		5.5		4.86	4.70	4.76	4.76	4.76		
V <sub>OL</sub>	Maximum Low Level Output Voltage	4.5	0.001	0.1	0.1	0.1	0.1	0.1	V	I <sub>OUT</sub> = 50 μA
		5.5	0.001	0.1	0.1	0.1	0.1	0.1		
		4.5		0.36	0.50	0.44	0.44	0.44	V	*V <sub>IN</sub> = V <sub>IL</sub> or V <sub>IH</sub> I <sub>OL</sub> = 24 mA 24 mA
		5.5		0.36	0.50	0.44	0.44	0.44		
I <sub>IN</sub>	Maximum Input Leakage Current	5.5		±0.1	±1.0	±1.0	±1.0	μA	V <sub>I</sub> = V <sub>CC</sub> , GND	
I <sub>OZ</sub>	Maximum TRI-STATE Leakage Current	5.5		±0.5	±10.0	±5.0	±5.0	μA	V <sub>I</sub> = V <sub>IL</sub> , V <sub>IH</sub> V <sub>O</sub> = V <sub>CC</sub> , GND	
I <sub>CC</sub>	Maximum I <sub>CC</sub> /Input	5.5	0.6		1.6	1.5	1.5	mA	V <sub>I</sub> = V <sub>CC</sub> - 2.1V	
I <sub>OLD</sub>	†Maximum Dynamic Output Current	5.5			50	75	75	mA	V <sub>OLD</sub> = 1.65V Max	
		5.5			-50	-75	-75	mA	V <sub>OHD</sub> = 3.85V Min	
I <sub>CC</sub>	Maximum Quiescent Supply Current	5.5		8.0	160.0	80.0	80.0	μA	V <sub>IN</sub> = V <sub>CC</sub> or GND (Note 1)	
V <sub>OLP</sub>	Maximum High Level Output Noise	5.0	1.1	1.5				V	Figures 1, 2 (Notes 2, 3)	
V <sub>OLV</sub>	Maximum Low Level Output Noise	5.0	-0.6	-1.2				V	Figures 1, 2 (Notes 2, 3)	
V <sub>IHD</sub>	Maximum High Level Dynamic Input Voltage	5.0	1.9	2.2				V	(Notes 2, 4)	
V <sub>ILD</sub>	Maximum Low Level Dynamic Input Voltage	5.0	1.2	0.8				V	(Notes 2, 4)	

\*All outputs loaded; thresholds on input associated with output under test.

†Maximum test duration 2.0 ms, one output loaded at a time.

Note 1: I<sub>CC</sub> for 54ACTQ @ 25°C is identical to 74ACTQ @ 25°C.

Note 2: Worst case package.

Note 3: Max number of outputs defined as (n). Data inputs are driven 0V to 3V. One output @ GND.

Note 4: Max number of data inputs (n) switching. (n-1) inputs switching 0V to 3V (ACTQ). Input-under-test switching: 3V to threshold (V<sub>ILD</sub>), 0V to threshold (V<sub>IHD</sub>). f = 1 MHz.

**AC Electrical Characteristics:** See Section 2 for Waveforms

Symbol	Parameter	V <sub>CC</sub> * (V)	74ACQ			54ACQ		74ACQ		Units	Fig. No.
			T <sub>A</sub> = +25°C C <sub>L</sub> = 50 pF			T <sub>A</sub> = -55°C to +125°C C <sub>L</sub> = 50 pF		T <sub>A</sub> = -40°C to +85°C C <sub>L</sub> = 50 pF			
			Min	Typ	Max	Min	Max	Min	Max		
f <sub>max</sub>	Maximum Clock Frequency	3.3 5.0	75 90					70 85		MHz	
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation Delay CP to $\bar{O}_n$	3.0 5.0	3.0 2.0	9.5 6.5	13.0 8.5			3.0 2.0	13.5 9.0	ns	2-3,4
t <sub>PZH</sub> t <sub>PZL</sub>	Output Enable Time	3.3 5.0	3.0 2.0	9.5 6.5	13.0 8.5			3.0 2.0	13.5 9.0	ns	2-5,6
t <sub>PHZ</sub> t <sub>PLZ</sub>	Output Disable Time	3.3 5.0	1.0 1.0	9.5 8.0	14.5 9.5			1.0 1.0	15.0 10.0	ns	2-5,6
t <sub>OSHL</sub> t <sub>OSLH</sub>	Output to Output Skew** CP to $\bar{O}_n$	3.3 5.0	1.0 0.5					1.5 1.0		ns	

\*Voltage Range 5.0 is 5.0V ±0.5V

Voltage Range 3.3 is 3.3V ±0.3V

\*\*Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device. The specification applies to any outputs switching in the same direction, either HIGH to LOW (t<sub>OSHL</sub>) or LOW to HIGH (t<sub>OSLH</sub>). Parameter guaranteed by design.

**AC Operating Requirements:** See Section 2 for Waveforms

Symbol	Parameter	V <sub>CC</sub> * (V)	74ACQ		54ACQ		74ACQ		Units	Fig. No.
			T <sub>A</sub> = +25°C C <sub>L</sub> = 50 pF		T <sub>A</sub> = -55°C to +125°C C <sub>L</sub> = 50 pF		T <sub>A</sub> = -40°C to +85°C C <sub>L</sub> = 50 pF			
			Typ	Guaranteed Minimum						
t <sub>S</sub>	Setup Time, HIGH or LOW D <sub>n</sub> to CP	3.3 5.0	0 0	3.0 3.0			3.0 3.0	ns	2-7	
t <sub>H</sub>	Hold Time, HIGH or LOW D <sub>n</sub> to CP	3.3 5.0	0 0	1.5 1.5			1.5 1.5	ns	2-7	
t <sub>W</sub>	LE Pulse Width, HIGH or LOW	3.3 5.0	2.0 2.0	4.0 4.0			4.0 4.0	ns	2-3	

\*Voltage Range 5.0 is 5.0V ±0.5V

Voltage Range 3.3 is 3.3V ±0.3V

**AC Electrical Characteristics:** See Section 2 for Waveforms

Symbol	Parameter	V <sub>CC</sub> * (V)	74ACTQ			54ACTQ		74ACTQ		Units	Fig. No.
			T <sub>A</sub> = +25°C C <sub>L</sub> = 50 pF			T <sub>A</sub> = -55°C to +125°C C <sub>L</sub> = 50 pF		T <sub>A</sub> = -40°C to +85°C C <sub>L</sub> = 50 pF			
			Min	Typ	Max	Min	Max	Min	Max		
f <sub>max</sub>	Maximum Clock Frequency	5.0	85					80		MHz	
t <sub>PLH</sub> , t <sub>PHL</sub>	Propagation Delay CP to $\bar{O}_n$	5.0	2.0	7.0	9.0			2.0	9.5	ns	2-3, 4
t <sub>PZH</sub> , t <sub>PZL</sub>	Output Enable Time	5.0	20	7.0	9.0			2.0	9.5	ns	2-5, 6
t <sub>PHZ</sub> , t <sub>PLZ</sub>	Output Disable Time	5.0	1.0	8.0	10.0			1.0	10.5	ns	2-7
t <sub>OSSL</sub> , t <sub>OSLH</sub>	Output to Output Skew** CP to $\bar{O}_n$	5.0	0.5			1.0		1.0		ns	

\*Voltage Range 5.0 is 5.0V ± 0.5V.

\*\*Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device. The specification applies to any outputs switching in the same direction, either HIGH to LOW (t<sub>OSSL</sub>) or LOW to HIGH (t<sub>OSLH</sub>). Parameter guaranteed by design.**AC Operating Requirements:** See Section 2 for Waveforms

Symbol	Parameter	V <sub>CC</sub> * (V)	74ACTQ		54ACTQ		74ACTQ		Units	Fig. No.
			T <sub>A</sub> = +25°C C <sub>L</sub> = 50 pF		T <sub>A</sub> = -55°C to +125°C C <sub>L</sub> = 50 pF		T <sub>A</sub> = -40°C to +85°C C <sub>L</sub> = 50 pF			
			Typ	Guaranteed Minimum						
t <sub>S</sub>	Setup Time, HIGH or LOW D <sub>n</sub> to CP	5.0	0	3.0			3.0	ns	2-7	
t <sub>H</sub>	Hold Time, HIGH or LOW D <sub>n</sub> to CP	5.0	0	1.5			1.5	ns	2-7	
t <sub>w</sub>	LE Pulse Width, HIGH or LOW	5.0	2.0	4.0			4.0	ns	2-3	

\*Voltage Range 5.0 is 5.0V ± 0.5V.

**Capacitance**

Symbol	Parameter	Typ	Units	Conditions
C <sub>IN</sub>	Input Capacitance	4.5	pF	V <sub>CC</sub> = 5.0V
C <sub>PD</sub>	Power Dissipation Capacitance	40.0	pF	V <sub>CC</sub> = 5.0V