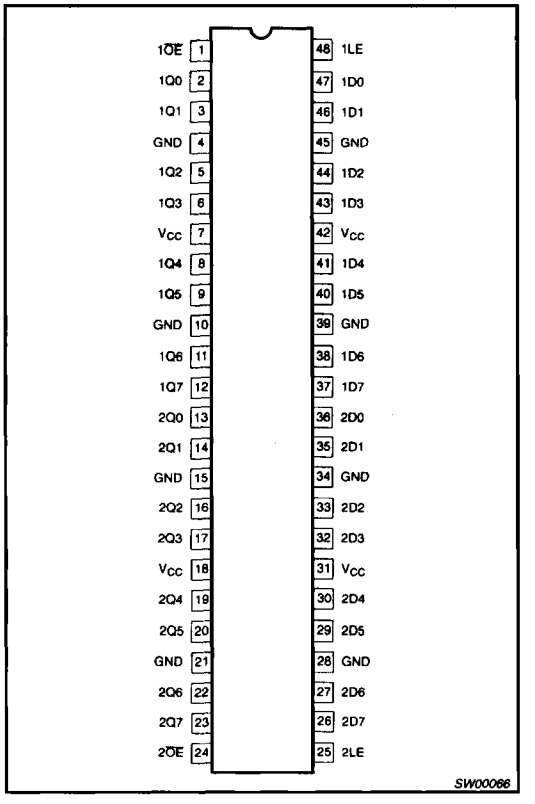
16-bit D-type transparent latch with 30Ω series termination resistors; (3-State)

74LVC162373A
74LVCH162373A

FEATURES

- 5 volt tolerant inputs/outputs for interfacing with 5V logic
- Wide supply voltage range of 1.2V to 3.6V
- Complies with JEDEC standard no. 8-1A
- CMOS low power consumption
- MULTIBYTE™ flow-through standard pin-out architecture
- Low inductance multiple power and ground pins for minimum noise and ground bounce
- Direct interface with TTL levels
- All data inputs have bushold (74LVCH162373A only)
- Integrated 30Ω termination resistors

PIN CONFIGURATION



DESCRIPTION

The 74LVC(H)162373A is a 16-bit D-type transparent latch featuring separate D-type inputs for each latch and 3-State outputs for bus oriented applications. One latch enable (LE) input and one output enable ($\overline{OE}$) are provided for each octal. Inputs can be driven from either 3.3V or 5V devices. In 3-State operation, outputs can handle 5V. These features allow the use of these devices in a mixed 3.3V/5V environment.

The 74LVC(H)162373 consists of 2 sections of eight D-type transparent latches with 3-State true outputs. When LE is HIGH, data at the Dn inputs enter the latches. In this condition the latches are transparent, i.e., a latch output will change each time its corresponding D-input changes.

When LE is LOW the latches store the information that was present at the D-inputs a set-up time preceding the HIGH-to-LOW transition of LE. When $\overline{OE}$ is LOW, the contents of the eight latches are available at the outputs. When $\overline{OE}$ is HIGH, the outputs go to the high impedance OFF-state. Operation of the $\overline{OE}$ input does not affect the state of the latches.

The 74LVC(H)162373A is designed with 30Ω series termination resistors to reduce line noise.

ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	OUTSIDE NORTH AMERICA	NORTH AMERICA	DWG NUMBER
48-Pin Plastic SSOP Type III	–40°C to +85°C	74LVC162373A DL	VC162373A DL	SOT370-1
48-Pin Plastic TSSOP Type II	–40°C to +85°C	74LVC162373A DGG	VC162373A DGG	SOT362-1
48-Pin Plastic SSOP Type III	–40°C to +85°C	74LVCH162373A DL	VCH162373A DL	SOT370-1
48-Pin Plastic TSSOP Type II	–40°C to +85°C	74LVCH162373A DGG	VCH162373A DGG	SOT362-1

QUICK REFERENCE DATA

GND = 0V; T_{amb} = 25°C; $t_r = t_f \leq 2.5$ns

SYMBOL	PARAMETER	CONDITIONS	TYPICAL	UNIT
t_{PHL}/t_{PLH}	Propagation delay Dn to Qn; LE to Qn	C_L = 50pF V_{CC} = 3.3V	4.0 4.5	ns
C_I	Input capacitance		5.0	pF
C_{PD}	Power dissipation capacitance per latch	V_I = GND to V_{CC}[1]	25	pF

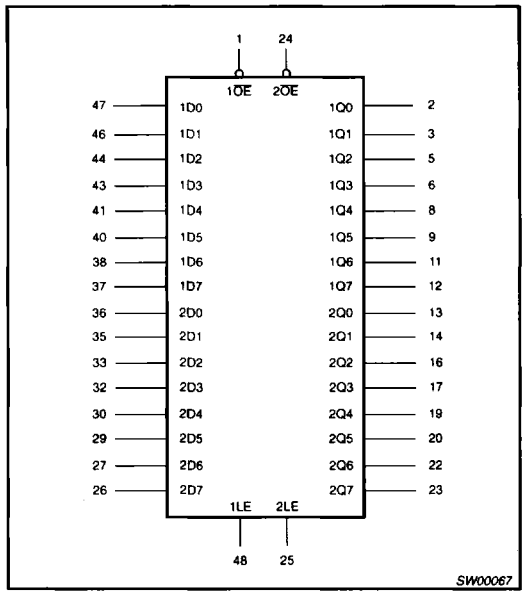
NOTES:

1. C_{PD} is used to determine the dynamic power dissipation (P_D in μW):
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz; C_L = output load capacity in pF;
   f_o = output frequency in MHz; V_{CC} = supply voltage in V;
   $\Sigma (C_L \times V_{CC}^2 \times f_o)$ = sum of outputs.

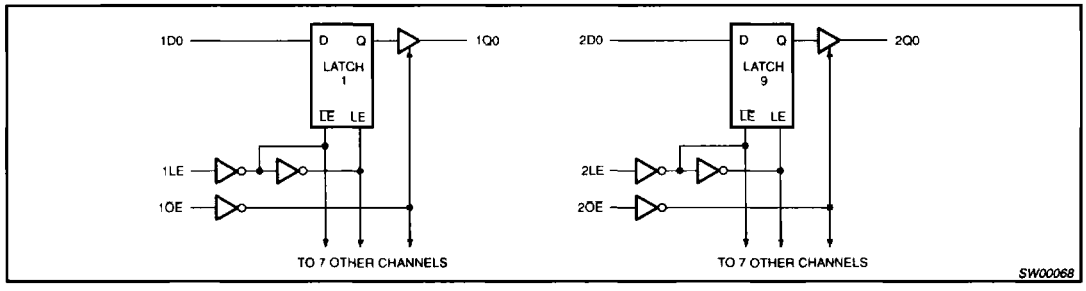
PIN DESCRIPTION

PIN NUMBER	SYMBOL	NAME AND FUNCTION
1	$1\overline{OE}$	Output enable input (active LOW)
2, 3, 5, 6, 8, 9, 11, 12	1Q0 to 1Q7	Data inputs/outputs
4, 10, 15, 21, 28, 34, 39, 45	GND	Ground (0V)
7, 18, 31, 42	V_{CC}	Positive supply voltage
13, 14, 16, 17, 19, 20, 22, 23	2Q0 to 2Q7	Data inputs/outputs
24	$2\overline{OE}$	Output enable input (active LOW)
25	2LE	Latch enable input (active HIGH)
36, 35, 33, 32, 30, 29, 27, 26	2D0 to 2D7	Data inputs
47, 46, 44, 43, 41, 40, 38, 37	1D0 to 1D7	Data inputs
48	1LE	Latch enable input (active HIGH)

LOGIC SYMBOL



LOGIC DIAGRAM

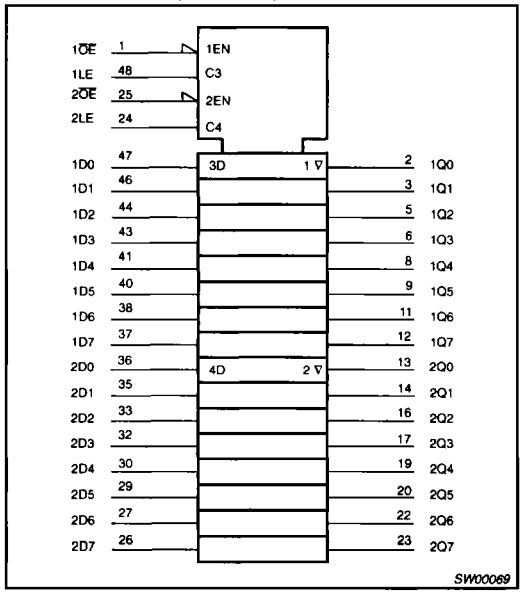


FUNCTION TABLE (per section of eight bits)

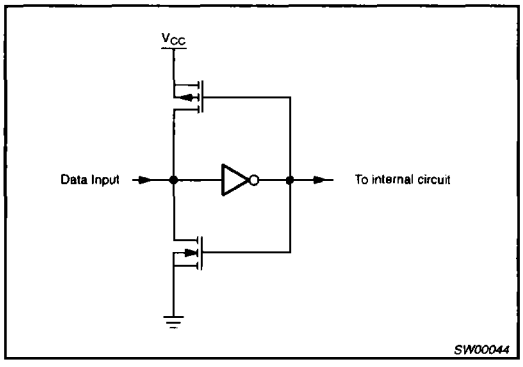
OPERATING MODES	INPUTS			INTERNAL LATCHES	OUTPUTS
	$\overline{OE}$	LE	Dn		Q0 to Q7
enable and read register (transparent mode)	L L	H H	L H	L H	L H
latch and read register	L L	L L	l h	L H	L H
latch register and disable outputs	H H	L L	l h	L H	Z Z

H = HIGH voltage level
h = HIGH voltage level one set-up time prior to the HIGH-to-LOW LE transition
L = LOW voltage level
l = LOW voltage level one set-up time prior to the HIGH-to-LOW LE transition
X = don't care
Z = high impedance OFF-state

LOGIC SYMBOL (IEEE/IEC)



BUSHOLD CIRCUIT



ABSOLUTE MAXIMUM RATINGS[1, 2]

In accordance with the Absolute Maximum Rating System (IEC 134) Voltages are referenced to GND (ground = 0V)

SYMBOL	PARAMETER	CONDITIONS	LIMITS		UNIT
			MIN	MAX	
V_{CC}	DC supply voltage		−0.5	+6.5	V
I_{IK}	DC input diode current	$V_I < 0$	−	−50	mA
V_I	DC input voltage	Note 3	−0.5	+6.5	V
I_{OK}	DC output diode current	$V_O > V_{CC}$ or $V_O < 0$	−	±50	mA
V_O	DC output voltage; output HIGH or LOW state	Note 3	−0.5	V_{CC} + 0.5	V
V_O	DC output voltage; output 3-State	Note 3	−0.5	6.5	V
I_O	DC output source or sink current	V_O = 0 to V_{CC}	−	±50	mA
I_{GND}, I_{CC}	DC V_{CC} or GND current		−	±100	mA
T_{stg}	Storage temperature range		−60	+150	°C
P_{tot}	Power dissipation per package – SO package – SSOP and TSSOP package	 Above +70°C derate linearly 8mW/K Above +60°C derate linearly 5.5mW/K	 − −	 500 500	mW

NOTES:

1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability. The maximum junction temperature of this integrated circuit should not exceed 150°C.
3. The input and output voltage ratings may be exceeded if the input and output clamp current ratings are observed.

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	CONDITIONS	LIMITS		UNIT
			MIN.	MAX.	
V_{CC}	DC supply voltage (for max. speed performance)		2.7	3.6	V
V_{CC}	DC supply voltage (for low-voltage applications)		1.2	3.6	V
V_I	DC Input voltage range		0	5.5	V
V_O	DC output voltage range; output HIGH or LOW state		0	V_{CC}	V
V_O	DC output voltage range; output 3-State		0	5.5	V
T_{amb}	Operating ambient temperature range in free air	See DC and AC characteristics for individual device	−40	+85	°C
t_r, t_f	Input rise and fall times	V_{CC} = 1.2 to 2.7V V_{CC} = 2.7 to 3.6V	0 0	20 10	ns/V

DC ELECTRICAL CHARACTERISTICS

Over recommended operating conditions
Voltages are referenced to GND (ground = 0V)

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			Temp = -40°C to +85°C			
			MIN	TYP[1]	MAX	
V_{IH}	HIGH level input voltage	V_{CC} = 1.2V	V_{CC}			V
		V_{CC} = 2.7 to 3.6V	2.0			
V_{IL}	LOW level input voltage	V_{CC} = 1.2V			GND	V
		V_{CC} = 2.7 to 3.6V			0.8	
V_{OH}	HIGH level output voltage	V_{CC} = 2.7; V_I = V_{IH} or V_{IL}; I_O = −12mA	V_{CC}-0.5			V
		V_{CC} = 3.0V; V_I = V_{IH} or V_{IL}; I_O = −100µA	V_{CC}-0.2	V_{CC}		
		V_{CC} = 3.0V; V_I = V_{IH} or V_{IL}; I_O = −18mA	V_{CC}-0.6			
		V_{CC} = 3.0V; V_I = V_{IH} or V_{IL}; I_O = −24mA	V_{CC}-0.8			
V_{OH}	HIGH level output voltage	V_{CC} = 2.7; V_I = V_{IH} or V_{IL}; I_O = −6mA[7]	V_{CC}-0.5			V
		V_{CC} = 3.0V; V_I = V_{IH} or V_{IL}; I_O = −100µA[7]	V_{CC}-0.2	V_{CC}		
		V_{CC} = 3.0V; V_I = V_{IH} or V_{IL}; I_O = −12mA[7]	V_{CC}-1.0			
V_{OL}	LOW level output voltage	V_{CC} = 2.7V; V_I = V_{IH} or V_{IL}; I_O = 12mA			0.40	V
		V_{CC} = 3.0V; V_I = V_{IH} or V_{IL}; I_O = 100µA			0.20	
		V_{CC} = 3.0V; V_I = V_{IH} or V_{IL}; I_O = 24mA			0.55	
V_{OL}	LOW level output voltage	V_{CC} = 2.7V; V_I = V_{IH} or V_{IL}; I_O = 6mA[7]			0.40	V
		V_{CC} = 3.0V; V_I = V_{IH} or V_{IL}; I_O = 100µA[7]			0.20	
		V_{CC} = 3.0V; V_I = V_{IH} or V_{IL}; I_O = 12mA[7]			0.55	
I_I	Input leakage current	V_{CC} = 3.6V; V_I = 5.5V or GND; not for I/O pins[6]		±0.1	±5	µA
I_{IHZ}/I_{ILZ}	Input current for common I/O pins	V_{CC} = 3.6V; V_I = 5.5V or GND; output disabled[6]		±0.1	±10	µA
I_{OZ}	3-State output OFF-state current	V_{CC} = 3.6V; V_I = V_{IH} or V_{IL}; V_O 5.5V or GND		0.1	±10	µA
I_{OFF}	Power off leakage current	V_{CC} = 0.0V; V_I or V_O = 5.5V			±10	µA
I_{CC}	Quiescent supply current	V_{CC} = 3.6V; V_I = V_{CC} or GND; I_O = 0		0.1	20	µA
ΔI_{CC}	Additional quiescent supply current given per input pin	V_{CC} = 2.7 to 3.6V; V_I = V_{CC} −0.6V; I_O = 0		5	500	µA
I_{BHL}	Bus hold LOW sustaining current	V_{CC} = 3.0V; V_I = 0.8V[2, 3, 4]	75			µA
I_{BHH}	Bus hold HIGH sustaining current	V_{CC} = 3.0V; V_I = 2.0V[2, 3, 4]	−75			µA
I_{BHLO}	Bus hold LOW overdrive current	V_{CC} = 3.6V[2, 3, 5]	500			µA
I_{BHHO}	Bus hold HIGH overdrive current	V_{CC} = 3.6V[2, 3, 5]	−500			µA

NOTES:

1. All typical values are at V_{CC} = 3.3V and T_{amb} = 25°C.
2. Valid for data inputs of bus hold parts (LVCH16-A) only.
3. For data inputs only, control inputs do not have a bus hold circuit.
4. The specified sustaining current at the data input holds the input below the specified V_I level.
5. The specified overdrive current at the data input forces the data input to the opposite logic input state.
6. For bus hold parts, the bus hold circuit is switched off when V_I exceeds V_{CC} allowing 5.5V on the input terminal.
7. For data outputs of damping resistor parts (LVC(H)16-A only.

AC CHARACTERISTICS

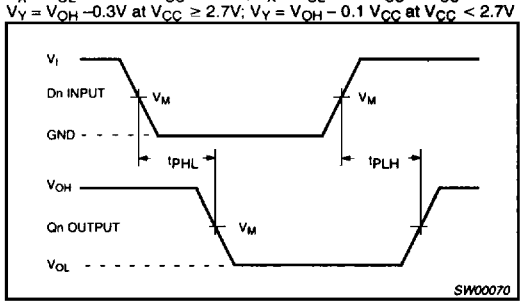
GND = 0V; $t_R = t_F$ = 2.5ns; C_L = 50pF; R_L = 500Ω; T_{amb} = −40°C to +85°C.

SYMBOL	PARAMETER	WAVEFORM	LIMITS					UNIT
			V_{CC} = 3.3V ±0.3V			V_{CC} = 2.7V		
			MIN	TYP[1]	MAX	MIN	MAX	
t_{PHL} t_{PLH}	Propagation delay Dn to Qn	1, 5			8.0		9.0	ns
t_{PHL} t_{PLH}	Propagation delay LE to Qn	2, 5			8.5		9.0	ns
t_{PZH} t_{PZL}	3-State output enable time $\overline{OE}$ to Qn	4, 5			8.0		9.0	ns
t_{PHZ} t_{PLZ}	3-State output disable time $\overline{OE}$ to Qn	4, 5			7.5		8.5	ns
t_W	LE pulse width HIGH	2	3.0			4.0		ns
t_{SU}	Set-up time Dn to LE	3	2.2			2.5		ns
t_h	hold time Dn to LE	3	2.2			2.5		ns

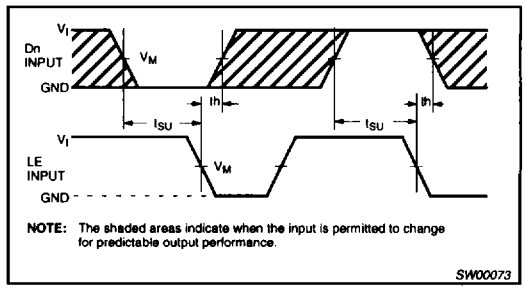
NOTE:
1. All typical values are at V_{CC} = 3.3V and T_{amb} = 25°C.

AC WAVEFORMS

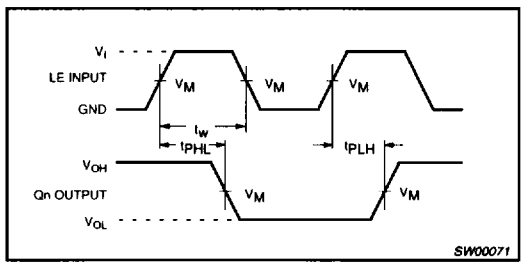
V_M = 1.5V at $V_{CC} \geq$ 2.7V; V_M = 0.5 V_{CC} at V_{CC} < 2.7V.
V_{OL} and V_{OH} are the typical output voltage drop that occur with the output load.
$V_X = V_{OL}$ + 0.3V at $V_{CC} \geq$ 2.7V; $V_X = V_{OL}$ + 0.1 V_{CC} at V_{CC} < 2.7V
$V_Y = V_{OH}$ −0.3V at $V_{CC} \geq$ 2.7V; $V_Y = V_{OH}$ − 0.1 V_{CC} at V_{CC} < 2.7V



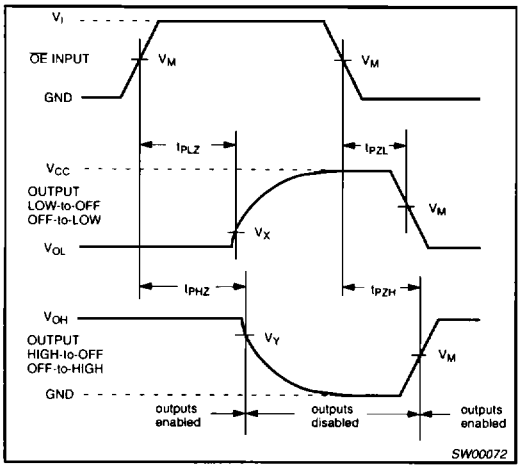
Waveform 1. Waveforms showing the input (Dn) to output (Qn) propagation delays



Waveform 3. Waveforms showing the data set-up and hold times for the Dn input to the LE input

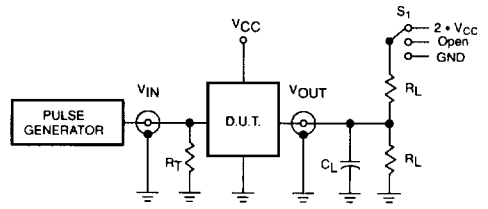


Waveform 2. Waveforms showing the latch enable input (LE) pulse width, the latch enable input to output (Qn) propagation delays



Waveform 4. Waveforms showing the 3-State enable and disable times

TEST CIRCUIT



Test Circuit for 3-State Outputs

SWITCH POSITION

TEST	SWITCH
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	2 * V_{CC}
t_{PHZ}/t_{PZH}	GND

V_{CC}	V_I
< 2.7V	V_{CC}
2.7 – 3.6V	2.7V

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.
C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.
R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

SW00047

Waveform 5. Load circuitry for switching times