ANALOG DEVICES

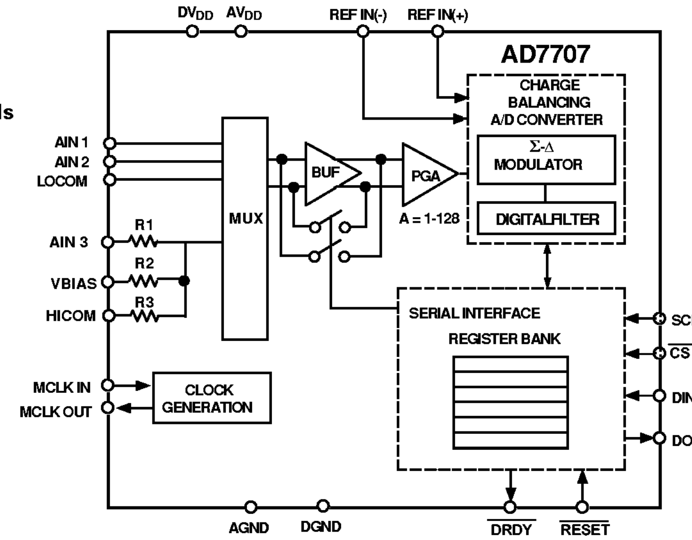
3V/5V, ± 10V Input Range, 1mW 3-Channel 16-Bit, Sigma-Delta ADC

Preliminary Technical Information — AD7707*

FEATURES

- Charge Balancing ADC
  - 16 Bits No Missing Codes
  - 0.003% Nonlinearity
- High Level (±10V) and Low Level (±10mV) Input Channels
- Programmable Gain Front End
  - Gains from 1 to 128
- Three-Wire Serial Interface
  - SPI™, QSPI™, MICROWIRE™ and DSP Compatible
  - Schmitt Trigger Input on SCLK
- Ability to Buffer the Analog Input
- 2.7 V to 3.3 V or 4.75 V to 5.25 V Operation
- Power Dissipation 1 mW max @ 3 V
- Standby Current 8 uA max
- 20-Lead SOIC and TSSOP Packages

FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The AD7707 is a complete analog front end for low frequency measurement applications. This three-channel device can accept either low level input signals directly from a transducer or high level (± 4 x V_{BIAS}) signals and produce a serial digital output. It employs a sigma-delta conversion technique to realize up to 16 bits of no missing codes performance. The selected input signal is applied to a proprietary programmable gain front end based around an analog modulator. The modulator output is processed by an on-chip digital filter. The first notch of this digital filter can be programmed via an on-chip control register allowing adjustment of the filter cutoff and output update rate.

The AD7707 operates from a single 2.7 V to 3.3 V or 4.75 V to 5.25 V supply. The AD7707 features two low level pseudo differential analog input channels, one high level input channel and a differential reference input. Input signal ranges of 0mV to +20mV through 0V to +2.5V can be incorporated on both low level input channels when operating with a V_{DD} of 5 V and a reference of 2.5 V. They can also handle bipolar input signal ranges of ± 20 mV through ± 2.5 V, which are referenced to the LCOM input. The AD7707, with 3 V supply and a 1.225 V reference, can handle unipolar input signal ranges of 0mV to +10mV through 0V to +1.225V. Its bipolar input signal ranges are ±10mV through ±1.225V.

The high level input channel can accept input signal ranges of ±10V, ±5V and 0 to 5V. The AD7707 thus perform all signal conditioning and conversion for a three-channel system.

The AD7707 is ideal for use in smart, microcontroller or DSP-based systems. It features a serial interface that can be configured for three-wire operation. Gain settings, signal polarity and update rate selection can be configured in software using the input serial port. The part contains self-calibration and system calibration options to eliminate gain and offset errors on the part itself or in the system.

CMOS construction ensures very low power dissipation, and the power-down mode reduces the standby power consumption to 20 µW typ. These parts are available in a 20-lead wide body (0.3 inch) small outline (SOIC) package and a low profile 20-lead TSSOP.

PRODUCT HIGHLIGHTS

1. The AD7707 consumes less than 1 mW at 3 V supplies and 1 MHz master clock, making it ideal for use in low power systems. Standby current is less than 8 µA.
2. On-board thin-film resistors allow ±10V, ±5V and 0 to 5V high level input signals to be directly accomodated on the analog inputs without requiring split supplies on dc-dc converters.
3. The low level input channels allow the AD7707 to accept input signals directly from a strain gauge or transducer removing a considerable amount of signal conditioning.
4. The part features excellent static performance specifications with 16 bits, no-missing-codes, ±0.003% accuracy and low rms noise (<600 nV). Endpoint errors and the effects of temperature drift are eliminated by on-chip calibration options, which remove zero-scale and full-scale errors.

*Protected by U.S. Patent Number 5,134,401.
SPI and QSPI are trademarks of Motorola.
MICROWIRE is a trademark of National Semiconductor.

PRELIM A2. 9/98

One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.
Tel: 781/329-4700 World Wide Web Site: http://www.analog.com
Fax: 781/326-8703

AD7707–SPECIFICATIONS

($AV_{DD} = DV_{DD}$ = +3 V or 5 V, REF IN(+) = +1.225 V with AV_{DD} = 3 V and +2.5 V with AV_{DD} = 5 V; REF IN(–) = GND; MCLK IN = 2.4576 MHz unless otherwise noted. All specifications T_{MIN} to T_{MAX} unless otherwise noted.)

Parameter	B Version[1]	Units	Conditions/Comments
STATIC PERFORMANCE			
No Missing Codes	16	Bits min	Guaranteed by Design. Filter Notch < 60 Hz
Output Noise	See Tables I and III		Depends on Filter Cutoffs and Selected Gain
Integral Nonlinearity[2]	±0.003	% of FSR max	Filter Notch < 60 Hz. Typically ±0.0003%
Unipolar Offset Error	See Note 3		
Unipolar Offset Drift[4]	0.5	μV/°C typ	
Bipolar Zero Error	See Note 3		
Bipolar Zero Drift[4]	0.5	μV/°C typ	For Gains 1, 2 and 4
	0.1	μV/°C typ	For Gains 8, 16, 32, 64 and 128
Positive Full-Scale Error[5]	See Note 3		
Full-Scale Drift[4, 6]	0.5	μV/°C typ	
Gain Error[7]	See Note 3		
Gain Drift[4, 8]	0.5	ppm of FSR/°C typ	
Bipolar Negative Full-Scale Error[2, 3]	±0.003	% of FSR typ	Typically ±0.001%
Bipolar Negative Full-Scale Drift[4]	1	μV/°C typ	For Gains of 1 to 4
	0.6	μV/°C typ	For Gains of 8 to 128
ANALOG INPUTS/REFERENCE INPUTS			Specifications for AIN and REF IN Unless Noted
Common-Mode Rejection (CMR)[2]			
V_{DD} = 5 V			
Gain = 1	96	dB typ	
Gain = 2	105	dB typ	
Gain = 4	110	dB typ	
Gain = 8v128	130	dB typ	
V_{DD} = 3 V			
Gain = 1	105	dB typ	
Gain = 2	110	dB typ	
Gain = 4	120	dB typ	
Gain = 8v128	130	dB typ	
Normal-Mode 50 Hz Rejection[2]	98	dB typ	For Filter Notches of 25 Hz, 50 Hz, ±0.02 ∞ f_{NOTCH}
Normal-Mode 60 Hz Rejection[2]	98	dB typ	For Filter Notches of 20 Hz, 60 Hz, ±0.02 ∞ f_{NOTCH}
Common-Mode 50 Hz Rejection[2]	150	dB typ	For Filter Notches of 25 Hz, 50 Hz, ±0.02 ∞ f_{NOTCH}
Common-Mode 60 Hz Rejection[2]	150	dB typ	For Filter Notches of 20 Hz, 60 Hz, ±0.02 ∞ f_{NOTCH}
Absolute/Common-Mode REF IN Voltage[2]	GND to V_{DD}	V min to V max	
Low Level Analog Input Channels (AIN1 & AIN2)			
Absolute/Common-Mode AIN Voltage[2, 9]	GND – 30 mV	V min	BUF Bit of Setup Register = 0
	V_{DD} + 30 mV	V max	
Absolute/Common-Mode AIN Voltage[2, 9]	GND + 50 mV	V min	BUF Bit of Setup Register = 1
	V_{DD} – 1.5 V	V max	
AIN DC Input Current[2]	1	nA max	
AIN Sampling Capacitance[2]	10	pF max	
AIN Differential Voltage Range[10]	0 to +V_{REF}/GAIN[11]	nom	Unipolar Input Range (B/U Bit of Setup Register = 1)
	±V_{REF}/GAIN	nom	Bipolar Input Range (B/U Bit of Setup Register = 0)
AIN Input Sampling Rate, f_S	GAIN ∞ f_{CLKIN}/64		For Gains of 1 to 4
	f_{CLKIN}/8		For Gains of 8 to 128
High Level Analog Input Channel (AIN3)			
Absolute/Common-Mode AIN Voltage[2, 9]	X mV	V min	BUF Bit of Setup Register = 0
	4*(V_{DD} + 30 mV)	V max	
Absolute/Common-Mode AIN Voltage[2, 9]	X	V min	BUF Bit of Setup Register = 1
	4*(V_{DD} – 1.5 V)	V max	
AIN DC Input Current[2]	TBD	nA max	
AIN Sampling Capacitance[2]	10	pF max	
AIN Differential Voltage Range[10]	0 to +4*V_{REF}/GAIN[11]	nom	Unipolar Input Range (B/U Bit of Setup Register = 1)
	±4*V_{REF}/GAIN	nom	Bipolar Input Range (B/U Bit of Setup Register = 0)
AIN Input Sampling Rate, f_S	GAIN ∞ f_{CLKIN}/64		For Gains of 1 to 4
	f_{CLKIN}/8		For Gains of 8 to 128
Reference Input Range			
REF IN(+) – REF IN(–) Voltage	1/1.75	V min/max	AV_{DD} = 2.7 V to 3.3 V. V_{REF} = 1.225 ± 1% for Specified Performance
REF IN(+) – REF IN(–) Voltage	1/3.5	V min/max	AV_{DD} = 4.75 V to 5.25 V. V_{REF} = 2.5 ± 1% for Specified Performance
REF IN Input Sampling Rate, f_S	f_{CLKIN}/64		
LOGIC INPUTS			
Input Current			
All Inputs Except MCLK IN	±1	μA max	Typically ±20 nA
MCLK	±10	μA max	Typically ±2 μA
All Inputs Except SCLK and MCLK IN			
V_{INL}, Input Low Voltage	0.8	V max	DV_{DD} = 5 V
	0.4	V max	DV_{DD} = 3 V
V_{INH}, Input High Voltage	2.0	V min	DV_{DD} = 3 V and 5 V

Parameter	B Version[1]	Units	Conditions/Comments
SCLK Only (Schmitt Triggered Input)			DV_{DD} = 5 V NOMINAL
V_{T+}	1.4/3	V min/V max	
V_{T-}	0.8/1.4	V min/V max	
$V_{T+} - V_{T-}$	0.4/0.8	V min/V max	
SCLK Only (Schmitt Triggered Input)			DV_{DD} = 3 V NOMINAL
V_{T+}	1/2.5	V min/V max	
V_{T-}	0.4/1.1	V min/V max	
$V_{T+} - V_{T-}$	0.375/0.8	V min/V max	
MCLK IN Only			DV_{DD} = 5 V NOMINAL
V_{INL}, Input Low Voltage	0.8	V max	
V_{INH}, Input High Voltage	3.5	V min	
MCLK IN Only			DV_{DD} = 3 V NOMINAL
V_{INL}, Input Low Voltage	0.4	V max	
V_{INH}, Input High Voltage	2.5	V min	
LOGIC OUTPUTS (Including MCLK OUT)			
V_{OL}, Output Low Voltage	0.4	V max	I_{SINK} = 800 µA Except for MCLK OUT.[12] DV_{DD} = 5 V.
V_{OL}, Output Low Voltage	0.4	V max	I_{SINK} = 100 µA Except for MCLK OUT.[12] DV_{DD} = 3 V.
V_{OH}, Output High Voltage	4	V min	I_{SOURCE} = 200 µA Except for MCLK OUT.[12] DV_{DD} = 5 V.
V_{OH}, Output High Voltage	DV_{DD} −0.6	V min	I_{SOURCE} = 100 µA Except for MCLK OUT.[12] DV_{DD} = 3 V.
Floating State Leakage Current	±10	µA max	
Floating State Output Capacitance[13]	9	pF typ	
Data Output Coding	Binary		Unipolar Mode
	Offset Binary		Bipolar Mode
SYSTEM CALIBRATION			
Low Level Input Channels (AIN1 & AIN2)			
Positive Full-Scale Calibration Limit[14]	(1.05 X V_{REF})/GAIN	V max	GAIN Is the Selected PGA Gain (1 to 128)
Negative Full-Scale Calibration Limit[14]	−(1.05 X V_{REF})/GAIN	V max	GAIN Is the Selected PGA Gain (1 to 128)
Offset Calibration Limit[14]	−(1.05 X V_{REF})/GAIN	V max	GAIN Is the Selected PGA Gain (1 to 128)
Input Span[15]	(0.8 X V_{REF})/GAIN	V min	GAIN Is the Selected PGA Gain (1 to 128)
	(2.1 X V_{REF})/GAIN	V max	GAIN Is the Selected PGA Gain (1 to 128)
High Level Input Channels (AIN3)			
Positive Full-Scale Calibration Limit[14]	(4.2 X V_{REF})/GAIN	V max	GAIN Is the Selected PGA Gain (1 to 128)
Negative Full-Scale Calibration Limit[14]	−(4.2 X V_{REF})/GAIN	V max	GAIN Is the Selected PGA Gain (1 to 128)
Offset Calibration Limit[14]	−(4.2 X V_{REF})/GAIN	V max	GAIN Is the Selected PGA Gain (1 to 128)
Input Span[15]	(3.2 X V_{REF})/GAIN	V min	GAIN Is the Selected PGA Gain (1 to 128)
	(8.4 X V_{REF})/GAIN	V max	GAIN Is the Selected PGA Gain (1 to 128)
POWER REQUIREMENTS			
Power Supply Voltages			
AV_{DD} Voltage	+2.7 to +3.3 or		
	+4.75 to +5.25	V	For Specified Performance
DV_{DD} Voltage	+2.7 to +5.25	V	For Specified Performance
Power Supply Currents			
AV_{DD} Current			AV_{DD} = 3 V or 5 V. BST bit of Filter High Register = 0[17]
	0.27	mA max	Typically 0.22mA. BUFFER = 0. $f_{CLK\ IN}$ = 1MHz or 2.4576MHz
	0.6	mA max	Typically 0.45mA. BUFFER = DV_{DD}. $f_{CLK\ IN}$ = 1MHz or 2.4576MHz
			AV_{DD} = 3V or 5V. BST bit of Filter High Register = 1[17]
	0.5	mA max	Typically 0.38 mA. BUFFER = 0V. $f_{CLK\ IN}$ = 2.4576 MHz
	1.1	mA max	Typically 0.81 mA. BUFFER = DV_{DD}. $f_{CLK\ IN}$ = 2.4576 MHz
DV_{DD} Current[18]			Digital I/Ps = 0 V or DV_{DD}. External MCLK IN
	0.080	mA max	Typically 0.06 mA. DV_{DD} = 3 V. $f_{CLK\ IN}$ = 1 MHz
	0.15	mA max	Typically 0.13 mA. DV_{DD} = 5 V. $f_{CLK\ IN}$ = 1 MHz
	0.18	mA max	Typically 0.15 mA. DV_{DD} = 3 V. $f_{CLK\ IN}$ = 2.4576 MHz
	0.35	mA max	Typically 0.3 mA. DV_{DD} = 5 V. $f_{CLK\ IN}$ = 2.4576 MHz
Power Supply Rejection[19]	See Note 20	dB typ	
Normal Mode Power Dissipation[18]			AV_{DD} = DV_{DD} = +3V. Digital I/Ps = 0V or DV_{DD} External MCLK IN
	1.05	mW max	Typically 0.84mW. BUFFER = 0. $f_{CLK\ IN}$ = 1 MHz, BST Bit = 0.
	2.04	mW max	Typically 1.53mW. BUFFER = 3V. $f_{CLK\ IN}$ = 1 MHz, BST Bit = 0.
	1.35	mW max	Typically 1.11mW. BUFFER = 0. $f_{CLK\ IN}$ = 2.4576MHz, BST Bit = 0.
	2.34	mW max	Typically 1.9mW. BUFFER = 3V. $f_{CLK\ IN}$ = 2.4576MHz, BST Bit = 0.
Normal Mode Power Dissipation[18]			AV_{DD} = DV_{DD} = +5V. Digital I/Ps = 0 V or DV_{DD} External MCLK IN
	2.1	mW max	Typically 1.75mW. BUFFER = 0. $f_{CLK\ IN}$ = 1 MHz, BST Bit = 0.
	3.75	mW max	Typically 2.9mW. BUFFER = 5V. $f_{CLK\ IN}$ = 1 MHz, BST Bit = 0.
	3.1	mW max	Typically 2.6mW. BUFFER = 0. $f_{CLK\ IN}$ = 2.4576MHz, BST Bit = 0.
	4.75	mW max	Typically 3.75mW. BUFFER = 5V. $f_{CLK\ IN}$ = 2.4576MHz, BST Bit = 0.
Standby (Power-Down) Current[21]	18	µA max	External MCLK IN = 0 V or DV_{DD}. Typically 9 µA. V_{DD} = +5V
Standby (Power-Down) Current[21]	8	µA max	External MCLK IN = 0 V or DV_{DD}. Typically 4 µA. V_{DD} = +3V

Power Supply Rejection[18]	See Note 19	dB typ

NOTES

[1]Temperature range as follows: B Version, –40°C to +85°C.

[2]These numbers are established from characterization or design at initial product release.

[3]A calibration is effectively a conversion so these errors will be of the order of the conversion noise shown in Tables I to IV. This applies after calibration at the temperature of interest.

[4]Recalibration at any temperature will remove these drift errors.

[5]Positive Full-Scale Error includes Zero-Scale Errors (Unipolar Offset Error or Bipolar Zero Error) and applies to both unipolar and bipolar input ranges.

[6]Full-Scale Drift includes Zero-Scale Drift (Unipolar Offset Drift or Bipolar Zero Drift) and applies to both unipolar and bipolar input ranges.

[7]Gain Error does not include Zero-Scale Errors. It is calculated as Full-Scale Error–Unipolar Offset Error for unipolar ranges and Full-Scale Error–Bipolar Zero Error for bipolar ranges.

[8]Gain Error Drift does not include Unipolar Offset Drift/Bipolar Zero Drift. It is effectively the drift of the part if zero scale calibrations only were performed.

[9]This common-mode voltage range is allowed provided that the input voltage on analog inputs does not go more positive than V_{DD} + 30 mV or go more negative than GND – 30 mV. Parts are functional with voltages down to GND – 200 mV, but with increased leakage at high temperature.

[10]The analog input voltage range on AIN(+) is given here with respect to the voltage on LCOM on the low level input channels (Ain1 and Ain2) and is given with respect to the HCOM input on the high level input channel Ain3. The absolute voltage on the low level analog inputs should not go more positive than V_{DD} + 30 mV, or go more negative than GND – 30 mV for specified performance, input voltages of GND – 200 mV can be accommodated, but with increased leakage at high temperature.

[11]V_{REF} = REF IN(+) – REF IN(–).

[12]These logic output levels apply to the MCLK OUT only when it is loaded with one CMOS load.

[13]Sample tested at +25°C to ensure compliance.

[14]After calibration, if the analog input exceeds positive full scale, the converter will output all 1s. If the analog input is less than negative full scale, the device will output all 0s.

[15]These calibration and span limits apply provided the absolute voltage on the analog inputs does not exceed V_{DD} + 30 mV or go more negative than GND – 30 mV. The offset calibration limit applies to both the unipolar zero point and the bipolar zero point.

[16]When using a crystal or ceramic resonator across the MCLK pins as the clock source for the device, the V_{DD} current and power dissipation will vary depending on the crystal or resonator type (see Clocking and Oscillator Circuit section).

[17]If the external master clock continues to run in standby mode, the standby current increases to 150 µA typical at 5 V and 75 µA at 3 V. When using a crystal or ceramic resonator across the MCLK pins as the clock source for the device, the internal oscillator continues to run in standby mode and the power dissipation depends on the crystal or resonator type (see Standby Mode section).

[18]Measured at dc and applies in the selected passband. PSRR at 50 Hz will exceed 120 dB with filter notches of 25 Hz or 50 Hz. PSRR at 60 Hz will exceed 120 dB with filter notches of 20 Hz or 60 Hz.

[19]PSRR depends on both gain and V_{DD}.

Gain	1	2	4	8–128
V_{DD} = 3 V	86	78	85	93
V_{DD} = 5 V	90	78	84	91

Specifications subject to change without notice.

TIMING CHARACTERISTICS[1, 2] ($AV_{DD} = DV_{DD}$ = +2.7 V to +5.25 V; AGND = DGND = 0 V; f_{CLKIN} = 2.4576 MHz; Input Logic 0 = 0 V, Logic 1 = DV_{DD} unless otherwise noted.)

Parameter	Limit at T_{MIN}, T_{MAX} (B Version)	Units	Conditions/Comments
f_{CLKIN}[3, 4]	400	kHz min	Master Clock Frequency: Crystal Oscillator or Externally Supplied
	5	MHz max	for Specified Performance
$t_{CLKIN LO}$	0.4 ∞ t_{CLKIN}	ns min	Master Clock Input Low Time. t_{CLKIN} = $1/f_{CLKIN}$
$t_{CLKIN HI}$	0.4 ∞ t_{CLKIN}	ns min	Master Clock Input High Time
t_1	500 ∞ t_{CLKIN}	ns nom	$\overline{DRDY}$ High Time
t_2	100	ns min	RESET Pulsewidth
Read Operation			
t_3	0	ns min	DRDY to CS Setup Time
t_4	120	ns min	CS Falling Edge to SCLK Rising Edge Setup Time
t_5[5]	0	ns min	SCLK Falling Edge to Data Valid Delay
	80	ns max	V_{DD} = +5 V
	100	ns max	V_{DD} = +3.0 V
t_6	100	ns min	SCLK High Pulsewidth
t_7	100	ns min	SCLK Low Pulsewidth
t_8	0	ns min	$\overline{CS}$ Rising Edge to SCLK Rising Edge Hold Time
t_9[6]	10	ns min	Bus Relinquish Time after SCLK Rising Edge
	60	ns max	V_{DD} = +5 V
	100	ns max	V_{DD} = +3.0 V
t_{10}	100	ns max	SCLK Falling Edge to DRDY High[7]
Write Operation			
t_{11}	120	ns min	CS Falling Edge to SCLK Rising Edge Setup Time
t_{12}	30	ns min	Data Valid to SCLK Rising Edge Setup Time
t_{13}	20	ns min	Data Valid to SCLK Rising Edge Hold Time
t_{14}	100	ns min	SCLK High Pulsewidth
t_{15}	100	ns min	SCLK Low Pulsewidth
t_{16}	0	ns min	CS Rising Edge to SCLK Rising Edge Hold Time

NOTES

[1] Sample tested at +25°C to ensure compliance. All input signals are specified with tr = tf = 5 ns (10% to 90% of V_{DD}) and timed from a voltage level of 1.6 V.

[2] See Figures 16 and 17.

[3] $f_{CLK IN}$ Duty Cycle range is 45% to 55%. $f_{CLK IN}$ must be supplied whenever the AD7705/AD7706 is not in Standby mode. If no clock is present in this case, the device can draw higher current than specified and possibly become uncalibrated.

[4] The AD7707 is production tested with $f_{CLK IN}$ at 2.4576 MHz (1 MHz for some I_{DD} tests). It is guaranteed by characterization to operate at 400 kHz.

[5] These numbers are measured with the load circuit of Figure 1 and defined as the time required for the output to cross the V_{OL} or V_{OH} limits.

[6] These numbers are derived from the measured time taken by the data output to change 0.5 V when loaded with the circuit of Figure 1. The measured number is then extrapolated back to remove effects of charging or discharging the 50 pF capacitor. This means that the times quoted in the timing characteristics are the true bus relinquish times of the part and as such are independent of external bus loading capacitances.

[7] DRDY returns high after the first read from the device after an output update. The same data can be read again, if required, while DRDY is high, although care should be taken that subsequent reads do not occur close to the next output update.

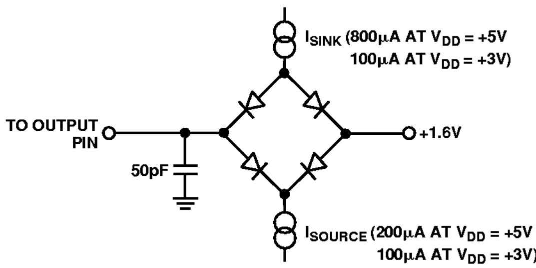


Figure 1. Load Circuit for Access Time and Bus Relinquish Time

ABSOLUTE MAXIMUM RATINGS*

(T_A = +25°C unless otherwise noted)

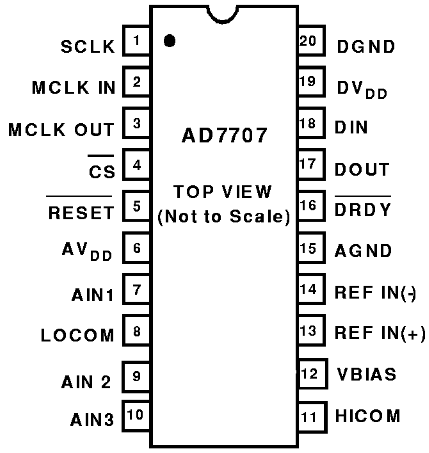
AV_{DD} to AGND . . . . –0.3 V to +7 V
AV_{DD} to DGND . . . . –0.3 V to +7 V
DV_{DD} to AGND . . . . –0.3 V to +7 V
DV_{DD} to DGND . . . . –0.3 V to +7 V
DGND to AGND . . . . –0.3 V to +7 V
Analog Input Voltage to AGND . . –0.3 V to V_{DD} + 0.3 V
Reference Input Voltage to AGND –0.3 V to V_{DD} + 0.3 V
Digital Input Voltage to DGND . . –0.3 V to V_{DD} + 0.3 V
Digital Output Voltage to DGND . –0.3 V to V_{DD} + 0.3 V
Operating Temperature Range
  Commercial (B Version) . . . . –40°C to +85°C
Storage Temperature Range . . . . –65°C to +150°C
Junction Temperature . . . . +150°C
Plastic DIP Package, Power Dissipation . . . . 450 mW
  θ_{JA} Thermal Impedance . . . . 105°C/W
  Lead Temperature, (Soldering, 10 sec) . . . . . . +260°C
SOIC Package, Power Dissipation . . . . 450 mW
  θ_{JA} Thermal Impedance . . . . 75°C/W
  Lead Temperature, Soldering
    Vapor Phase (60 sec) . . . . +215°C
    Infrared (15 sec) . . . . +220°C
TSSOP Package, Power Dissipation . . . . 450 mW
  θ_{JA} Thermal Impedance . . . . 139°C/W
  Lead Temperature, Soldering
    Vapor Phase (60 sec) . . . . +215°C
    Infrared (15 sec) . . . . +220°C
ESD Rating . . . . >4000 V

*Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ORDERING GUIDE

Model	V_{DD} Supply	Temperature Range	Package Description	Package Options
AD7707BR	2.7 V to 5.25 V	–40°C to +85°C	SOIC	R-20
AD7707BRU	2.7 V to 5.25 V	–40°C to +85°C	TSSOP	RU-20
EVAL-AD7707EB		Evaluation Board		

PIN CONFIGURATIONS



PIN FUNCTION DESCRIPTIONS

Pin No.	Mnemonic	Function
1	SCLK	Serial Clock. Schmitt-Triggered Logic Input. An external serial clock is applied to this input to access serial data from the AD7707. This serial clock can be a continuous clock with all data transmitted in a continuous train of pulses. Alternatively, it can be a noncontinuous clock with the information being transmitted to the AD7707 in smaller batches of data.
2	MCLK IN	Master Clock signal for the device. This can be provided in the form of a crystal/resonator or external clock. A crystal/resonator can be tied across the MCLK IN and MCLK OUT pins. Alternatively, the MCLK IN pin can be driven with a CMOS-compatible clock and MCLK OUT left unconnected. The part can be operated with clock frequencies in the range 500 kHz to 5 MHz.
3	MCLK OUT	When the master clock for the device is a crystal/resonator, the crystal/resonator is connected between MCLK IN and MCLK OUT. If an external clock is applied to MCLK IN, MCLK OUT provides an inverted clock signal. This clock can be used to provide a clock source for external circuitry and is capable of driving one CMOS load. If the user does not require it, this MCLK OUT can be turned off via the CLK DIS bit of the Clock Register. This ensures that the part is not burning unnecessary power driving capacitive loads on MCLK OUT.
4	CS	Chip Select. Active low Logic Input used to select the AD7707. With this input hard-wired low, the AD7707 can operate in its three-wire interface mode with SCLK, DIN and DOUT used to interface to the device. CS can be used to select the device in systems with more than one device on the serial bus or as a frame synchronization signal in communicating with the AD7707.
5	RESET	Logic Input. Active low input that resets the control logic, interface logic, calibration coefficients, digital filter and analog modulator of the part to power-on status.
6	AV_{DD}	Analog Supply Voltage, +2.7 V to +5.25 V operation.
7	AIN1	Low Level Analog Input Channel 1.
8	LOCOM	COMMON Input for low level input channels. Analog inputs on Ain1 and Ain2 must be referenced to this input.
9	AIN2	Low Level Analog Input Channel 2.
10	AIN3	High Level Analog Input Channel 3.
11	HICOM	COMMON Input for high level input channel. Analog input on Ain3 must be referenced to this input.
12	VBIAS	VBIAS is used to signal condition the high level input channel signal. This signal is used to ensure that the AIN(+) and AIN(–) signals seen by the internal buffer are within its common mode range. VBIAS is normally connected to the REF IN(+).
13	REF IN(+)	Reference Input. Positive input of the differential reference input to the AD7707. The reference input is differential with the provision that REF IN(+) must be greater than REF IN(–). REF IN(+) can lie anywhere between AV_{DD} and AGND.

Pin No.	Mnemonic	Function
14	REF IN (–)	Reference Input. Negative input of the differential reference input to the AD7707. The REF IN (–) can lie anywhere between AV_{DD} and AGND provided REF IN (+) is greater than REF IN (–).
15	AGND	Analog Ground. Ground reference point for the AD7707's internal analog circuitry.
16	DRDY	Logic Output. A logic low on this output indicates that a new output word is available from the AD7707 data register. The DRDY pin will return high upon completion of a read operation of a full output word. If no data read has taken place between output updates, the DRDY line will return high for 500 ∞ $t_{CLK\ IN}$ cycles prior to the next output update. While DRDY is high, a read operation should neither be attempted nor in progress to avoid reading from the data register as it is being updated. The DRDY line will return low again when the update has taken place. DRDY is also used to indicate when the AD7707 has completed its on-chip calibration sequence.
17	DOUT	Serial Data Output with serial data being read from the output shift register on the part. This output shift register can contain information from the setup register, communications register, clock register or data register, depending on the register selection bits of the Communications Register.
18	DIN	Serial Data Input with serial data being written to the input shift register on the part. Data from this input shift register is transferred to the setup register, clock register or communications register, depending, on the register selection bits of the Communications Register.
19	DV_{DD}	Digital Supply Voltage, +2.7 V to +5.25 V operation.
20	DGND	Ground reference point for the AD7707's internal digital circuitry.

OUTPUT NOISE (5 V OPERATION)

Table I shows the AD7707 output rms noise for the selectable notch and –3 dB frequencies for the part, as selected by FS0 and FS1 of the Clock Register. The numbers given are for the bipolar input ranges with a V_{REF} of +2.5 V and V_{DD} = 5 V. These numbers are typical and are generated at an analog input voltage of 0 V with the part used in either buffered or unbuffered mode. Table II meanwhile shows the output *peak-to-peak* noise for the selectable notch and –3 dB frequencies for the part. *It is important to note that these numbers represent the resolution for which there will be no code flicker. They are not calculated based on rms noise but on peak-to-peak noise*. The numbers given are for bipolar input ranges with a V_{REF} of +2.5 V and for either buffered or unbuffered mode. These numbers are typical and are rounded to the nearest LSB. The numbers apply for the CLK DIV bit of the Clock Register set to 0.

Table I. Output RMS Noise vs. Gain and Output Update Rate @ 5 V

Filter First Notch and O/P Data Rate	–3 dB Frequency	Typical Output RMS Noise in uV Gain of 1	Gain of 2	Gain of 4	Gain of 8	Gain of 16	Gain of 32	Gain of 64	Gain of 128
MCLK IN = 2.4576 MHz									
10 Hz	2.62 Hz	1.7	1	0.7	0.46	0.45	0.4	0.4	0.4
50 Hz	13.1 Hz	4.1	2.1	1.2	0.75	0.7	0.66	0.63	0.6
60 Hz	15.72 Hz	5.1	2.5	1.4	0.8	0.75	0.7	0.67	0.62
250 Hz	65.5 Hz	110	49	31	17	8	3.6	2.3	1.7
500 Hz	131 Hz	550	285	145	70	41	22	9.1	4.7
MCLK IN = 1 MHz									
4.05 Hz	1.06 Hz	1.7	1	0.7	0.46	0.45	0.4	0.4	0.4
20 Hz	5.24 Hz	4.1	2.1	1.2	0.75	0.7	0.66	0.63	0.6
25 Hz	6.55 Hz	5.1	2.5	1.4	0.8	0.75	0.7	0.67	0.62
100 Hz	26.2 Hz	110	49	31	17	8	3.6	2.3	1.7
200 Hz	52.4 Hz	550	285	145	70	41	22	9.1	4.7

Table II. Peak-to-Peak Resolution vs. Gain and Output Update Rate @ 5 V

Filter First Notch and O/P Data Rate	-3 dB Frequency	Typical Peak-to-Peak Resolution Bits Gain of 1	Gain of 2	Gain of 4	Gain of 8	Gain of 16	Gain of 32	Gain of 64	Gain of 128
MCLK IN = 2.4576 MHz									
10 Hz	2.62 Hz	16	16	16	16	16	16	15	14
50 Hz	13.1 Hz	16	16	16	16	16	16	15	14
60 Hz	15.72 Hz	16	16	16	16	15	14	14	13
250 Hz	65.5 Hz	13	13	13	13	13	13	12	12
500 Hz	131 Hz	10	10	10	10	10	10	10	10
MCLK IN = 1 MHz									
4.05 Hz	1.06 Hz	16	16	16	16	16	16	15	14
20 Hz	5.24 Hz	16	16	16	16	16	16	15	14
25 Hz	6.55 Hz	16	16	16	16	15	14	14	13
100 Hz	26.2 Hz	13	13	13	13	13	13	12	12
200 Hz	52.4 Hz	10	10	10	10	10	10	10	10

OUTPUT NOISE (3 V OPERATION)

Table III shows the AD7707 output rms noise for the selectable notch and −3 dB frequencies for the part, as selected by FS0 and FS1 of the Clock Register. The numbers given are for the bipolar input ranges with a V_{REF} of +1.225 V and a V_{DD} = 3 V. These numbers are typical and are generated at an analog input voltage of 0 V with the part used in either buffered or unbuffered mode. Table II meanwhile shows the output *peak-to-peak* noise for the selectable notch and −3 dB frequencies for the part. *It is important to note that these numbers represent the resolution for which there will be no code flicker. They are not calculated based on rms noise but on peak-to-peak noise.* The numbers given are for bipolar input ranges with a V_{REF} of +1.225 V and for either buffered or unbuffered mode. These numbers are typical and are rounded to the nearest LSB. The numbers apply for the CLK DIV bit of the Clock Register set to 0.

Table III. Output RMS Noise vs. Gain and Output Update Rate @ 3 V

Filter First Notch and O/P Data Rate	-3 dB Frequency	Typical Output RMS Noise in uV Gain of 1	Gain of 2	Gain of 4	Gain of 8	Gain of 16	Gain of 32	Gain of 64	Gain of 128
MCLK IN = 2.4576 MHz									
10 Hz	2.62 Hz	1.68	1.33	0.73	0.5	0.49	0.49	0.48	0.47
50 Hz	13.1 Hz	3.8	2.4	1.5	1.3	1.1	1.0	0.9	0.9
60 Hz	15.72 Hz	5.1	2.9	1.7	1.5	1.2	1.0	0.9	0.9
250 Hz	65.5 Hz	50	25	14	9.9	5.1	2.6	2.3	2.0
500 Hz	131 Hz	270	135	65	41	22	9.7	5.1	3.3
MCLK IN = 1 MHz									
4.05 Hz	1.06 Hz	1.68	1.33	0.73	0.5	0.49	0.49	0.48	0.47
20 Hz	5.24 Hz	3.8	2.4	1.5	1.3	1.1	1.0	0.9	0.9
25 Hz	6.55 Hz	5.1	2.9	1.7	1.5	1.2	1.0	0.9	0.9
100 Hz	26.2 Hz	50	25	14	9.9	5.1	2.6	2.3	2.0
200 Hz	52.4 Hz	270	135	65	41	22	9.7	5.1	3.3

Table IV. Peak-to-Peak Resolution vs. Gain and Output Update Rate @ 3 V

Filter First Notch and O/P Data Rate	-3 dB Frequency	Typical Peak-to-Peak Resolution in Bits Gain of 1	Gain of 2	Gain of 4	Gain of 8	Gain of 16	Gain of 32	Gain of 64	Gain of 128
MCLK IN = 2.4576 MHz									
10 Hz	2.62 Hz	16	16	15	15	14	13	13	12
50 Hz	13.1 Hz	16	16	15	15	14	13	13	12
60 Hz	15.72 Hz	16	16	15	14	14	13	13	12
250 Hz	65.5 Hz	13	13	13	13	12	12	11	11
500 Hz	131 Hz	10	10	10	10	10	10	10	10
MCLK IN = 1 MHz									
4.05 Hz	1.06 Hz	16	16	15	15	14	13	13	12
20 Hz	5.24 Hz	16	16	15	15	14	13	13	12
25 Hz	6.55 Hz	16	16	15	14	14	13	13	12
100 Hz	26.2 Hz	13	13	13	13	12	12	11	11
200 Hz	52.4 Hz	10	10	10	10	10	10	10	10

Typical Performance Characteristics–

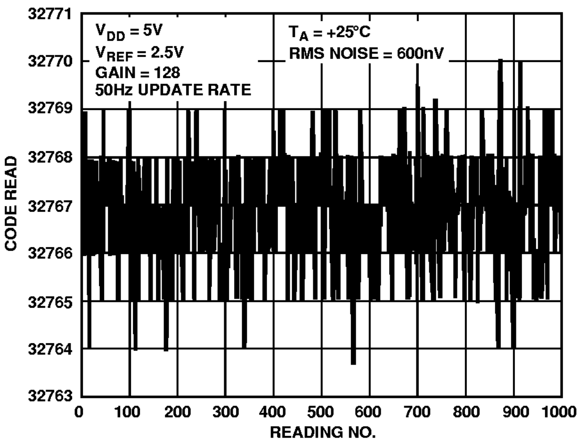


Figure 2. Typical Noise Plot @ Gain = 128 with 50 Hz Update Rate

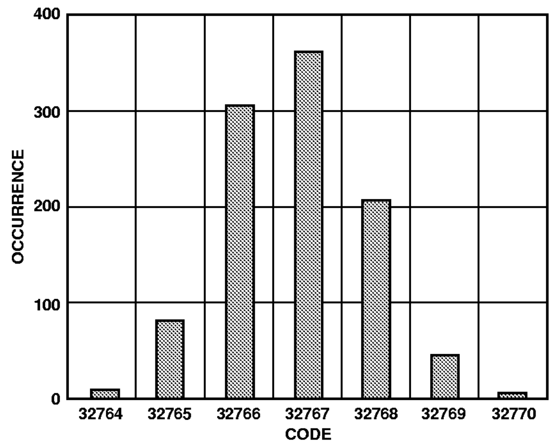


Figure 5. Histogram of Data in Figure 2

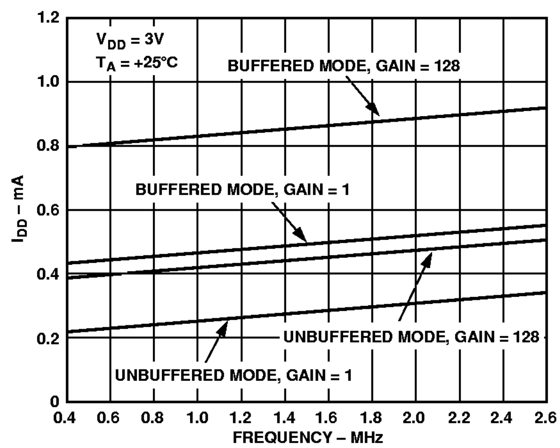


Figure 3. Typical I_{DD} vs. MCLKIN Frequency @ 3 V

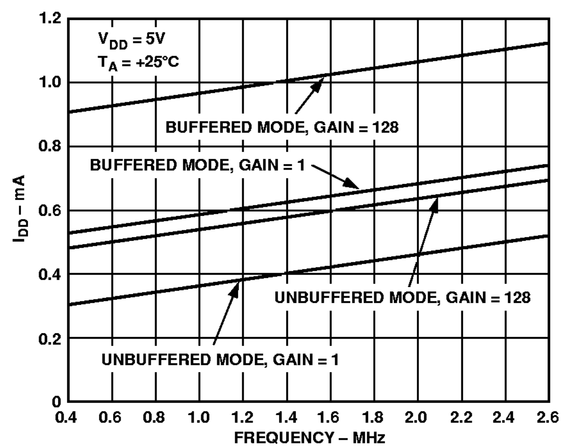


Figure 6. Typical I_{DD} vs. MCLKIN Frequency @ 5 V

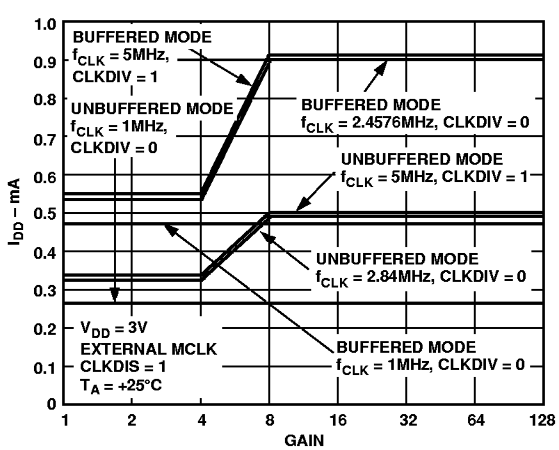


Figure 4. Typical I_{DD} vs. Gain and Clock Frequency @ 3 V

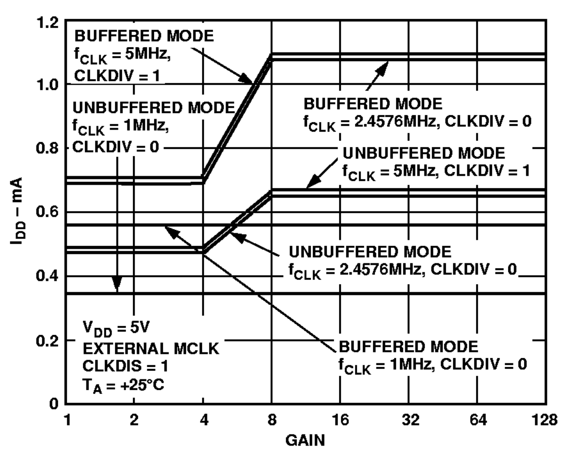


Figure 7. Typical I_{DD} vs. Gain and Clock Frequency @ 5 V

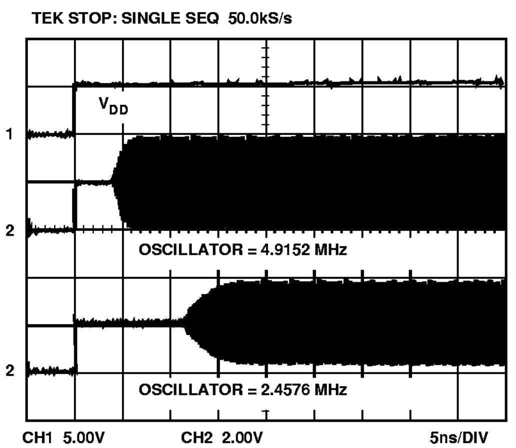


Figure 8. Typical Crystal Oscillator Power-Up Time

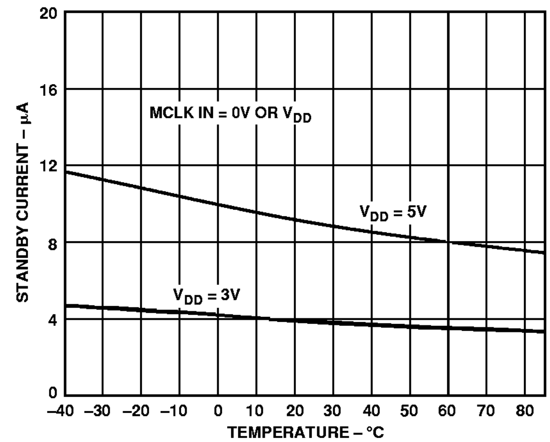


Figure 9. Standby Current vs. Temperature

ON-CHIP REGISTERS

The AD7707 contains eight on-chip registers which can be accessed via the serial port of the part. The first of these is a Communications Register that controls the channel selection, decides whether the next operation is a read or write operation and also decides which register the next read or write operation accesses. All communications to the part must start with a write operation to the Communications Register. After power-on or RESET, the device expects a write to its Communications Register. The data written to this register determines whether the next operation to the part is a read or a write operation and also determines to which register this read or write operation occurs. Therefore, write access to any of the other registers on the part starts with a write operation to the Communications Register followed by a write to the selected register. A read operation from any other register on the part (including the Communications Register itself and the output data register) starts with a write operation to the Communications Register followed by a read operation from the selected register. The Communications Register also controls the standby mode and channel selection and the DRDY status is also available by reading from the Communications Register. The second register is a Setup Register that determines calibration mode, gain setting, bipolar/unipolar operation and buffered mode. The third register is labelled the Clock Register and contains the filter selection bits and clock control bits. The fourth register is the Data Register from which the output data from the part is accessed. The final registers are the calibration registers which store channel calibration data. The registers are discussed in more detail in the following sections.

Communications Register (RS2, RS1, RS0 = 0, 0, 0)

The Communications Register is an 8-bit register from which data can either be read or to which data can be written. All communications to the part must start with a write operation to the Communications Register. The data written to the Communications Register determines whether the next operation is a read or write operation and to which register this operation takes place. Once the subsequent read or write operation to the selected register is complete, the interface returns to where it expects a write operation to the Communications Register. This is the default state of the interface, and on power-up or after a RESET, the AD7707 is in this default state waiting for a write operation to the Communications Register. In situations where the interface sequence is lost, if a write operation of sufficient duration (containing at least 32 serial clock cycles) takes place with DIN high, the AD7707 returns to this default state. Table V outlines the bit designations for the Communications Register.

Table V. Communications Register

0/DRDY (0)	RS2 (0)	RS1 (0)	RS0 (0)	R/W (0)	STBY (0)	CH1 (0)	CH0 (0)

0/DRDY — For a write operation, a "0" must be written to this bit so that the write operation to the Communications Register actually takes place. If a "1" is written to this bit, the part will not clock on to subsequent bits in the register. It will stay at this bit location until a "0" is written to this bit. Once a "0" is written to this bit, the next seven bits will be loaded to the Communications Register. For a read operation, this bit provides the status of the DRDY flag from the part. The status of this bit is the same as the DRDY output pin.

RS2–RS0 — Register Selection Bits. These three bits select to which one of eight on-chip registers the next read or write operation takes place, as shown in Table VI, along with the register size. When the read or write operation to the selected register is complete, the part returns to where it is waiting for a write operation to the Communications Register. It does not remain in a state where it will continue to access the register.

Table VI. Register Selection

RS2	RS1	RS0	Register	Register Size
0	0	0	Communications Register	8 Bits
0	0	1	Setup Register	8 Bits
0	1	0	Clock Register	8 Bits
0	1	1	Data Register	16 Bits
1	0	0	Test Register	8 Bits
1	0	1	No Operation	
1	1	0	Offset Register	24 Bits
1	1	1	Gain Register	24 Bits

R/W Read/Write Select. This bit selects whether the next operation is a read or write operation to the selected register. A "0" indicates a write cycle for the next operation to the appropriate register, while a "1" indicates a read operation from the appropriate register.

STBY Standby. Writing a "1" to this bit puts the part into its standby or power-down mode. In this mode, the part consumes only 8μA of power supply current. The part retains its calibration coefficients and control word information when in STANDBY. Writing a "0" to this bit places the part in its normal operating mode.

CH1–CH0 Channel Select. These two bits select a channel for conversion or for access to the calibration coefficients as outlined in Table VII. Three pairs of calibration registers on the part are used to store the calibration coefficients following a calibration on a channel. They are shown in Tables VII for the AD7707 to indicate which channel combinations have independent calibration coefficients. With CH1 at Logic 1 and CH0 at a Logic 0, the part looks at the LOCOM input internally shorted to itself. This can be used as a test method to evaluate the noise performance of the part with no external noise sources. In this mode, the LOCOM input should be connected to an external voltage within the allowable common-mode range for the part.

Table VII. Channel Selection for AD7707

CH1	CH0	AIN	Reference	Calibration Register Pair
0	0	AIN1	LOCOM	Register Pair 0
0	1	AIN2	LOCOM	Register Pair 1
1	0	LOCOM	LOCOM	Register Pair 0
1	1	AIN3	HICOM	Register Pair 2

Setup Register (RS2, RS1, RS0 = 0, 0, 1); Power-On/Reset Status: 01 Hex

The Setup Register is an eight bit register from which data can either be read or to which data can be written. Table IX outlines the bit designations for the Setup Register.

Table IX. Setup Register

MD1 (0)	MD0 (0)	G2 (0)	G1 (0)	G0 (0)	B/U (0)	BUF (0)	FSYNC (1)

MD1	MD0	Operating Mode
0	0	Normal Mode: this is the normal mode of operation of the device whereby the device is performing normal conversions.
0	1	Self-Calibration: this activates self-calibration on the channel selected by CH1 and CH0 of the Communications Register. This is a one-step calibration sequence and when complete the part returns to Normal Mode with MD1 and MD0 returning to 0, 0. The DRDY output or bit goes high when calibration is initiated and returns low when this self-calibration is complete and a new valid word is available in the data register. The zero-scale calibration is performed at the selected gain on internally shorted (zeroed) inputs and the full-scale calibration is performed at the selected gain on an internally-generated V_{REF}/Selected Gain.
1	0	Zero-Scale System Calibration: this activates zero scale system calibration on the channel selected by CH1 and CH0 of the Communications Register. Calibration is performed at the selected gain on the input voltage provided at the analog input during this calibration sequence. This input voltage should remain stable for the duration of the calibration. The DRDY output or bit goes high when calibration

		is initiated and returns low when this zero-scale calibration is complete and a new valid word is available in the data register. At the end of the calibration, the part returns to Normal Mode with MD1 and MD0 returning to 0, 0.
1	1	Full-Scale System Calibration: this activates full-scale system calibration on the selected input channel. Calibration is performed at the selected gain on the input voltage provided at the analog input during this calibration sequence. This input voltage should remain stable for the duration of the calibration. Once again, the DRDY output or bit goes high when calibration is initiated and returns low when this full-scale calibration is complete and a new valid word is available in the data register. At the end of the calibration, the part returns to Normal Mode with MD1 and MD0 returning to 0, 0.

G2–G0 Gain Selection Bits. These bits select the gain setting for the on-chip PGA as outlined in Table X.

Table X. Gain Selection

G2	G1	G0	Gain Setting
0	0	0	1
0	0	1	2
0	1	0	4
0	1	1	8
1	0	0	16
1	0	1	32
1	1	0	64
1	1	1	128

B/U Bipolar/Unipolar Operation. A "0" in this bit selects Bipolar Operation. A "1" in this bit selects Unipolar Operation.

BUF Buffer Control. With this bit at "0," the on-chip buffer on the analog input is shorted out. With the buffer shorted out, the current flowing in the V_{DD} line is reduced. When this bit is high, the on-chip buffer is in series with the analog input allowing the input to handle higher source impedances.

FSYNC Filter Synchronization. When this bit is high, the nodes of the digital filter, the filter control logic and the calibration control logic are held in a reset state and the analog modulator is also held in its reset state. When this bit goes low, the modulator and filter start to process data and a valid word is available in 3 x 1/(output update rate), i.e., the settling time of the filter. This FSYNC bit does not affect the digital interface and does not reset the DRDY output if it is low.

Clock Register (RS2, RS1, RS0 = 0, 1, 0); Power-On/Reset Status: 05 Hex

The Clock Register is an 8-bit register from which data can either be read or to which data can be written. Table XI outlines the bit designations for the Clock Register.

Table XI. Clock Register

Zero(0)	Zero(0)	CLKDIS(0)	CLKDIV(0)	CLK(1)	FS2(0)	FS1(0)	FS0(1)

ZERO Zero. A zero MUST be written to these bits to ensure correct operation of the AD7707. Failure to do so may result in unspecified operation of the device.

CLKDIS Master Clock Disable Bit. A Logic 1 in this bit disables the master clock from appearing at the MCLK OUT pin. When disabled, the MCLK OUT pin is forced low. This feature allows the user the flexibility of using the MCLK OUT as a clock source for other devices in the system or of turning off the MCLK OUT as a power saving feature. When using an external master clock on the MCLK IN pin, the AD7707 continues to have internal clocks and will convert normally with the CLKDIS bit active. When using a crystal oscillator or ceramic resonator across the MCLK IN and MCLK OUT pins, the AD7707 clock is stopped and no conversions take place when the CLKDIS bit is active.

CLKDIV Clock Divider Bit. With this bit at a Logic 1, the clock frequency appearing at the MCLK IN pin is divided by two before being used internally by the AD7707. For example, when this bit is set to 1, the user can operate with a 4.9152 MHz crystal between MCLK IN and MCLK OUT and internally the part will operate with the specified 2.4576 MHz. With this bit at a Logic 0, the clock frequency appearing at the MCLK IN pin is the frequency used internally by the part.

CLK Clock Bit. This bit should be set in accordance with the operating frequency of the AD7705/AD7706. If the device has a master clock frequency of 2.4576 MHz (CLKDIV = 0) or 4.9152 MHz (CLKDIV = 1), then this bit should be set to a "1." If the device has a master clock frequency of 1 MHz (CLKDIV = 0) or 2 MHz (CLKDIV = 1), this bit should be set to a "0." This bit sets up the appropriate scaling currents for a given operating frequency and also chooses (along with FS1 and FS0) the output update rate for the device. If this bit is not set correctly for the master clock frequency of the device, then the AD7705/AD7706 may not operate to specification.

FS2, FS1, FS0 Filter Selection Bits. Along with the CLK bit, FS2, FS1 and FS0 determine the output update rate, filter first notch and –3 dB frequency as outlined in Table XII. The on-chip digital filter provides a $sinc^3$ (or $Sinx/x^3$) filter response. Placing the first notch at 10 Hz places notches at both 50 and 60 Hz giving better than 150dB rejection at these frequencies. In association with the gain selection the filter cutoff also determines the output noise of the device. Changing the filter notch frequency, as well as the selected gain, impacts resolution. Tables I to IV show the effect of filter notch frequency and gain on the output noise and effective resolution of the part. The output data rate (or effective conversion time) for the device is equal to the frequency selected for the first notch of the filter. For example, if the first notch of the filter is selected at 50 Hz, a new word is available at a 50 Hz output rate or every 20 ms. If the first notch is at 500 Hz, a new word is available every 2 ms. A calibration should be initiated when any of these bits are changed.

The settling time of the filter to a full-scale step input is worst case 4 x 1/(output data rate). For example, with the filter first notch at 50 Hz, the settling time of the filter to a full-scale step input is 80 ms max. If the first notch is at 500 Hz, the settling time is 8 ms max. This settling time can be reduced to 3 ∞ 1/(output data rate) by synchronizing the step input change to a reset of the digital filter. In other words, if the step input takes place with the FSYNC bit high, the settling-time will be 3 x 1/(output data rate) from when the FSYNC bit returns low.

The –3 dB frequency is determined by the programmed first notch frequency according to the relationship:

filter –3 dB frequency = 0.262 x *filter first notch frequency*

Table XII. Output Update Rates

CLK*	FS2	FS1	FS0	Output Update Rate	–3 dB Filter Cutoff
0	0	0	0	20 Hz	5.24 Hz
0	0	0	1	25 Hz	6.55 Hz
0	0	1	0	100 Hz	26.2 Hz
0	0	1	1	200 Hz	52.4 Hz
1	0	0	0	50 Hz	13.1 Hz
1	0	0	1	60 Hz	15.7 Hz
1	0	1	0	250 Hz	65.5 Hz
1	0	1	1	500 Hz	131 Hz
0	1	0	0	4.054Hz	1.06 Hz
0	1	0	1	4.23 Hz	1.11 Hz
0	1	1	0	4.84 Hz	1.27 Hz
0	1	1	1	4.96 Hz	1.3 Hz
1	1	0	0	10 Hz	2.62 Hz
1	1	0	1	10.34 Hz	2.71 Hz
1	1	1	0	11.90 Hz	3.13 Hz
1	1	1	1	12.2 Hz	3.2 Hz

*Assumes correct clock frequency on MCLK IN pin with CLKDIV bit set appropriately.

Data Register (RS2, RS1, RS0 = 0, 1, 1)

The Data Register on the part is a 16-bit read-only register that contains the most up-to-date conversion result from the AD7707. If the Communications Register sets up the part for a write operation to this register, a write operation must actually take place to return the part to where it is expecting a write operation to the Communications Register. However, the 16 bits of data written to the part will be ignored by the AD7707.

Test Register (RS2, RS1, RS0 = 1, 0, 0); Power-On/Reset Status: 00 Hex

The part contains a Test Register that is used when testing the device. The user is advised not to change the status of any of the bits in this register from the default (Power-on or RESET) status of all 0s as the part will be placed in one of its test modes and will not operate correctly.

Zero-Scale Calibration Register (RS2, RS1, RS0 = 1, 1, 0); Power-On/Reset Status: 1F4000 Hex

The AD7707 contains independent sets of zero-scale registers, one for each of the input channels. Each of these registers is a 24-bit read/write register; 24 bits of data must be written otherwise no data will be transferred to the register. This register is used in conjunction with its associated full-scale register to form a register pair. These register pairs are associated with input channel pairs as outlined in Table VII. While the part is set up to allow access to these registers over the digital interface, the part itself no longer has access to the register coefficients to correctly scale the output data. As a result, there is a possibility that after accessing the calibration registers (either read or write operation) the first output data read from the part may contain incorrect data. In addition, a write to the calibration register should not be attempted while a calibration is in progress. These eventualities can be avoided by taking the FSYNC bit in the mode register high before the calibration register operation and taking it low after the operation is complete.

Full-Scale Calibration Register (RS2, RS1, RS0 = 1, 1, 1); Power-On/Reset Status: 5761AB Hex

The AD7707 contains independent sets of full-scale registers, one for each of the input channels. Each of these registers is a 24-bit read/write register; 24 bits of data must be written otherwise no data will be transferred to the register. This register is used in conjunction with its associated zero-scale register to form a register pair. These register pairs are associated with input channel pairs as outlined in Table VII. While the part is set up to allow access to these registers over the digital interface, the part itself no longer has access to the register coefficients to correctly scale the output data. As a result, there is a possibility that after accessing the calibration registers (either read or write operation) the first output data read from the part may contain incorrect data. In addition, a write to the calibration register should not be attempted while a calibration is in progress. These eventualities can be avoided by taking FSYNC bit in the mode register high before the calibration register operation and taking it low after the operation is complete.

CALIBRATION SEQUENCES

The AD7707 contains a number of calibration options as previously outlined. Table XIII summarizes the calibration types, the operations involved and the duration of the operations. There are two methods of determining the end of calibration. The first is to monitor when DRDY returns low at the end of the sequence. DRDY not only indicates when the sequence is complete, but also that the part has a valid new sample in its data register. This valid new sample is the result of a normal conversion which follows the calibration sequence. The second method of determining when calibration is complete is to monitor the MD1 and MD0 bits of the Setup Register. When these bits return to 0 (0 following a calibration command), it indicates that the calibration sequence is complete. This method does not give any indication of there being a valid new result in the data register. However, it gives an earlier indication than DRDY that calibration is complete. The duration to when the Mode Bits (MD1 and MD0) return to 0 (0 represents the duration of the calibration carried out). The sequence to when DRDY goes low also includes a normal conversion and a pipeline delay, t_P, to correctly scale the results of this first conversion. t_P will never exceed 2000 x t_{CLKIN}. The time for both methods is given in the table.

Table XIII. Calibration Sequences

Calibration Type	MD1, MD0	Calibration Sequence	Duration to Mode Bits	Duration to DRDY
Self-Calibration	0, 1	Internal ZS Cal @ Selected Gain + Internal FS Cal @ Selected Gain	6 x 1/Output Rate	9 x 1/Output Rate + t_P
ZS System Calibration	1, 0	ZS Cal on AIN @ Selected Gain	3 x 1/Output Rate	4 x 1/Output Rate + t_P
FS System Calibration	1, 1	FS Cal on AIN @ Selected Gain	3 x 1/Output Rate	4 x 1/Output Rate + t_P

CIRCUIT DESCRIPTION

The AD7707 is a sigma-delta A/D converter with on-chip digital filtering, intended for the measurement of wide dynamic range, low frequency signals such as those in industrial control or process control applications. It contains a sigma-delta (or charge-balancing) ADC, a calibration microcontroller with on-chip static RAM, a clock oscillator, a digital filter and a bi-directional serial communications port. The part consumes only 320µA of power supply current, making it ideal for battery-powered or loop-powered instruments. On-board thin-film resistors allow ±10V, ±5V and 0 to 5V high level input signals to be directly accomodated on the analog inputs without requiring split supplies on dc-dc converters. This part operates with a supply voltage of 2.7 V to 3.3 V or 4.75 V to 5.25 V.

The AD7707 contains two low level (AIN1 & AIN2) programmable-gain pseudo differential analog input channels and one high level (AIN3) input channels.The selectable gains on these inputs are 1, 2, 4, 8, 16, 32, 64 and 128 allowing the part to accept unipolar signals of between 0 mV to +20mV and 0 V to +2.5V, or bipolar signals in the range from ±20mV to ±2.5V when the reference input voltage equals +2.5V on the low level input channels. With a reference voltage of +1.225V, the input ranges are from 0 mV to +10mV to 0 V to +1.225V in unipolar mode, and from ±10mV to ±1.225 V in bipolar mode on the low level input channels. The high level input channel can accept signals as large as ±10 V on its analog input. Note that the signal ranges are with respect to the LOCOM input on the low level input channels, and with respect to HICOM on the high level input channel, and not with respect to AGND or DGND.

The input signal to the analog input is continuously sampled at a rate determined by the frequency of the master clock, MCLK IN, and the selected gain. A charge-balancing A/D converter (Sigma-Delta Modulator) converts the sampled signal into a digital pulse train whose duty cycle contains the digital information. The programmable gain function on the analog input is also incorporated in this sigma-delta modulator with the input sampling frequency being modified to give the higher gains. A $sinc^3$ digital low-pass filter processes the output of the sigma-delta modulator and updates the output register at a rate determined by the first notch frequency of this filter. The output data can be read from the serial port randomly or periodically at any rate up to the output register update rate. The first notch of this digital filter (and hence its −3 dB frequency) can be programmed via the Setup Register bits FS0 and FS1. With a master clock frequency of 2.4576MHz, the programmable range for this first notch frequency is from 10Hz to 500Hz, giving a programmable range for the −3 dB frequency of 2.62Hz to 131 Hz. With a master clock frequency of 1MHz, the programmable range for this first notch frequency is from 4Hz to 200Hz, giving a programmable range for the −3 dB frequency of 1.06 Hz to 52.4 Hz.

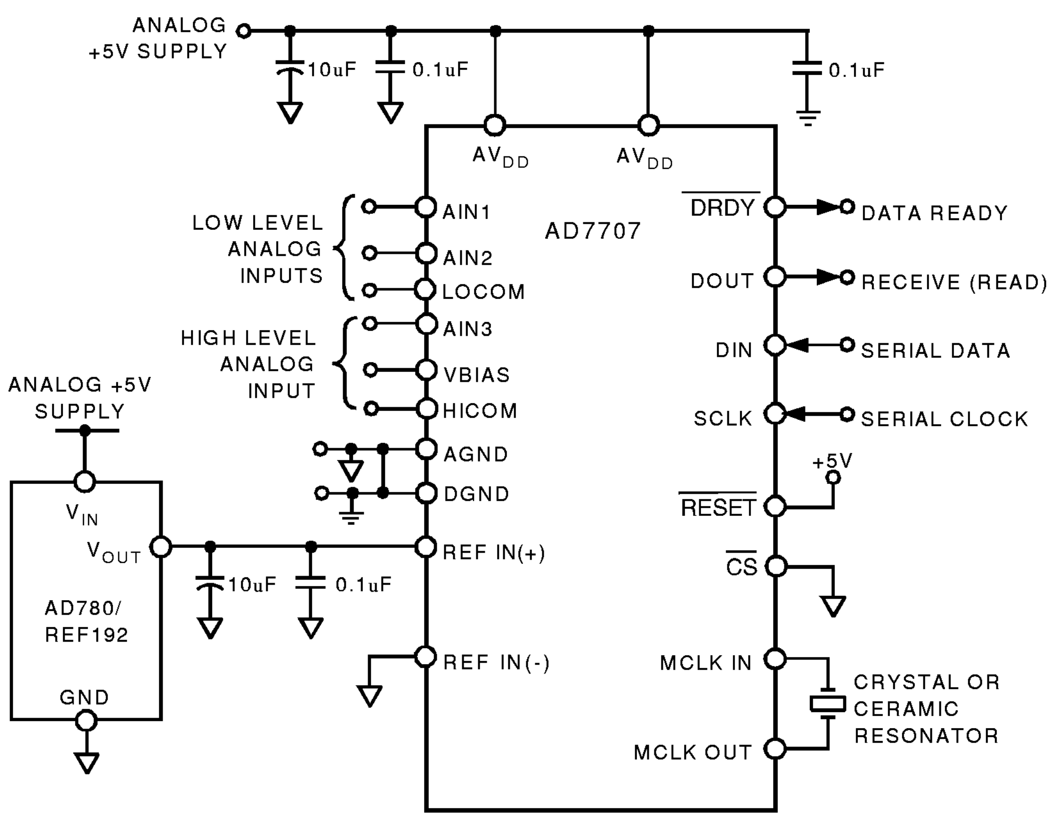


Figure 10. AD7707 Basic Connection Diagram for 5V Operation.

The basic connection diagram for the AD7707 is shown in Figure 10. This shows the AD7707 being driven from the analog +5V supply. An AD780 or REF192, precision +2.5 V reference, provides the reference source for the part. On the digital side, the part is configured for three-wire operation with CS tied to DGND. A quartz crystal or ceramic resonator provide the master clock source for the part. In most cases, it will be necessary to connect capacitors on the crystal or resonator to ensure that it does not oscillate at overtones of its fundamental operating frequency. The values of capacitors will vary, depending on the manufacturer's. A similar circuit is applicable for operation with 3V supplies, in this case a 1.225V reference (AD1580) should be used for specified performance.

ANALOG INPUT

Analog Input Ranges

The AD7707 contains two low level pseudo differential analog input channels AIN1 and AIN2. These input pairs provide programmable-gain, differential input channels that can handle either unipolar or bipolar input signals. It should be noted that the bipolar input signals are referenced to the LOCOM input. The AD7707 also has a high level analog input channel AIN3 which is referenced to HICOM.

In unbuffered mode, the common-mode range of the low level input channels is from AGND to AV_{DD}, provided that the absolute value of the analog input voltage lies between AGND − 30mV and V_{DD} + 30mV. This means that in unbuffered mode the part can handle both unipolar and bipolar input ranges for all gains. Absolute voltages of AGND − 200 mV can be accommodated on the analog inputs at 25°C without degradation in performance, but leakage current increases appreciably with increasing temperature. In buffered mode, the analog inputs can handle much larger source impedances, but the absolute input voltage range is restricted to between AGND + 50mV to AV_{DD} − 1.5V which also places restrictions on the common-mode range. This means that in buffered mode there are some restrictions on the allowable gains for bipolar input ranges. Care must be taken in setting up the common-mode voltage and input voltage range so that the above limits are not exceeded, otherwise there will be a degradation in linearity performance.

In unbuffered mode, the analog inputs look directly into the 7 pF input sampling capacitor, C_{SAMP}. The dc input leakage current in this unbuffered mode is 1 nA maximum. As a result, the analog inputs see a dynamic load that is switched at the input sample rate (see Figure 11). This sample rate depends on master clock frequency and selected gain. C_{SAMP} is charged to the selected AIN and discharged to LOCOM every input sample cycle. The effective on-resistance of the switch, R_{SW}, is typically 7 kΩ.

C_{SAMP} must be charged through R_{SW} and through any external source impedances every input sample cycle. Therefore, in unbuffered mode, source impedances mean a longer charge time for C_{SAMP} and this may result in gain errors on the part. Table XIV shows the allowable external resistance/capacitance values, for unbuffered mode, such that no gain error to the 16-bit level is introduced on the part. Note that these capacitances are total capacitances on the analog input, external capacitance plus 10 pF capacitance from the pins and lead frame of the device.

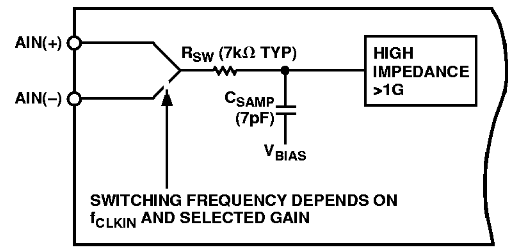


Figure 11. Unbuffered Analog Input Structure

Table XIV. External R, C Combination for No 16-Bit Gain Error (Unbuffered Mode Only)

	External Capacitance (pF)					
Gain	**0**	**50**	**100**	**500**	**1000**	**5000**
1	368 kΩ	90.6 kΩ	54.2 kΩ	14.6 kΩ	8.2 kΩ	2.2 kΩ
2	177.2 kΩ	44.2 kΩ	26.4 kΩ	7.2 kΩ	4 kΩ	1.12 kΩ
4	82.8 kΩ	21.2 kΩ	12.6 kΩ	3.4 kΩ	1.94 kΩ	540 Ω
8–128	35.2 kΩ	9.6 kΩ	5.8 kΩ	1.58 Ω	880 Ω	240 Ω

In buffered mode, the analog inputs look into the high-impedance inputs stage of the on-chip buffer amplifier. C_{SAMP} is charged via this buffer amplifier such that source impedances do not affect the charging of C_{SAMP}. This buffer amplifier has an offset leakage current of 1 nA. In this buffered mode, large source impedances result in a small dc offset voltage developed across the source impedance, but not in a gain error.

Input Sample Rate

The modulator sample frequency for the AD7707 remains at $f_{CLKIN}/128$ (19.2 kHz @ f_{CLKIN} = 2.4576 MHz) regardless of the selected gain. However, gains greater than 1 are achieved by a combination of multiple input samples per modulator cycle and a scaling of the ratio of reference capacitor to input capacitor. As a result of the multiple sampling, the input sample rate of the device varies with the selected gain (see Table XV). In buffered mode, the input is buffered before the input sampling capacitor. In unbuffered mode, where the analog input looks directly into the sampling capacitor, the effective input impedance is $1/C_{SAMP} \cdot f_S$ where C_{SAMP} is the input sampling capacitance and f_S is the input sample rate.

Table XV. Input Sampling Frequency vs. Gain

Gain	Input Sampling Frequency (f_S)
1	$f_{CLK IN}$/64 (38.4 kHz @ $f_{CLK IN}$ = 2.4576 MHz)
2	2 x $f_{CLK IN}$/64 (76.8 kHz @ $f_{CLK IN}$ =2.4576 MHz)
4	4 x $f_{CLK IN}$/64 (76.8 kHz @ $f_{CLK IN}$ =2.4576 MHz)
8-128	8 x $f_{CLK IN}$/64 (307.2 kHz @ $f_{CLK IN}$ = 2.4576 MHz)

POWER SUPPLIES

The AD7707 operates with a V_{DD} power supply between 2.7 V and 5.25 V. While the latch-up performance of the AD7707 is good, it is important that power is applied to the AD7707 before signals at REF IN, AIN or the logic input pins in order to avoid excessive currents. If this is not possible, the current that flows in any of these pins should be limited. If separate supplies are used for the AD7707 and the system digital circuitry, the AD7707 should be powered up first. If it is not possible to guarantee this, current limiting resistors should be placed in series with the logic inputs to again limit the current. Latch-up current is greater than 100 mA.

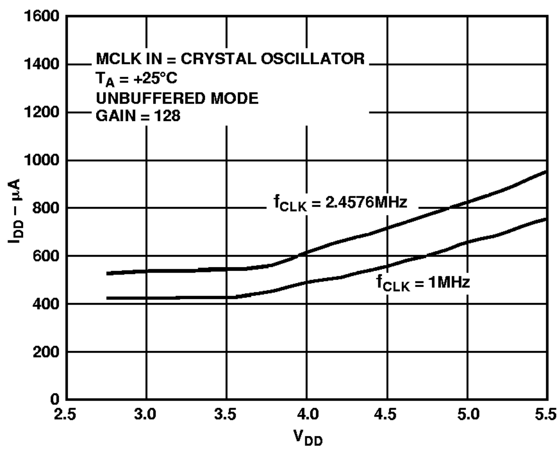


Figure . I_{DD} vs. Supply Voltage

Supply Current

The current consumption on the AD7707 is specified for supplies in the range +2.7 V to +3.3 V and in the range +4.75 V to +5.25 V. The part operates over a +2.7 V to +5.25 V supply range and the I_{DD} for the part varies as the supply voltage varies over this range. There is an internal current boost bit on the AD7707 that is set internally in accordance with the operating conditions. This affects the current drawn by the analog circuitry within these devices. Minimum power consumption is achieved when the AD7707 is operated with an $f_{CLK IN}$ of 1 MHz or at gains of 1 to 4 with $f_{CLK IN}$ = 2.4575 MHz as the internal boost bit is off reducing the analog current consumption. Figure 15 shows the variation of the typical I_{DD} with V_{DD} voltage for both a 1 MHz crystal oscillator and a 2.4576 MHz crystal oscillator at +25°C. The AD7707 is operated in unbuffered mode. The relationship shows that the I_{DD} is minimized by operating the part with lower V_{DD} voltages. I_{DD} on the AD7707 is also minimized by using an external master clock or by optimizing external components when using the on-chip oscillator circuit. Figures 3, 4, 6 and 7 show variations in I_{DD} with gain, V_{DD} and clock frequency using an external clock.

Grounding and Layout

Since the analog inputs and reference input are differential, most of the voltages in the analog modulator are common-mode voltages. The excellent common-mode rejection of the part will remove common-mode noise on these inputs. The digital filter will provide rejection of broadband noise on the power supplies, except at integer multiples of the modulator sampling frequency. The digital filter also removes noise from the analog and reference inputs provided those noise sources do not saturate the analog modulator. As a result, the AD7707 is more immune to noise interference than a conventional high resolution converter. However, because the resolution of the AD7707 is so high, and the noise levels from the AD7707 so low, care must be taken with regard to grounding and layout.

The printed circuit board that houses the AD7707 should be designed so that the analog and digital sections are separated and confined to certain areas of the board. This facilitates the use of ground planes which can be separated easily. A minimum etch technique is generally best for ground planes as it gives the best shielding. Digital and analog ground planes should only be joined in one place to avoid ground loops. If the AD7707 is in a system where multiple devices require AGND-to-DGND connections, the connection should be made at one point only, a star ground point which should be established as close as possible to the AD7707 GND.

Avoid running digital lines under the device as these will couple noise onto the die. The analog ground plane should be allowed to run under the AD7707 to avoid noise coupling. The power supply lines to the AD7707 should use as large a trace as possible to provide low impedance paths and reduce the effects of glitches on the power supply line. Fast switching signals like clocks should be shielded with digital ground to avoid radiating noise to other sections of the board and clock signals should never be run near the analog inputs. Avoid crossover of digital and analog signals. Traces on opposite sides of the board should run at right angles to each other. This will reduce the effects of feedthrough through the board. A microstrip technique is by far the best, but is not always possible with a double-sided board. In this technique, the component side of the board is dedicated to ground planes while signals are placed on the solder side.

Good decoupling is important when using high resolution ADCs. All analog supplies should be decoupled with 10 µF tantalum in parallel with 0.1 µF ceramic capacitors to GND. To achieve the best from these decoupling components, they have to be placed as close as possible to the device, ideally right up against the device. All logic chips should be decoupled with 0.1 µF disc ceramic capacitors to DGND.

DIGITAL INTERFACE

As previously outlined, the AD7707's programmable functions are controlled using a set of on-chip registers. Data is written to these registers via the part's serial interface and read access to the on-chip registers is also provided by this interface. All communications to the part must start with a write operation to the Communications Register. After power-on or RESET, the device expects a write to its Communications Register. The data written to this register determines whether the next operation to the part is a read or a write operation and also determines to which register this read or write operation occurs. Therefore, write access to any of the other registers on the part starts with a write operation to the Communications Register followed by a write to the selected register. A read operation from any other register on the part (including the output data register) starts with a write operation to the Communications Register followed by a read operation from the selected register.

The AD7707's serial interface consists of five signals, CS, SCLK, DIN, DOUT and DRDY. The DIN line is used for transferring data into the on-chip registers while the DOUT line is used for accessing data from the on-chip registers. SCLK is the serial clock input for the device and all data transfers (either on DIN or DOUT) take place with respect to this SCLK signal. The DRDY line is used as a status signal to indicate when data is ready to be read from the AD7707's data register. DRDY goes low when a new data word is available in the output register. It is reset high when a read operation from the data register is complete. It also goes high prior to the updating of the output register to indicate when *not* to read from the device to ensure that a data read is not attempted while the register is being updated. CS is used to select the device. It can be used to decode the AD7707 in systems where a number of parts are connected to the serial bus.

Figures 16 and 17 show timing diagrams for interfacing to the AD7707 with CS used to decode the part. Figure 16 is for a read operation from the AD7707's output shift register while Figure 17 shows a write operation to the input shift register. It is possible to read the same data twice from the output register even though the DRDY line returns high after the first read operation. Care must be taken, however, to ensure that the read operations have been completed before the next output update is about to take place.

The AD7707 serial interface can operate in three-wire mode by tying the CS input low. In this case, the SCLK, DIN and DOUT lines are used to communicate with the AD7707 and the status of DRDY can be obtained by interrogating the MSB of the Communications Register. This scheme is suitable for interfacing to microcontrollers. If CS is required as a decoding signal, it can be generated from a port bit. For microcontroller interfaces, it is recommended that the SCLK idles high between data transfers.

The AD7707 can also be operated with CS used as a frame synchronization signal. This scheme is suitable for DSP interfaces. In this case, the first bit (MSB) is effectively clocked out by CS since CS would normally occur after the falling edge of SCLK in DSPs. The SCLK can continue to run between data transfers provided the timing numbers are obeyed.

The serial interface can be reset by exercising the RESET input on the part. It can also be reset by writing a series of 1s on the DIN input. If a Logic 1 is written to the AD7707 DIN line for at least 32 serial clock cycles the serial interface is reset. This ensures that in three-wire systems, if the interface gets lost either via a software error or by some glitch in the system, it can be reset back to a known state. This state returns the interface to where the AD7707 is expecting a write operation to its Communications Register. This operation in itself does not reset the contents of any registers but since the interface was lost, the information written to any of the registers is unknown and it is advisable to set up all registers again.

Some microprocessor or microcontroller serial interfaces have a single serial data line. In this case, it is possible to connect the AD7707's DATA OUT and DATA IN lines together and connect them to the single data line of the processor. A 10 kΩ pull-up resistor should be used on this single data line. In this case, if the interface gets lost, because the read and write operations share the same line the procedure to reset it back to a known state is somewhat different than previously described. It requires a read operation of 24 serial clocks followed by a write operation where a Logic 1 is written for at least 32 serial clock cycles to ensure that the serial interface is back into a known state.

MICROCOMPUTER/MICROPROCESSOR INTERFACING

The AD7707's flexible serial interface allows for easy interface to most microcomputers and microprocessors. The flowchart of Figure 10 outlines the sequence that should be followed when interfacing a microcontroller or microprocessor to the AD7707. The serial interface on the AD7707 is capable of operating from just three wires and is compatible with SPI interface protocols. The three-wire operation makes the part ideal for isolated systems where minimizing the number of interface lines minimizes the number of opto-isolators required in the system. The serial clock input is a Schmitt triggered input to accommodate slow edges from opto-couplers. The rise and fall times of other digital inputs to the AD7707 should be no longer than 1 µs.

Most of the registers on the AD7707 are 8-bit registers, which facilitates easy interfacing to the 8-bit serial ports of microcontrollers. The Data Register on the AD7707 is 16 bits, and the offset and gain registers are 24-bit registers but data transfers to these registers can consist of multiple 8-bit transfers to the serial port of the microcontroller. DSP processors and microprocessors generally transfer 16 bits of data in a serial data operation. Some of these processors, such as the ADSP-2105, have the facility to program the amount of cycles in a serial transfer. This allows the user to tailor the number of bits in any transfer to match the register length of the required register in the AD7707.

Even though some of the registers on the AD7707 are only eight bits in length, communicating with two of these registers in successive write operations can be handled as a single 16-bit data transfer if required. For example, if the Setup Register is to be updated, the processor must first write to the Communications Register (saying that the next operation is a write to the Setup Register) and then write eight bits to the Setup Register. If required, this can all be done in a single 16-bit transfer because once the eight serial clocks of the write operation to the Communications Register have been completed, the part immediately sets itself up for a write operation to the Setup Register.

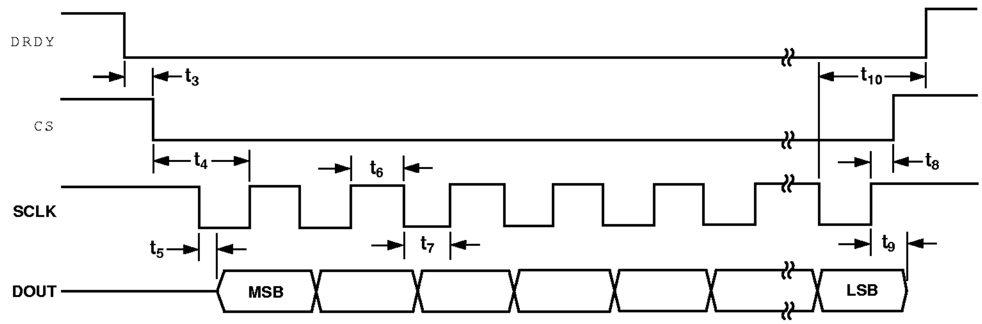


Figure 16. Read Cycle Timing Diagram

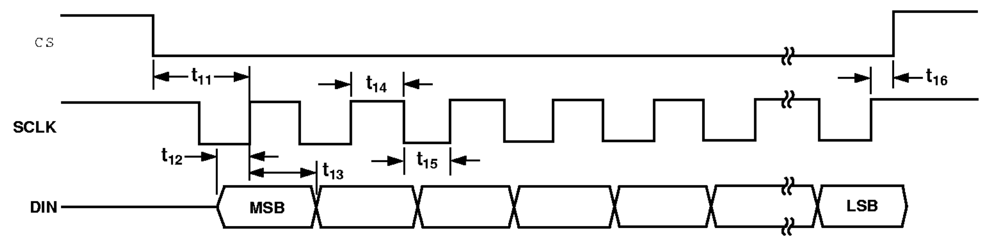


Figure 17. Write Cycle Timing Diagram