D6305A

EASYTAD™ Chip for an All-Digital Answering Machine

GENERAL DESCRIPTION

The D6305A chip is a digital speech/signal processing subsystem that implements all the functions of speech compression, telephone line signal processing, memory management, and TRUESPEECH™ natural-sound voice prompting for an all digital telephone answering machine. The D6305A is fully controlled by the system host through a simple interface protocol. The host processor provides activation and control of all system functions such as speech recording and playback, DTMF and call progress tone detection and generation, and voice prompting.

The fully digital solution has no moving parts, yielding high reliability. The chip's programmability enables a full range of answering device features for the end user. The D6305A is a single-chip, digital signal processor that includes all of the necessary circuitry to interface with an external HOST, memory, and an analog front end.

FEATURES

- High quality, variable low rate digital speech compression - 15 -17 minutes of recording time per each 4 Mbit ARAM (Audio grade DRAM)
- Flexible storage of incoming messages (ICM) and outgoing messages (OGM). Supports multiple OGMs and multiple mailboxes
- TRUESPEECH™ natural-sound voice prompting, for Day/Time stamp and voice instructions
- DTMF generation and detection with near-end echo cancellation for superior performance
- Low power consumption
- 8-bit HOST interface
- Storage for 32 telephone numbers for speed dialing
- Special commands for production line testing

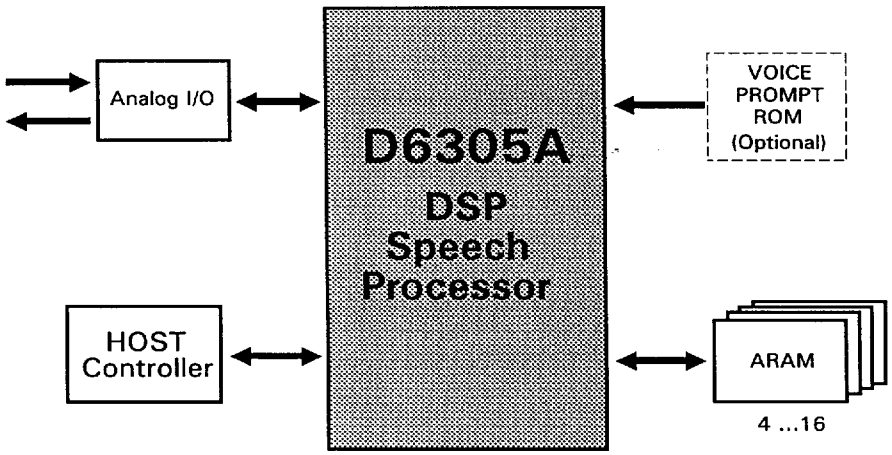

Figure 1. D6305A Block Diagram

All specifications are subject to change without prior notice

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CHIP CONFIGURATION

- D6305A-11 Digital Telephone Answering Device (TAD) Processor (80-pin PQFP)—1 each

ADDITIONAL SYSTEM COMPONENTS (supplied by the customer according to DSP Group's specifications)

- D0000-29 Analog I/O Interface (16-pin DIP)—1 each
- D0000-35A 4-Mbit ARAM Message Memory (SOJ)—Up to four devices per chipset

Notes:

1. For Voice Prompt storage an external EPROM/ROM (access time is 400ns or less) is required. Each 16K x 8 block will support 19.5 seconds of voice prompt (up to 64K).

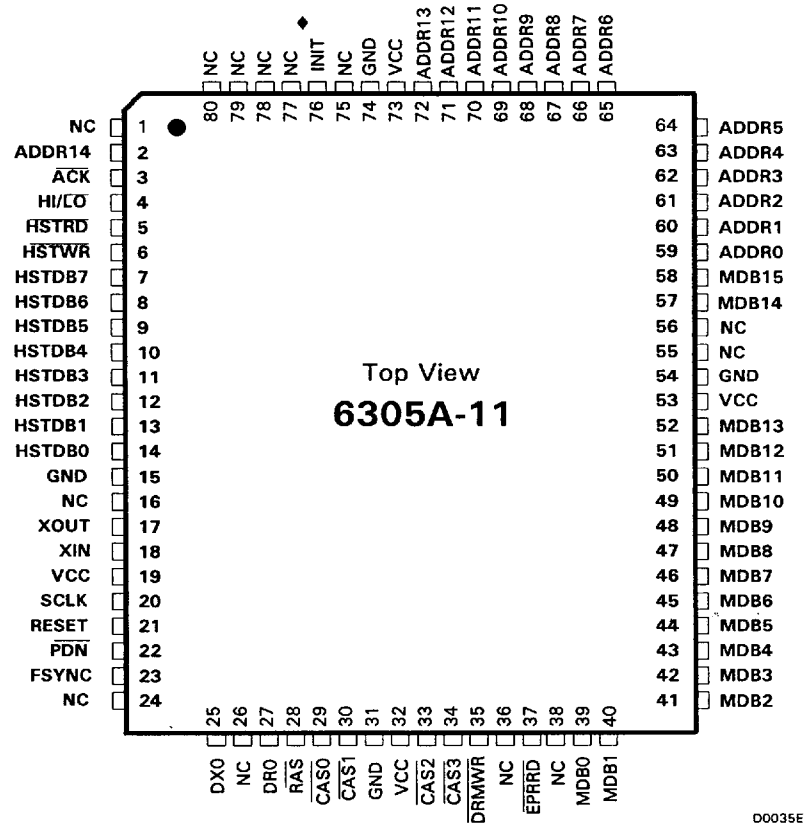

Figure 2. D6305A -11

♦Applicable for D6305A-11DQC and later version

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PIN DESCRIPTIONS

D6305A-11 (DSP)			
Pin		I/O/Z*	Description
Name	No.		
HSTDB0 (LSB)	14	I/O/Z	HOST DATA BUS. The HOST writes commands and reads status to/from the D6305A via this bus. The HI/LO pin selects between the low byte and the high byte of the command/status. This bus is used for input when HSTWR is low, and for output when HSTRD is low. It has high impedance when HSTWR and HSTRD are high or RESET is low.
HSTDB1	13	I/O/Z	
HSTDB2	12	I/O/Z	
HSTDB3	11	I/O/Z	
HSTDB4	10	I/O/Z	
HSTDB5	9	I/O/Z	
HSTDB6	8	I/O/Z	
HSTDB7 (MSB)	7	I/O/Z	
HI/LO	4	I	HIGH/LOW BYTE SELECT. When this signal is low, the HOST can read/write the low byte of the status/command. When high, the high byte is selected.
HSTRD	5	I	HOST READ. When low, the HOST reads the low/high byte of the status word.
HSTWR	6	I	HOST WRITE. When low the HOST writes commands to the D6305A via HSTDB 0-7.
ACK	3	O	HOST ACKNOWLEDGE. This pin goes low when the D6305A sends a status word to the HOST. It goes high when the HOST reads the high byte of the status word.
ADDR0 (LSB)	59	O	EXTERNAL MEMORY ADDRESS BUS
ADDR1	60	O	
ADDR2	61	O	
ADDR3	62	O	
ADDR4	63	O	
ADDR5	64	O	
ADDR6	65	O	
ADDR7	66	O	
ADDR8	67	O	
ADDR9	68	O	
ADDR10	69	O	
ADDR11	70	O	
ADDR12	71	O	
ADDR13	72	O	
ADDR14 (MSB)	2	O	
MDB0 (LSB)	39	I/O/Z	EXTERNAL MEMORY DATA BUS.
MDB1	40	I/O/Z	
MDB2	41	I/O/Z	
MDB3	42	I/O/Z	
MDB4	43	I/O/Z	
MDB5	44	I/O/Z	
MDB6	45	I/O/Z	
MDB7	46	I/O/Z	
MDB8	47	I/O/Z	
MDB9	48	I/O/Z	
MDB10	49	I/O/Z	
MDB11	50	I/O/Z	
MDB12	51	I/O/Z	
MDB13	52	I/O/Z	
MDB14	57	I/O/Z	
MDB15 (MSB)	58	I/O/Z	

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D6305A-11 (DSP)			
EPRRD	37	O	Voice prompt ROM/EPROM read (active low)
DRMWR	35	O	ARAM WRITE (active low)
CAS0	29	O	ARAM CAS (0 for first ARAM, 1 for second ARAM, etc.)
CAS1	30	O	
CAS2	33	O	
CAS3	34	O	4 Mbit ARAM CAS (ARAM 4)
RAS	28	O	ARAM RAS
DR	27	I	Serial input for CODEC PCM data
DX	25	O	Serial output for CODEC PCM data
FSYNC	23	O	Frame synchronization signal for CODEC
SCLK	20	O	Clock output to CODEC
XIN	18	I	Crystal input pin for internal oscillator. The frequency is 29,4912 MHz.
XOUT	17	O	Crystal output pin for internal oscillator.
GND	15	PWR	GROUND PIN
GND	31	PWR	GROUND PIN
GND	54	PWR	GROUND PIN
GND	74	PWR	GROUND PIN
V_{CC}	19	PWR	+5V battery backed-up power supply input. This power source should be connected to the ARAMs, and voice prompt ROM/EPROM.
V_{CC}	32	PWR	
V_{CC}	73	PWR	
V_{CC}	53	PWR	
PDN	22	I	V_{CC} power fail sensor input. When a low level is detected on this pin, the D6305A enters power-down mode.
RESET	21	I	Reset input (active high)
INIT♦	76	I	If set to "1" this pin forces the D6305A to "cold start" when RESET is applied.
NC	1		These pins should be left unconnected.
NC	16		
NC	24		
NC	26		
NC	36		
NC	38		
NC	55		
NC	56		
NC	75		
NC	77		
NC	78		
NC	79		
NC	80		

♦Applicable for D6305A-11DQC and later version

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PIN DESCRIPTIONS

D0000-29 (Analog I/O Interface)			
Pin		I/O/Z*	Description
Name	No.		
V_{BB}	1	PWR	Negative power supply pin. V_{BB} = –5V
GNDA	2	PWR	Analog ground. All signals are referenced to this pin.
VF_RO	3	O	Analog output of the receive power amplifier.
V_{CC}	4	PWR	Positive power supply pin. VCC = +5V.
FS_R	5	I	Receive frame sync pulse which enables $BCLK_R$ to shift PCM data into D_R.
D_R	6	I	Receive data input. PCM data is shifted into D_R following the FS_R leading edge.
$BCLK_R$/ CLKSEL	7	I	Logic input which selects either 1.536 MHz/1.544 MHz or 2.048 MHz for master clock in synchronous mode and $BCLK_X$ is used for both transmit and receive directions. This input should be tied to ground.
$MCLK_R$/ PDN	8	I	Receive master clock. When $MCLK_R$ is connected continuously low, $MCLK_X$ is selected for all internal timing. When $MCLK_R$ is connected continuously high, the device is powered down.
$MCLK_X$	9	I	Transmit master clock. Must be 1.536 MHz, 1.544 MHz or 2.048 MHz. May be asynchronous with $MCLK_R$. Best performance is realized from synchronous operation.
$BCLK_X$	10	I	The bit clock which shifts out the PCM data on DX. May vary from 64 KHz to 2.048 MHz, but must be synchronous with $MCLK_X$.
D_X	11	O/Z	PCM data output which is enabled by FS_X.
FS_X	12	I	Transmit frame sync pulse input which enables $BCLK_X$ to shift out the PCM data on D_X. FS_X is an 8 KHz pulse train.
TS_X	13	O	Open drain output which pulses low during the encoder time slot.
GS_X	14	O	Analog output of the transmit input amplifier. Used to externally set gain.
VF_XI-	15	I	Inverting input of the transmit input amplifier.
VF_XI+	16	I	Non-inverting input of the transmit input amplifier.

D0000-35A (4 MEG ARAM)			
Pin		I/O/Z*	Description
Name	No.		
A0	9	I	Row and column address bits. Row address bits are latched in the chip by the $\overline{RAS}$ signal. Column address bits are latched in by the $\overline{CAS}$ signal.
A1	10	I	
A2	11	I	
A3	12	I	
A4	14	I	
A5	15	I	
A6	16	I	
A7	17	I	
A8	18	I	
A9	5	I	
RAS	4	I	Row address strobe
CAS	23	I	Column address strobe
WE	3	I	Write enable input which selects read or write mode
VCC	13	–	+5V supply
VSS	26	–	Ground
OE	22	I	Output enable
D1	1	I/O	Data inputs/outputs
D2	2	I/O	
D3	24	I/O	
D4	25	I/O	

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FUNCTIONAL DESCRIPTION

HOST Interface

The host interface is an 8-bit parallel data port, used for control and status information transfer. The host controls the operation of the D6305A using a simple command protocol. D6305A status information is updated after each command.

The command and status protocol enables the host to have full control over the functions of the D6305A. The protocol is described in the next section.

Voice Message Storage—Incoming and Outgoing Messages

The D6305A message storage utilizes a proprietary high quality, variable rate speech compression technique. The compression algorithm is programmable and can be activated by HOST in different modes. When activated with a fixed compression rate, the D6305A provides the maximum rate at 6.72 Kbps. This allows storage of 10.2 minutes of speech in the first 4 Mbit of ARAM and 10.4 minutes in each of the consecutive devices. The chip can totally support up to four 4 Mbit devices. Selecting the variable compression rate will increase the recording time to 12 minutes per 4 Mbit.

The D6305A also supports the "gap coding" method, which reduces the data rate of the speech signal. When the compression algorithm utilizes both variable rate and "gap coding", the D6305A achieves a recording time of 15 - 17 minutes per 4 Mbit and a total of more than one hour per system (16 Mbit).

Use of the compression technique is enhanced by an error correction algorithm that enables the use of ARAM memory without degradation of speech quality. The chipset supports up to 64 variable length incoming and outgoing messages. Multiple outgoing messages and multiple mailboxes for incoming messages are supported.

During recording, the D6305A performs telephone line signal monitoring. The HOST can stop recording, and delete the last n*0.266 seconds from the memory using a Record command with Tail Cut Factor.

The D6305A is capable of reporting to the HOST the status of the currently available ARAM memory storage space, as well as the overall status of the ARAMs and the number of recorded messages.

Digital Voice-Activated Recording (VOX)

Digital voice activity detection is implemented in the D6305A and can be activated only in Record mode. According to the HOST command recording of the speech signal may either start upon a positive result of voice activity detection or immediately after issuing a Record command.

The voice activity detector output is reported to the HOST via a status bit every 33 ms when in Record mode. The HOST reads this information and decides when to stop the recording of this message.

Message Playback

The D6305A supports random access for playback of any recorded message. During playback, the D6305A monitors the telephone line.

Message playback can be stopped by using the Pause command, which is initiated by the HOST. After Pause, playback may be resumed from the same point. Normally, during playback, the status word will contain information about the line and the playback status and will notify HOST when end of message is reached.

Message Deletion

The D6305A enables selective deletion of any prerecorded message from memory. After each deletion the message directory is updated accordingly. To improve memory utilization, the D6305A supports "Garbage Collection," which eliminates empty spaces in the message memory.

Message Time Stamp

The HOST may attach a 16-bit data to each of the 64 messages of the D6305A. This data can be used for time stamping the recorded message.

DTMF Detection

DTMF detection is implemented by the D6305A in software. This function may be used for remote operation of the answering device. The identification code of one of 12 detected DTMF signals is transferred to the host for further processing.

Tone Generation

Single and double tone signals can be generated by D6305A. The levels and frequencies are programmable and controlled by HOST. During tone generation the D6305A monitors the line.

Call Progress Tone Detection

The D6305A monitors the line for incoming telephone line signals and detects the presence of call progress tones in a predefined frequency region. The D6305A supports call progress tone detection by utilizing filter/detector with a band width of 300 - 640 Hz. Indication of the presence of call progress tones is transferred to the HOST, and may be used for terminating recording.

Speed Dial Telephone Number Storage

The D6305A may store up to 32 telephone numbers, each with up to 16 digits for speed dialing.

Self Test and Initialization

The D6305A supports a self test function which is responsible for testing and mapping of the ARAMs and system initialization. The results of each device test are returned to the HOST.

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Voice Prompt Generation

The D6305 implements high-quality Voice Prompt playback, utilizing the built-in speech decoder and an external EPROM/ROM, which stores the vocabulary. The D6305A supports up to a 64-Kbyte EPROM/ROM which allow storage of up to 78 seconds of voice prompts. The vocabulary supports up to 128 phrases or utterances. The D6305A receives the phrase number from the host as part of the Voice Prompt command, and outputs the appropriate speech segment via the CODEC interface. The gap between two consecutive phrases is controlled by the host and can be as low as 0.

During playback of the Voice Prompts, the D6305A monitors the telephone line.

The EPROM/ROM is built with a Voice Prompt Workstation which is available through DSP Group, Inc.

Near End Echo Cancellation

A near-end echo canceller is activated during Playback, Tone Generator and Voice Prompt Generation modes. This echo canceller enhances the performance of the DTMF and Call Progress Tone detectors in presence of audio echo.

Power Down Mode

The D6305A is capable of maintaining the messages and data stored in the ARAM during power failure. The D6305A will switch to low power consumption mode and will continue processing the refresh mode to the ARAM as long as D6305A and ARAM are powered by backup batteries.

OPERATIONAL DESCRIPTION

INITIAL PROCEDURE ♦

After power up, the input PDN\ signal (pin 22) should be set high followed by the input RESET pulse. Upon getting power up RESET the D6305A calculates the checksum of the entire ERAM* and compares it with the checksum calculated prior to power failure and responds to one of the situations:

1. The ERAM status is OK (checksum remained unchanged during battery backed-up power failure) - warm start. The D6305A restores the previous conditions and system parameters. The message directory and all the messages remain saved.
2. The ERAM status is bad (checksum has been changed during power failure or checksum was not calculated previously - cold start. The D6305A initializes all parameters to their default values. All of the messages will be lost.

After the above system initialization the D6305A will automatically perform "Garbage Collection" in order to remove gaps between messages, in case the power fail occurred before or during Garbage Collection. After completing Garbage Collection, the D6305A will send its status to the HOST and will enter Idle mode. The HOST should read this status by polling the $\overline{\text{ACK}}$ line (pin 3) and, when low, read the status word. From then on, the HOST will send a command and wait for the status word from the D6305A. For each command, a status word is expected within 1 to 33 msec (see table on page 11), except for Self Test & Init and Garbage Collection. In order to perform an appropriate power-up sequence, Host should send Read Memory Status command and determine whether it was "cold" or "warm" start by checking the ERAM status (bit 8).

If the input signal INIT is set to high during RESET, the D6305A will perform "cold start" regardless of the ERAM status. If the INIT pin (pin 76) is set to low or left unconnected, it does not effect the initial procedure.

*ERAM is the first part of the ARAM devoted for internal use.

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MODES OF OPERATION

The D6305A is normally in Idle mode. Each time a command other than Idle is issued, the system will enter the new mode. From some of the modes, the system will automatically return to Idle mode after completion of the operation. Other modes (Record, Playback, Tone Generation, Line Monitoring, Voice Prompt Generation, Speaker-Phone) require Idle command to return to Idle mode.

There are 14 modes of operation. Each of these modes is entered from the monitor program through Idle mode. The 14 modes are as follows:

0. Idle—The D6305A performs command polling. It checks the command register in the HOST-D6305A interface and transfers to the requested operating mode.
1. Record—The D6305A performs speech compression and records the message to the ARAM.*
2. Playback—The D6305A performs message playback using compressed speech data stored in the ARAM.*
3. Read Memory Status—The D6305A returns information on the Memory status to the HOST, e.g., the number of messages stored in the ARAM, the availability of memory for recording the next message, program ROM checksum status, voice prompt EPROM checksum status and ERAM status.
4. Write Telephone Number—In this mode the D6305A receives a 16-digit telephone number from the HOST and stores it in the telephone number directory.
5. Read Telephone Number—The D6305A returns to the HOST a telephone number stored in the telephone directory under the index number given by the HOST.
6. Tone Generation—The D6305A generates a single or double tone with programmable parameters.*
7. Line Monitoring—The D6305A monitors the telephone line for the presence of DTMF signals and call progress tones.*
8. Delete Message—The D6305A can erase any selected ARAM message entry whose number is specified by the HOST from the messages directory. The D6305A is able to perfom Garbage Collection to remove unused memory space between messages.
9. Set Current Time—The HOST sends the D6305A the current time & date stamp to be attached to the next recorded message.
10. Get Time Stamp—The D6305A returns to the HOST the time & date stamp asociated with the specific ARAM message.
11. Get Available Record Time—The D6305A reports the currently available ARAM record time.
12. Self Test & Initialize Memory—The D6305A performs ARAM testing and mapping.
13. Voice Prompt Generation—The D6305A implements a TRUESPEECH™ Voice Prompt playback from an external EPROM/ROM.*

*These modes require Idle command to return to Idle mode.

DESCRIPTION OF MODES OF OPERATION

Idle

This is a polling mode in which the D6305A monitors the D6305A-HOST interface for HOST commands. Transition to any other mode must always be done through the Idle mode.

Record

When the HOST sends a Record command, the D6305A performs speech compression and stores the message in the ARAM. If bit 6 (VOX) in the first Record command is "0", the D6305A starts recording immediately after receiving the Record command. If VOX bit is set to "1", the D6305A starts recording after detecting voice activity.

The compression algorithm, implemented in the D6305A is HOST programmable and is able to utilize fixed and variable compression rates as well as "gap coding". Mode (bits 7 - 9 of the first Record command) is as follows:

000 - fixed compression rate
001 - variable compression rate
010 - fixed rate plus "gap coding"
011 - variable rate plus "gap coding"

The compression algorithm is defined by the first Record command and cannot be changed while in Record mode.

While in this mode, the D6305A monitors the communication port every 33 ms for HOST commands. If no new command is detected, the D6305A continues recording. If an additional Record command is detected, the D6305A returns the status word with VOX status (bit 6), memory status (bit 7), code of detected DTMF (bits 0 - 3), and call progress tone presence (bit 4) to the HOST.

If an Idle command is detected, the D6305A stops recording, updates message directory, and returns to Idle mode.The D6305A reports to the HOST by sending the Idle mode status word. The D6305A assigns the next available message number to a newly recorded message. The first message will be assigned the number "0", the second message will be assigned the number "1", and so on, up to "63".

Record mode can be terminated by sending a Record command with "Tail Cut" information. The D6305A stops recording and automatically deletes the last n*0.266 seconds from memory (Tail Cut function). The D6305A then returns to Idle mode.

If the ARAM has become full, the Memory bit (bit 7) in the status word is set. The D6305A stops recording, remains in Record mode and continues to perform line monitoring and VOX functions.

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Playback

In playback mode, the D6305A performs message playback and line monitoring. The first playback command is used by the HOST to instruct the D6305A which message to play (bits 0 - 6 message number). The second playback command instructs the D6305A to play back messages from the beginning. D6305A does not support OFFSET, so 11-0 will always be "0". Message playback starts immediately after receiving the second playback command.

After starting playback, the D6305A monitors the HOST command register every 33 ms. The HOST issues additional playback commands during playback in order to perform line monitoring and/or pause playback. If the pause bit (bit 11) is "0" the D6305A will continue playback and will return a line status in the status word. If pause is set, playback will stop until the pause bit returns to "0". Line monitoring will continue during pause.

The line status word contains information about the tones detected from the line, and End of Play flag (bit 7), which indicates whether the end of the current message has been reached. When this bit is low, the message is still being played; when it is high, playback has stopped. The D6305A will continue to stay in playback mode and monitor the line. If the requested message number does not exist, the D6305A will return a status word with End of Play "1" following the third playback command. If the D6305A detects a DTMF tone, the number of this tone will be contained in bits 0-3 of the status word. The presence of a call progress tone will be contained in bit 4. The host will monitor these tones every 33 ms and will act accordingly. Playback will be terminated by Idle command and the D6305A will return to Idle mode.

Read Memory Status

In this mode, there are two submodes:

1) Get memory status (mode = 00)

In this submode the D6305A returns to the HOST a status word containing the following information:

- — Number of recorded messages
- — Memory full indication
- — ERAM status
- — Program ROM status
- — Voice Prompt EPROM status

When 64 messages were recorded or when there is no available memory space for recording further messages, Memory Full Flag (bit 7) is set.

ERAM status bit indicates whether an internal memory check was successful. The ERAM status is used to select between "cold start" or "warm start" for power up procedure after Reset. For detailed description see INITIAL PROCEDURE.

After sending the memory status, the D6305A returns automatically to Idle mode.

2) Get Product Number (mode = 01)

In this submode, the D6305A returns four digits of product number, i.e. 6305 (0110 0011 0000 0101).

Write Telephone Number

In this mode the D6305A receives from the HOST a word containing 4 telephone digits and writes it in the telephone directory under the entry number specified in the command word (the first word). This stored information can be actually used for any other host needs. The D6305A automatically returns to the Idle mode after this command.

Read Telephone Number

In this mode the D6305A returns to the HOST a word containing 4 telephone digits from the telephone directory, or any other information previously stored by the HOST, using the entry specified in the first command word. The D6305A automatically returns to the Idle mode after this command.

Tone Generation Mode

In this mode the D6305A generates a single or double tone with HOST programmable gains and frequencies. All the parameters of the tones are defined by the sequence of three Tone Generation commands. The first command defines "Tone 0" output gain in bits 0 - 3 and "Tone 1" output gain in bits 4 - 7. Each tone can be programmed from -24 dB (gain code 1111) to 6 dB (gain code 0000) with resolution of 2 dB. The second and third commands define the Tone 0 frequency and Tone 1 frequency respectively by the following expression:

$$32767*\cos(2*\pi*fm/7200)$$

where: fm is the desirable frequence

To generate a single tone either the second or third command has to be 7FFFH. The D6305A starts tone generation only after receiving the third command. The D6305A checks the host port every 33 ms for a new HOST command. If no new command is sent, the D6305A continues generating the same single or double tone. To change parameters of the generated signal, the sequence of three commands should be sent to the D6305A. The duration of this sequence should not be more than 30 ms.

While in this mode, the D6305A monitors the line for presence of DTMF and call progress tones. An Idle command will terminate generation and return the D6305A to Idle mode.

Line Monitoring Mode

In this mode the D6305A monitors the telephone line for the detection of a DTMF signal and/or existence of Call Progress tone. While in this mode, the D6305A is monitoring the communication

port every 33 msec for a HOST command. If no new command is detected, the D6305A continues monitoring the line.

The D6305A returns a status word to the HOST containing the call progress tone flag (bit 4) and the index of the DTMF signal that has been detected:

INDEX	DTMF CODE
0	No Tone
1	1
2	2
3	3
4	4
5	5
6	6
7	7
8	8
9	9
A	*
B	0
C	#

The D6305A will stop monitoring the line and return to Idle mode when an Idle command will be sent.

Delete Message

In this mode the D6305A performs one of the following functions:

1. If the Garbage Collection bit (bit 11) is 0, the D6305A removes the message entry specified in bits 0 - 6 from the message directory, shifts all higher message entries one place down in the directory and decreases the total number of messages by one. Deletion of a message will not free up memory space until a Garbage Collection command will be performed.
2. If the Garbage Collection bit is 1, the D6305A performs Garbage Collection to get rid of empty spaces in the message memory. The D6305A moves one message at at time and returns the status 8800H after moving each of the messages (but the last one). After moving the last message, the D6305A returns the status 8880H. Memory is freed only after moving the last message.

Notes:

1) The D6305A performs Garbage Collection automatically after each release of RESET signal from the chip.

2) The D6305A response time to the Garbage Collection command depends on the length of the messages to be relocated in the memory. For 8 megabits of memory, Garbage Collection can take up to 4 seconds.

Set Current Time

In this mode the HOST sends to the D6305A the current time and date mark that will be used for time stamping of the next message to be recorded. This Time Stamp is attached to the message and can beretrieved by Get Time Stamp command. The D6305A automatically returns to the Idle mode after this command.

Get Time Stamp

In this mode the D6305A sends to the HOST the time and date stamp of the message specified in the command word. The D6305A automatically returns to the Idle mode after this command.

Get Available Record Time

In this mode, the D6305A sends to the HOST the minimum available ARAM record time in 1.22 second units. The D6305A automatically returns to the Idle mode after this command.

Self Test and Initialize Memory

In this mode the D6305A performs memory testing and initialization of the system parameters. There are two submodes in this mode:

1) ARAM Test and Initialization (Test Mode = 000)

This submode is normally used after first power up of the system. The HOST must send this command to the D6305A in order to initialize and map the system memory. The D6305A performs ARAM mapping in order to determine the ARAM size. The D6305A reports whether each of the installed ARAMS passed the test.

At the end of the memory initialization process, the D6305A writes known patterns to some predefined locations of the upper area of the ARAM called ERAM. This pattern is used for ERAM status test.

If the memory was not initialized after first power-up, the D6305A assumes that the system has 16 Mbit DRAM.

2) Fast ARAM Test (Test Mode = 001)

This submode can be useful for production line testing. It gives fast indication on the existance of each of the ARAM chips in the system.

Voice Prompt Generation

In this mode the D6305A plays back a speech segment that was previously stored in an external ROM/EPROM using the speech decompression algorithm. The host is indicating to the D6305A the phrase number to play (0 - 127) in bits 0 - 6 in the command word. The D6305A will load the phrase, start playing it and send the status word to the HOST containing line status and playback status. The line status part will contain information about DTMF and call progress tones in the same way as for the Line Monitor command. The status word also contains two flags: END OF PLAY and READY. The HOST can continuously monitor the status by issuing a VOICE PROMPT command (every 33 ms) and act according to the returned flags.

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READY - this bit (bit 10) is set to "1" by the D6305A two frames (frame = 33 ms) before the end of the phrase playback. It indicates that the D6305A is ready to load a new phrase. The HOST will load the new phrase by setting LOAD bit (bit 11) to "1" in the next command and indicating the new phrase number in bits 0 - 6. Sending Load command while ready bit is "0" will not load the new phrase. If the HOST sends a LOAD command immediately after status with READY bit high, there will be no silence gap between the two phrases. The HOST can delay the Load command for a few frames and create a gap between two phrases in units of 33 ms. In that case, the D6305A will transmit silence to the codec but will stay in Voice Prompt mode.

END OF PLAY - this bit (bit 7) is set one frame after the Ready bit and indicates that the D6305A is playing the last frame of the phrase.

The Voice Prompt mode is terminated by sending Idle command.

Notes:
1) If the phrase number is higher than the last phrase recorded in the ROM/EPROM, the status word will return END OF PLAY and READY bits high and no playback will be performed.

2) The amount of recording time for voice prompts depends on the ROM/EPROM size and it is 19.5 seconds for each 16 Kbytes of memory space.

HOST INTERFACE PERFORMANCE

The D6305A maximum response times to HOST commands are as follows:

COMMAND	MAX STAT US RESPONSE TIME
Idle	33 msec
Record	33 msec
First Playback	1 msec
Second Playback (offset)	1 msec
Next Playback (Continue)	33 msec
Line Monitor	33 msec
Delete Message without Garbage Collection	1 msec
Delete Message with Garbage Collection	4 sec*
Set Current Time	1 msec
Get Time	1 msec
Get Available Record Time	1 msec
Read Memory	6 msec
Write Telephone Number	1 msec
Read Telephone Number	1 msec
Tone Generation (three program commands)	1 msec
Tone Generation (Continue)	33 msec
Voice Prompt Generation	33 msec
Self Test	5 sec*

* execution time for D6305A system with 8Mbit ARAM.

Power Down Operation ♦

The system needs two sources of power:

- VCC - Battery backed 5VDC supply, connected continuously to the D6305A-11 and ARAM.
- VCC1 - 5VDC that supplies power only during power on, connected to the CODEC, EPROM and other components.

Power fail indication signal is supplied to the D6305A through $\overline{PDN}$ pin (pin 22). A RESET input signal is also connected to the D6305A (pin 21).

In power up sequence, the $\overline{PDN}$ signal should go high after VCC1 and crystal oscillation have become stable (usually 20 - 50 msec after VCC1 is high). The RESET pulse should be sent with a minimum delay of 5 usec after $\overline{PDN}$ is high. RESET should be at least 10 usec long.

When power failure happens, the $\overline{PDN}$ signal should go low and the D6305A will enter Power Down mode. While in power down mode the D6305A is not operating and will not respond to external signals. While in Power Down mode, the D6305A supports $\overline{CAS}$ before $\overline{RAS}$ ARAM refresh mode.

If the INIT signal (pin 76) is set to high during RESET, the D6305A will perform "cold start" regardless of the ERAM status. If INIT is set low or left unconnected it will not effect the D6305A power up procedure.

The INIT pin can be used for low battery indication. If the back-up battery is connected, the INIT pin should get a low level. In this case, the D6305A will perform normal power up procedure described under INITIAL PROCEDURE (see Page 7). If the battery voltage is low or the battery is not installed, high level should be sent to the INIT pin. This will ensure "cold start" even if the power failure duration is very short.

♦Applicable for D6305A-11DQC and later version

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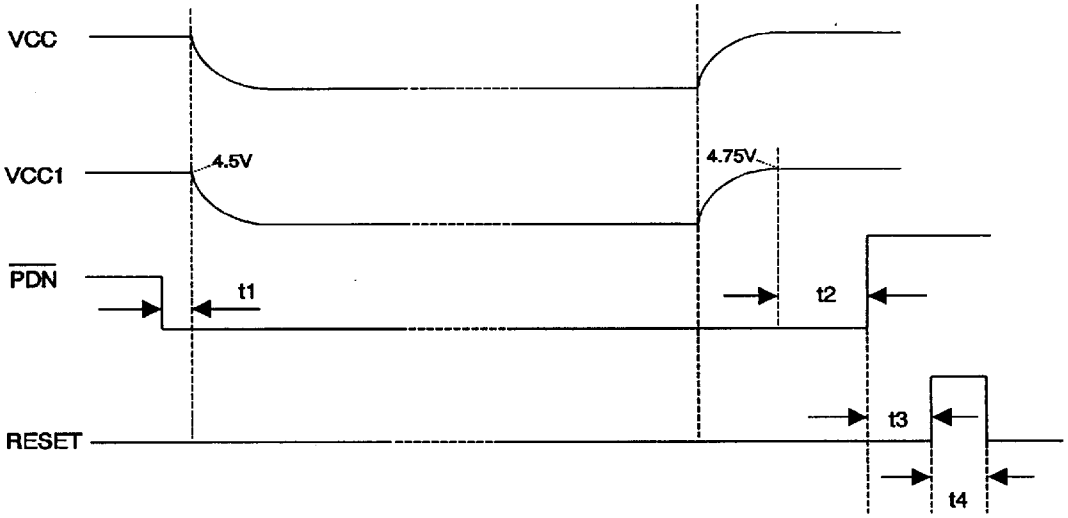

Figure 3. Timing Diagram of Initial Power Up and Power Down/Up without Battery Backup

t1	>0 msec
t2	>50 msec
t3	>5 µsec
t4	>10 µsec

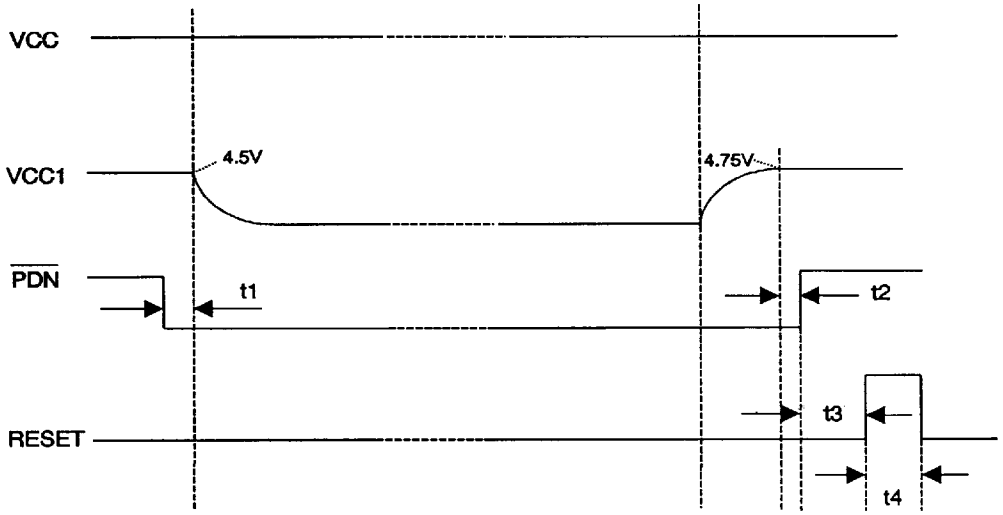

Figure 4. Timing Diagram of Power Down and Power Up with Battery Backup

t1	>3 msec
t2	>0 msec
t3	>5 µsec
t4	>10 µsec

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0. IDLE

Command:

0000	000000000000
(15 - 12)	*(11 - 0)*

Status:

0000	000000000000
(15 - 12)	(11 - 0)

1. RECORD

Command (first):

0001	00	MODE	VOX	000000
(15 - 12)	*(11 - 10)*	*(9 - 7)*	*(6)*	*(5 - 0)*

MODE: = 000 - Fixed rate compression
= 001 - Variable rate compression
= 010 - Fixed rate + gap coding
= 011 - Variable rate + gap coding
= 1XX - Reserved

VOX: = 1 - Start recording on positive VOX detection
= 0 - Start recording immediately without VOX detection

Status:

0001	00	MODE	VOX	000000
(15 - 12)	(11 - 10)	(9 - 7)	(6)	(3 - 0)

Command (second and on):

0001	00	000	END/TAIL CUT FACTOR
(15 - 12)	*(11 - 10)*	*(9 - 7)*	*(6 - 0)*

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When END/TAIL CUT FACTOR = 0 (Continue recording):

Status:

0001	00	0	0	MEM FULL	VOX	0	TONE	DTMF
(15 - 12)	(11 - 10)	(9)	(8)	(7)	(6)	(5)	(4)	(3 - 0)

MEM FULL: 1 - Indicates a full memory condition
VOX: 1 - Speech frame detected
TONE: 1 - Call progress tone detected
DTMF: Code of valid DTMF signal detected

When END/TAIL CUT FACTOR = non zero:

Status:

0001	00	0	0	MEM FULL	TAIL CUT FACTOR
(15 - 12)	(11 - 10)	(9)	(8)	(7)	(6 - 0)

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2. PLAYBACK

Command (first):

0010	000000	MESSAGE NUMBER
(15 - 12)	(11 - 7)	(6 - 0)

Status:

0010	000000	MESSAGE NUMBER
(15 - 12)	(11 - 7)	(6 - 0)

Command (second):

0010	000000000000
(15 - 12)	(11 - 0)

Status:

0010	000000000000
(15 - 12)	(11 - 0)

Command (third and on):

0010	PAUSE	000000000000
(15 - 12)	(11)	(10 - 0)

PAUSE: 0 - Continue playback
1 - Pause

Status:

0010	PAUSE	000	END OF PLAY	00	TONE	DTMF
(15 - 12)	(11)	(10 - 8)	(7)	(6 - 5)	(4)	(3 - 0)

END OF PLAY: 1 - End of message
TONE: 1 - Call Progress Tone detected
DTMF: Code of valid DTMF signal detected

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3. READ MEMORY STATUS

Command:

0011	MODE	0000000000
(15 - 12)	(11 - 10)	(9 - 0)

MODE: = 00: Get memory status
= 01: Get product number
= 1X: Reserved

(MODE 00):

Status:

0011	VOICE PROMPT ROM STATUS	0	PROGRAM ROM STATUS	ERAM STATUS	MEMORY FULL	# OF ARAM MSGES
(15 - 12)	(11)	(10)	(9)	(8)	(7)	(6 - 0)

MEMORY FULL: 1 - Full memory status (message memory full, or directory full)

ERAM STATUS: 0 - External ERAM OK

PROGRAM ROM STATUS: 0 - ROM test OK

VOICE PROMPT ROM STATUS: 0 - Voice Prompt ROM/EPROM test OK

(MODE 01):

Status:

DIGIT 1	DIGIT 2	DIGIT 3	DIGIT 4
(15 - 12)	(11 - 8)	(7 - 4)	(3 - 0)

DIGIT 1..4: 4 digit product no. = 6305 (Digit 1 = MS)

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4. WRITE TELEPHONE NUMBER

Command (First):

0100	00000	DIRECTORY INDEX	GROUP INDEX
(15 - 12)	(11 - 7)	(6 - 2)	(1 - 0)

DIRECTORY INDEX: Telephone number index (0 - 31)
GROUP INDEX: 4 digit group index (0 - 3)

Status:

0100	00000	DIRECTORY INDEX	GROUP INDEX
(15 - 12)	(11 - 7)	(6 - 2)	(1 - 0)

Command (Second):

DIGIT 1	DIGIT 2	DIGIT 3	DIGIT 4
(15 - 12)	(11 - 8)	(7 - 4)	(3 - 0)

Status:

DIGIT 1	DIGIT 2	DIGIT 3	DIGIT 4
(15 - 12)	(11 - 8)	(7 - 4)	(3 - 0)

5. READ TELEPHONE NUMBER

Command:

0101	00000	DIRECTORY INDEX	GROUP INDEX
(15 - 12)	(11 - 7)	(6 - 2)	(1 - 0)

DIRECTORY INDEX: Telephone number index (0 - 31)
GROUP INDEX: 4 digit group index (0 - 3)

Status:

DIGIT 1	DIGIT 2	DIGIT 3	DIGIT 4
(15 - 12)	(11 - 8)	(7 - 4)	(3 - 0)

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6. TONE GENERATOR

Tone Initialization

Command (C1):

0110	1 1	0 0	GAIN 1	GAIN 0
(15 - 12)	(11 - 10)	(9 - 8)	(7 - 4)	(3 - 0)

GAIN 0, 1 = 16 levels with 2 dB steps
0000: +6 dB0
1111: -24 dB0

Status (S1):

0110	1 1	0 0	GAIN 1	GAIN 0
(15 - 12)	(11 -10)	(9 - 8)	(7 - 4)	(3 - 0)

Command (C2):

FREQUENCY FACTOR FOR TONE #0
(15 - 0)

Status (S2):

FREQUENCY FACTOR FOR TONE #0
(15 - 0)

Command (C3):

FREQUENCY FACTOR FOR TONE #1
(15 - 0)

Status (S3):

FREQUENCY FACTOR FOR TONE #1
(15 - 0)

Line Monitoring While In Tone Generator

Command (C4):

0110	0 0	0 0 0 0 0 0 0 0 0 0
(15 - 12)	(11 - 10)	(9 - 0)

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Status (S4):

0110	00	00000	TONE	DTMF
(15 - 12)	(11 - 10)	(9 - 5)	(4)	(3 - 0)

Notes:
To generate a single or double tone, all first three commands should be given in a sequence, with an appropriate status received after each one. To generate a single tone, one of the frequency factors has to be 7FFFH. To stop the tone generation, an IDLE command should be given. To continue generation and monitor the line, the C4 command should be given with bits 11 - 10 set to 00. During monitoring, the status is returned after each frame, only if a command (C4) was issued during this frame (frame is 33 msec).

7. LINE MONITOR

Command:

0111	*0*	*00000000000*
(15 - 12)	*(11)*	*(10 - 0)*

Status:

0111	0000000	TONE	DTMF
(15 - 12)	(11 - 5)	(4)	(3 - 0)

TONE: 1 - Call progress tone detected

DTMF: Code of valid DTMF signal detected

NOTES:

Line monitoring is ended by an IDLE command. Status is returned after each frame only if a command was issued during this frame (frame is 33 msecs).

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8. DELETE MESSAGE

Command:

1000	GC	0000	MESSAGE NUMBER
(15 - 12)	*(11)*	*(10 - 7)*	*(6 - 0)*

GC: 0 - Delete a message, according to MESSAGE NUMBER
1 - Perform Garbage Collection (MESSAGE NUMBER = 0)

For Delete

Status:

1000	0	000	E	MESSAGE NUMBER
(15 - 12)	(11)	(10 - 8)	(7)	(6 - 0)

E: 0 - Valid message has been deleted
1 - Non valid (empty) message

For Garbage Collection

Status:

1000	1	000	E	0000000
(15 - 12)	(11)	(10 - 8)	(7)	(6 - 0)

E: 0 - One messge has been moved
1 - The last message has been moved (procedure has been completed)

9. SET CURRENT TIME

Command (First):

1001	000000000000
(15 - 12)	*(11 - 0)*

Status:

1001	000000000000
(15 - 12)	(11 - 0)

Command (Second):

TIME STAMP
(15 - 0)

Status:

TIME STAMP
(15 - 0)

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10. GET TIME STAMP

Command:

1010	00000	MESSAGE NUMBER
(15 - 12)	(11 - 7)	(6 - 0)

Status:

TIME STAMP
(15 - 0)

11. GET AVAILABLE RECORD TIME

Command:

1011	000000000000
(15 - 12)	(11 - 0)

Status:

1011	0	AVAILABLE TIME
(15 - 12)	(11)	(10 - 0)

AVAILABLE TIME: Minimum available time in units of 1.22 seconds. Largest possible value is 7FCH (111 1111 1100B) for 16 Mbit ARAM.

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12. SELF TEST AND INITIALIZATION

Command:

1100	TEST MODE	00000	ARAM3	ARAM2	ARAM1	ARAM0
(15 - 12)	(11 - 9)	(8 - 4)	(3)	(2)	(1)	(0)

TEST MODE: 000 - ARAM test and initialization mode
001 - Fast ARAM test
1XX - Reserved
X1X - Reserved

ARAM 3..0 1 - ARAM No. 3..0 installed

Status:

1100	TEST MODE	00000	ARAM3	ARAM2	ARAM1	ARAM0
(15 - 12)	(11 - 9)	(8 - 4)	(3)	(2)	(1)	(0)

For test mode = 000 (ARAM test and Initialization

ARAM 3..0 0 - ARAM No. 3..0 passed test, initialization performed up to first bad device (all messages will be erased)
1 - bad or non-installed ARAM

For test mode = 001 (Fast ARAM test)

ARAM 3..0 0 - ARAM No. 3..0 test OK. No initialization
1 - bad or non-installed ARAM

13. VOICE PROMPT GENERATION

Command:

1101	LOAD	0000	PHRASE NUMBER
(15 - 12)	(11)	(10 - 7)	(6 - 0)

LOAD: 0 - Monitor Status
1 - Load new phrase number for playback

PHRASE NUMBER: The serial number of the speech phrase located in the EPROM/ROM, whiich has to be played back (0 - 127).

Status:

1101	LOAD	READY	0 0	END OF PLAY	0 0	TONE	DTMF
(15 - 12)	(11)	(10)	(9 - 8)	(7)	(6 - 5)	(4)	(3 - 0)

READY: 1 - Ready for loading a new phrase for playback
END OF PLAY: 1 - End of message
TONE: 1 - Call Progress Tone detected
DTMF: Code of valid DTMF signal detected

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FUNCTIONAL BLOCKS

The block diagram in Figure 5 shows the D6305A functional blocks and interface.

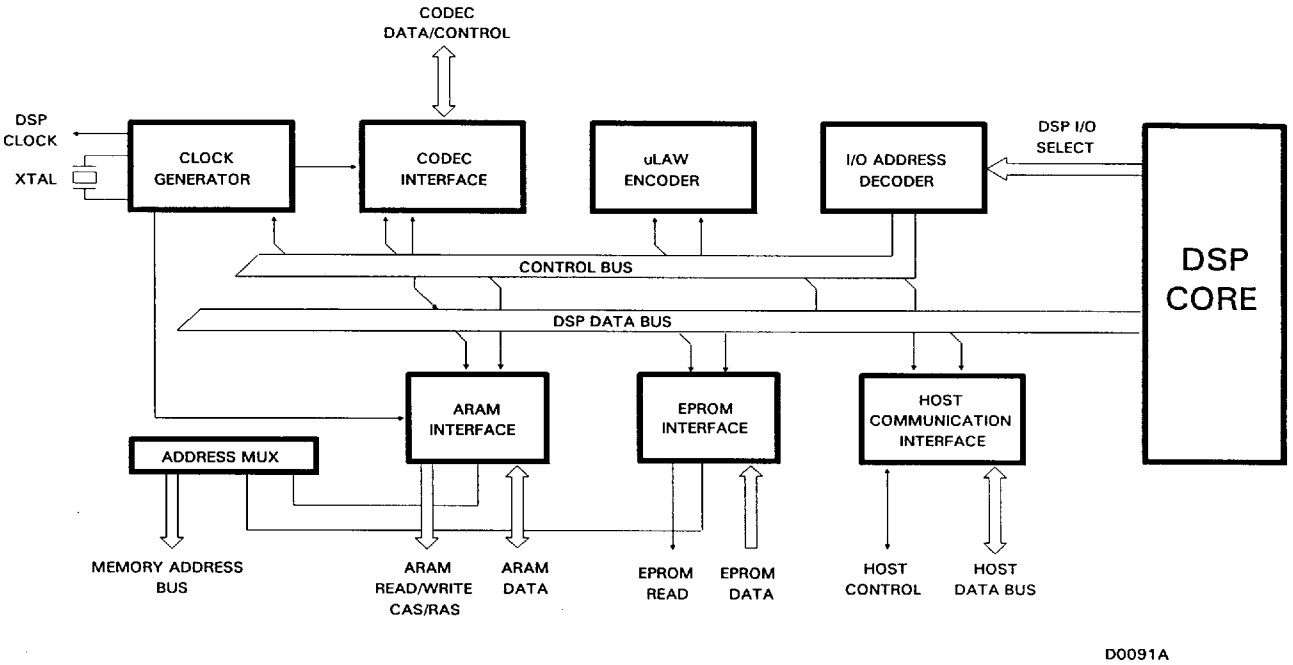

Figure 5. D6305A-11 Block Diagram

DSP CORE

At the heart of the chipset is the DSP core. All of the software algorithms such as compression, decompression, tone detection, tone generation, and echo cancellation run on that processor. The DSP core controls the system, memory and message management. The DSP program ROM is masked internally. The DSP is connected via an internal bus to most of the other modules within the D6305A-11 chip.

ADDRESS MUX

Address MUX controls external memory select signals and memory address bus.

ARAM INTERFACE

The ARAM interface provides access to the ARAM message storage. The interface supports up to 4 ARAM chips with 1Mx4 configuration.

The interface provides also refresh cycles to the ARAM. The interface performs refresh cycles in normal mode, Power Down mode, and when RESET is applied. CAS before RAS refresh mode, implemented by the interface, provides minimum power consumption.

CLOCK GENERATOR

This block provides clock signals to the DSP core and all the internal devices. It also includes clock rate reduction in Power Down mode. When in Power Down mode the ARAM interface only is supplied with clocks

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VOICE PROMPT EPROM/ROM INTERFACE

The interface allows to read data from up to two 32Kx8 EPROMs using 8 bits of the memory data bus for each of these devices (MDB0 - MDB7 for the first 32Kx8 EPROM and MDB8 - MDB15 for the second one).

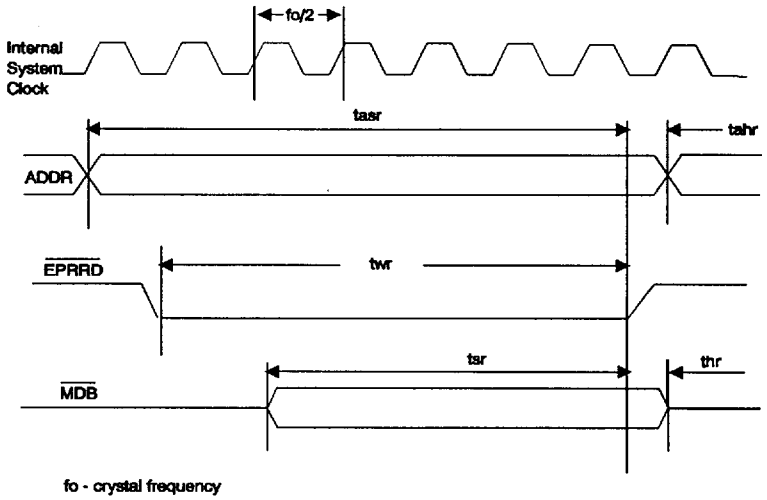

Figure 6. EPROM/ROM Read Timing

PARAMETER	DESCRIPTION	MIN	TYP	MAX	UNITS
tasr	Address setup time	400			ns
tahr	Address hold time	0			ns
tsr	Data setup time	10			ns
thr	Data hold time	0			ns
twr	Read pulse width		396		ns

mLAW ENCODER

This interface provides converting linear code (14-bit) to 8-bit μlaw PCM code.

CODEC INTERFACE

The Analog I/O Interface implements the data transfer and sychronization functions required to interface the DSP with the Analog I/O interface (codec) chip. The data transfer to/from the codecs is serial. The Analog I/O Controller supports fixed rate codecs.

I/O ADDRESS DECODER

The I/O Address Decoder generates the required I/O read and write pulses for the internal DSP peripheral devices.

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HOST—D6305A COMMUNICATION INTERFACE

The host communication port is a 16-bit bidirectional register. The D6305A will access this register internally by one 16-bit wide access. The HOST accesses this register via the 8-bit bus in two accesses: first low byte then a high byte.

After the HOST writes a command to the High byte of this register the D6305A accepts this command.

When the D6305A writes a status word to the communication register it sets the $\overline{ACK}$ pin low (external pin) which is connected to the HOST for indication. The host can use this pin as an interrupt or poll this signal periodically. When the HOST reads the high byte of this register it sets the $\overline{ACK}$ bit high. The choice of high/low byte for the host will be made by the HI/LO pin. The host should read the low byte of the status word first, then the high byte.

The D6305A will send a status word only in response to a host command except for the initial Garbage Collection status word.

Table 1. Communication Interface Signals

Pin Name	Type(*)	Description
HSTDB[0..7]	Input/Output	HOST 8-bit data bus
HSTRD	Input	HOST READ line from register
HSTWR	Input	HOST WRITE line into register
ACK	Output	Flag to HOST–status byte ready in register
HI/$\overline{LO}$	Input	High or Low byte select

*Input and Output are referenced to the D6305A-11.

Figure 7 shows the host interface for the D6305A—8051. Figure 8 shows timing data for the D6305A Communication Interface.

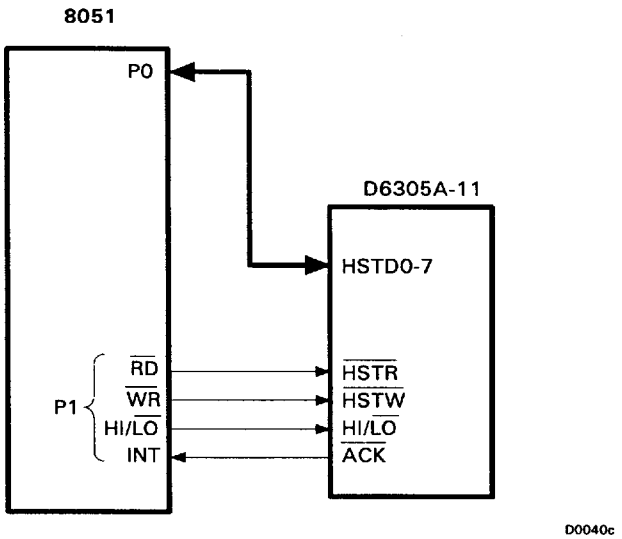

Figure 7. Host Interface D6305A–8051

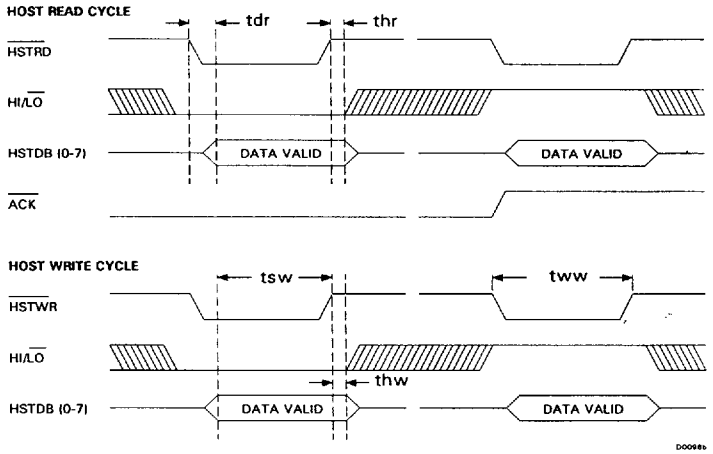

Figure 8. D6305A - Host Interface Timing Data

thr:	= 2ns min
tdr:	=25ns max
thw:	= 5ns min
tsw:	= 30ns min
tww:	= 66ns min

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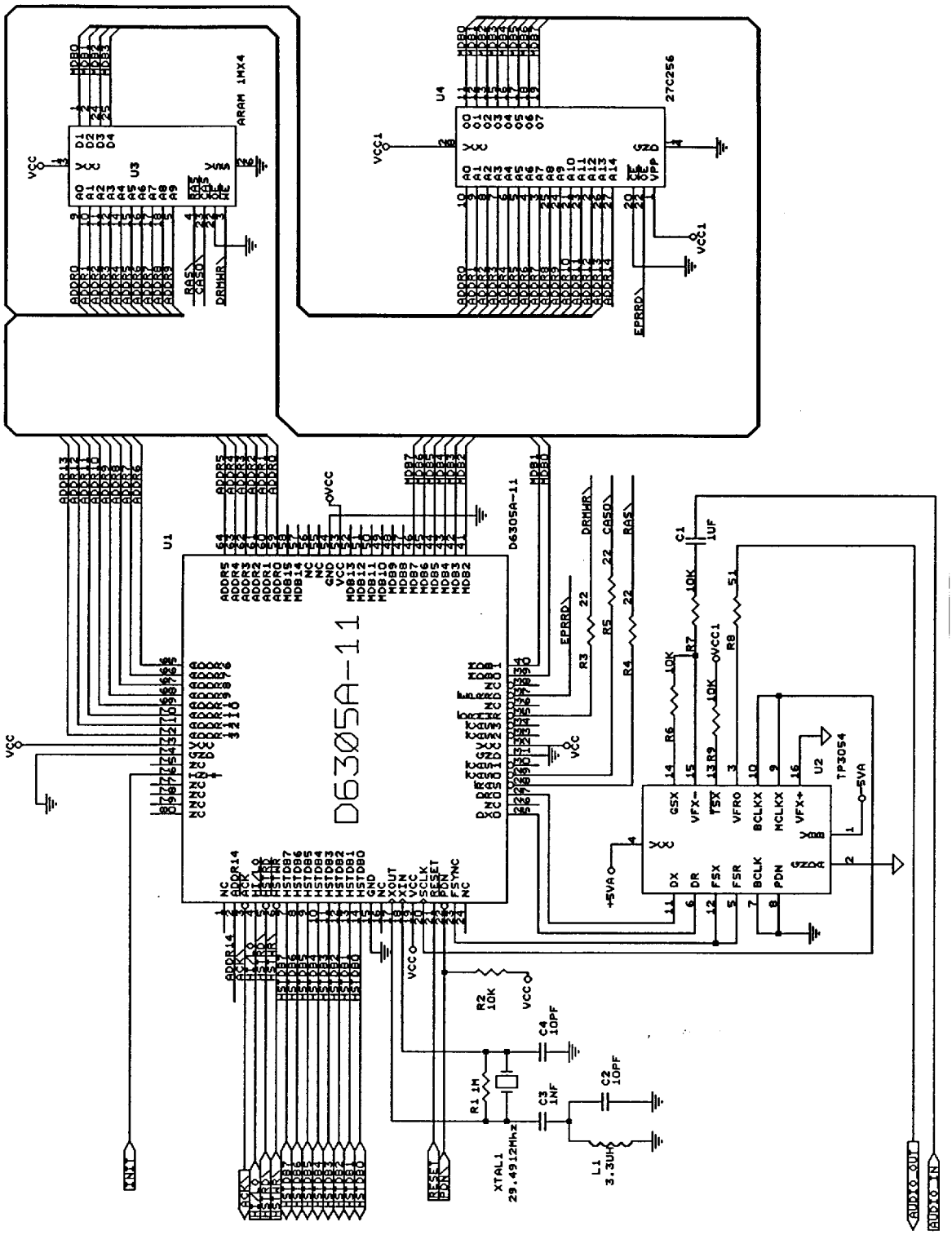

Figure 9. Chipset Interconnection with One 4 Megabit ARAM and One Voice Prompt EPROM

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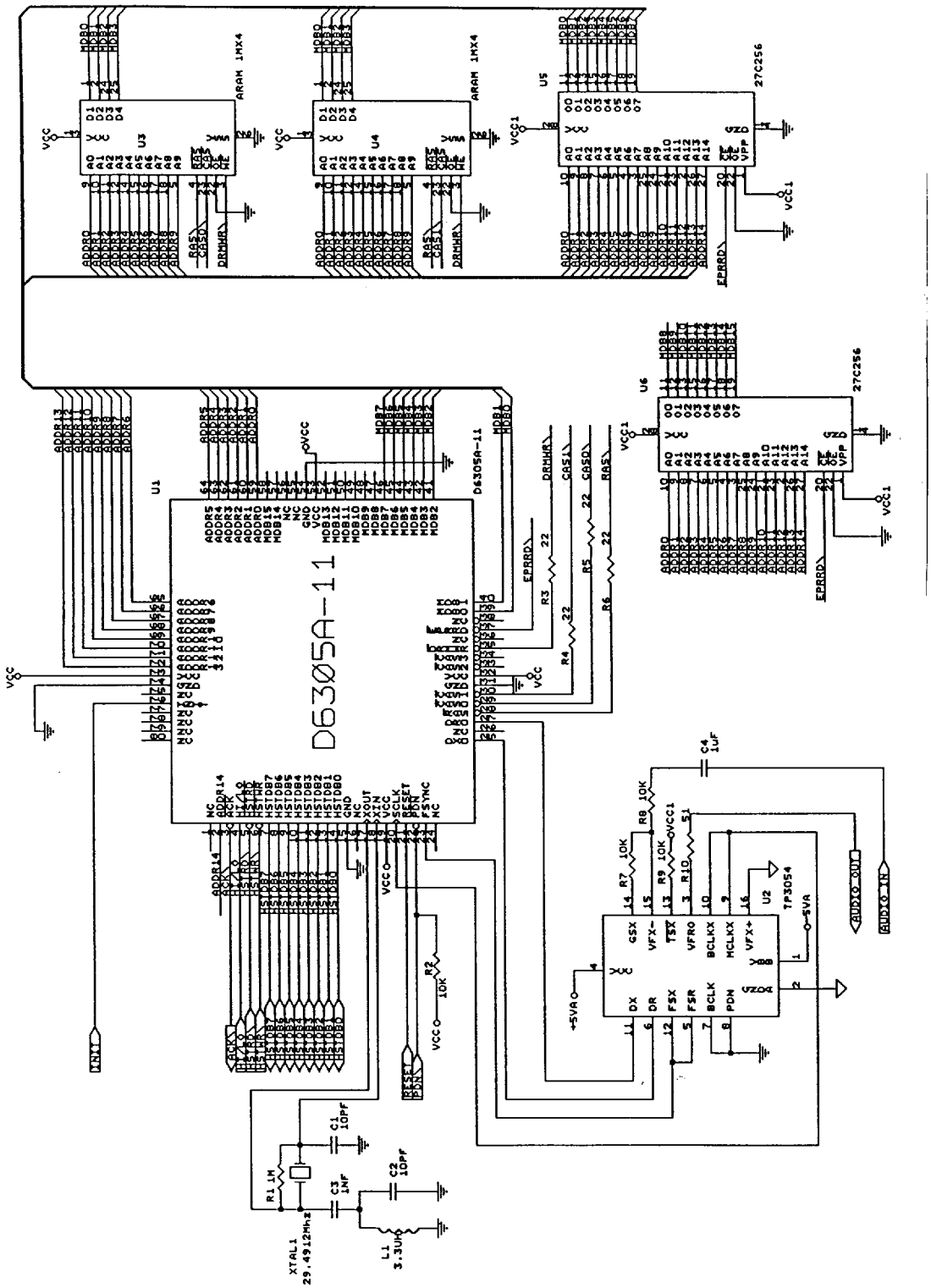

Figure 10. Chipset Interconnection with Two 4 Megabit ARAMS and Two Voice Prompt EPROMS

APPLICATION HINTS

Good printed circuit board (PCB) layout is as important as the overall circuit design itself in achieving high audio quality. To achieve this, the designer has to be conscious of noise both in the D6305A chip and the front-end analog circuitry. Switching mode power supplies are not recommended as the switching spikes will feed through. Other causes of concerns are ground loops and digital feedthrough.

Layout Hints

Ensure that the layout for printed circuit board has digital and analog signal lines separated as much as possible. Take care not to run any digital track along side an analog signal. Guard the analog input with GNDA. Establish a single point analog ground separate from the digital ground. Low impedance analog and digital power supply common returns are essential to low noise operation.

Power Supply Considerations

Since the D6305A is a chipset with analog input and output, its performance (especially the analog front-end) may be adversely affected by the noise of the power supply. In order to prevent mixing of noise, observe the following cautions:

- Separate the power supply to the digital parts and analog parts.
- GNDs of two power supplies should be connected at only one point. Furthermore, that connecting point should be close to the supplies. This will minimize the effect of noise from the digital power supply to the analog power supply.

The power supply should have the least ripple possible, and a series regulator power supply is recommended for best condition.

Good engineering practice calls for proper supply decoupling between the various components. This may be achieved by running separate VCC and ground return lines to the D6305A and ARAMS and placing 0.1 µF ceramic decoupling capacitors near each Vcc supply pin.

Microphone and Speaker Considerations

An often overlooked fact is that the sound quality produced by D6305A chipset is directly related to the quality of the microphone and speaker connected to them. Use a good quality microphone and speaker with good frequency response. Design carefully the microphone preamplifier circuit. The physical location of the microphone, along with the characteristics of the microphone, play a large role in the playback sound quality.

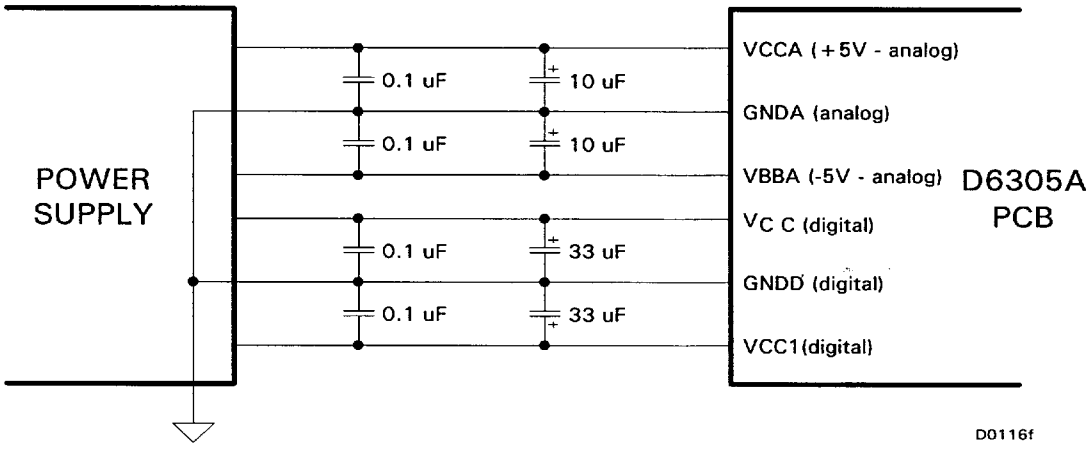

Figure 11. Power Supply

DSP GROUP, INC., 2855 KIFER ROAD, SUITE 200
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ELECTRICAL CHARACTERISTICS

D6305A-11

Absolute maximum ratings over specified temperature range

Supply voltage range, V_{CC}	–0.3 V to 7 V
Input voltage range	–0.3 V to 7 V
Output voltage range	–0.3 V to 7 V
Operating free-air temperature range	0°C to 70°C
Storage temperature range	–55°C to 150°C

Recommended operating conditions

	MIN	TYP	MAX	UNIT
V_{CC} Supply voltage	4.5	5	5.5	V
V_{SS} Supply voltage		0		V
V_{IH} High-level input voltage	2			V
V_{IL} Low-level input voltage			0.8	V
VT+ Positive-going $\overline{RESET}$ and $\overline{PDN}$ threshold		3.35		V
VT– Negative-going $\overline{RESET}$ and $\overline{PDN}$ threshold		1.9		V
I_{OH} High-level output current (all pins except SCLK)			+4	mA
I_{OL} Low-level output current (all pins except SCLK)			-4	mA
I_{OH} High-level output current SCLK			+1	mA
I_{OL} Low-level output current SCLK			-1	mA
Crystal oscillator (100 ppm)		29.4912		MHz
T_A Operating free-air temperature	0		70	°C

Electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TE ST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OH} High-level output voltage (all pins except SCLK)		VCC = 5V	3.5			V
V_{OH} High-level output voltage SCLK		VCC = 5V	2.4			V
V_{OL} Low-level output voltage					0.4	V
I_{oz} Off-state output current		VCC = Max			20	mA
I_I Input current					±20	µA
ICC Supply current	Operating Mode	f = 29,4912MHz; VCC = 5V		68		mA
	Suspend Mode			7.5		mA
CI Input capacitance					20	pF

NOTE: Current consumption is for first revision only.

D0000-29 (Analog I/O interface)

Absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC}	–0.3 V to 7 V
Output voltage, V_O	–0.3 V to 7 V
Input voltage, V_I	–0.3 V to 7 V
Digital ground voltage	–0.3 V to 7 V
Operating free-air temperature range	0°C to 70°C
Storage temperature range	–65°C to 150°C

Recommended operating conditions

		MIN	TYP	MAX	UNIT
V_{CC} Supply voltage		4.75	5	5.25	V
V_{BB} Supply voltage		–4.75	–5	–5.25	V
V_{IH} High-level input voltage, all inputs except CLKSEL		2.2			V
V_{IL} Low-level input voltage, all inputs except CLKSEL				0.6	V
R_L Load resistance	No change transmit	10			kΩ
	At VFR0 Receive	600			Ω
C_L Load capacitance	At GSX			50	pF
	At VFR0			500	
T_A Operating free-air temperature		0		70	°C

Electrical characteristics over recommended ranges of supply voltage and operating free-air temperature supply current, f_{DCLK} 2.048 MHz, outputs not loaded

PARAMETER		TEST CONDITIONS	TYP	MAX	UNIT
I_{CC} Supply current from V_{CC}	Operating		6	9	mA
	Power-down		0.5	1.5	
I_{BB} Supply Current from V_{BB}	Operating		–6	–9	mA
	Power-down		–0.5	–1.5	
Power dissipation	Operating		60	90	mW
	Power-down		5	15	

Transmit amplifier input

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Input current at ANLG IN+, ANLG IN –	V_I = –2.17 V to 2.17 V			±200	nA
Input offset voltage at ANLG IN+, ANLG IN –	V_I = –2.17 V to 2.17 V			±20	mV
Common-mode rejection at ANLG IN+, ANLG IN –	V_I = –2.17 V to 2.17 V	60			dB
Open-loop voltage amplification at GSX		5000			V/V
Open-loop unity-gain bandwidth at GSX			2		MHz
Input resistance at ANLG IN+, ANLG IN –		10			MΩ

Receive filter output

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Output offset voltage PWRO+, PWRO – (single-ended)	Relative to ANLG GND	–200		200	mV
Output resistance at PWRO+, PWRO –			1		Ω

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D0000-35A (4 Mbit ARAM)

Absolute maximum ratings over operating temperature range

Voltage range on any pin	–1 V to 7.0V
Voltage range on V_{CC}	–1 V to 7.0 V
Short circuit output current	50 mA
Power dissipation	1 W
Operating free-air temperature range	0°C to 70°C
Storage temperature range	–55°C to 150°C

Recommended operating conditions

	MIN	TYP	MAX	UNIT
V_{CC} Supply voltage	4.75	5	5.25	V
V_{IH} High-level input voltage	2.4		5.25	V
V_{IL} Low-level input voltage	–0.5		0.4	V
V_{OH} High-level output voltage	2.4			V
V_{OL} Low-level output voltage			0.4	V
T_A Operating free-air temperature range	0		70	°C

Electrical characteristics over full range of recommended operating conditions (unless otherwise noted)

PARAMETER	TEST CONDITIONS	TYP	MAX	UNIT
V_{OH} High level output voltage	I_{OH} = -5mA	2.4		V
V_{OL} Low-level output voltage	I_{OL} = 3.0 mA		0.4	V
I_I Input current (leakage)	V_I = 0 V to 5.25 V, V_{CC} = 5.25 V, all other pins = 0 V to V_{CC}		±20	µA
I_O Output current (leakage)	V_O = 0 V to V_{CC}, V_{CC} = 5.25 V, $\overline{CAS}$ high		±20	µA
I_{CC1} Read or write cycle current	Minimum cycle, V_{CC} = 5.25 V		80	mA
I_{CC2} Standby cycle	After 1 memory cycle, $\overline{RAS}$ and $\overline{CAS}$ high, V_{CC} = 0.2 V		5	mA
I_{CC3} Average refresh current	Minimum cycle, V_{CC} = 5.25 V $\overline{RAS}$ cycling, $\overline{CAS}$ high		70	mA
I_{CC4} Average page (word) current	$t_{C(P)}$ = minimum, V_{CC} = 5.25 V $\overline{RAS}$ low, $\overline{CAS}$ cycling		35	mA

DTMF & VOX Characteristics

PARAMETER	MIN	TYP	MAX	UNIT
DTMF Signal level for detection *	–35		0	dB0
DTMF Twist (High/Low Tone)			±8	dB
DTMF Frequency Detect Band width	±(1.5% + 2Hz)		3.5%	%fc
DTMF Noise tolerance**			–12	dB
DTMF tone duration accept	40			ms
DTMF tone duration reject			23	ms
DTMF interdigit pause accept	40			ms
DTMF interdigit pause reject			23	ms
VOX detection *	–37		+6	dB0
Tone generator frequency accuracy	-0.1		+0.1	%fc
Tone generator level***	-24		+6	dB0
Tone generator level accuracy	-0.5		+0.5	dB

Call Progress Tone Detector Performance

PARAMETER	MIN	TYP	MAX	UNIT
Detection Level *	-29			dB0
Rejection Level *			–34	dB0
Rejection Frequency Range	800		2500	Hz
Frequency Range	300		640	Hz
Signal Duration Accept	200			ms
Pause Duration Accept	200			ms
Response Time			150	ms
Noise Tolerance	-12			dB

*0.707 V RMS is defined as the 0 dB0

**BW limited (0–3.0KHz) Gaussian noise

***0 dB0 is 0.707V RMS programmable with resolution 2dB.

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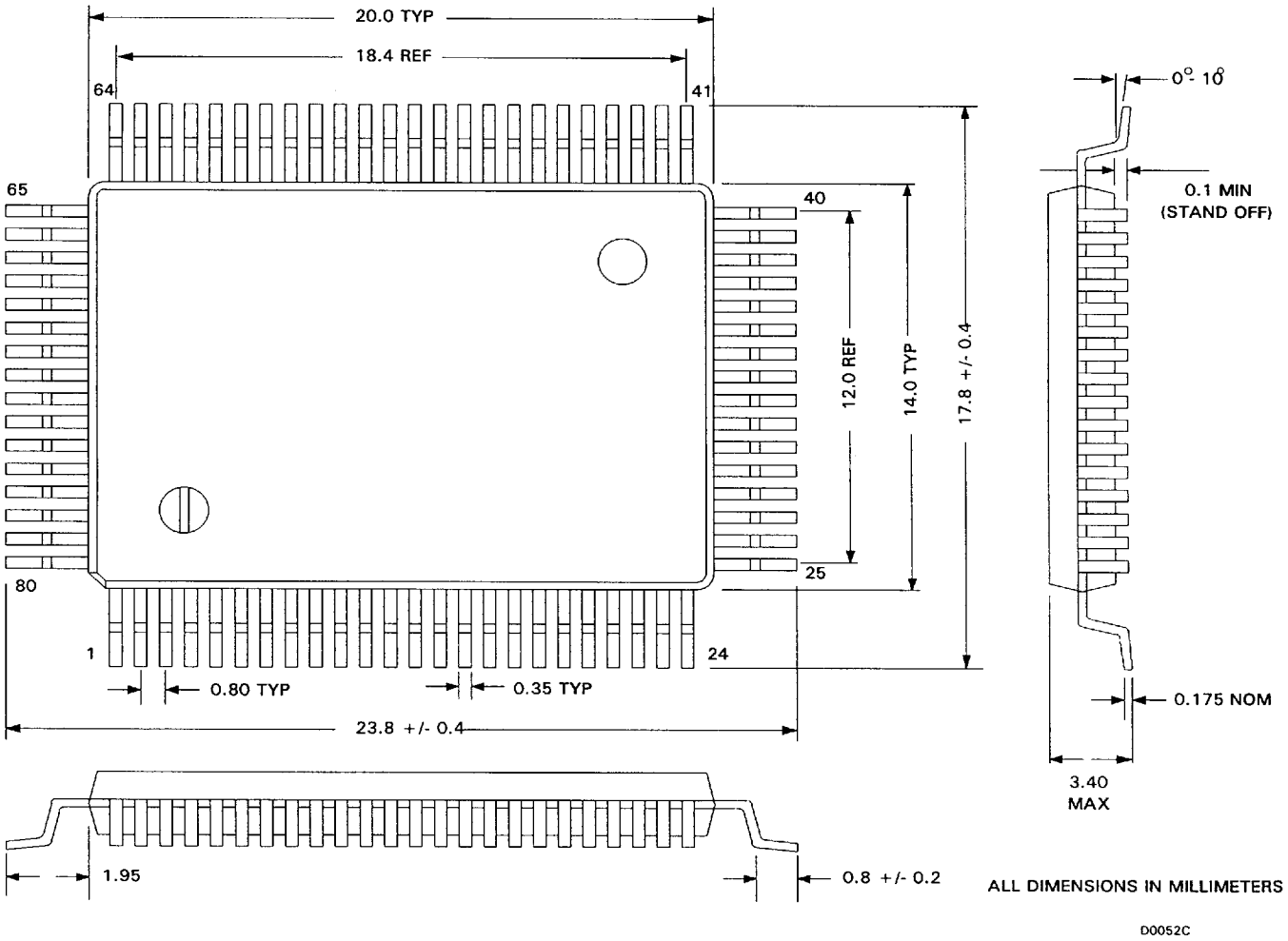
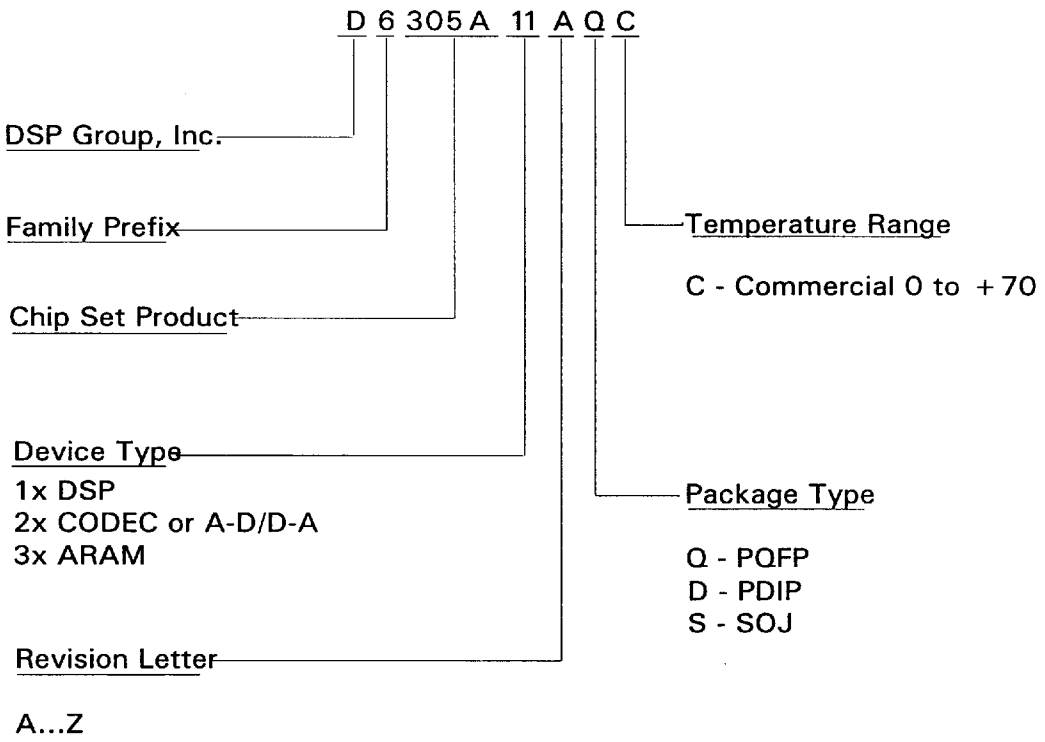


Figure 12. D6305-11 Mechanical Data

DSPG CHIP SET PART NUMBER SYSTEM



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