DS1210

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DS1210
Nonvolatile Controller Chip

FEATURES

- Converts CMOS RAMs into nonvolatile memories

- Unconditionally write protects when V_{cc} is out of tolerance

- Automatically switches to battery when power fail occurs

- Space saving 8-pin DIP

- Consumes less than 100 nA of battery current

- Tests battery condition on power up

- Provides for redundant batteries

- Optional 5% or 10% power fail detection

- Low forward voltage drop on the V_{cc} switch

- Optional 16-pin SOIC surface mount package

PIN DESCRIPTION

DS1210 8-Pin DIP
(300 Mil.)

DS1210S 16-Pin SOIC
(300 Mil.)
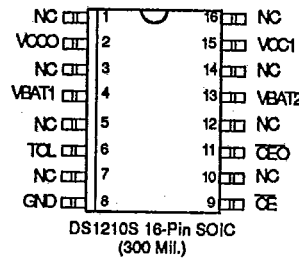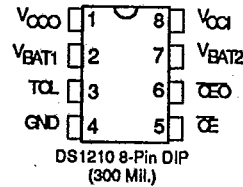
PIN NAMES (\ Denotes Condition Low)

VCCO	RAM Supply
VBAT1	+ Battery 1
TOL	Power Supply Tolerance
GND	Ground
CE\	Chip Enable Input
CEO\	Chip Enable Output
VBAT2	+ Battery 2
VCCI	+ Supply
NC	No Connect

DESCRIPTION

The DS1210 Nonvolatile Controller Chip is a CMOS circuit which solves the application problem of converting CMOS RAM into nonvolatile memory. Incoming power is monitored for an out-of-tolerance condition. When such a condition is detected, chip enable is inhibited to accomplish write protection and the battery is switched on to supply the RAM with uninterrupted power. Special circuitry uses a low-leakage CMOS process which affords precise voltage detection at extremely low battery consumption. The 8-pin DIP package keeps PC board real estate requirements to a minimum. By combining the DS1210 Nonvolatile Controller Chip with a CMOS memory and batteries, nonvolatile RAM operation can be achieved.

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OPERATION

The DS1210 nonvolatile controller performs five circuit functions required to battery back up a RAM. First, a switch is provided to direct power from the battery or the incoming supply (V_{CCI}) depending on which is greater. This switch has a voltage drop of less than 0.3V. The second function which the nonvolatile controller provides is power fail detection. The DS1210 constantly monitors the incoming supply. When the supply goes out of tolerance a precision comparator detects power fail and inhibits chip enable (CEO\). The third function of write protection is accomplished by holding the CEO\ output signal to within 0.2 volts of the V_{CCI} or battery supply. If CE\ input is low at the time power fail detection occurs, the CEO\ output is kept in its present state until CE\ is returned high. The delay of write protection until the current memory cycle is completed prevents the corruption of data. Power fail detection occurs in the range of 4.75 volts to 4.5 volts with the tolerance Pin 3 grounded. If Pin 3 in connected to V_{CCO}, then power fail detection occurs in the range of 4.5 volts to 4.25 volts. During nominal supply conditions CEO\ will follow CE\ with a maximum propagation delay of 20ns. The fourth function the DS1210 performs is a battery status warning so that potential data loss is avoided. Each time that the circuit is powered up the battery voltage is checked with a precision comparator. If the battery voltage is less than 2.0 volts, the second memory cycle is inhibited. Battery status can, therefore, be determined by performing a read cycle after power-up to any location in memory, verifying that memory location content. A subsequent write cycle can then be executed to the same memory location altering the data. If the next read cycle fails to verify the written data, then the batteries are less than 2.0V and data is

in danger of being corrupted. The fifth function of the nonvolatile controller provides for battery redundancy. In many applications, data integrity is paramount. In these applications it is often desirable to use two batteries to ensure reliability. The DS1210 controller provides an internal isolation switch which allows the connection of two batteries. During battery backup operation the battery with the highest voltage is selected for use. If one battery should fail, the other will take over the load. The switch to a redundant battery is transparent to circuit operation and to the user. A battery status warning will occur when the battery in use falls below 2.0 volts. A grounded V_{BAT2} pin will not activate a battery fail warning. In applications where battery redundancy is not required, a single battery should be connected to the BAT1 pin. The BAT2 battery pin must be grounded. The nonvolatile controller contains circuitry to turn off the battery back-up. This is to maintain the battery(s) at its highest capacity until the equipment is powered up and valid data is written to the SRAM. While in the freshness seal mode the CEO\ and V_{CCO} will be forced to V_{OL}. When the batteries are first attached to one or both of the V_{BAT} pins, V_{CCO} will not provide battery back-up until V_{CCI} exceeds V_{CCTP}, as set by the T_{OL} pin, and then falls below V_{BAT}.

Figure 1 shows a typical application incorporating the DS1210 in a microprocessor-based system. Section A shows the connections necessary to write protect the RAM when V_{CC} is less than 4.75 volts and to back up the supply with batteries. Section B shows the use of the DS1210 to halt the processor when V_{CC} is less than 4.75 volts and to delay its restart on power-up to prevent spurious writes.

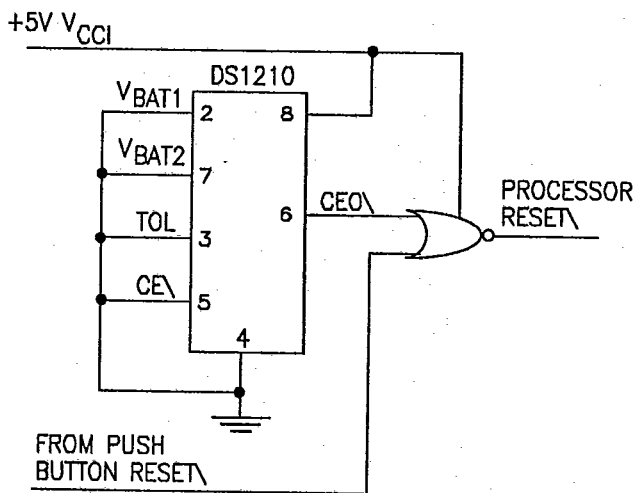## SECTION A - BATTERY BACKUP Figure 1   T-46-23-37
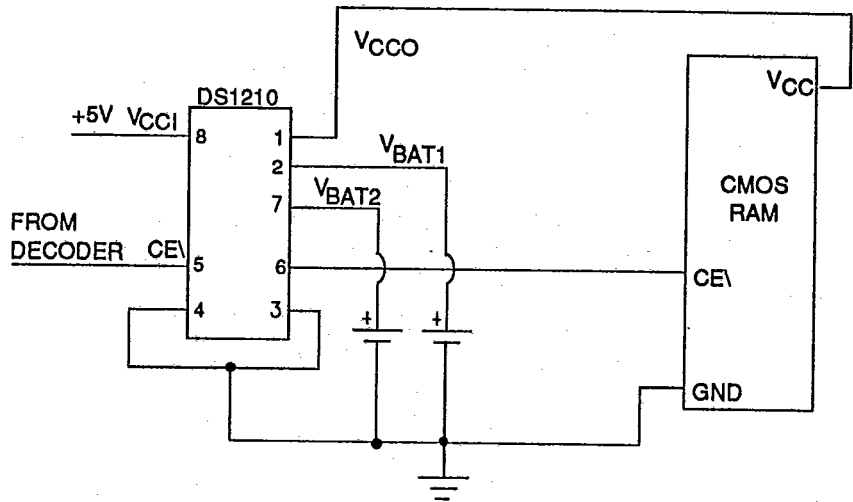
BATTERY BACKUP CURRENT DRAIN EXAMPLE
CONSUMPTION

DS1210 I_{BAT}	100 nA
RAM I_{CCO2}	10 uA
Total Drain	10.1 uA

SECTION B - PROCESOR RESET

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ABSOLUTE MAXIMUM RATINGS*

Voltage on any Pin Relative to Ground	-0.3V to +7.0V
Operating Temperature	0°C to 70°C
Storage Temperature	-55°C to +125°C
Soldering Temperature	260°C for 10 seconds

* This is a stress rating only and functional operation of the device at these or any other conditions outside those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS   (0°C to 70°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Pin 3 = GND Supply Voltage	V_{CCI}	4.75	5.0	5.5	V	1
Pin 3 = V_{CCO} Supply Voltage	V_{CCI}	4.5	5.0	5.5	V	1
Logic 1 Input	V_{IH}	2.2		$V_{CC}+0.3$	V	1
Logic 0 Input	V_{IL}	-0.3		+0.8	V	1
Battery Input	V_{BAT1}, V_{BAT2}	2.0		4.0	V	1,2

(0°C to 70°C, V_{CCI} = 4.75V to 5.5V, Pin 3 = GND)

DC ELECTRICAL CHARACTERISTICS   (V_{CCI} = 4.5 to 5.5V, Pin 3 = V_{CCO})

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Supply Current	I_{CCI}			5	mA	3
Supply Voltage	V_{CCO}	$V_{CC}-0.2$			V	1
Supply Current	I_{CCO1}			80	mA	4
Input Leakage	I_{IL}	-1.0		+1.0	uA	
Output Leakage	I_{LO}	-1.0		+1.0	uA	
CEO\ Output @2.4V	I_{OH}	-1.0			mA	5
CEO\ Output @0.4V	I_{OL}			4.0	mA	5
V_{CC} Trip Point (TOL=GND)	V_{CCTP}	4.50	4.62	4.74	V	1
V_{CC} Trip Point (TOL=V_{CC})	V_{CCTP}	4.25	4.37	4.49	V	1

(0°C to 70°C, V_{CCI} = < V_{BAT})

CEO\ Output	V_{OHL}	V_{BAT} - 0.2			V	
V_{BAT1} or V_{BAT2} Battery Current	I_{BAT}			100	nA	2,3
Battery Backup Current @ V_{CCO} = V_{BAT} - 0.3V	I_{CCO2}			50	uA	6,7

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CAPACITANCE

$(t_A = 25°C)$

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Capacitance	C_{IN}			5	pF	
Output Capacitance	C_{OUT}			7	pF	

AC ELECTRICAL CHARACTERISTICS

$(0°C \text{ to } 70°C, V_{CCI} = 4.75V \text{ to } 5.5V, \text{Pin } 3 = GND)$
$(V_{CCI} = 4.5 \text{ to } 5.5V, \text{Pin3} = V_{CCO})$

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
CE\ Propagation Delay	t_{PD}	5	10	20	ns	5
CE\ High to Power Fail	t_{PF}			0	ns	

$(0°C \text{ to } 70°C, V_{CCI} < 4.75V, \text{Pin } 3 = GND)$
$(V_{CCI} < 4.5, \text{Pin } 3 = V_{CCO})$

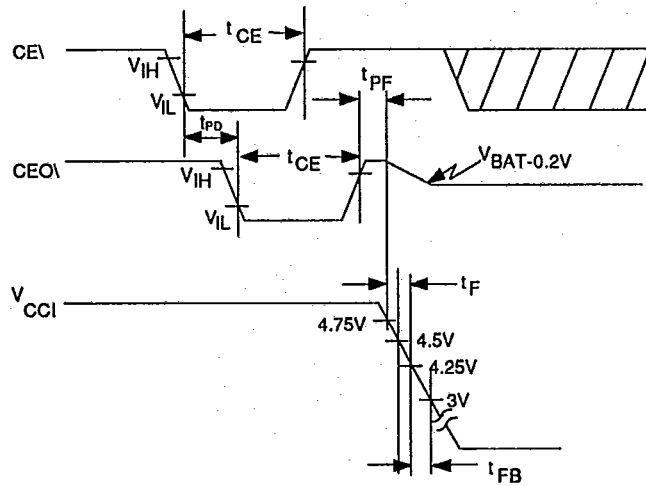| PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Recovery at Power Up	t_{REC}	2	80	125	ms	
V_{CC} Slew Rate Power Down	t_F	300			us	
V_{CC} Slew Rate Power Down	t_{FB}	10			us	
V_{CC} Slew Rate Power Up	t_R	0			us	
CE\ Pulse Width	t_{CE}			1.5	us	7,8

NOTES
1. All voltages are referenced to ground.
2. Only one battery input is required.
3. Measured with V_{CCO} and CEO\ open.
4. I_{CCO1} is the maximum average load which the DS1210 can supply to the memories.
5. Measured with a load as shown in Figure 2.
6. I_{CCO2} is the maximum average load current which the DS1210 can supply to the memories in the battery backup mode.
7. t_{CE} max. must be met to ensure data integrity on power loss.
8. CEO\ can only sustain leakage current in the battery backup mode.

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TIMING DIAGRAM - POWER UP

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CE\

V_{IH}

V_{BAT}-0.2V

CEO\

V_{IH}

t_{PD}

t_{REC}

4.75V
4.5V
4.25V

V_{CCI}

t_R

TIMING DIAGRAM - POWER DOWN

t_{CE}

CE\

V_{IH}
V_{IL}

t_{PF}

t_{PD}

CEO\

V_{IH}

t_{CE}

V_{BAT}-0.2V

V_{IL}

V_{CCI}

t_F

4.75V
4.5V
4.25V
3V

t_{FB}

OUTPUT LOAD Figure 2

+5 VOLTS

1.1K

PIN 6 CEO\

680Ω

50Pf

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