

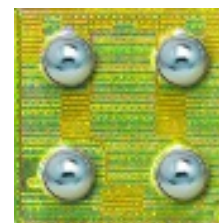
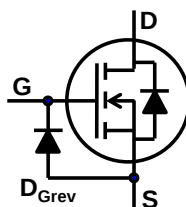
EPC2038 – Enhancement Mode Power Transistor

Preliminary Specification Sheet

Status: Engineering

Features:

- V_{DS} , 100V
- Internal Gate Diode
- Maximum $R_{DS(on)}$, 2.8 Ω
- I_D , 0.5 A
- Pb-Free (RoHS Compliant), Halogen Free



EPC2038 eGaN® FETs are supplied only in passivated die form with solder balls

Die Size: 0.9 mm x 0.9 mm

Applications:

- High Frequency DC-DC Conversion
- Wireless Power Transfer
- LiDAR/Pulsed Power Applications

MAXIMUM RATINGS

Parameter	Value
Maximum Drain – Source Voltage	100 V
Gate – Source Maximum Voltage Range	-4 V < V_{GS} < 6 V
Continuous Drain Current, ($T_A = 25\text{ }^\circ\text{C}$, $R_{\theta JA} = 120\text{ }^\circ\text{C/W}$)	0.5 A
Maximum Pulsed Drain Current, 25 $^\circ\text{C}$, $T_{pulse} = 300\text{ }\mu\text{s}$	0.5 A
Optimum Temperature Range	-40 $^\circ\text{C}$ < T_J < 150 $^\circ\text{C}$

STATIC CHARACTERISTICS

Parameter	Conditions	Value
Maximum Drain – Source Leakage	$V_{DS} = 80\text{ V}$, $V_{GS} = 0\text{ V}$	0.1 mA
Maximum $R_{DS(on)}$	$V_{GS} = 5\text{ V}$, $I_D = 0.05\text{ A}$	2.8 Ω
Typical $R_{DS(on)}$	$V_{GS} = 5\text{ V}$, $I_D = 0.05\text{ A}$	2.1 Ω
Gate – Source Threshold Voltage	$V_{DS} = V_{GS}$, $I_D = 0.06\text{ mA}$	0.8 V < $V_{GS(TH)}$ < 2.5 V
Gate – Source Maximum Positive Leakage	$V_{GS} = 5\text{ V}$	1 mA
Gate – Source Maximum Negative Leakage	$V_{GS} = -1\text{ V}$	-0.1 mA
Source-Gate Maximum Forward Voltage	$I_{SG} = 0.2\text{ mA}$, $V_{DS} = 0\text{ V}$	-2.5 V

$T_J = 25\text{ }^\circ\text{C}$ unless otherwise stated

Specifications are with Substrate shorted to Source

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DYNAMIC CHARACTERISTICS

Parameter	Conditions	Typical Value
C_{ISS} (Input Capacitance)	$V_{DS} = 50\text{ V}, V_{GS} = 0\text{ V}$	7 pF
C_{OSS} (Output Capacitance)		1.7 pF
C_{RSS} (Reverse Transfer Capacitance)		0.02 pF
Q_G (Total Gate Charge)	$V_{DS} = 50\text{ V}, I_D = 0.05\text{ A}, V_{GS} = 5\text{ V}$	44 pC
Q_{GS} (Gate to Source Charge)	$V_{DS} = 50\text{ V}, I_D = 0.05\text{ A}$	16 pC
Q_{GD} (Gate to Drain Charge)		5 pC
$Q_{G(TH)}$ (Gate Charge at Threshold)		14 pC
Q_{OSS} (Output Charge)	$V_{DS} = 50\text{ V}, V_{GS} = 0\text{ V}$	140 pC
Q_{RR} (Source-Drain Recovery Charge)		0

$T_J = 25\text{ }^{\circ}\text{C}$ unless otherwise stated

Specifications are with Substrate shorted to Source

THERMAL CHARACTERISTICS

		TYP	
$R_{\theta JC}$	Thermal Resistance, Junction to Case	27	$^{\circ}\text{C/W}$
$R_{\theta JB}$	Thermal Resistance, Junction to Board	91	$^{\circ}\text{C/W}$
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Note 1)	100	$^{\circ}\text{C/W}$

Note 1: $R_{\theta JA}$ is determined with the device mounted on one square inch of copper pad, single layer 2 oz copper on FR4 board.

See http://epc-co.com/epc/documents/product-training/Appnote_Thermal_Performance_of_eGaN_FETs.pdf for details

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Figure 1: Typical Output Characteristics at 25°C

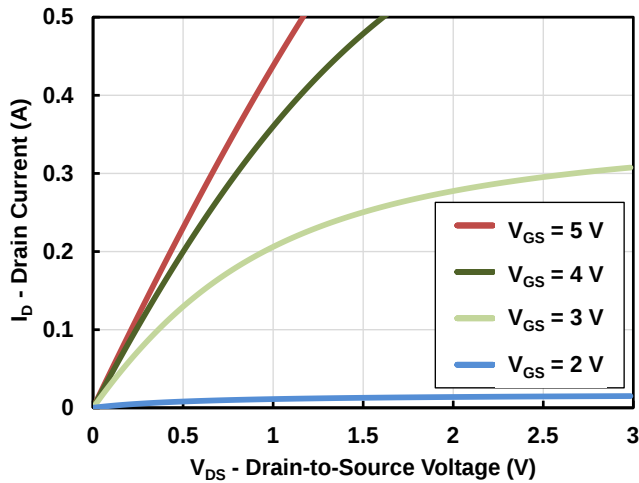


Figure 2: Transfer Characteristics

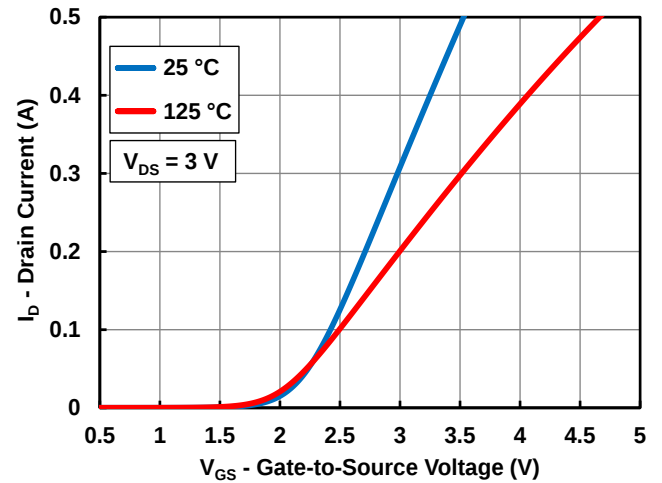


Figure 3: $R_{DS(on)}$ vs. V_{GS} for Various Drain Currents

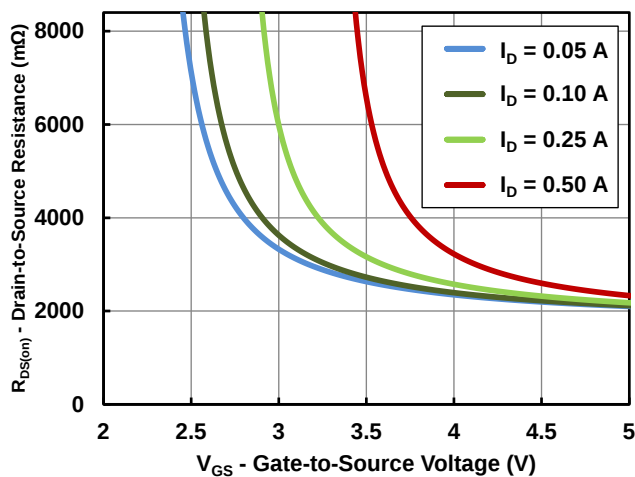


Figure 4: $R_{DS(on)}$ vs. V_{GS} for Various Drain Temperatures

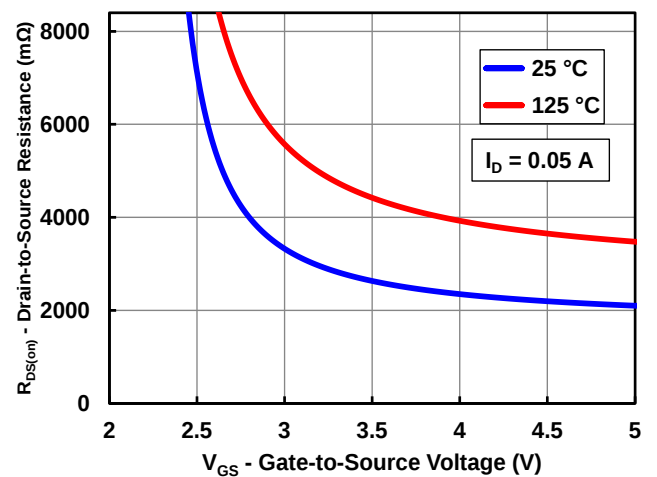


Figure 5a: Capacitance (Linear Scale)

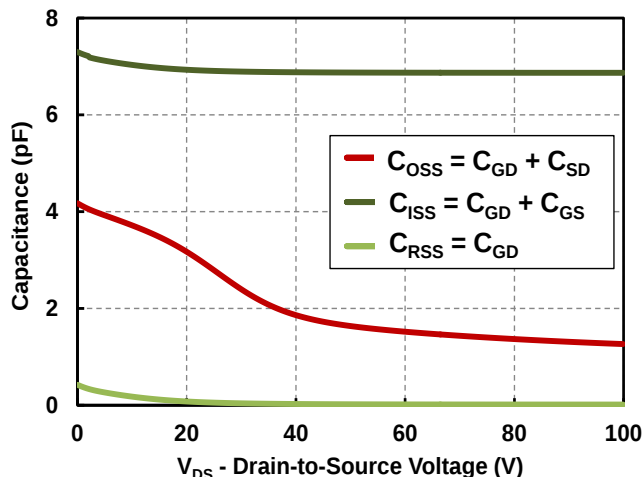
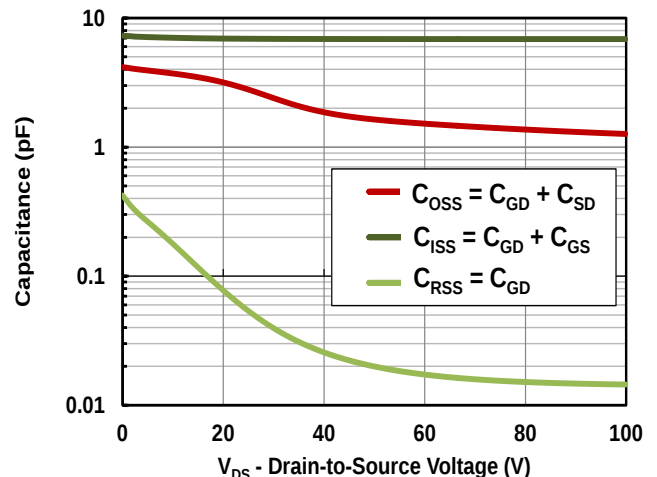


Figure 5b: Capacitance (Log Scale)



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Figure 6: Gate Charge

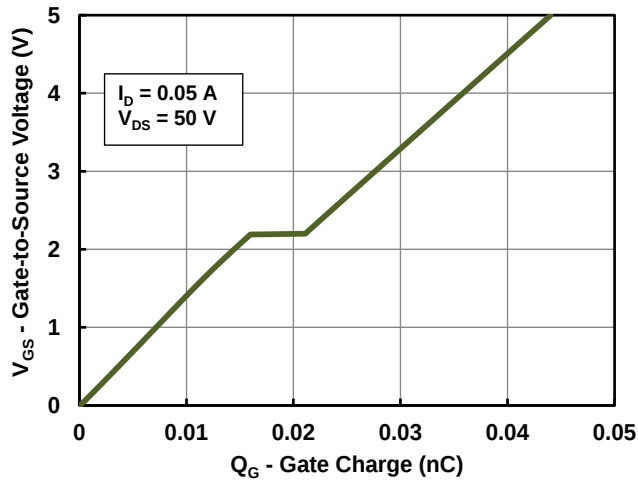


Figure 7: Reverse Drain-Source Characteristics

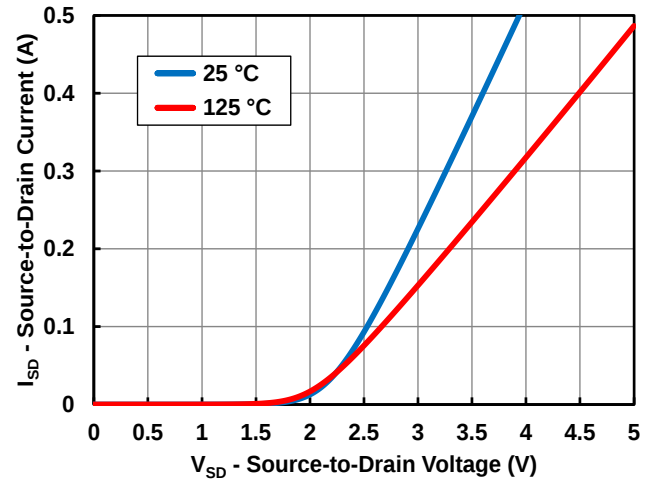


Figure 8: Normalized On Resistance vs. Temperature

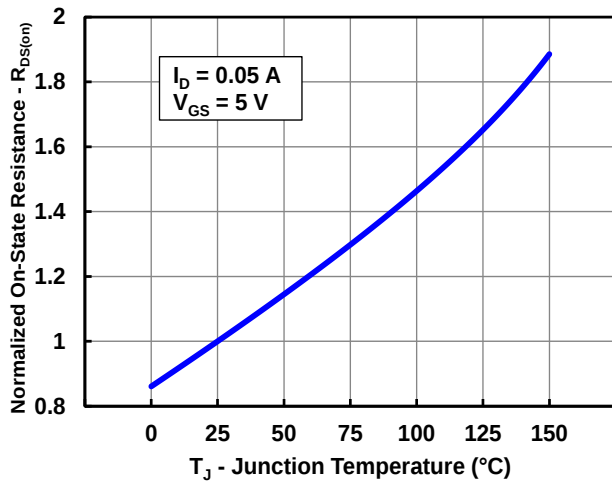


Figure 9: Normalized Threshold Voltage vs. Temperature

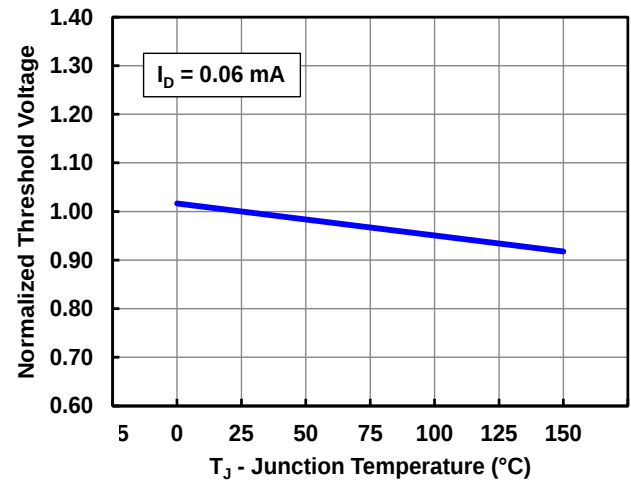
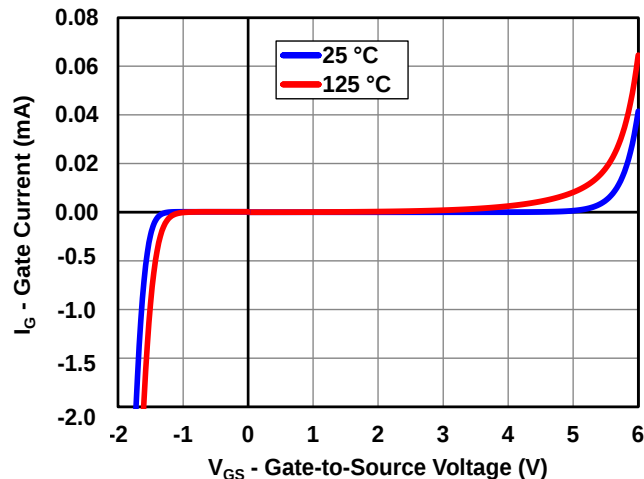


Figure 10: Gate-Source Characteristics

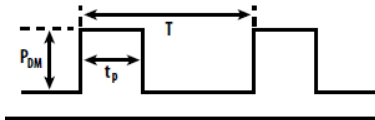
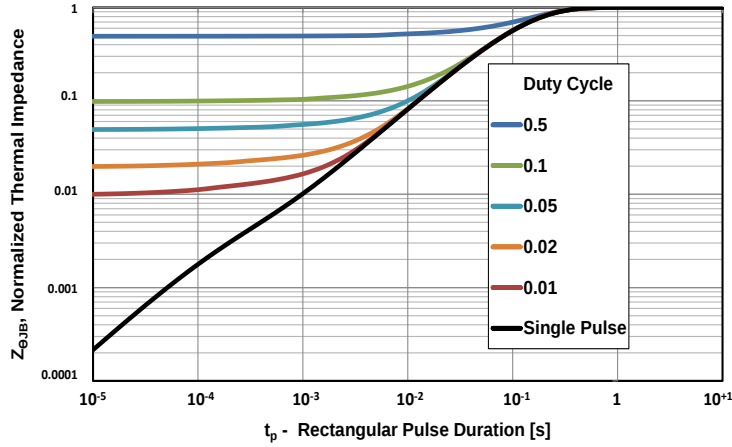


All measurements were done with substrate shorted to source

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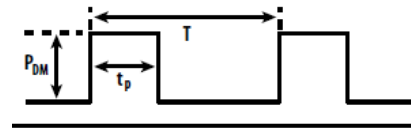
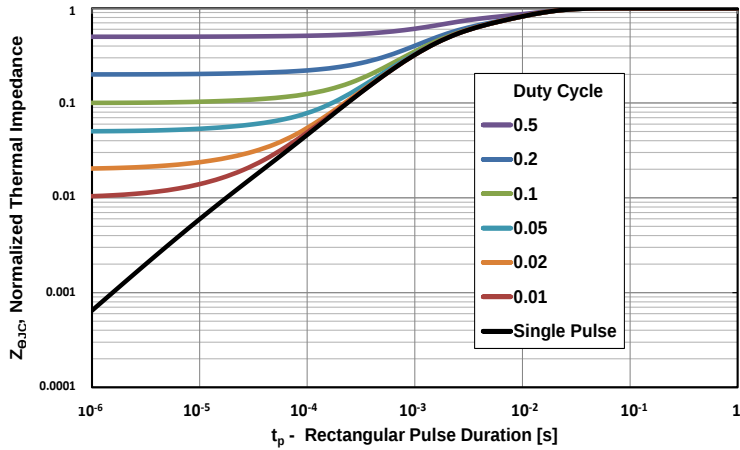
Figure 11: Transient Thermal Response Curves

Junction-to-Board



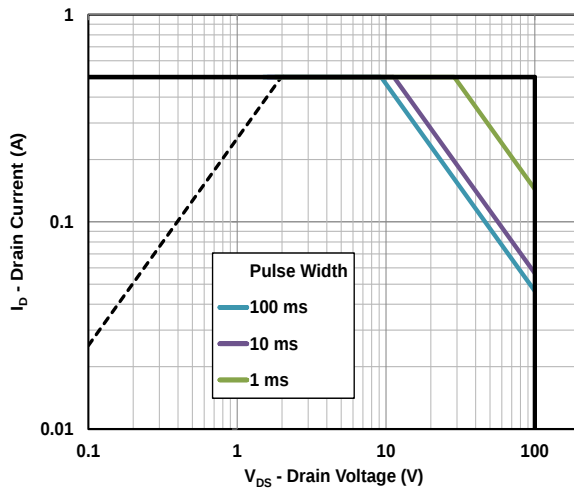
Notes:
Duty Factor = t_p/T
Peak $T_J = P_{DM} \times Z_{\theta JB} \times R_{\theta JB} + T_B$

Junction-to-Case



Notes:
Duty Factor = t_p/T
Peak $T_J = P_{DM} \times Z_{\theta JC} \times R_{\theta JC} + T_C$

Figure 12: Safe Operating Area

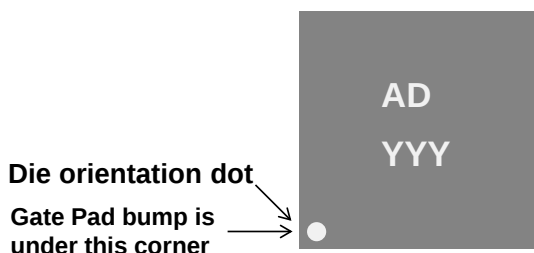


$T_J = \text{Max Rated}, T_C = +25^\circ\text{C}, \text{Single Pulse}$

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DIE MARKINGS

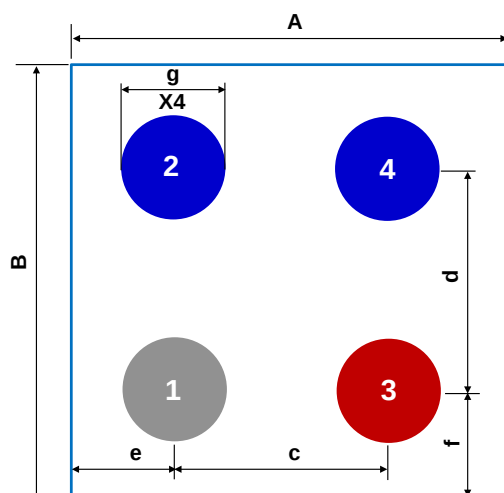


Part Number	Laser Marking	
	Part # Marking Line 1	Lot_Date Code Marking Line 2
EPC2038ENGR	AD	YYY

DIE OUTLINE

Solder Bar View

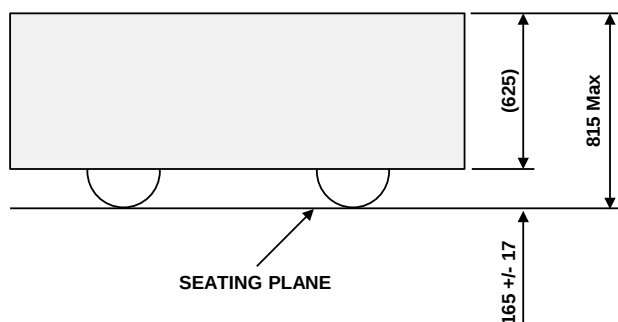
All measurements in micrometers (μm)



Pads 1 is Gate;
Pad 3 is Drain;
Pads 2, 4 are Source

DIM	MICROMETERS		
	MIN	Nominal	MAX
A	870	900	930
B	870	900	930
c	450	450	450
d	450	450	450
e	210	225	240
f	210	225	240
g	187	208	229

Side View

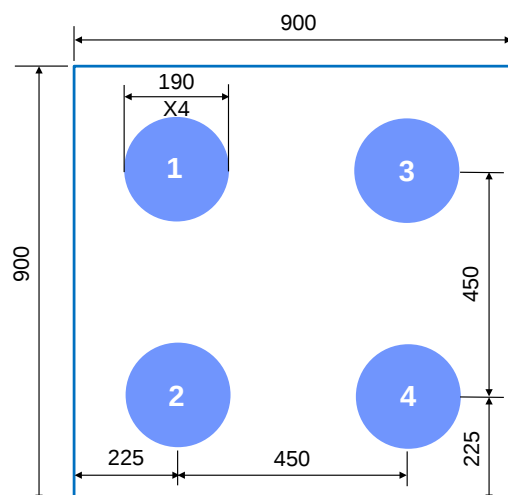


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RECOMMENDED LAND PATTERN

(Units in μm)

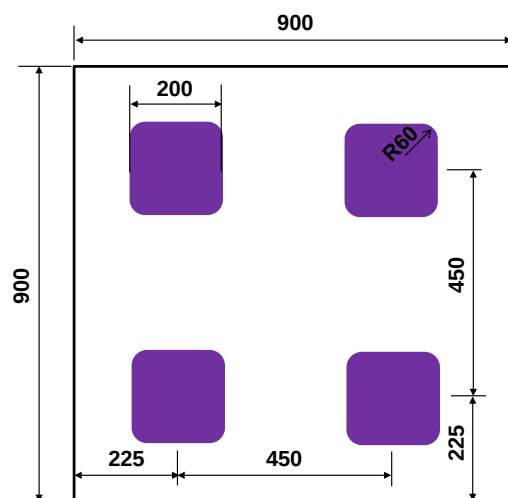


The land pattern is solder mask defined
Solder mask is 10 μm smaller per side than bump

Pads 1 is Gate;
Pad 3 is Drain;
Pads 2, 4 are Source

RECOMMENDED STENCIL

(Units in μm)



Recommended stencil should be 4mil (100µm) thick, must be laser cut, openings per drawing.

Intended for use with SAC305 Type 4 solder, reference
88.5% metals content

Additional assembly resources available at <http://epc-co.com/epc/DesignSupport/AssemblyBasics.aspx>

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U.S. Patents 8,350,294; 8,404,508; 8,431,960; 8,436,398; 8,785,974; 8,890,168; 8,969,918; 8,853,749; 8,823,012

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