

FEATURES

- Fixed gain of 29 dB**
- Operation from 2.3 GHz to 2.4 GHz**
- EVM $\leq 3\%$ at $P_{OUT} = 25$ dBm with 16 QAM OFDMA**
- Input internally matched to 50 Ω**
- Power supply: 3.2 V to 4.2 V**
- Quiescent current**
 - 130 mA in high power mode**
 - 70 mA in low power mode**
- Power-added efficiency (PAE): 20%**
- Multiple operating modes to reduce battery drain**
 - Low power mode: 100 mA**
 - Standby mode: 1 mA**
 - Sleep mode: <1 μ A**

APPLICATIONS

WiMAX/WiBro mobile terminals

GENERAL DESCRIPTION

The ADL5570 is a high linearity 2.3 GHz to 2.4 GHz power amplifier designed for WiMAX terminals using TDD operation at a duty cycle of 31%. With a gain of 29 dB and an output compression point of 31 dBm at 2.35 GHz, it can operate at an output power level up to 26 dBm while maintaining an EVM of $\leq 3\%$ (OFDM 16 or 64 QAM) with a supply voltage of 3.5 V. PAE is 20% @ $P_{OUT} = 25$ dBm.

The ADL5570 RF input is matched on-chip and provides an input return loss of less than -10 dB. The open-collector output is externally matched with strip-line and external shunt capacitance.

FUNCTIONAL BLOCK DIAGRAM

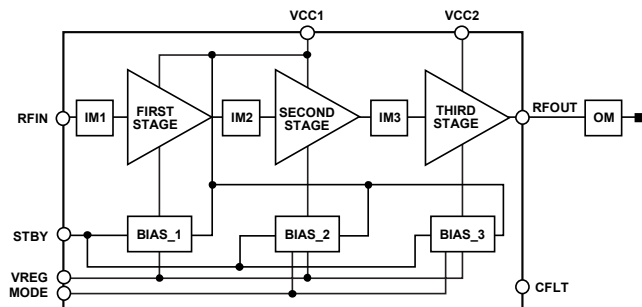


Figure 1.

The ADL5570 operates over a supply voltage range from 3.2 V to 4.2 V with a supply current of 440 mA burst rms when delivering 25 dBm (3.5 V supply). A low power mode is also available for operation at power levels of ≤ 10 dBm with optimized operating and quiescent currents of 100 mA and 70 mA, respectively. A standby mode is available that reduces the quiescent current to 1 mA, which is useful when a TDD terminal is receiving data.

The ADL5570 is fabricated in a GaAs HBT process and is packaged in a 4 mm $\times$ 4 mm, 16-lead, Pb-free RoHS-compliant LFCSP that uses an exposed paddle for excellent thermal impedance. It operates from -40°C to $+85^{\circ}\text{C}$.

Rev. 0

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ADL5570* Product Page Quick Links

Last Content Update: 11/01/2016

Comparable Parts

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Documentation

Application Notes

- AN-1389: Recommended Rework Procedure for the Lead Frame Chip Scale Package (LFCSP)
- AN-772: A Design and Manufacturing Guide for the Lead Frame Chip Scale Package (LFCSP)

Data Sheet

- ADL5570: 2.3 GHz to 2.4 GHz WiMAX Power Amplifier Data Sheet

Tools and Simulations

- ADIsimPLL™
- ADIsimRF

Design Resources

- ADL5570 Material Declaration
- PCN-PDN Information
- Quality And Reliability
- Symbols and Footprints

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REVISION HISTORY

5/07—Rev. 0: Initial Version

SPECIFICATIONS

$V_{CC} = 3.5\text{ V}$

$T_A = 25^\circ\text{C}$, 1024 FFT, 16 QAM OFDMA modulated carrier, 10 MHz channel BW, 16 QAM, $Z_L = 50\ \Omega$, MODE = 0 V, STBY = 0 V, VREG = 2.85 V, 31% duty cycle, unless otherwise noted.

Table 1.

Parameter	Conditions	Min	Typ	Max	Unit
FREQUENCY RANGE		2.3		2.4	GHz
LINEAR OUTPUT POWER	MODE = 0 V, 16 QAM, $\text{EVM} \leq 3\%$ MODE = 2.5 V, 16 QAM, $\text{EVM} \leq 3\%$		25 10		dBm dBm
GAIN			29		dB
vs. Frequency	$\pm 5\text{ MHz}$		± 0.1		dB
vs. Temperature	$-40^\circ\text{C} \leq T_A \leq +85^\circ\text{C}$		± 1.5		dB
vs. Supply	3.2 V to 4.2 V		± 0.5		dB
OP1dB	Unmodulated input		31		dBm
EVM	$P_{\text{OUT}} = 25\text{ dBm}$		3		% rms
INPUT RETURN LOSS			10		dB
WiBro SPECTRAL MASK @ $P_{\text{OUT}} = 25\text{ dBm}$ (CARRIER OFFSETS SCALED TO 10 MHz BW SIGNAL) ¹	$\pm 5.45\text{ MHz carrier offset}$		36		dBr
	$\pm 10.9\text{ MHz carrier offset}$		42		dBr
	$\pm 15.12\text{ MHz carrier offset}$		48		dBr
	$\pm 20.26\text{ MHz carrier offset}$		52		dBr
FCC SPECTRAL MASK @ $P_{\text{OUT}} = 25\text{ dBm}$	$\pm 5\text{ MHz carrier offset}$		36		dBr
	$\pm 6\text{ MHz carrier offset}$		38		dBr
	$\pm 10.5\text{ MHz carrier offset}$		42		dBr
	$\pm 20\text{ MHz carrier offset}$		52		dBr
HARMONIC DISTORTION			43		dBc
POWER SUPPLY INTERFACE	$V_{CC} = 3.5\text{ V}$				
SUPPLY CURRENT	$P_{\text{OUT}} = 25\text{ dBm}$, MODE = 0 V $P_{\text{OUT}} = 10\text{ dBm}$, MODE = 2.5 V		440 100		mA mA
PAE	$P_{\text{OUT}} = 25\text{ dBm}$, MODE = 0 V		20		%
STANDBY MODE	VREG = 2.85 V, STBY = 2.5 V		1		mA
SLEEP MODE	VREG = 0 V		10		μA
TURN ON/OFF TIME			1		μs
VSWR SURVIVABILITY			10:1		

¹ OFDMA carrier, 16 QAM, 10 MHz channel BW, 1024 FFT.

ABSOLUTE MAXIMUM RATINGS

Table 2.

Parameter	Rating
Supply Voltage	
V _{CC}	5.0 V
V _{REG}	3 V
STBY	3 V
MODE	3 V
RFOUT (Modulated—High Power Mode) ¹	29 dBm
Output Load VSWR	10:1
Operating Temperature Range	–40°C to +85°C
Storage Temperature Range	–65°C to +150°C
Maximum Solder Reflow Temperature	260°C (30 sec)

¹ OFDMA carrier, 16 QAM, 10 MHz channel BW, 1024 FFT.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ESD CAUTION



ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

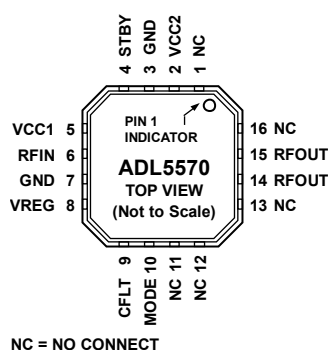


Figure 2. Pin Configuration

Table 3. Pin Function Descriptions

Pin No.	Mnemonic	Description
1, 11 to 13, 16	NC	No Connect. Do not connect these pins.
2	VCC2	This power supply pin should be connected to the supply via a choke circuit (see Figure 10).
3, 7	GND	Connected to Ground.
4	STBY	When STBY is low (0 V), the device operates in transmit mode. When the radio is receiving data, STBY can be taken high (2.5 V), reducing supply current to 1 mA.
5	VCC1	Connect to Power Supply.
6	RFIN	Matched RF Input.
8	VREG	When VREG is low, the device goes into sleep mode, reducing supply current to 10 μ A. When VREG is high (2.85 V), the device operates in its normal transmit mode. When high, VREG draws a bias current of approximately 10 mA.
9	CFLT	A ground-referenced capacitor should be connected to this pin to reduce bias line noise (see Figure 10).
10	MODE	Switches Between High Power and Low Power Modes. When MODE is low (0 V), the device operates in high power mode. When MODE is high (2.5 V), the device operates in low power mode. See Table 4 for appropriate biasing. In cases where the MODE feature is not used, this pin should be connected to ground through a 50 k Ω resistor.
14, 15	RFOUT	Unmatched RF Output. These parallel outputs can be matched to 50 Ω using strip-line and shunt capacitance. The power supply voltage should be connected to these pins through a choke inductor.
	Exposed Paddle	The exposed paddle should be soldered down to a low impedance ground plane (if multiple ground layers are present, use multiple vias (9 minimum) to stitch together the ground planes) for optimum electrical and thermal performance.

Table 4. $V_{CC} = 3.5$ V Operating Modes¹

Mnemonic	High Power Mode, $P_{OUT} > 10$ dBm	Low Power Mode, $P_{OUT} \leq 10$ dBm	Standby Mode	Sleep Mode
VREG	High	High	High	Low
MODE	Low	High	X	X
STBY	Low	Low	High	X

¹ X = don't care.

Table 5. VREG, MODE, and STBY Pins

Mnemonic	Nominal High (V)	High Range (V)	Nominal Low (V)	Low Range (V)
VREG	2.85	2.75 to 2.95	0	NA
MODE	2.5	>2.4	0	<1
STBY	2.5	>2.4	0	<1

TYPICAL PERFORMANCE CHARACTERISTICS

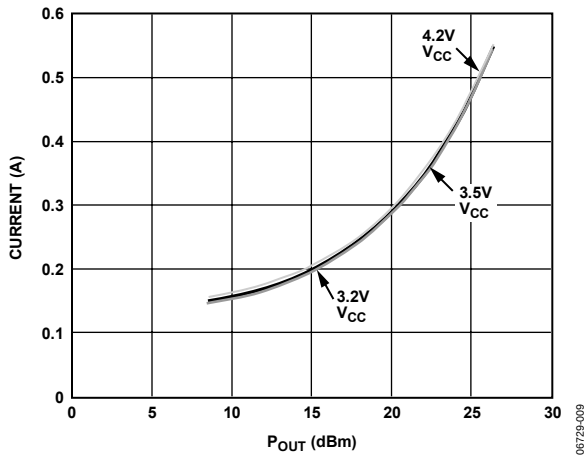


Figure 3. Current vs. P_{OUT} , 16 QAM at 2.35 GHz and 31% Duty Cycle

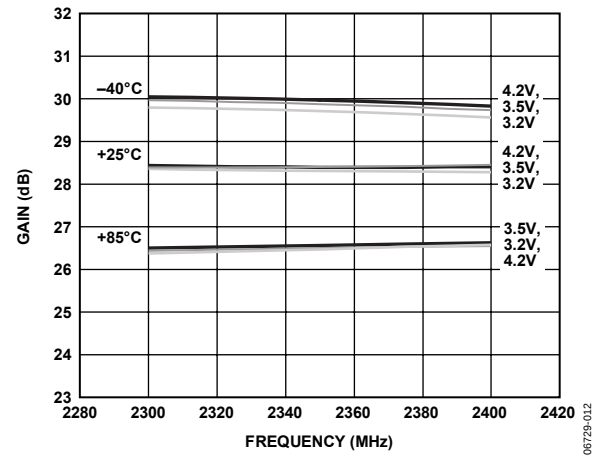


Figure 6. Gain vs. Frequency, 16 QAM at $P_{IN} = -2$ dBm

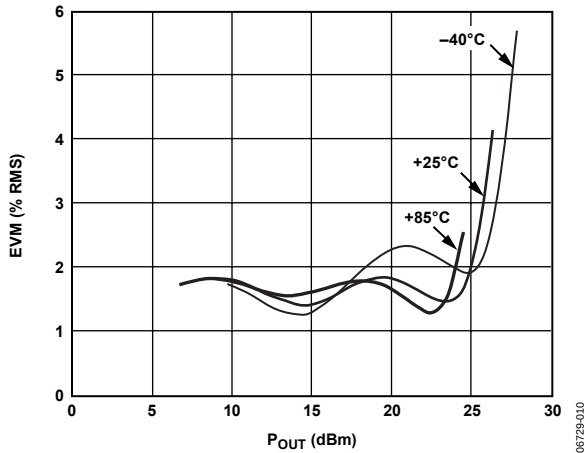


Figure 4. EVM vs. P_{OUT} , 16 QAM 3/4 @ $f = 2.35$ GHz at $V_{CC} = 3.5$ V

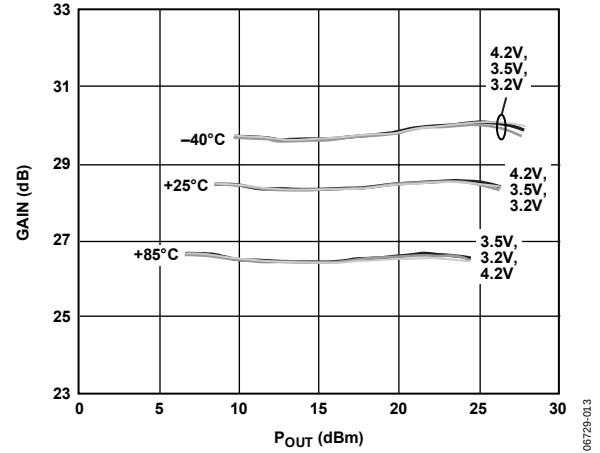


Figure 7. Gain vs. P_{OUT} at 2.35 GHz

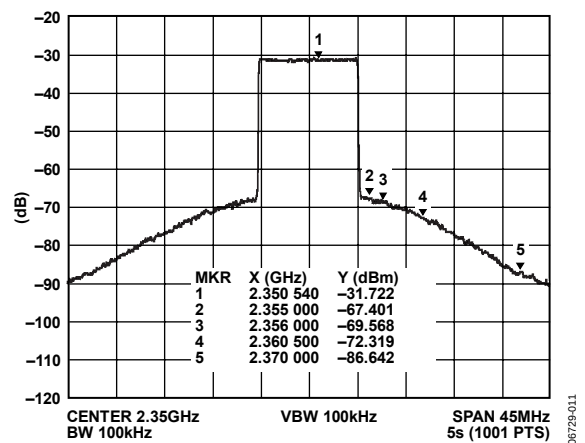


Figure 5. WiMAX Spectrum with FCC Spectral Mask at 2.35 GHz, $V_{CC} = 3.5$ V, $P_{OUT} = 25$ dBm

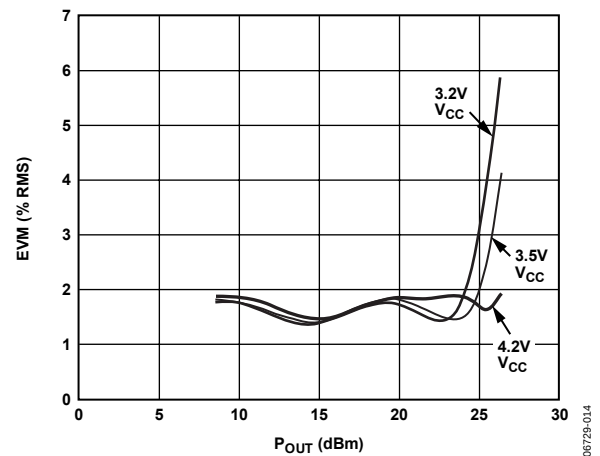


Figure 8. EVM vs. P_{OUT} at $f = 2.35$ GHz

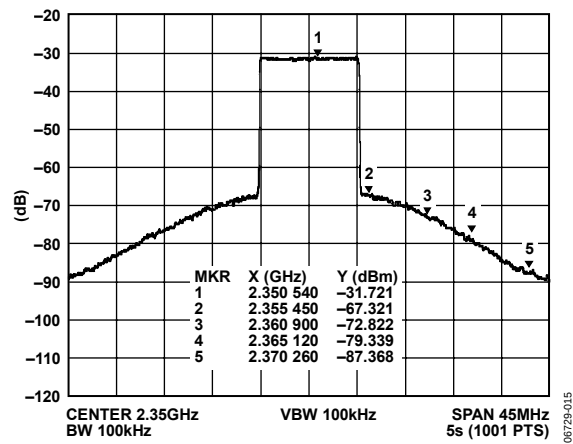


Figure 9. WiMAX Spectrum with WiBro Spectral Mask at 2.35 GHz, $V_{CC} = 3.5\text{ V}$, $P_{OUT} = 25\text{ dBm}$

APPLICATIONS

BASIC CONNECTIONS

Figure 10 shows the basic connections for the ADL5570.

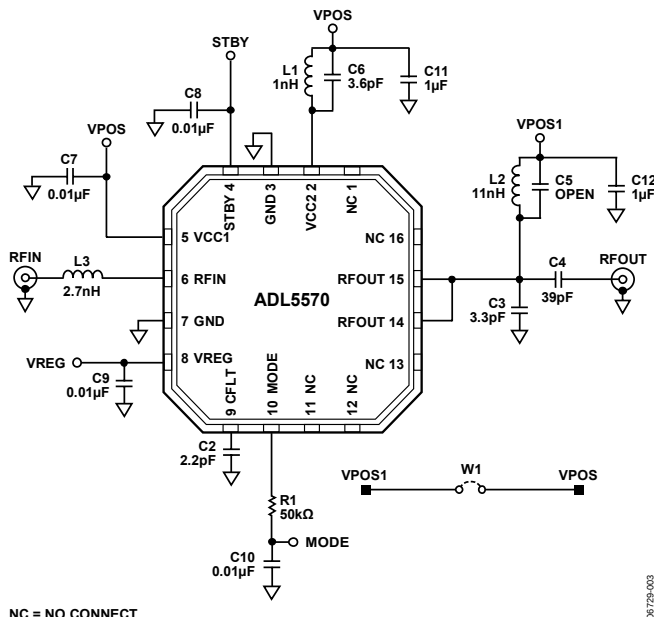


Figure 10. ADL5570 Basic Connections

Power Supply

The voltage supply on the ADL5570, which ranges from 3.2 V to 4.2 V, should be connected to the VCCx pins. VCC1 is decoupled with Capacitor C7, whereas VCC2 uses a tank circuit to prevent RF signals from propagating on the dc lines.

RF Input Interface

The RFIN pin is the port for the RF input signal to the power amplifier. The L3 inductor, 2.7 nH, matches the input impedance to 50 Ω.



Figure 11. RF Input with Matching Component

RF Output Interface

The parallel RF output ports have a shunt capacitance, C3 (3.3 pF), and the line inductance of the microstrip-line for optimized output power and linearity. The characteristics of the ADL5570 are described for 50 Ω impedance after the output matching capacitor (load after C3).

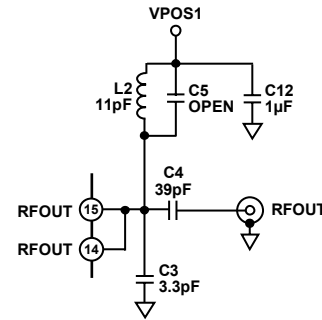


Figure 12. RF Output

C4 provides dc blocking on the RF output.

Transmit/Standby Enable

During normal transmit mode, the STBY pin is biased low (0 V). However, during receive mode, the pin can be biased high (2.5 V) to shift the device into standby mode, which reduces current consumption to less than 1 mA.

VREG Enable

During normal transmit, the VREG pin is biased to 2.85 V and draws 10 mA of current. When the VREG pin is low (0 V), the device suspends itself into sleep mode (irrespective of supply and MODE biasing). In this mode, the device draws 10 μA of current.

MODE High Power/Low Power Enable

The MODE pin is used to choose between high power mode and low power mode. When MODE is biased low (0 V), the device operates in high power mode. When MODE is biased high (2.5 V), the device operates in low power mode. Appropriate biasing must be followed for 3.5 V and 4.2 V operation. See Table 4 and Table 5 for configuration of the MODE pin.

64 QAM OFDMA PERFORMANCE

The ADL5570 shows exceptional performance when used with a higher order modulation scheme, such as a 64 QAM system. Figure 13, Figure 14, and Figure 15 illuminate the EVM, gain, and current consumption performance within the context of a 64 QAM OFDMA system.

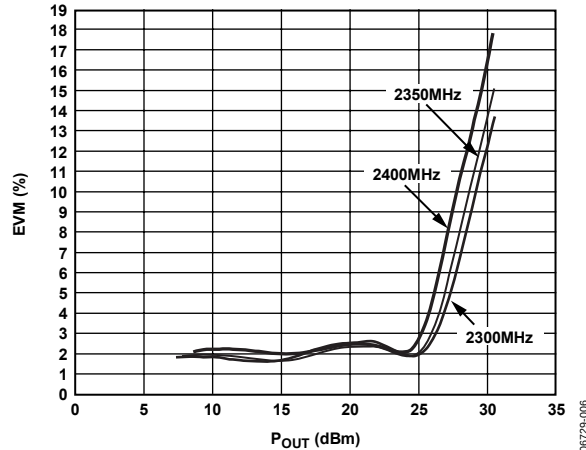


Figure 13. EVM vs. P_{OUT} Performance at $V_{CC} = 3.5$ V and 64 QAM OFDMA Signal

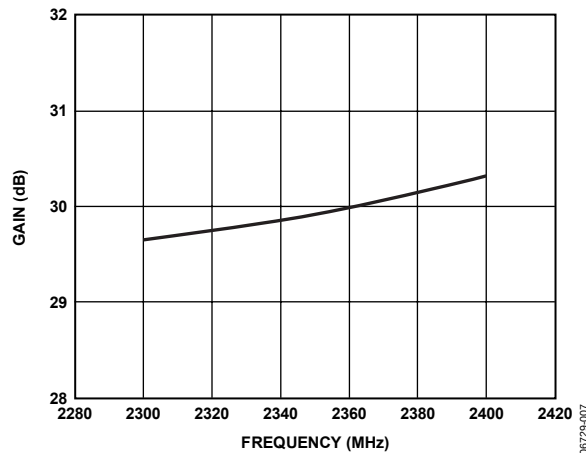


Figure 14. Gain vs. Frequency Performance at $V_{CC} = 3.5$ V and 64 QAM OFDMA Signal

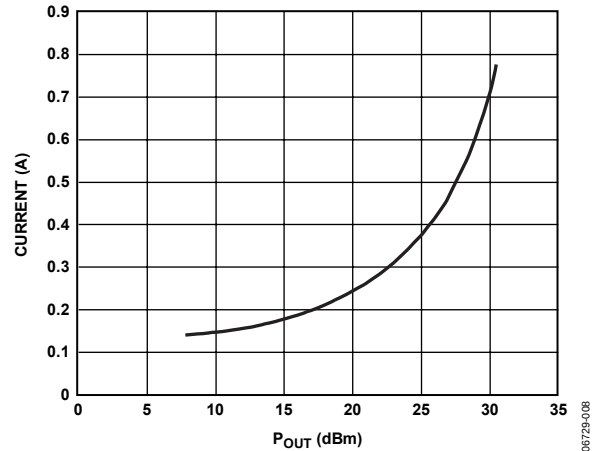


Figure 15. Burst Current vs. P_{OUT} at $V_{CC} = 3.5$ V, 64 QAM, 2350 MHz, 31% 802.16e OFDMA Signal

POWER-ADDED EFFICIENCY

The efficiency of the ADL5570 is defined on the current that it draws during the data burst of an 802.16e OFDMA signal. In typical test setup, the average rms current, I_{AVG} , is measured. However,

$$I_{AVG} = \text{Duty Cycle (in decimal)} \times I_{BURST} + (1 - \text{Duty Cycle [in decimal]}) \times I_{DEFAULT}$$

where:

I_{BURST} is the rms current during the data burst of an OFDMA signal.

$I_{DEFAULT}$ can be the quiescent current drawn when there is no data burst and the device remains biased, the sleep current (1 mA) if the device is defaulted to sleep mode, or the standby current.

For example, in a 31% duty cycle 802.16e OFDMA signal, the burst current is calculated by rearranging the previous equation to get

$$I_{BURST} = \frac{(I_{AVG} - 0.69 \times I_{DEFAULT})}{0.31}$$

Finally, the PAE is calculated by

$$PAE (\%) = \frac{RF \text{ Output Power (mW)} - RF \text{ Input Power (mW)}}{V_{CC} (V) \times I_{BURST} (mA)} \times 100$$

When RF = 2.35 GHz, 31% 16 QAM OFDMA signal, $V_{CC} = 3.5$ V, RF output power = 25 dBm, and RF input power = -4 dBm, the ADL5570 consumes a burst current, $I_{BURST} = 450$ mA and PAE = 21%.

EVALUATION BOARD

The evaluation board layout is shown in Figure 16. The ADL5570 performance data was taken on a FR4 board. During board layout, 50 Ω RF trace impedance must be ensured. The output matching capacitor, C3, is placed 30 mils from the package edge.

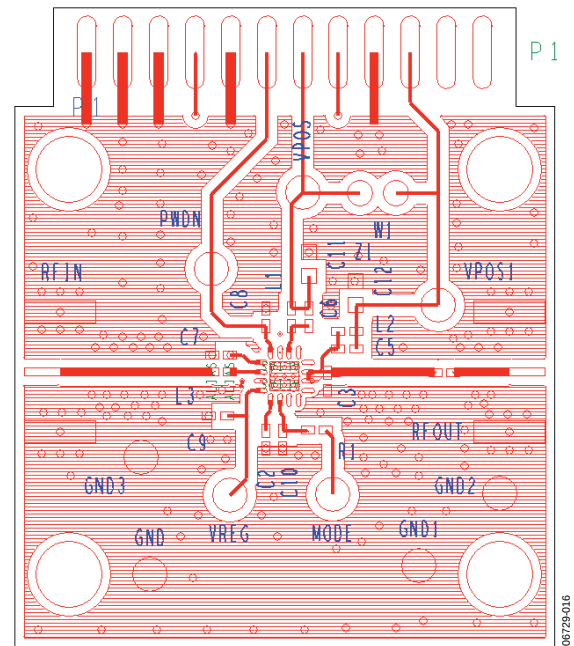


Figure 16. Evaluation Board Layout

Table 6. Evaluation Board Configuration Options

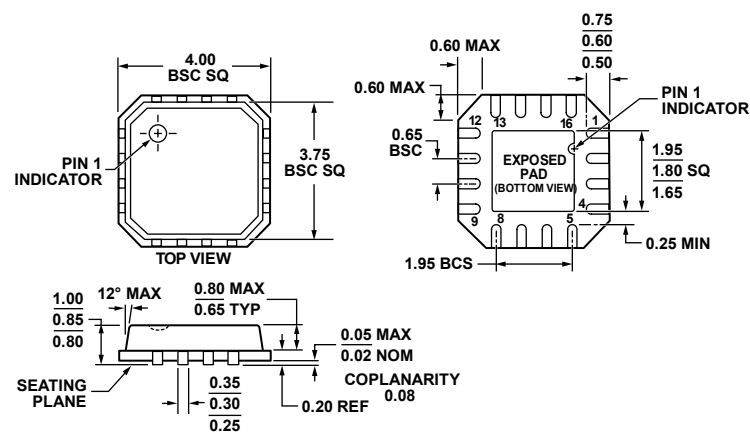
Component	Function	Default Value
VPOS, VPOS1, GND	Supply and Ground Connections.	W1 = Installed
TP1 (STBY)	Transmit/Standby Mode: When STBY is low (0 V), the device operates in transmit mode. When the radio is receiving data, STBY can be taken high (2.5 V), reducing the supply current to 10 mA.	Not applicable
TP2 (VREG)	Normal/Sleep Mode: When VREG is low, the device goes into sleep mode, reducing the supply current to 10 μ A. When VREG is high (2.85 V), the device operates in its normal transmit mode. When high, VREG draws a bias current of approximately 10 mA.	Not applicable
TP5 (MODE), R1	High/Low Power Mode: Switches between high power mode and low power mode. When MODE is low (0 V), the device operates in high power mode. When MODE is high (2.5 V), the device operates in low power mode.	R1 = 50 k Ω (Size 0402)
L3	Input Interface: L3 matches the input to 50 Ω .	L3 = 2.7 nH (Size 0402)
C3, C4	Output Interface: C4 provides dc blocking, and C3 matches the output to 50 Ω .	C4 = 39 pF (Size 0402) C3 = 3.3 pF (Size 0402) (Tight tolerance recommended)
C2	Filter Interface: A ground-referenced capacitor should be connected to this node to reduce bias line noise.	C2 = 2.2 pF (Size 0402)
C7 to C12	Power Supply Decoupling: The capacitors, C7 through C12, are used for power supply decoupling. They should be placed as close as possible to the DUT.	C7 to C10 = 0.01 μ F (Size 0402) C11, C12 = 1 μ F (Size 0402)
L1, L2, C6, C5	RF Trap: L1, C6 and L2, C5 form tank circuits and prevent RF from propagating on the dc supply lines.	L1 = 1 nH (Size 0402) C6 = 3.6 pF (Size 0402) L2 = 11 nH (Size 0402) C5 = Open

**MEASUREMENT SETUP USING THE ADL5570
EVALUATION BOARD**

When using the ADL5570 evaluation board, the following setup must be used:

1. Connect the output of the WiMAX signal generator to the RF input through a cable.
2. Connect the RF output SMA of the ADL5570 to the Spectrum Analyzer (preferably through an attenuator).
3. Connect the power supply to VPOS. Set voltage to the desired supply level. Be sure to keep the current limit on this source to 1 A.
4. Ensure that Jumper W1 is in place. Alternatively, use a jumper cable to connect VPOS to VPOS1.
5. Follow Table 4 for measurement in desired mode.
6. Turn the RF source on.
7. Turn all voltage supplies on.

OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MO-220-VGGC.

Figure 17. 16-Lead Lead Frame Chip Scale Package [LFCSP_VQ]
4 mm × 4 mm Body, Very Thin Quad
(CP-16-16)
Dimensions shown in millimeters

061607-D

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option	Ordering Quantity
ADL5570ACPZ-R7 ¹	−40°C to +85°C	16-Lead LFCSP_VQ	CP-16-16	1,500
ADL5570-EVALZ ¹		Evaluation Board		

¹ Z = RoHS Compliant Part.