3.3 V, Upstream, Cable Line Driver

Data Sheet

AD8324

FEATURES

- Supports DOCSIS 2.0 and EuroDOCSIS specifications for reverse path transmission systems
- Gain programmable in 1 dB steps over a 59 dB range
- Low distortion at 61 dBmV output
  - –59 dBc SFDR at 21 MHz
  - –54 dBc SFDR at 65 MHz
- Output noise level at minimum gain 1.3 nV/√Hz
- Maintains 75 Ω output impedance in transmit-enable and transmit-disable condition
- Upper bandwidth of 100 MHz (full gain range)
- 3.3 V supply operation
- Supports SPI® interfaces

APPLICATIONS

- DOCSIS 2.0 and EuroDOCSIS cable modems
- CATV set-top boxes
- CATV telephony modems
- Coaxial and twisted pair line drivers

FUNCTIONAL BLOCK DIAGRAM

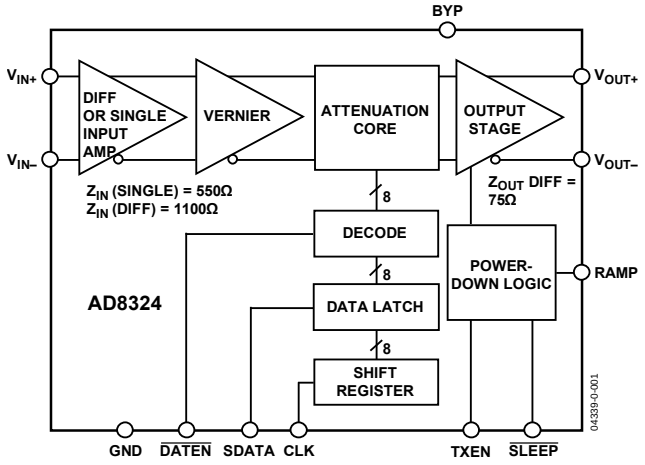

Figure 1.

GENERAL DESCRIPTION

The AD8324 is a low cost amplifier designed for coaxial line driving. The features and specifications make the AD8324 ideally suited for DOCSIS® 2.0 and EuroDOCSIS applications. The gain of the AD8324 is digitally controlled. An 8-bit serial word determines the desired output gain over a 59 dB range, resulting in gain changes of 1 dB/LSB.

The AD8324 accepts a differential or single-ended input signal. The output is specified for driving a 75 Ω load through a 1:1 transformer.

Distortion performance of –54 dBc is achieved with an output level up to 61 dBmV at 65 MHz bandwidth.

This device has a sleep mode function that reduces the quiescent current to 30 µA and a full power-down function that reduces power-down current to 2.5 mA.

The AD8324 is packaged in a low cost, 20-lead LFCSP and a 20-lead QSOP. The AD8324 operates from a single 3.3 V supply.

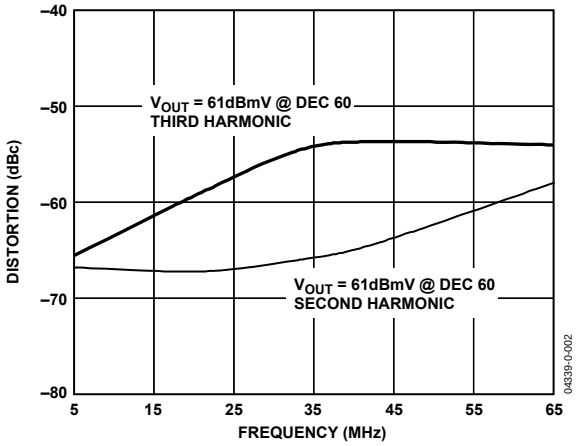

Figure 2. Worst Harmonic Distortion vs. Frequency

Rev. C

Document Feedback

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Comparable Parts

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Documentation

Application Notes

- AN-851: A WiMax Double Downconversion IF Sampling Receiver Design

Data Sheet

- AD8324: 3.3 V Upstream Cable Line Driver Data Sheet

Reference Materials

Product Selection Guide

- Variable Gain Amplifier Selection Table

Design Resources

- AD8324 Material Declaration
- PCN-PDN Information
- Quality And Reliability
- Symbols and Footprints

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10/03—Revision 0: Initial Version

SPECIFICATIONS

T_A = 25°C, V_{CC} = 3.3 V, R_L = R_{IN} = 75 Ω, V_{IN} (differential) = 27.5 dBmV, unless otherwise noted. The AD8324 is characterized using a 1:1 transformer[1] at the device output.

Table 1.

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
INPUT CHARACTERISTICS					
Specified AC Voltage	Output = 61 dBmV, maximum gain		27.5		dBmV
Input Resistance	Single-ended input		550		Ω
	Differential input		1100		Ω
Input Capacitance			2		pF
GAIN CONTROL INTERFACE					
Voltage Gain Range		58	59	60	dB
Maximum Gain	Gain code = 60 decimal code	32.5	33.5	34.5	dB
Minimum Gain	Gain code = 1 decimal code	−26.5	−25.5	−24.5	dB
Output Step Size[2]		0.6	1.0	1.4	dB/LSB
Output Step Size Temperature Coefficient	T_A = −40°C to +85°C		±0.004		dB/°C
OUTPUT CHARACTERISTICS					
Bandwidth (−3 dB)	All gain codes (1 decimal code to 60 decimal codes)		100		MHz
Bandwidth Roll-Off	f = 65 MHz		1.7		dB
1 dB Compression Point[3]	Maximum gain, f = 10 MHz, output referred	19.6	21		dBm
	Minimum gain, f = 10 MHz, input referred	2.1	3.7		dBm
Output Noise[2]					
Maximum Gain	f = 10 MHz		157	166	nV/√Hz
Minimum Gain	f = 10 MHz		1.3	1.5	nV/√Hz
Transmit Disable	f = 10 MHz		1.1	1.2	nV/√Hz
Noise Figure[2]					
Maximum Gain	f = 10 MHz		15.5	16.0	dB
Differential Output Impedance	Transmit enable and transmit disable		75 ± 30%[4]		Ω
OVERALL PERFORMANCE					
Second-Order Harmonic Distortion[5, 3]					
	f = 33 MHz, V_{OUT} = 61 dBmV at maximum gain		−66	−60	dBc
	f = 65 MHz, V_{OUT} = 61 dBmV at maximum gain		−58	−53	dBc
Third-Order Harmonic Distortion (SFDR)[5, 3]	f = 21 MHz, V_{OUT} = 61 dBmV at maximum gain		−59	−57.5	dBc
	f = 65 MHz, V_{OUT} = 61 dBmV at maximum gain		−54	−52.5	dBc
Adjacent Power Channel Ratio (APCR)[2, 6]			−61	−58	dBc
Isolation (Transmit Disable)[2]	Maximum gain, f = 65 MHz		−75	−70	dB
POWER CONTROL					
Transmit Enable Settling Time	Maximum gain, V_{IN} = 0		2.5		µs
Transmit Disable Settling Time	Maximum gain, V_{IN} = 0		3.8		µs
Output Switching Transients[3]	Equivalent output = 31 dBmV		2.5	6	mV p-p
	Equivalent output = 61 dBmV		27	71	mV p-p
Output Settling					
Due to Gain Change	Minimum gain to maximum gain		60		ns
Due to Input Step Change	Maximum gain, V_{IN} = 27.5 dBmV		30		ns

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
POWER SUPPLY					
Operating Range		3.13	3.3	3.47	V
Quiescent Current	Maximum gain	195	207	235	mA
	Minimum gain	25	39	50	mA
	Transmit disable (TXEN = 0)	1	2.5	4	mA
	$\overline{\text{SLEEP}}$ mode (power down)		30	500	µA
OPERATING TEMPERATURE RANGE	20-lead LFCSP	−40		+85	°C
	20-lead QSOP	−25		+70	°C

[1] TOKO 458PT-1556 used for above specifications. Typical insertion loss of 0.5 dB at 10 MHz.
[2] Guaranteed by design and characterization to ±6 sigma for T_A = 25°C.
[3] Guaranteed by design and characterization to ±3 sigma for T_A = 25°C.
[4] Measured through a 1:1 transformer.
[5] Specification is worst case over all gain codes.
[6] V_{IN} = 27.5 dBmV, QPSK modulation, 160 kSPS symbol rate.

LOGIC INPUTS (TTL-/CMOS-COMPATIBLE LOGIC)

$\overline{\text{DATEN}}$, CLK, SDATA, TXEN, $\overline{\text{SLEEP}}$, V_{CC} = 3.3 V, unless otherwise noted.

Table 2.

Parameter	Min	Typ	Max	Unit
Logic 1 Voltage	2.1		3.3	V
Logic 0 Voltage	0		0.8	V
Logic 1 Current (V_{INH} = 3.3 V), CLK, SDATA, $\overline{\text{DATEN}}$	0		20	nA
Logic 0 Current (V_{INL} = 0 V), CLK, SDATA, $\overline{\text{DATEN}}$	−600		−100	nA
Logic 1 Current (V_{INH} = 3.3 V), TXEN	50		190	µA
Logic 0 Current (V_{INL} = 0 V), TXEN	−250		−30	µA
Logic 1 Current (V_{INH} = 3.3 V), $\overline{\text{SLEEP}}$	50		190	µA
Logic 0 Current (V_{INL} = 0 V), $\overline{\text{SLEEP}}$	−250		−30	µA

TIMING REQUIREMENTS

V_{CC} = 3.3 V, $t_R = t_F$ = 4 ns, f_{CLK} = 8 MHz, unless otherwise noted.

Table 3.

Parameter	Min	Typ	Max	Unit
Clock Pulse Width (t_{WH})	16.0			ns
Clock Period (t_C)	32.0			ns
Setup Time SDATA vs. Clock (t_{DS})	5.0			ns
Setup Time $\overline{\text{DATEN}}$ vs. Clock (t_{ES})	15.0			ns
Hold Time SDATA vs. Clock (t_{DH})	5.0			ns
Hold Time $\overline{\text{DATEN}}$ vs. Clock (t_{EH})	3.0			ns
Input Rise and Fall Times, SDATA, $\overline{\text{DATEN}}$, Clock (t_R, t_F)			10	ns

Timing Diagrams

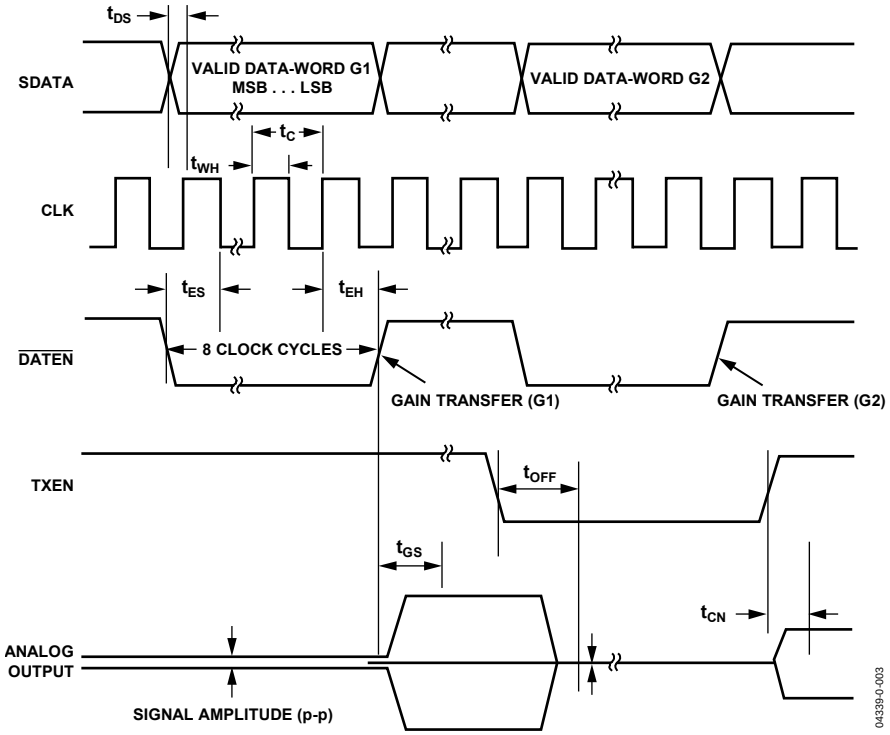


Figure 3. Serial Interface Timing

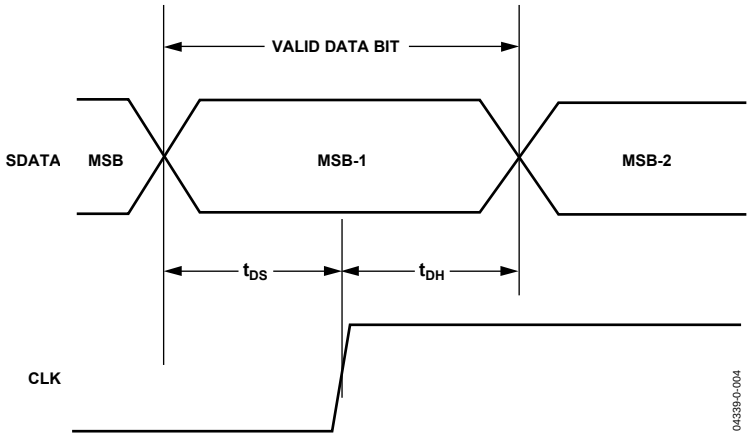


Figure 4. SDATA Timing

ABSOLUTE MAXIMUM RATINGS

Table 4.

Parameter	Rating
Supply Voltage, V_{CC}	3.63 V
Input Voltage	
VIN+, VIN–	1.5 V p-p
$\overline{\text{DATEN}}$, SDATA, CLK, $\overline{\text{SLEEP}}$, TXEN	–0.5 V to +3.63 V
Internal Power Dissipation	776 mW
Operating Temperature Range	
20-Lead LFCSP	–40°C to +85°C
20-Lead QSOP	–25°C to +70°C
Storage Temperature Range	–65°C to +150°C
Lead Temperature (Soldering, 60 sec)	300°C

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

THERMAL RESISTANCE

Table 5.

Model	θ_{JA}	Unit
20-Lead QSOP	83.2[1]	°C/W
20-Lead LFCSP	30.4[2]	°C/W

[1] Thermal resistance measured on SEMI standard 4-layer board.
[2] Thermal resistance measured on SEMI standard 4-layer board, paddle soldered to board.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

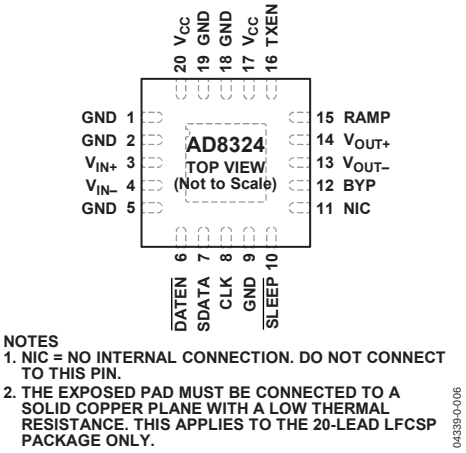


Figure 5. 20-Lead LFCSP Pin Configuration

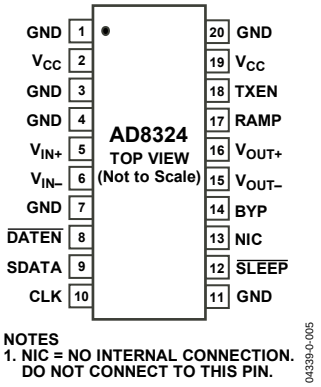


Figure 6. 20-Lead QSOP Pin Configuration

Table 6. Pin Function Descriptions

Pin No.			
20-Lead LFCSP	**20-Lead QSOP**	**Mnemonic**	**Description**
1, 2, 5, 9, 18, 19	1, 3, 4, 7, 11, 20	GND	Common External Ground Reference.
3	5	V_{IN+}	Noninverting Input. DC-biased to approximately $V_{CC}/2$. Must be ac-coupled with a 0.1 µF capacitor.
4	6	V_{IN-}	Inverting Input. DC-biased to approximately $V_{CC}/2$. Must be ac-coupled with a 0.1 µF capacitor.
6	8	$\overline{\text{DATEN}}$	Data Enable Low Input. This port controls the 8-bit parallel data latch and shift register. A Logic 0 to Logic 1 transition transfers the latched data to the attenuator core (updates the gain) and simultaneously inhibits serial data transfer into the register. A Logic 1 to Logic 0 transition inhibits the data latch (holds the previous and simultaneously enables the register for serial data load).
7	9	SDATA	Serial Data Input. This digital input allows an 8-bit serial (gain) word to be loaded into the internal register with the most significant bit (MSB) first.
8	10	CLK	Clock Input. The clock port controls the serial attenuator data transfer rate to the 8-bit master-slave shift register. Logic 0 to Logic 1 transition latches the data bit, and a Logic 1 to Logic 0 transfers the data bit to the slave. This requires the input serial data-word to be valid at or before this clock transition.
10	12	$\overline{\text{SLEEP}}$	Low Power Sleep Mode. In sleep mode, the supply current of the AD8324 is reduced to 30 µA. A Logic 0 powers down the device (high Z_{OUT} state), and a Logic 1 powers up the device.
11	13	NIC	No Internal Connection. Do not connect to this pin.
12	14	BYP	Internal Bypass. This pin must be externally decoupled (0.1 µF capacitor).
13	15	V_{OUT-}	Negative Output Signal. Must be biased to V_{CC}. See Figure 23.
14	16	V_{OUT+}	Positive Output Signal. Must be biased to V_{CC}. See Figure 23.
15	17	RAMP	External RAMP Capacitor (Optional).
16	18	TXEN	Transmit Enable. Logic 0 disables forward transmission, and Logic 1 enables forward transmission.
17, 20	2, 19	V_{CC}	Common Positive External Supply Voltage.
0	Not applicable	EPAD	Exposed Pad. The exposed pad must be connected to a solid copper plane with low thermal resistance. This applies to the 20-lead LFCSP package only.

TYPICAL PERFORMANCE CHARACTERISTICS

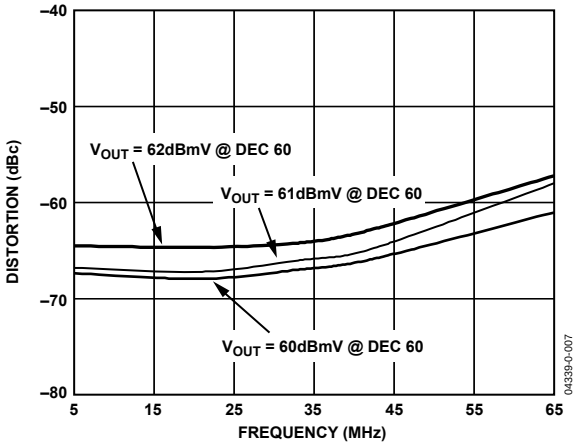


Figure 7. Second-Order Harmonic Distortion vs. Frequency for Various Output Powers

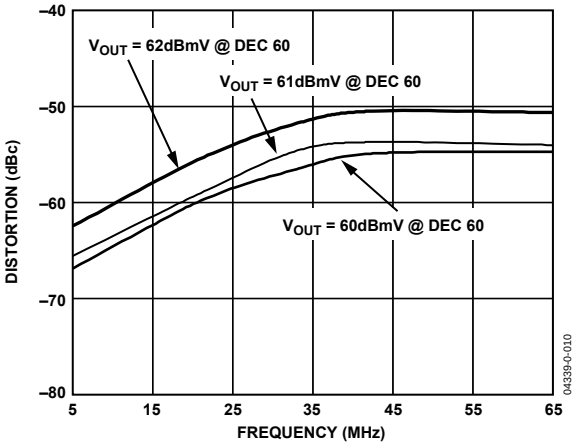


Figure 10. Third-Order Harmonic Distortion vs. Frequency for Various Output Powers

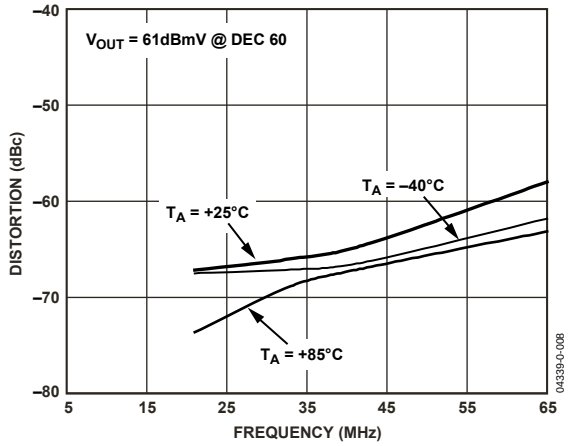


Figure 8. LFCSP Second-Order Harmonic Distortion vs. Frequency for Various Temperatures

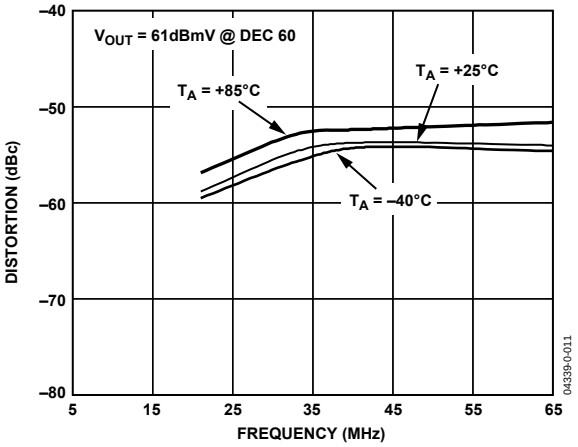


Figure 11. LFCSP Third-Order Harmonic Distortion vs. Frequency for Various Temperatures

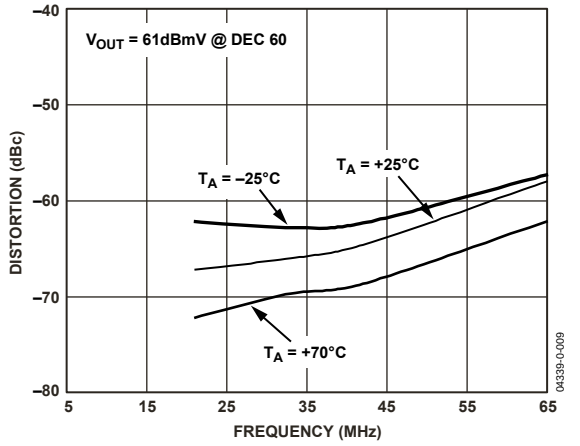


Figure 9. QSOP Second-Order Harmonic Distortion vs. Frequency for Various Temperatures

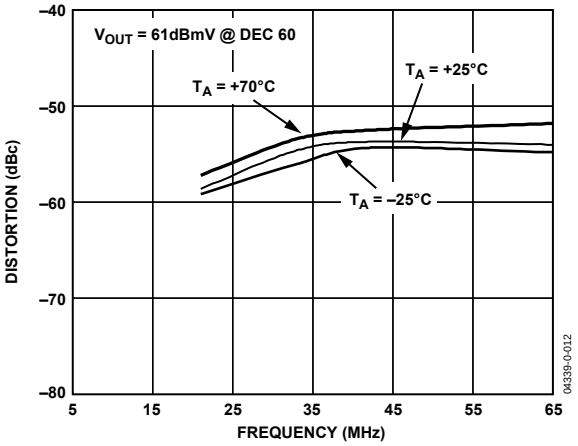


Figure 12. QSOP Third-Order Harmonic Distortion vs. Frequency for Various Temperatures

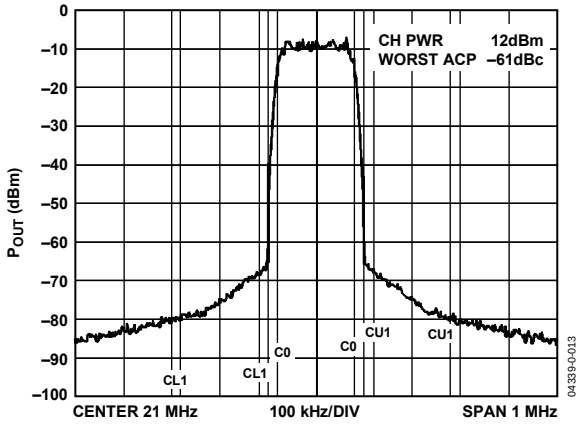


Figure 13. Adjacent Channel Power

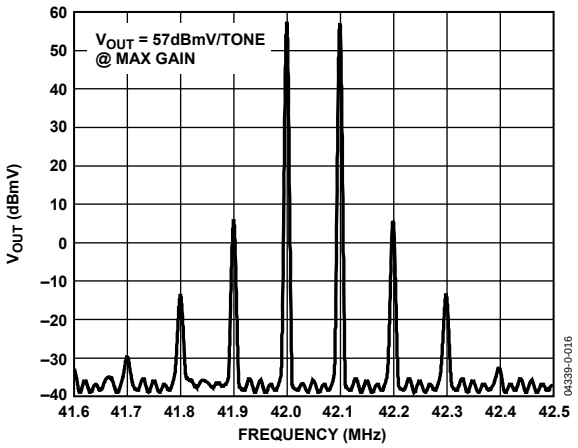


Figure 16. Two-Tone Intermodulation Distortion

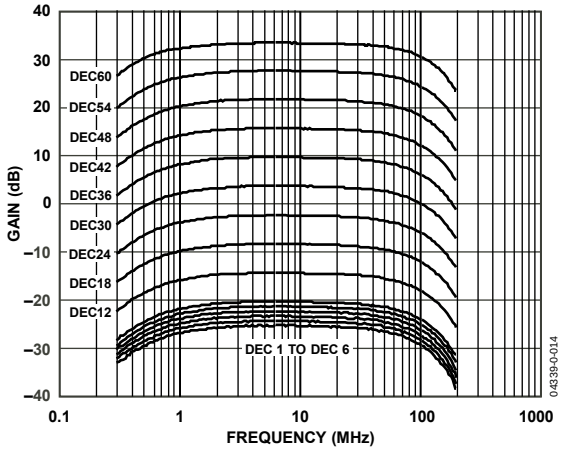


Figure 14. AC Response

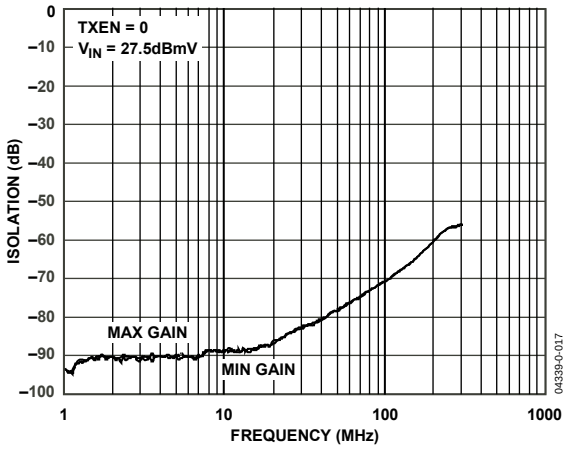


Figure 17. Isolation in Transmit Disable Mode vs. Frequency

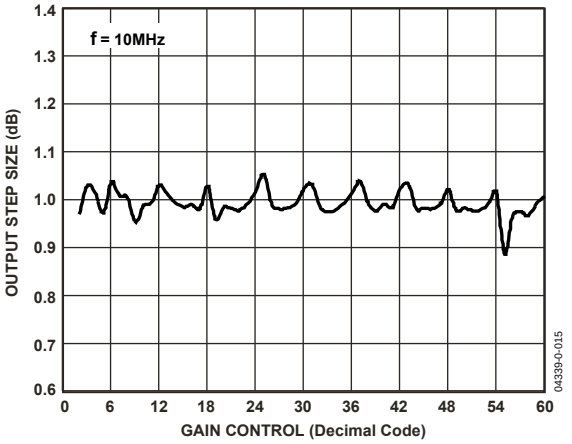


Figure 15. Output Step Size vs. Gain Control

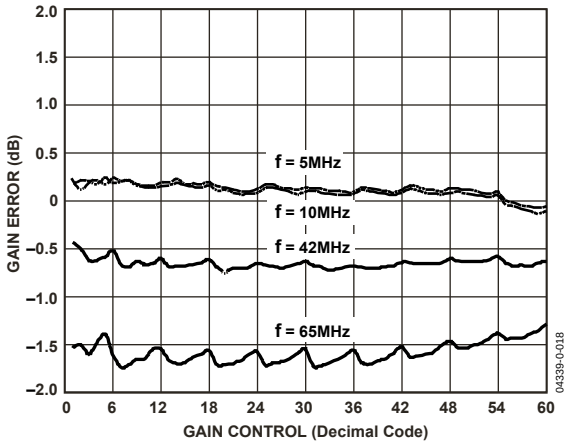


Figure 18. Gain Error vs. Gain Control for Various Frequencies

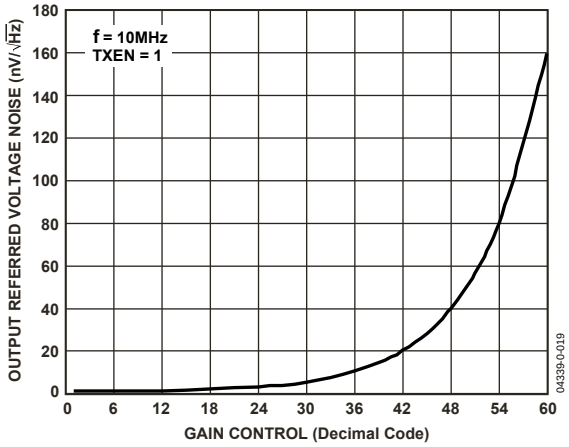


Figure 19. Output Referred Voltage Noise vs. Gain Control

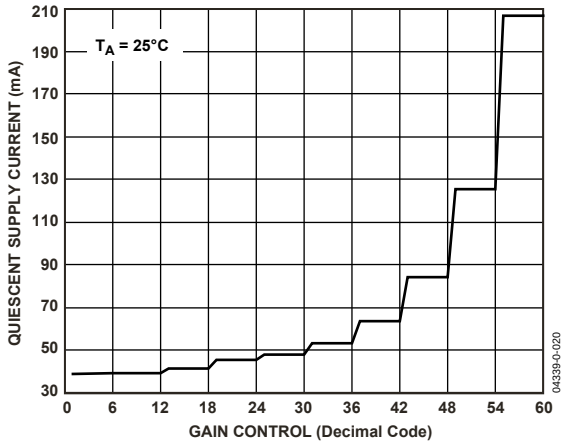


Figure 20. Quiescent Supply Current vs. Gain Control

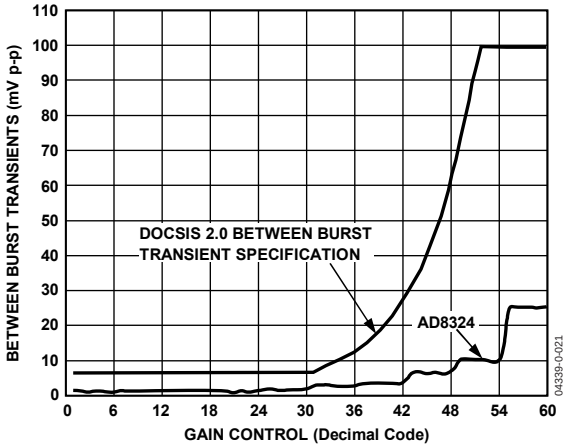


Figure 21. Between Burst Transient vs. Gain Control

TEST CIRCUIT

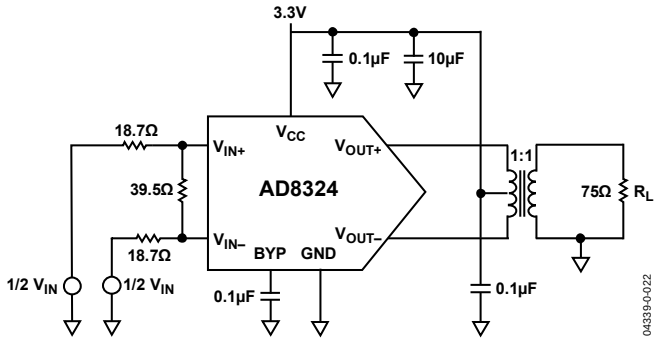


Figure 22. Typical Characterization Circuit

APPLICATIONS INFORMATION

GENERAL APPLICATIONS

The AD8324 is primarily intended for use as the upstream power amplifier (PA) in Data-Over-Cable Service Interface Specification (DOCSIS) certified cable modems and CATV set-top boxes. The upstream signal is either a quadrature phase shift keying (QPSK) or a quadrature amplitude modulation (QAM) signal generated by a digital signal processor (DSP), a dedicated QPSK/QAM modulator, or a digital-to-analog converter (DAC). In all cases, the signal must be low-pass filtered before it is applied to the PA in order to filter out-of-band noise and higher order harmonics from the amplified signal.

Due to the varying distances between the cable modem and the headend, the upstream PA must be capable of varying the output power by applying gain or attenuation. The ability to vary the output power of the AD8324 ensures that the signal from the cable modem has the proper level when it arrives at the headend. The upstream signal path commonly includes a diplexer and cable splitters. The AD8324 is designed to overcome losses associated with these passive components in the upstream cable path.

CIRCUIT DESCRIPTION

The AD8324 is composed of three analog functions in the transmit enable mode. The input amplifier (preamp) can be used in a single-ended or differential configuration. If the input is used in the differential configuration, ensure that the input signals are 180° out of phase and of equal amplitude. A vernier is used in the input stage for controlling the fine 1 dB gain steps. This stage then drives a DAC that provides the bulk of the attenuation for the AD8324. The signals in the preamp and DAC blocks are differential to improve the power supply rejection ratio (PSRR) and linearity. A differential current is fed from the DAC into the output stage. The output stage maintains 75 Ω differential output impedance in all power modes.

GAIN PROGRAMMING FOR THE AD8324

The AD8324 features a serial peripheral interface (SPI) for programming the gain code settings. The SPI interface consists of three digital data lines: CLK, $\overline{\text{DATEN}}$, and SDATA. The $\overline{\text{DATEN}}$ pin must be held low while the AD8324 is being programmed. The SDATA pin accepts the serial data stream for programming the AD8324 gain code. The CLK pin accepts the clock signal to latch in the data from the SDATA line.

The AD8324 uses a 6-bit shift register for clocking in the data. The shift register is designed to be programmed MSB first. The timing interface for programming the AD8324 can be seen in Table 2, Table 3, Figure 3, and Figure 4. While the $\overline{\text{DATEN}}$ pin is held low, the serial bits on the SDATA line are shifted into the register on the rising edge of the CLK pin.

For existing software that uses eight bits to program the cable driver, the two MSBs are ignored. This allows the AD8324 to be compatible with some existing system designs.

The AD8324 recognizes Gain Code 1 through Gain Code 60 (all gain codes are in decimal, unless otherwise noted). When the AD8324 is programmed with Gain Code 61 to Gain Code 63, it internally defaults to maximum gain (Gain Code 60). If the programmed gain code is above 63, the AD8324 recognizes the six LSBs only. For example, Gain Code 75 (01001011 binary) is interpreted as Gain Code 11 (001011 binary) because the two MSBs are ignored.

The programming range of the AD8324 is from −25.5 dB (Gain Code 1) to +33.5 dB (Gain Code 60). The 59 dB gain range is linear with a 1 dB change in a 1 LSB change in gain code. Figure 15 illustrates the gain step size of the AD8324 vs. gain code. The AD8324 is characterized with a differential input signal and a TOKO 458PT-1457 1:1 transformer at the output.

INPUT BIAS, IMPEDANCE, AND TERMINATION

The V_{IN+} and V_{IN-} inputs have a dc bias level of $V_{CC}/2$; therefore, ac-couple the input signal as shown in the typical application circuit (see Figure 23). The differential input impedance of the AD8324 is approximately 1.1 kΩ, and the single-ended input is 550 Ω. The high input impedance of the AD8324 allows flexibility in termination and properly matching filter networks. The AD8324 exhibits optimum performance when driven with a pure differential signal.

OUTPUT BIAS, IMPEDANCE, AND TERMINATION

The output stage of the AD8324 requires a bias of 3.3 V. Connect the 3.3 V power supply to the center tap of the output transformer. In addition, decouple the V_{CC} that is applied to the center tap of the transformer as shown in the typical application circuit (see Figure 23).

The output impedance of the AD8324 is 75 Ω, regardless of whether the amplifier is in transmit enable, transmit disable, or sleep mode. When combined with a 1:1 voltage ratio transformer, this eliminates the need for external back termination resistors. If the output signal is evaluated using standard 50 Ω test equipment, use a minimum loss 75 Ω to 50 Ω pad to provide the test circuit with the proper impedance match. When using a matching attenuator, note that there is 5.7 dB of power loss (7.5 dB voltage) through the network.

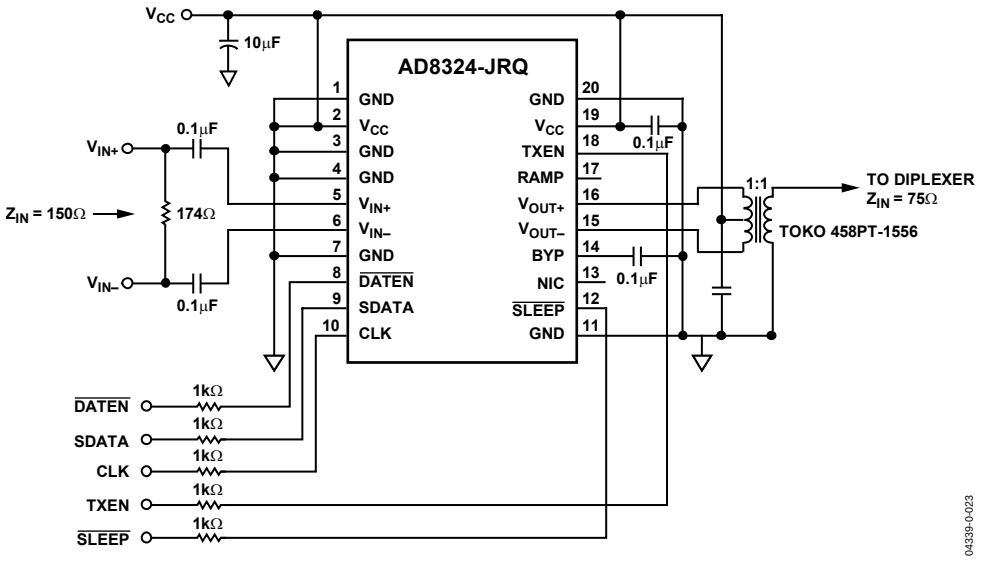


Figure 23. Typical Application Circuit

Table 7. Adjacent Channel Power

	Adjacent Channel Symbol Rate (kSym/s)					
Channel Symbol Rate (kSym/s)	**160**	**320**	**640**	**1280**	**2560**	**5120**
160	−63	−64	−68	−71	−72	−66
320	−63	−64	−66	−70	−72	−67
640	−64	−64	−65	−67	−71	−67
1280	−67	−65	−65	−66	−68	−67
2560	−70	−67	−66	−66	−67	−65
5120	−72	−70	−67	−67	−64	−64

POWER SUPPLY

Deliver the 3.3 V supply to each of the VCC pins via a low impedance power bus. This ensures that each pin is at the same potential. Decouple the power bus to ground using a 10 µF tantalum capacitor located close to the AD8324. In addition to the 10 µF capacitor, decouple the V_{CC} pins to ground with ceramic chip capacitors located close to the pins. In addition, decouple the bypass pin (BYP). The printed circuit board (PCB) must have a low impedance ground plane covering all unused portions of the board, except in areas of the board where input and output traces are in close proximity to the AD8324 and the output transformer. Connect all AD8324 ground pins to the ground plane to ensure proper grounding of all internal nodes.

SIGNAL INTEGRITY LAYOUT CONSIDERATIONS

Careful attention to PCB layout details prevents problems due to board parasitics. Proper radio frequency (RF) design techniques are mandatory. Keep the differential input and output traces as short as possible. Keeping the traces short minimizes parasitic capacitance and inductance, which is most critical between the outputs of the AD8324 and the 1:1 output transformer. It is also critical that all differential signal paths be symmetrical in length and width. In addition, the input and output traces must be adequately spaced to minimize coupling (crosstalk) through the board. Following these guidelines optimizes the overall performance of the AD8324 in all applications.

INITIAL POWER-UP

When the supply voltage is first applied to the AD8324, the gain of the amplifier is initially set to Gain Code 1. As power is first applied to the amplifier, hold the TXEN pin low (Logic 0) to prevent forward signal transmission. After power is applied to the amplifier, the gain can be set to the desired level by following the procedure provided in the Gain Programming for the AD8324 section. The TXEN pin can then be brought from Logic 0 to Logic 1, enabling forward signal transmission at the desired gain level.

RAMP PIN AND BYP PIN FEATURES

The RAMP pin (Pin 15/Pin 17) is used to control the length of the burst on and off transients. By default, leaving the RAMP pin unconnected results in a transient that is fully compliant with DOCSIS 2.0 Radio Frequency Interface (RFI) Specification, Section 6.2.21.2, Spurious Emissions During Burst On/Off Transients. DOCSIS requires that all between burst transients be dissipated no faster than 2 µs. Adding capacitance to the RAMP pin slows the dissipation even more.

The BYP pin (Pin 12/Pin 14) is used to decouple the output stage to ground. Typically, for normal DOCSIS operation, decouple the BYP pin to ground with a 0.1 µF capacitor. In applications that require transient on/off times faster than 2 µs, smaller capacitors can be used; however, note that the BYP pin must always be decoupled to ground.

POWER SAVING FEATURES

The AD8324 incorporates three distinct methods of reducing power consumption: transmit disable and sleep modes for between burst and shutdown modes, and gain dependent quiescent current for transmit enable mode.

The asynchronous TXEN pin is used to place the AD8324 into between burst mode. In this reduced current state, the 75 Ω output impedance is maintained. Applying Logic 0 to the TXEN pin deactivates the on-chip amplifier, providing a 98.8% reduction in consumed power. For 3.3 V operation, the supply current is typically reduced from 207 mA to 2.5 mA. In this mode of operation, between burst noise is minimized and high input to output isolation is achieved. In addition to the TXEN pin, the AD8324 also incorporates an asynchronous $\overline{\text{SLEEP}}$ pin that can be used to further reduce the supply current to approximately 30 µA. Applying Logic 0 to the $\overline{\text{SLEEP}}$ pin places the amplifier into $\overline{\text{SLEEP}}$ mode. Transitioning into or out of $\overline{\text{SLEEP}}$ mode results in a transient voltage at the output of the amplifier.

In addition to the sleep and transmit disable functions, the AD8324 provides yet another means of reducing system power consumption. While in the transmit enable state, the AD8324 incorporates supply current scaling that allows for lower power consumption at lower gain codes. Figure 20 shows the typical relationship between supply current and gain code.

DISTORTION, ADJACENT CHANNEL POWER, AND DOCSIS

To deliver the DOCSIS specification required 58 dBmV of QPSK signal and 55 dBmV of 16 QAM signal, the PA is required to deliver up to 61 dBmV. This added power is required to compensate for losses associated with the diplex filter or other passive components that may be included in the upstream path of cable modems or set-top boxes. Note that the AD8324 is characterized with a differential input signal. Figure 7 and Figure 10 show the AD8324 second and third harmonic distortion performance vs. the fundamental frequency for various output power levels. These figures are useful for determining the in-band harmonic levels from 5 MHz to 65 MHz. Harmonics higher in frequency (more than 42 MHz for DOCSIS 2.0 specifications and more than 65 MHz for EuroDOCSIS specifications) are sharply attenuated by the low-pass filter function of the diplexer.

Another measure of signal integrity is adjacent channel power (ACP). DOCSIS 2.0 RFI Specification, Section 6.2.21.1.1, states, "Spurious emissions from a transmitted carrier may occur in an adjacent channel that could be occupied by a carrier of the same or different modulation rate." Figure 13 shows the typical ACP for a 61 dBmV (approximately 12 dBm) QPSK signal taken at the output of the AD8324 during product characterization. The transmit channel width and adjacent channel width in Figure 13 correspond to the symbol rates of 160 kSym/s. Table 7 shows the ACP results for the AD8324 driving a QPSK, 61 dBmV signal for all conditions in DOCSIS RFI Specification, Table 6-10, Adjacent Channel Spurious Emissions Relative to the Transmitted Burst Power Level.

UTILIZING DIPLEX FILTERS

The AD8324 is designed to drive 61 dBmV without any external filtering and still meet DOCSIS spurious emissions and distortion requirements. However, in most upstream CATV applications, a diplex filter is used to separate the upstream and downstream signal paths from one another. The diplex filter does have insertion loss that the upstream driver needs to overcome, but it also provides a low-pass filter. The addition of this low-pass filter to the signal chain greatly attenuates second harmonic products of channels more than 21 MHz and third harmonic products of channels at or more than 14 MHz up for diplexers with a 42 MHz upstream cutoff. Similar performance gains can be achieved using European-specified diplexers to filter second harmonics for channels more than 33 MHz and third harmonics for channels more than 22 MHz (65 MHz upstream cutoff). This filtering allows the AD8324 to drive up to 63 dBmV of QPSK (this level varies by application and modulation type).

NOISE AND DOCSIS

At minimum gain, the AD8324 output noise spectral density is 1.3 nV/√Hz measured at 10 MHz. DOCSIS 2.0 RFI Specification Table 6-11, Spurious Emissions in 5 to 42 MHz Relative to the Transmitted Burst Power Level, specifies the output noise for various symbol rates. The calculated noise power in dBmV for 160 kSym/s is

$$20 \times \log [\sqrt{(1.3\ \text{nV}/\sqrt{\text{Hz}})^2 \times 160\ \text{kHz}}] + 60 = -65.7\ \text{dBmV}$$

Comparing the computed noise power of −65.7 dBmV to the +8 dBmV signal yields −73.7 dBc, which meets the required level set forth in DOCSIS 2.0 RFI Specification Table 6-11. As the AD8324 gain is increased above this minimum value, the output signal increases at a faster rate than the noise, resulting in a signal-to-noise ratio that improves with gain. In transmit disable mode, the output noise spectral density is 1.1 nV/√Hz, which results in −67 dBmV when computed over 160 kSym/s.

DIFFERENTIAL SIGNAL SOURCE

Typical applications for the AD8324 use a differential input signal from a modulator or a DAC. Refer to Table 8 for common values of R4, or calculate other input configurations using the equation in Figure 24. This circuit configuration gives optimal distortion results due to the symmetric input signals. Note that this configuration is used to characterize the AD8324.

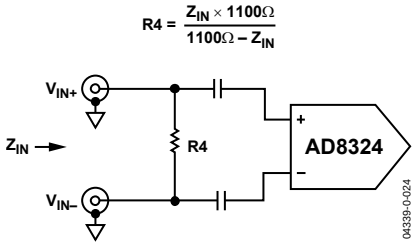


Figure 24. Differential Circuit

DIFFERENTIAL SIGNAL FROM SINGLE-ENDED SOURCE

To implement a differential signal from a single-ended signal source, a 1:1 balun transformer is used to approximate the differential signal as shown in Figure 25. Because of the non-ideal nature of real transformers, the differential signal is not purely equal and opposite in amplitude. Although this circuit slightly sacrifices even order harmonic distortion due to asymmetry, it does provide a convenient way to evaluate the AD8324 with a single-ended source.

Table 8 provides typical R4 values for common input configurations. Other input impedances can be calculated using the equation in Figure 25.

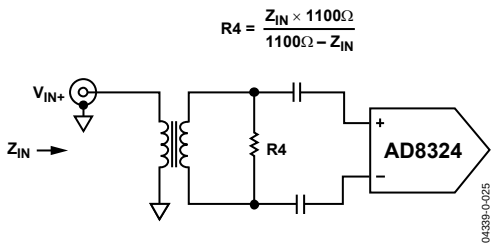


Figure 25. Single-to-Differential Circuit

SINGLE-ENDED SOURCE

Although the AD8324 is designed to have optimal DOCSIS performance when used with a differential input signal, the AD8324 can also be used as a single-ended receiver, or as an IF digitally controlled amplifier. However, as with the single ended to differential configuration noted previously, even-order harmonic distortion is slightly degraded.

When operating the AD8324 in single-ended input mode, terminate the device as illustrated in Figure 26. Table 8 shows the correct values for R1 and R17 for some common input configurations. Other input impedance configurations may be accommodated using the equations in Figure 26.

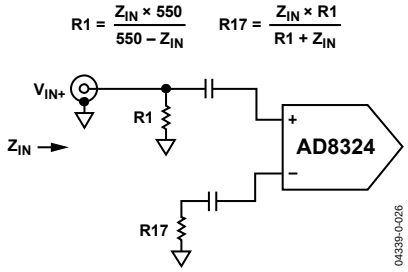
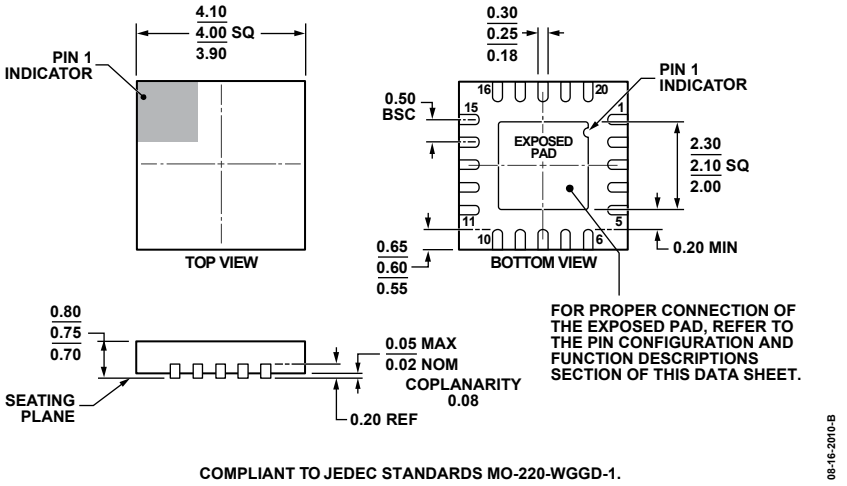


Figure 26. Single-Ended Circuit

Table 8. Common Matching Resistors

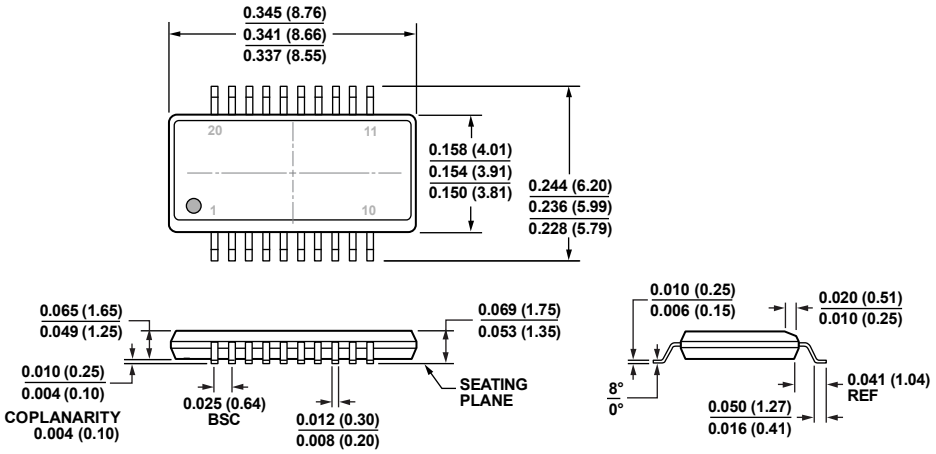
Differential Input Termination		Single-Ended Input Termination	
Z_{IN} (Ω)	R4 (Ω)	Z_{IN} (Ω)	R1/R17 (Ω)
50	52.3	50	54.9/26.1
75	80.6	75	86.6/40.2
100	110		
150	174		

OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MO-220-WGGD-1.

Figure 27. 20-Lead Lead Frame Chip Scale Package [LFCSP]
4 mm × 4 mm Body, and 0.75 mm Package Height
(CP-20-6)
Dimensions shown in millimeters



COMPLIANT TO JEDEC STANDARDS MO-137-AD

CONTROLLING DIMENSIONS ARE IN INCHES; MILLIMETER DIMENSIONS (IN PARENTHESES) ARE ROUNDED-OFF INCH EQUIVALENTS FOR REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN.

Figure 28. 20-Lead Shrink Small Outline Package [QSOP]
(RQ-20)
Dimensions shown in inches and (millimeters)

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Package Option
AD8324ACPZ	−40°C to +85°C	20-Lead Lead Frame Chip Scale Package [LFCSP]	CP-20-6
AD8324ACPZ-REEL7	−40°C to +85°C	20-Lead Lead Frame Chip Scale Package [LFCSP]	CP-20-6
AD8324JRQZ-REEL7	−25°C to +70°C	20-Lead Shrink Small Outline Package [QSOP]	RQ-20

[1] Z = RoHS Compliant Part.