Logic Controlled, High-Side Power Switch

Data Sheet

ADP194

FEATURES

- Low RDS_{ON} of 80 mΩ at 1.8 V
- Low input voltage range: 1.1 V to 3.6 V
- 500 mA continuous operating current
- Built-in level shift for control logic that can be operated by 1.2 V logic
- Low 2 µA (maximum) ground current
- Ultralow shutdown current <0.7 µA
- Reverse current blocking
- Ultrasmall 0.8 mm × 0.8 mm × 0.5mm, 4-ball, 0.4 mm pitch WLCSP

APPLICATIONS

- Mobile phones
- Digital cameras and audio devices
- Portable and battery-powered equipment

TYPICAL APPLICATIONS CIRCUIT

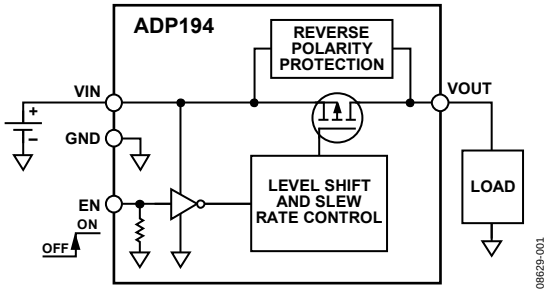

Figure 1.

GENERAL DESCRIPTION

The ADP194 is a high-side load switch designed for operation from 1.1 V to 3.6 V and is protected against reverse current flow from output to input. This load switch provides power domain isolation for extended power battery life. The device contains a low on-resistance P-channel MOSFET that supports more than 500 mA of continuous load current and minimizes power loss. The low 2 µA (maximum) ground current and ultralow shutdown current make the ADP194 ideal for battery-operated portable equipment. The built-in level shifter in the enable logic input makes the ADP194 compatible with modern processors and GPIO controllers.

Beyond operating performance, the ADP194 occupies minimal printed circuit board (PCB) space with an area of less than 0.64 mm^2 and a height of 0.50 mm. The ADP194 is available in an ultrasmall 0.8 mm × 0.8 mm, 4-ball, 0.4 mm pitch WLCSP.

Rev. A

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REVISION HISTORY

9/11—Rev. 0 to Rev. A

Changes to Table 2 4

5/11—Revision 0: Initial Version

SPECIFICATIONS

V_{IN} = 1.8 V, V_{EN} = V_{IN}, I_{LOAD} = 200 mA, T_A = 25°C, unless otherwise noted.

Table 1.

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
INPUT VOLTAGE RANGE	V_{IN}	T_J = −40°C to +85°C	1.1		3.6	V
EN INPUT						
EN Input Threshold	V_{EN_TH}	1.1 V ≤ V_{IN} ≤ 1.3 V, T_J = −40°C to +85°C	0.3		1.0	V
		1.3 V < V_{IN} < 1.8 V, T_J = −40°C to +85°C	0.35		1.2	V
		1.8 V ≤ V_{IN} ≤ 3.6 V, T_J = −40°C to +85°C	0.45		1.2	V
Logic High Voltage	V_{IH}	1.1 V ≤ V_{IN} ≤ 3.6 V	1.2			V
Logic Low Voltage	V_{IL}	1.1 V ≤ V_{IN} ≤ 3.6 V			0.3	V
EN Input Pull-Down Resistance	R_{EN}			4		MΩ
CURRENT						
Ground Current[1]	I_{GND}	VOUT open, T_J = −40°C to +85°C			2	µA
Shutdown Current	I_{OFF}	EN = GND		0.7		µA
		EN = GND, T_J = −40°C to +85°C			2	µA
REVERSE BLOCKING						
V_{OUT} Current		V_{EN} = 0 V, V_{IN} = 0 V, V_{OUT} = 3.6 V		4		µA
Hysteresis		$\lvert V_{IN} - V_{OUT} \rvert$		50		mV
VIN to VOUT RESISTANCE	RDS_{ON}	V_{IN} = 3.6 V, EN = 1.5 V		55		mΩ
		V_{IN} = 2.5 V, EN = 1.5 V		65		mΩ
		V_{IN} = 1.8 V, EN = 1.5 V, T_J = −40°C to +85°C		80	120	mΩ
		V_{IN} = 1.5 V, EN = 1.5 V		105		mΩ
		V_{IN} = 1.2 V, EN = 1 V		160		mΩ
VOUT TIME						
Turn-On Delay Time	t_{ON_DLY}	EN = 1.5 V, C_{LOAD} = 1 µF		7		µs
		V_{IN} = 3.6 V, EN = 1.5 V, C_{LOAD} = 1 µF		1.5		µs

[1] Ground current includes EN pull-down current.

TIMING DIAGRAM

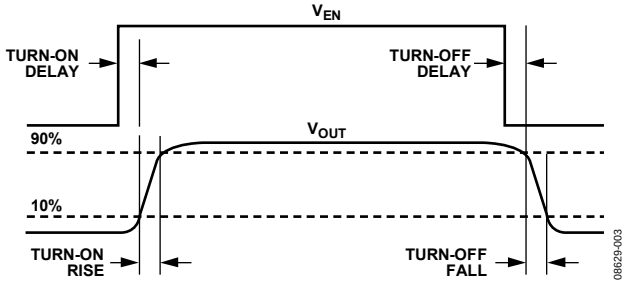

Figure 2. Timing Diagram

ABSOLUTE MAXIMUM RATINGS

Table 2.

Parameter	Rating
VIN to GND	−0.3 V to +4.0 V
VOUT to GND	−0.3 V to +4.0 V
EN to GND	−0.3 V to +4.0 V
Continuous Drain Current	
T_A = 25°C	±1 A
T_A = 85°C	±500 mA
Continuous Diode Current	−50 mA
Storage Temperature Range	−65°C to +150°C
Operating Junction Temperature Range	−40°C to +125°C
Operating Ambient Temperature Range	−40°C to +85°C
Soldering Conditions	JEDEC J-STD-020

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

THERMAL DATA

Absolute maximum ratings apply individually only, not in combination. The ADP194 may be damaged if the junction temperature limits are exceeded. Monitoring ambient temperature does not guarantee that T_J is within the specified temperature limits. In applications with high power dissipation and poor PCB thermal resistance, the maximum ambient temperature may need to be derated.

In applications with moderate power dissipation and low PCB thermal resistance, the maximum ambient temperature can exceed the maximum limit as long as the junction temperature is within specification limits. The junction temperature (T_J) of the device is dependent on the ambient temperature (T_A), the power dissipation of the device (P_D), and the junction-to-ambient thermal resistance of the package (θ_{JA}).

Maximum junction temperature (T_J) is calculated from the ambient temperature (T_A) and power dissipation (P_D) using the formula

$$T_J = T_A + (P_D \times \theta_{JA})$$

Junction-to-ambient thermal resistance (θ_{JA}) of the package is based on modeling and calculation using a 4-layer board. The junction-to-ambient thermal resistance is highly dependent on the application and board layout. In applications where high maximum power dissipation exists, close attention to thermal board design is required. The value of θ_{JA} may vary, depending on PCB material, layout, and environmental conditions. The specified values of θ_{JA} are based on a 4-layer, 4 inch × 3 inch PCB. See JESD51-7 and JESD51-9 for detailed information regarding board construction. For additional information, see the AN-617 application note, *MicroCSP™ Wafer Level Chip Scale Package*.

Ψ_{JB} is the junction-to-board thermal characterization parameter with units of °C/W. Ψ_{JB} of the package is based on modeling and calculation using a 4-layer board. The JESD51-12 document, *Guidelines for Reporting and Using Electronic Package Thermal Information*, states that thermal characterization parameters are not the same as thermal resistances. Ψ_{JB} measures the component power flowing through multiple thermal paths rather than through a single path, as in thermal resistance (θ_{JB}). Therefore, Ψ_{JB} thermal paths include convection from the top of the package as well as radiation from the package, factors that make Ψ_{JB} more useful in real-world applications. Maximum junction temperature (T_J) is calculated from the board temperature (T_B) and the power dissipation (P_D) using the formula

$$T_J = T_B + (P_D \times \Psi_{JB})$$

See JESD51-8, JESD51-9, and JESD51-12 for more detailed information about Ψ_{JB}.

THERMAL RESISTANCE

θ_{JA} and Ψ_{JB} are specified for the worst-case conditions, that is, a device soldered in a circuit board for surface-mount packages.

Table 3. Thermal Resistance

Package Type	θ_{JA}	Ψ_{JB}	Unit
4-Ball, 0.4 mm Pitch WLCSP	260	58.4	°C/W

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

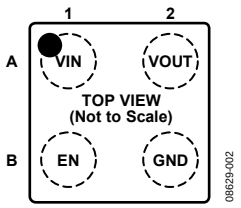

Figure 3. Pin Configuration

Table 4. Pin Function Descriptions

Pin No.	Mnemonic	Description
A1	VIN	Input Voltage.
B1	EN	Enable Input. Drive EN high to turn on the switch; drive EN low to turn off the switch.
A2	VOUT	Output Voltage.
B2	GND	Ground.

TYPICAL PERFORMANCE CHARACTERISTICS

V_{IN} = 1.8 V, V_{EN} = V_{IN} > V_{IH}, I_{LOAD} = 100 mA, T_A = 25°C, unless otherwise noted.

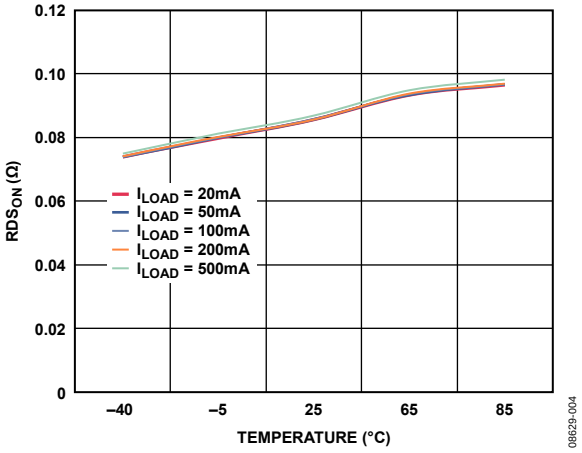

Figure 4. RDS_{ON} vs. Temperature

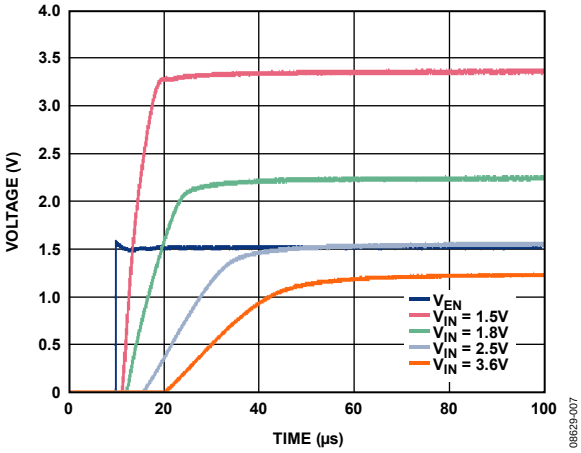

Figure 7. Start-Up and Turn-On Delay vs. Input Voltage

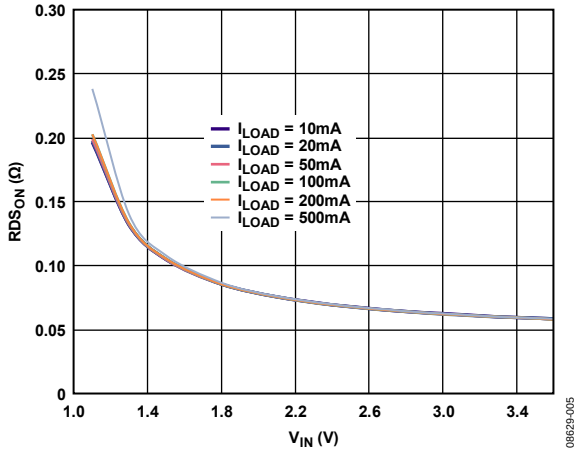

Figure 5. RDS_{ON} vs. Input Voltage, V_{IN}

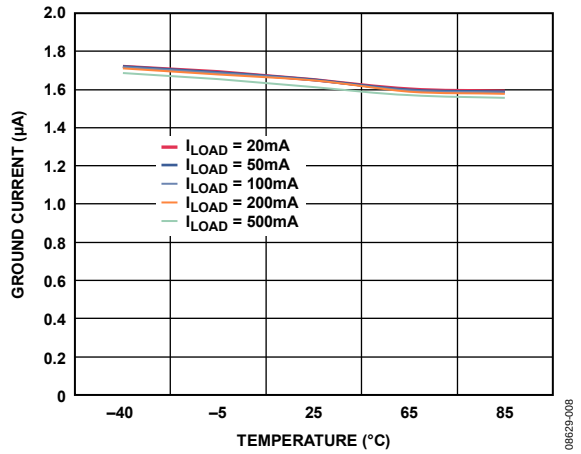

Figure 8. Ground Current vs. Temperature

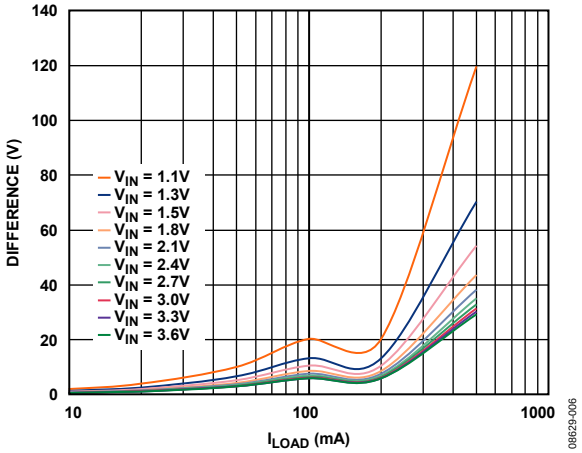

Figure 6. Voltage Drop vs. Load Current

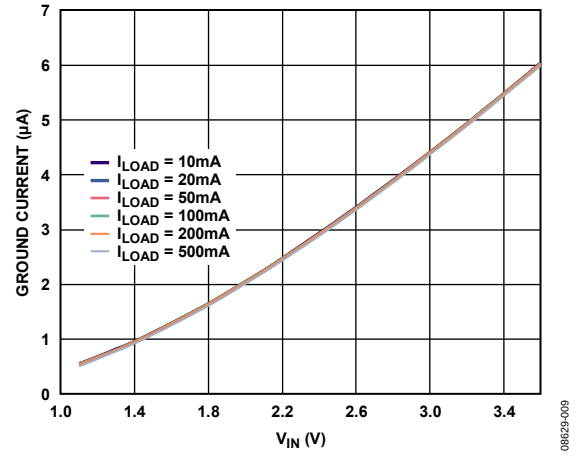

Figure 9. Ground Current vs. Input Voltage, V_{IN}

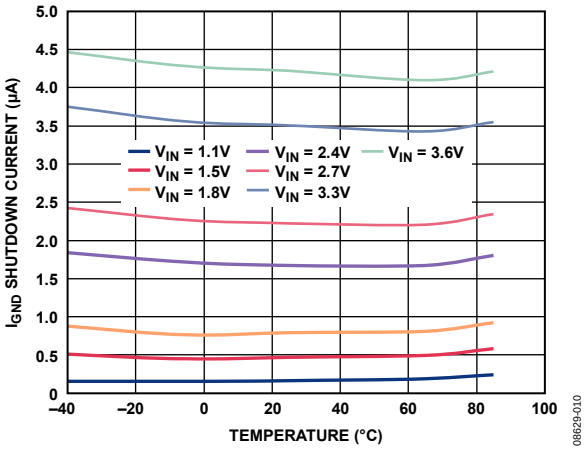

Figure 10. Shutdown Current vs. Temperature, V_{OUT} Open

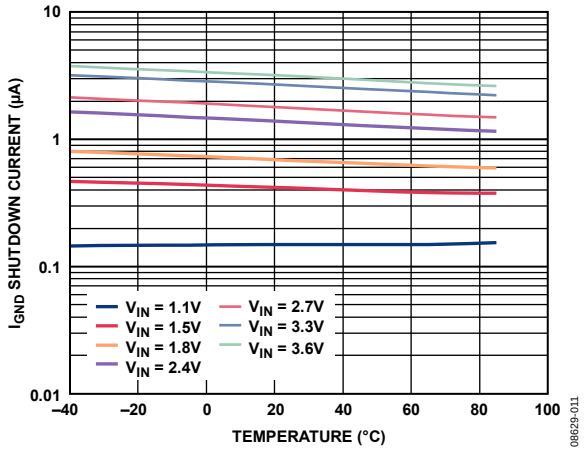

Figure 11. Shutdown Current vs. Temperature, V_{OUT} = 0 V

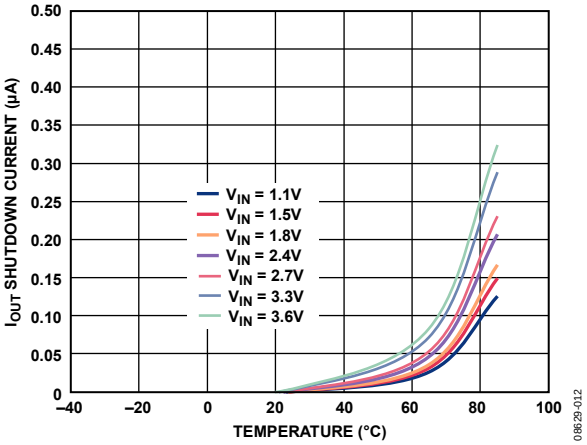

Figure 12. I_{OUT} Shutdown Current vs. Temperature, V_{OUT} = 0 V

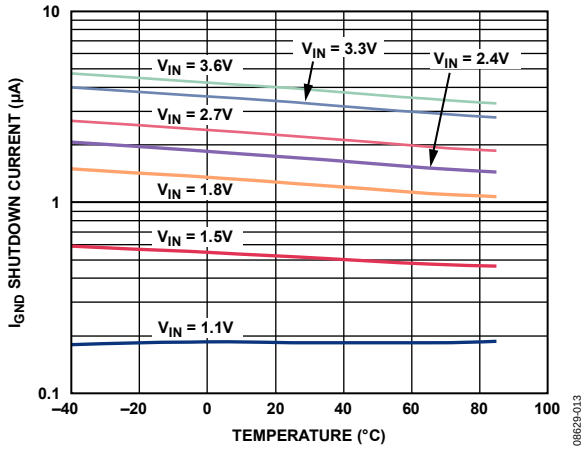

Figure 13. Reverse Shutdown Current vs. Temperature, V_{OUT} = 0 V

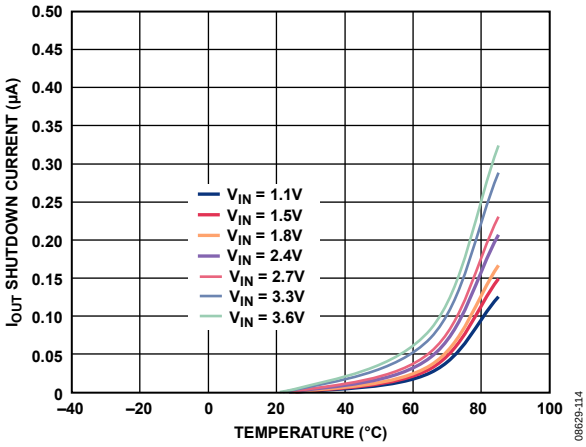

Figure 14. I_{OUT} Reverse Current vs. Temperature, V_{OUT} = 0 V

THEORY OF OPERATION

The ADP194 is a high-side PMOS load switch. It is designed to operate from a supply range from 1.1 V to 3.6 V. The PMOS load switch is designed for low on resistance, 80 mΩ at V_{IN} = 1.8 V, and supports 500 mA of continuous output current. The ADP194 is a low ground current device with a nominal 4 MΩ pull-down resistor on its enable pin.

The reverse current protection circuitry prevents current flow backwards through the ADP194 when the output voltage is greater than the input voltage. A comparator senses the difference between the input and output voltages. When the difference between the input voltage and output voltage exceeds 50 mV, the body of the PFET is switched to V_{OUT} and turned off or opened. In other words, the gate is connected to VOUT.

The package is a space-saving 0.8 mm × 0.8 mm, 4-ball WLCSP.

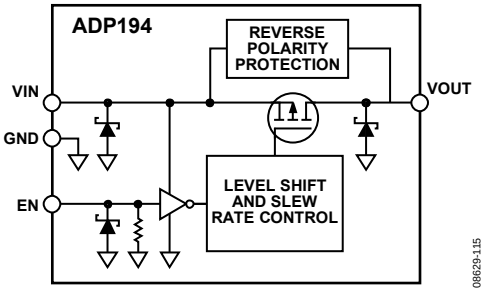

Figure 15. Functional Block Diagram

APPLICATIONS INFORMATION

GROUND CURRENT

The major source for ground current in the ADP194 is the 4 MΩ pull-down resistor on the enable (EN) pin. Figure 16 shows typical ground current when $V_{EN} = V_{IN}$ and V_{IN} varies from 1.1 V to 3.6 V.

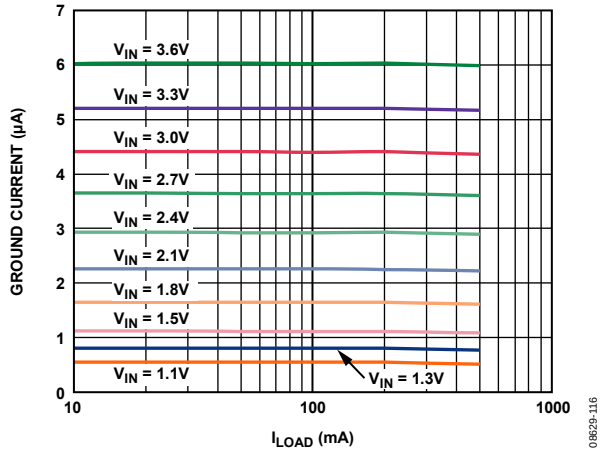

Figure 16. Ground Current vs. Load Current, Different Input Voltages

As shown in Figure 17, an increase in ground current can occur when $V_{EN} \neq V_{IN}$. This is caused by the CMOS logic nature of the level shift circuitry as it translates an EN signal ≥ 1.1 V to a logic high. This increase is a function of the $V_{IN} - V_{EN}$ delta.

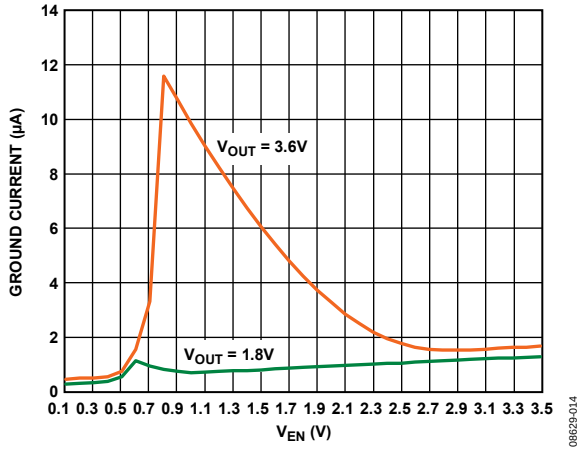

Figure 17. Typical Ground Current when $V_{EN} \neq V_{IN}$

ENABLE FEATURE

The ADP194 uses the EN pin to enable and disable the VOUT pin under normal operating conditions. As shown in Figure 18, when a rising voltage on EN crosses the active threshold, VOUT turns on. When a falling voltage on EN crosses the inactive threshold, VOUT turns off.

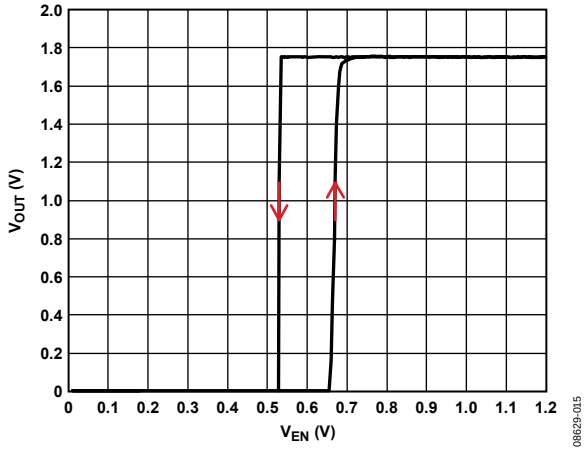

Figure 18. Typical EN Operation, V_{IN} = 1.8 V

The EN input has built-in hysteresis, as shown in Figure 18. The hysteresis prevents on/off oscillations that can occur due to noise on the EN pin as V_{EN} passes through the threshold points.

The EN input active/inactive thresholds derive from the V_{IN} voltage; therefore, these thresholds vary with changing input voltage. Figure 19 shows typical EN active/inactive thresholds when the input voltage varies from 1.1 V to 3.6 V.

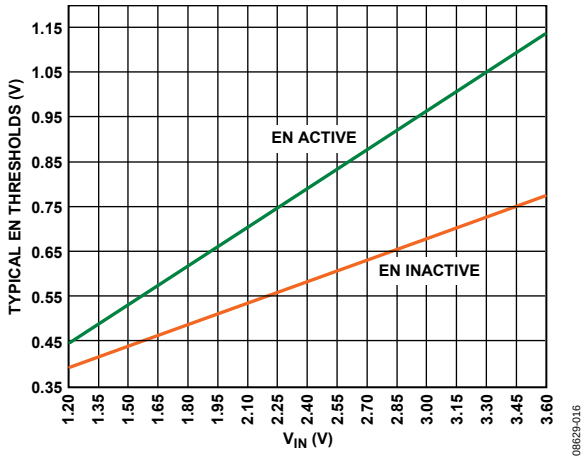

Figure 19. Typical EN Pin Thresholds vs. Input Voltage, V_{IN}

TIMING

Turn-on delay is defined as the delta between the time that EN reaches >1.1 V until VOUT rises to ~10% of its final value. The ADP194 includes circuitry to set the typical 1.5 µs turn-on delay at 3.6 V V_{IN} to limit the V_{IN} inrush current. As shown in Figure 20, the turn-on delay is dependent on the input voltage.

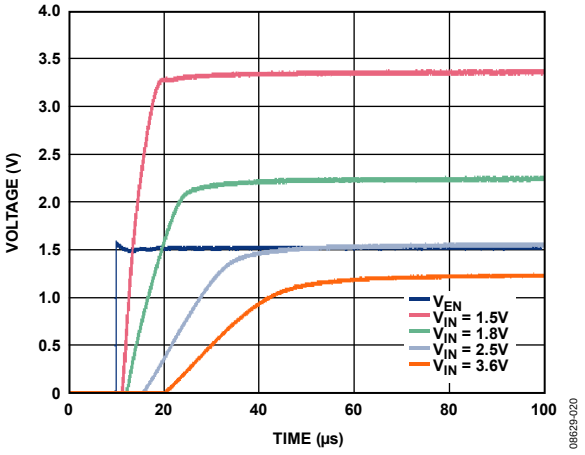

Figure 20. Typical Turn-On Delay Time with Varying Input Voltage

The rise time of VOUT is defined as the time delta between the 10% and 90% points of VOUT as it transitions to its final value. It is dependent on the RC time constant where C = load capacitance (C_{LOAD}) and R = $RDS_{ON}||R_{LOAD}$. Because RDS_{ON} is usually smaller than R_{LOAD}, an adequate approximation for RC is $RDS_{ON} \times C_{LOAD}$. The ADP194 does not need any input or load capacitor, but capacitors can be used to suppress noise on the board. If significant load capacitance is connected, inrush current may be a concern.

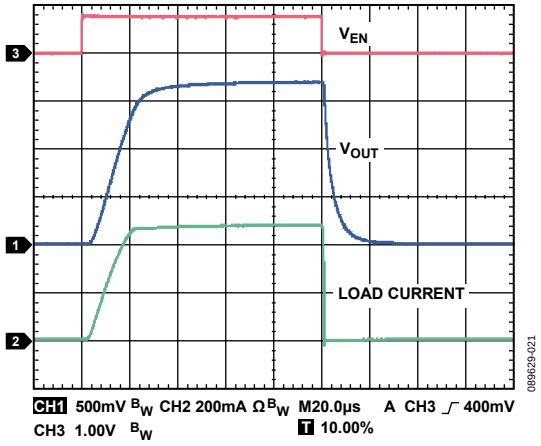

Figure 21. Typical Rise Time and Inrush Current with V_{IN} = 1.8 V, C_{LOAD} = 1 µF

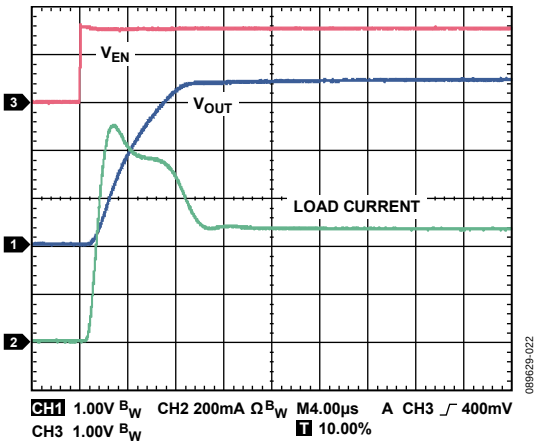

Figure 22. Typical Rise Time and Inrush Current with V_{IN} = 3.6 V, C_{LOAD} = 1 µF

The fall time or turn-off time of VOUT is defined as the time delta between the 90% and 10% points of VOUT as it transitions to its final value. The turn-off time is also dependent on the RC time constant.

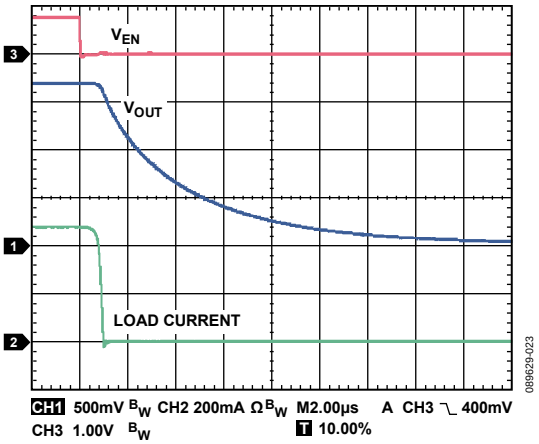

Figure 23. Typical Turn-Off Time, V_{IN} = 1.8 V, R_{LOAD} = 3.6 Ω

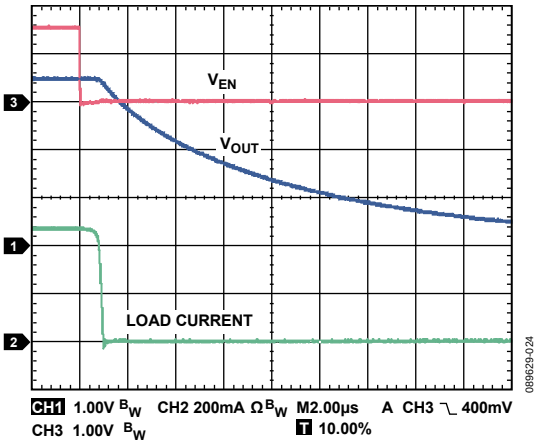

Figure 24. Typical Turn-Off Time, V_{IN} = 3.6 V, R_{LOAD} = 7.5 Ω

THERMAL CONSIDERATIONS

In most applications, the ADP194 does not dissipate much heat due to its low on-channel resistance. However, in applications with high ambient temperature and high load current, the heat dissipated in the package can cause the junction temperature of the die to exceed the maximum junction temperature of 125°C.

The junction temperature of the die is the sum of the ambient temperature of the environment and the temperature rise of the package due to the power dissipation, as shown in Equation 1.

To guarantee reliable operation, the junction temperature of the ADP194 must not exceed 125°C. To ensure that the junction temperature stays below this maximum value, the user must be aware of the parameters that contribute to junction temperature changes. These parameters include ambient temperature, power dissipation in the device, and thermal resistances between the junction and ambient air (θ_{JA}). The θ_{JA} value is dependent on the package assembly compounds that are used and the amount of copper used to solder the package GND pin to the PCB. Table 5 shows typical θ_{JA} values of the 4-ball WLCSP for various PCB copper sizes. Table 6 shows the typical Ψ_{JB} value of the 4-ball WLCSP.

Table 5. Typical θ_{JA} Values for WLCSP

Copper Size (mm²)	θ_{JA} (°C/W)
0[1]	260
50	159
100	157
300	153
500	151

[1] Device soldered to minimum size pin traces.

Table 6. Typical Ψ_{JB} Values

Package	Ψ_{JB}	Unit
4-Ball WLCSP	58.4	°C/W

The junction temperature of the ADP194 is calculated from the following equation:

$$T_J = T_A + (P_D \times \theta_{JA}) \quad (1)$$

where:
T_A is the ambient temperature.
P_D is the power dissipation in the die, given by

$$P_D = [(V_{IN} - V_{OUT}) \times I_{LOAD}] + (V_{IN} \times I_{GND}) \quad (2)$$

where:
I_{LOAD} is the load current.
I_{GND} is the ground current.
V_{IN} and V_{OUT} are the input and output voltages, respectively.

Power dissipation due to ground current is quite small and can be ignored. Therefore, the junction temperature equation simplifies to the following:

$$T_J = T_A + \{[(V_{IN} - V_{OUT}) \times I_{LOAD}] \times \theta_{JA}\} \quad (3)$$

In cases where the board temperature is known, use the thermal characterization parameter, Ψ_{JB}, to estimate the junction temperature rise. Maximum junction temperature (T_J) is calculated from the board temperature (T_B) and power dissipation (P_D) using the formula

$$T_J = T_B + (P_D \times \Psi_{JB}) \quad (4)$$

PCB LAYOUT CONSIDERATIONS

The heat dissipation capability of the package can be improved by increasing the amount of copper attached to the pins of the ADP194. However, as listed in Table 5, a point of diminishing returns is eventually reached, beyond which an increase in the copper size does not yield significant heat dissipation benefits.

It is critical to keep the input and output traces as wide and as short as possible to minimize the circuit board trace resistance.

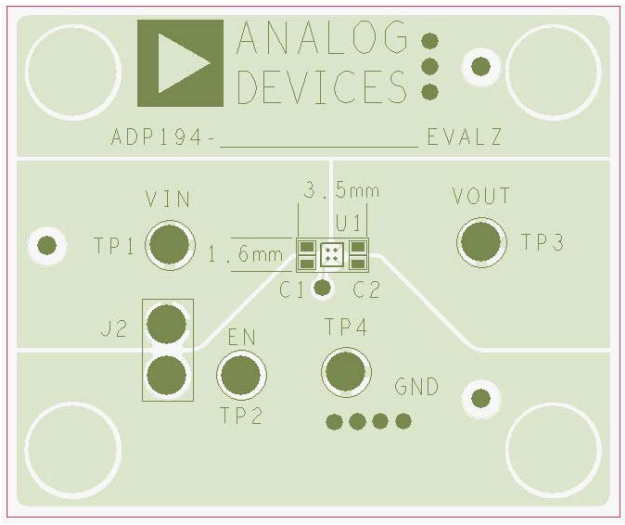

Figure 25. ADP194 PCB Layout

OUTLINE DIMENSIONS

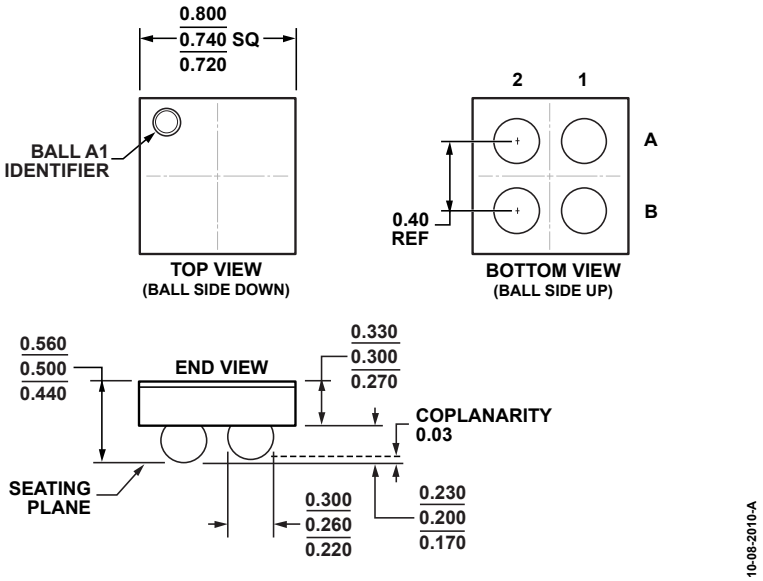

Figure 26. 4-Ball Wafer Level Chip Scale Package [WLCSP]
(CB-4-5)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Package Option	Branding
ADP194ACBZ-R7	−40°C to +85°C	4-Ball Wafer Level Chip Scale Package [WLCSP]	CB-4-5	76
ADP194CB-EVALZ		Evaluation Board		

[1] Z = RoHS Compliant Part.

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