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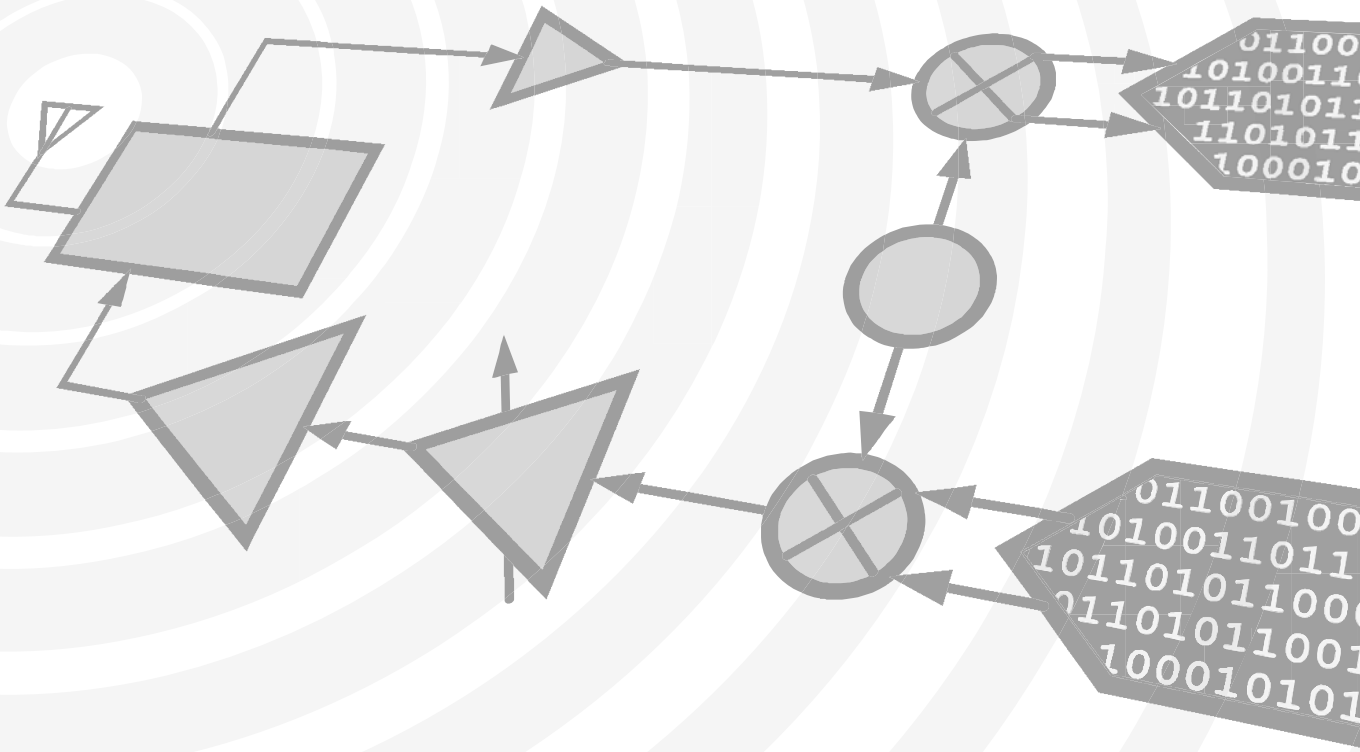
NO CONTENT ON THE ATTACHED DOCUMENT HAS CHANGED



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HMC440* Product Page Quick Links

Last Content Update: 11/01/2016

Comparable Parts

View a parametric search of comparable parts

Evaluation Kits

- HMC440QS16G Evaluation Board

Documentation

Data Sheet

- HMC440 Data Sheet

Tools and Simulations

- Using the HMC Design Tool for Synthesizers with a PFD Output

Reference Materials

Quality Documentation

- HMC Legacy PCN: QS##, QS##E and QS##G,QS##GE packages - Relocation of pre-existing production equipment to new building
- Package/Assembly Qualification Test Report: Plastic Encapsulated QSOP (QTR: 02015 REV: 11)
- PCN: MS, QS, SOT, SOIC packages - Sn/Pb plating vendor change
- Semiconductor Qualification Test Report: GaAs HBT-A (QTR: 2013-00228)

Design Resources

- HMC440 Material Declaration
- PCN-PDN Information
- Quality And Reliability
- Symbols and Footprints

Discussions

View all HMC440 EngineerZone Discussions

Sample and Buy

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HMC440QS16G / 440QS16GE

v03.0808

2.8 GHz INTEGER-N SYNTHESIZER (N = 2 - 32)

Typical Applications

The HMC440QS16G(E) is ideal for:

- Satellite Communication Systems
- Point-to-Point Radios
- Military Applications
- Sonet Clock Generation

Features

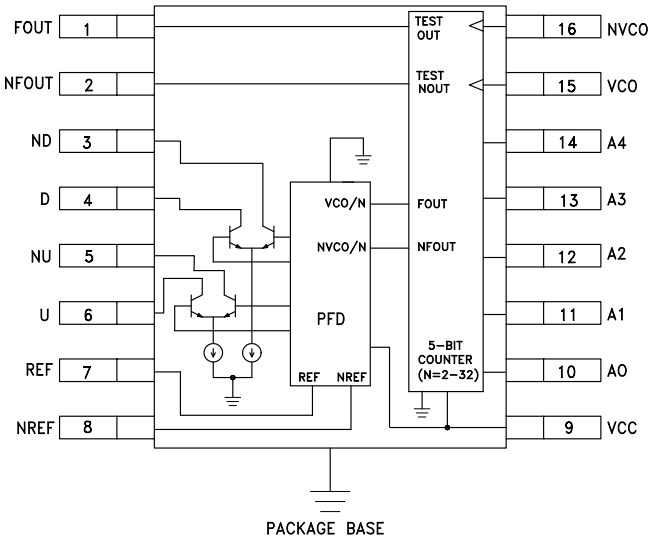
Ultra Low SSB Phase Noise Floor:
-153 dBc/Hz @ 10 kHz offset @ 100 MHz Reference Frequency.

Programmable Divider (N = 2 - 32) Operating up to 2.8 GHz

Open Collector Output Buffer Amplifiers for Interfacing w/ Op-Amp Based Loop Filter

QSOP16G SMT Package: 29.4 mm^2

Functional Diagram



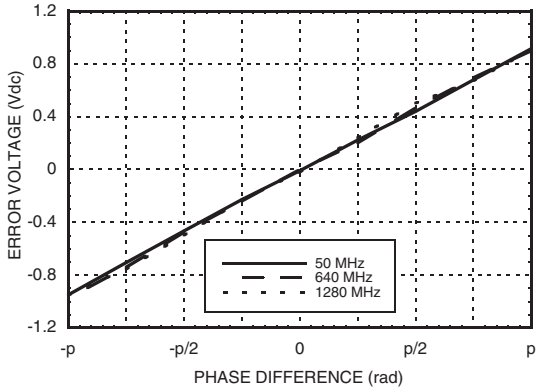
General Description

The HMC440QS16G(E) is an Integer-n synthesizer that incorporates a 10 to 1300 MHz digital Phase-Frequency Detector with 10 to 2800 MHz 5-Bit Frequency Counter (continuous division from 2 to 32) in miniature 16 lead QSOP plastic packages. It is intended for use in low phase noise offset-synthesizer applications. The HMC440QS16G(E)'s combination of high frequency operation along with ultra low phase noise floor make possible synthesizers with wide loop bandwidth and low N resulting in fast settling and very low phase noise. When used in conjunction with a differential loop amplifier, the HMC440QS16G(E) generates an output voltage that can be used to phase lock a VCO to a reference oscillator.

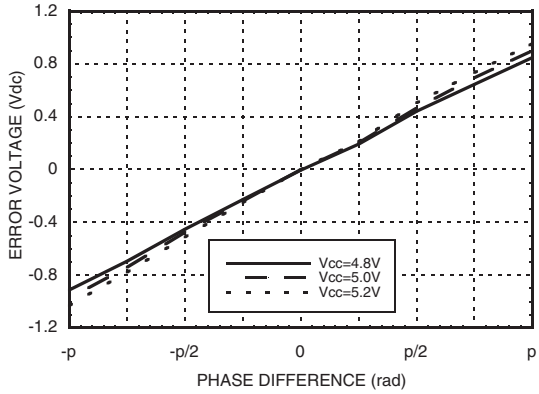
Electrical Specifications, T_A = +25° C, Vcc= 5V

Parameter	Conditions	Min.	Typ.	Max.	Units
Maximum Ref. Input Frequency	Sine or Square Wave Input	1300			MHz
Minimum Ref. Input Frequency	Square Wave Input			10	MHz
Reference Input Power Range	100 MHz Frequency	-10		+10	dBm
Maximum VCO Input Frequency	Sine or Square Wave Input	2800			MHz
Minimum VCO Input Frequency	Square Wave Input			10	MHz
VCO Input Power Range	100 MHz Input Frequency	-15		+10	dBm
Output Voltage	200 Ohm Pull Up to Vcc		2000		mV, Pk - Pk
SSB Phase Noise	@ 10 kHz Offset @ 100 MHz Ref. Input, Pin= 0 dBm		-153		dBc/Hz
Supply Current			250		mA

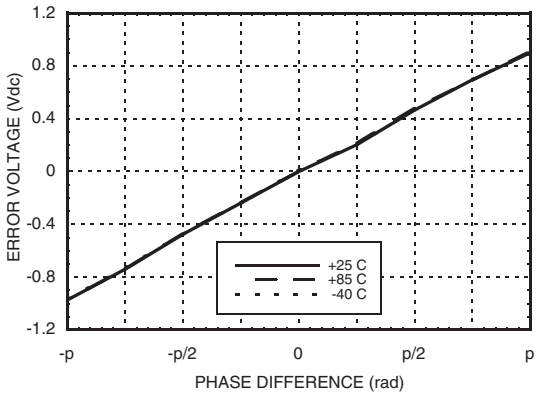
Error Voltage vs. Frequency, Pin= 0 dBm*



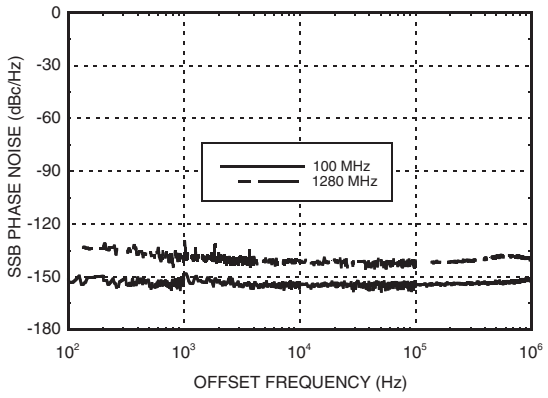
Error Voltage vs. Supply Voltage, Pin= 0 dBm, Fin= 640 MHz*



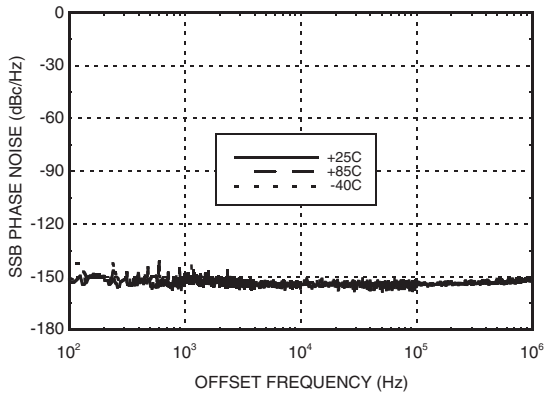
Error Voltage vs. Temperature, Pin= 0 dBm, Fin= 640 MHz*



SSB Phase Noise Performance, Pin= 0 dBm, T= 25 °C



SSB Phase Noise Performance, Pin= 0 dBm, Fin= 100 MHz



** See Gain & Error Voltage Test Circuit herein.*

HMC440QS16G / 440QS16GE

v03.0808

2.8 GHz INTEGER-N SYNTHESIZER (N = 2 - 32)

Absolute Maximum Ratings

RF Input (Vcc= +5V)	+13 dBm
Supply Voltage (Vcc)	+5.5V
Counter Logic Input (A_0 - A_4)	-0.5V to (0.5V + Vcc)
Channel Temperature (Tc)	135 °C
Continuous Pdiss (T = 85 °C) (derate 56.8 mW/° C above 85 °C)	2.84 W
Thermal Resistance (Junction to ground paddle)	17.6 °C/W
Storage Temperature	-65 to +150 °C
Operating Temperature	-40 to +85 °C

ELECTROSTATIC SENSITIVE DEVICE
OBSERVE HANDLING PRECAUTIONS

Typical Supply Current vs. Vcc

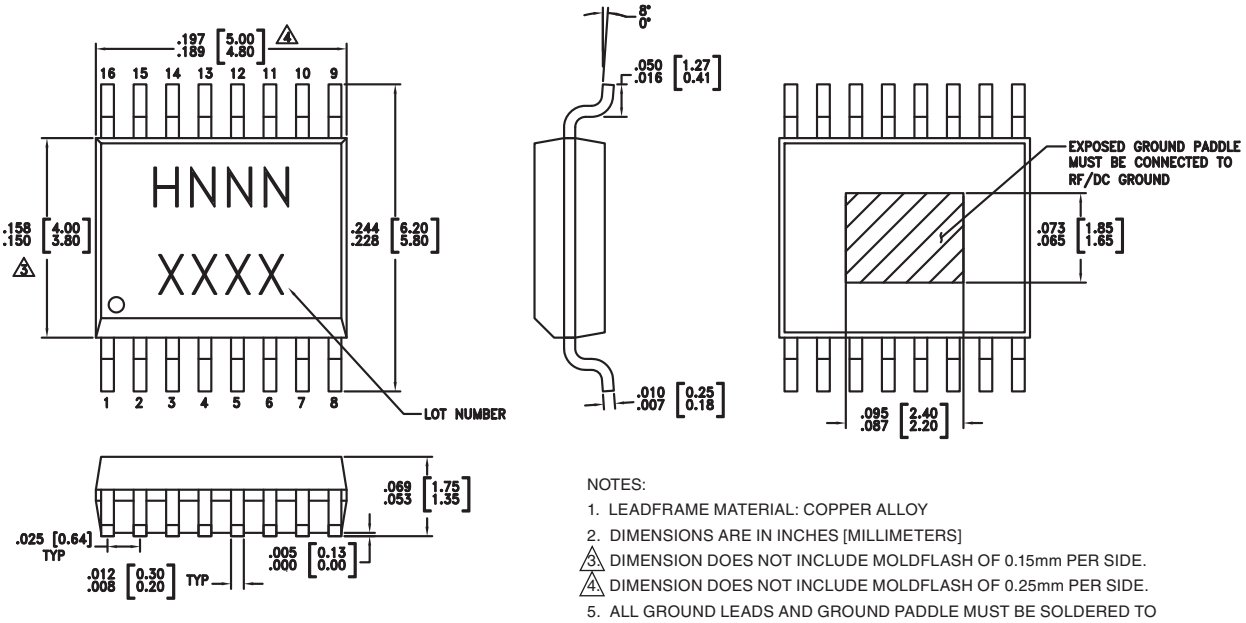
Vcc (Vdc)	Icc (mA)
4.8	229
5.0	250
5.2	266

Note: HMC440QS16G will work over full voltage range above.

Typical DC Characteristics @ Vcc = +5V

Symbol	Characteristics	+25C			Units
		Min.	Typ.	Max.	
Icc	Power Supply Current	229	250	266	mA
Voh	Output High Voltage	5.0	5.0	5.0	V
Vol	Output Low Voltage	2.9	3	3.1	V

Outline Drawing



NOTES:

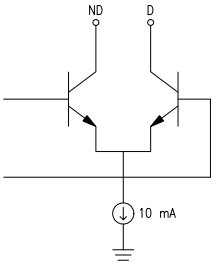
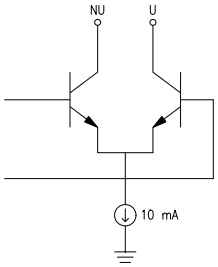
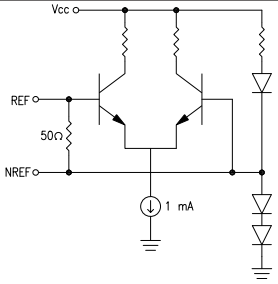
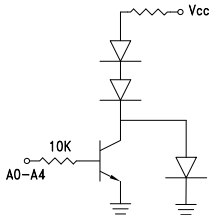
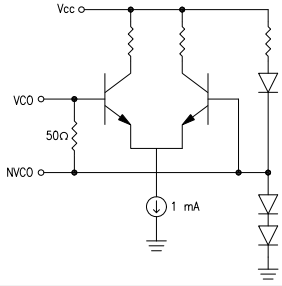
1. LEADFRAME MATERIAL: COPPER ALLOY
2. DIMENSIONS ARE IN INCHES [MILLIMETERS]
3. DIMENSION DOES NOT INCLUDE MOLDFLASH OF 0.15mm PER SIDE.
4. DIMENSION DOES NOT INCLUDE MOLDFLASH OF 0.25mm PER SIDE.
5. ALL GROUND LEADS AND GROUND PADDLE MUST BE SOLDERED TO PCB RF GROUND.

Package Information

Part Number	Package Body Material	Lead Finish	MSL Rating	Package Marking [3]
HMC440QS16G	Low Stress Injection Molded Plastic	Sn/Pb Solder	MSL1 [1]	H440 XXXX
HMC440QS16GE	RoHS-compliant Low Stress Injection Molded Plastic	100% matte Sn	MSL1 [2]	H440 XXXX

[1] Max peak reflow temperature of 235 °C
[2] Max peak reflow temperature of 260 °C
[3] 4-Digit lot number XXXX

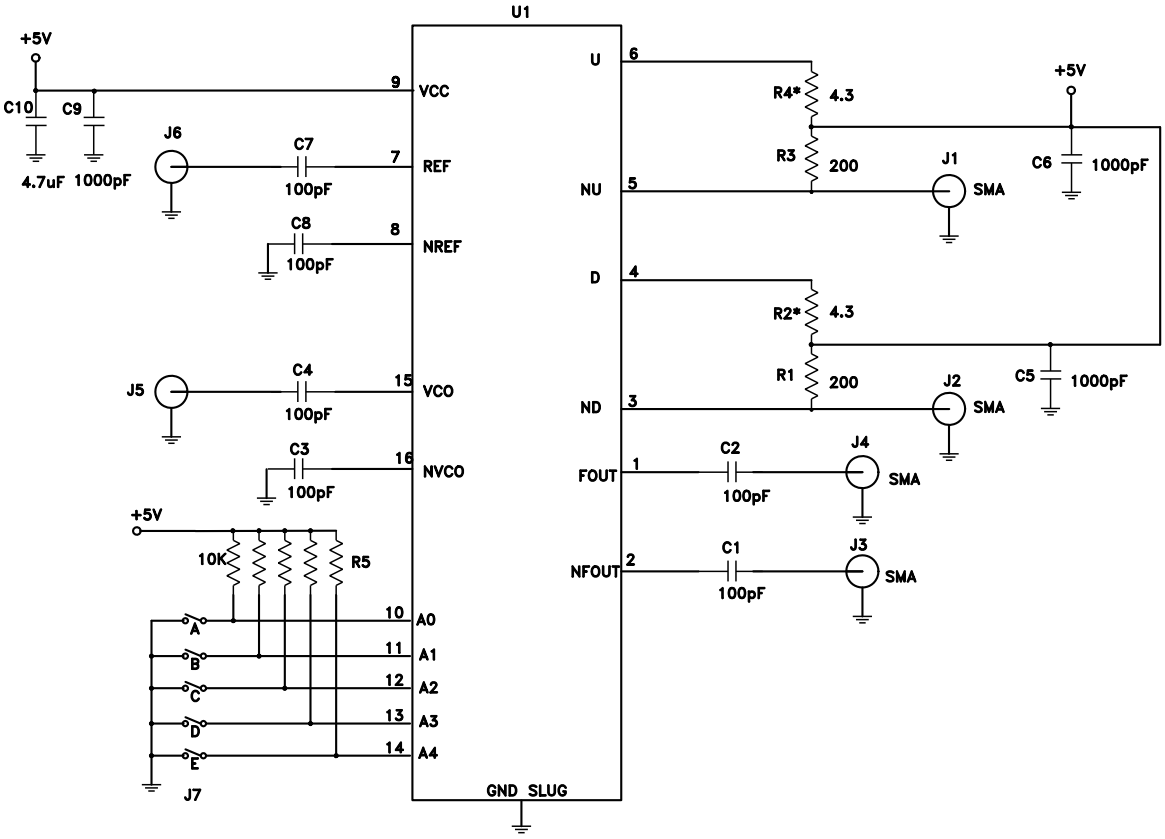
Pin Description

Pin Number	Function	Description	Interface Schematic
1 2	FOUT NFOUT	(These pins are DC coupled and must be DC blocked externally). Both outputs are test ports only and are intended for use with hi-impedance scope probes.	
3 4	ND D	Down Output Compliment Down Output	
5 6	NU U	Up Output Compliment Up Output	
7 8	REF NREF	(These pins are AC coupled and must be DC blocked externally.) Reference Input Reference Input Compliment	
9	Vcc	Supply voltage 5V ± 0.2V	
10 - 14	A0 - A4	CMOS compatible control input bit 0 (LSB) - 4.	
15 16	VCO NVCO	(These pins are AC coupled and must be DC blocked externally.) VCO Input VCO Input Compliment	

HMC440QS16G Programming Truth Table

Function	(LSB) A0	A1	A2	A3	A4
Output Low	0	0	0	0	0
/ 2	1	0	0	0	0
/ 3	0	1	0	0	0
/ 4	1	1	0	0	0
-	-	-	-	-	-
/ 32	1	1	1	1	1
Note: A0 through A4 are CMOS compatible logic control inputs.					

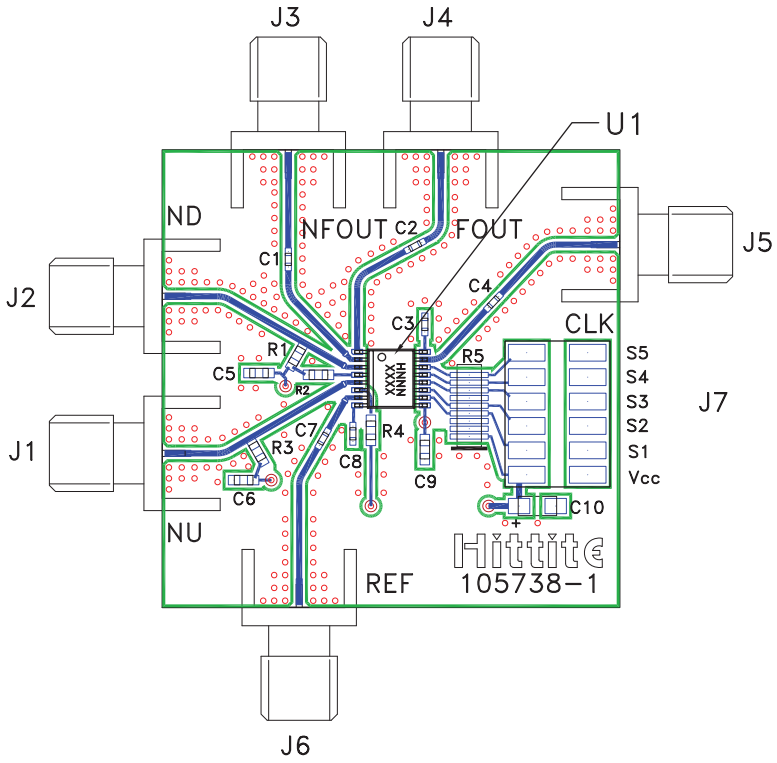
Evaluation PCB Circuit



* Choose values of R2 & R4 between 4.3 and 20 Ohms for best noise performance.

For price, delivery, and to place orders, please contact Hittite Microwave Corporation:
20 Alpha Road, Chelmsford, MA 01824 Phone: 978-250-3343 Fax: 978-250-3373
Order On-line at www.hittite.com

Evaluation PCB



The circuit board used in the final application should use RF circuit design techniques. Signal lines should have 50 ohm impedance while the package ground leads and backside ground slug should be connected directly to the ground plane similar to that shown. A sufficient number of via holes should be used to connect the top and bottom ground planes. The evaluation circuit board shown is available from Hittite upon request.

List of Materials for Evaluation PCB 105811 [1]

Item	Description
J1 - J6	PC Mount SMA RF Connector
J7	2 mm DC Header
C1-C4, C7, C8	100 pF Capacitor, 0402 Pkg.
C5, C6, C9	1000 pF Capacitor, 0603 Pkg.
C10	4.7 µF Capacitor
R1, R3	200 Ohm Resistor, 0603 Pkg.
R2[3], R4 [3]	4.3 Ohm Resistor, 0603 Pkg.
R5	Resistor Network, 10k Ohm
U1	HMC440QS16G / HMC440QS16GE
PCB [2]	105738 Eval Board

[1] Reference this number when ordering complete evaluation PCB

[2] Circuit Board Material: Rogers 4350

[3] Choose values of R2 & R4 between 4.3 and 20 Ohms for best noise performance

Evaluation PCB Truth Table

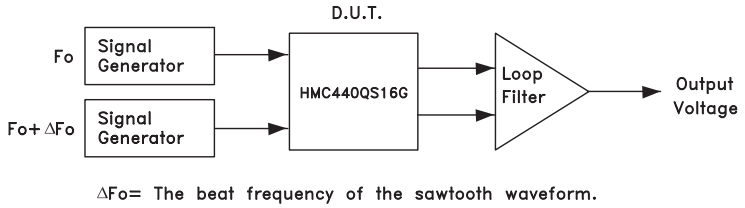
Function	S1	S2	S3	S4	S5
Output Low	0	0	0	0	0
/ 2	1	0	0	0	0
/ 3	0	1	0	0	0
/ 4	1	1	0	0	0
-	-	-	-	-	-
/ 32	1	1	1	1	1

Note: 0 = Jumper Installed.
1 = Jumper Not Installed.

Note: The evaluation PCB for the HMC440QS16G contains 10K Ohm pull up resistors for each of the five control inputs A0 through A4. Programming the 31 distinct division ratios consists of installing or removing jumpers S1 through S5, as shown below.

Gain & Error Voltage Test Circuit:

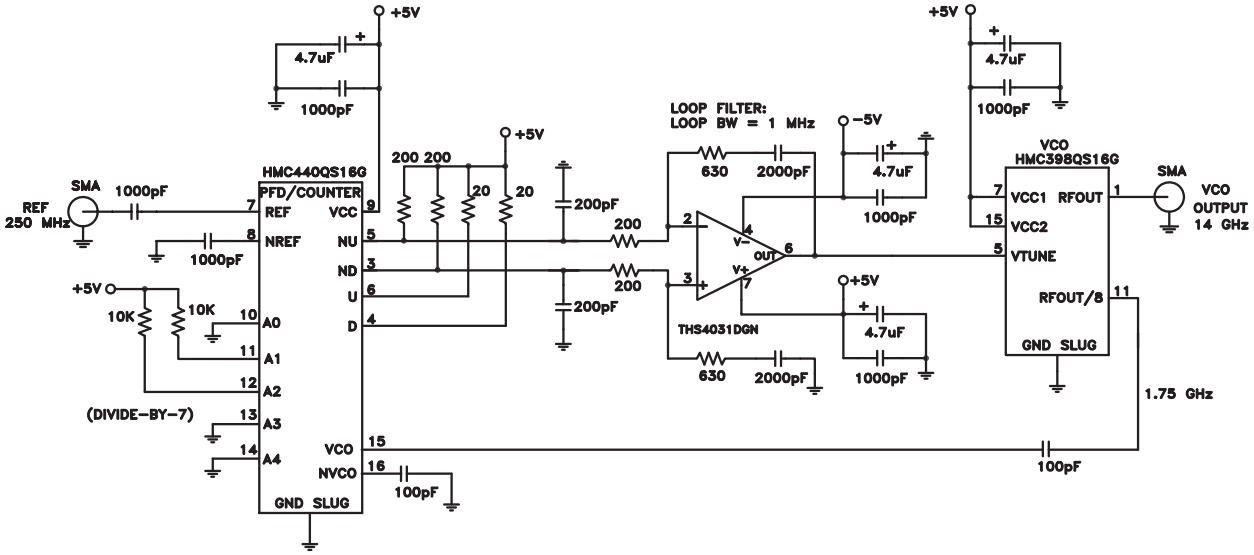
Gain & Error Voltage data taken using test circuit below. Loop filter gain has been subtracted from the result.



ΔFo= The beat frequency of the sawtooth waveform.

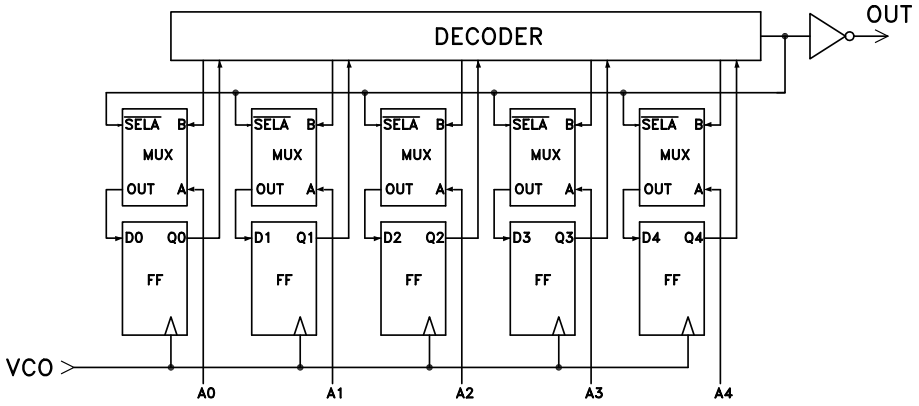
Typical PLL Application Circuit using HMC440QS16G

PLL application shown for a 14.0 GHz Fout. Contact HMC to discuss your specific application.



Applications Information

Simplified Block Diagram of 5-Bit Counter



Asynchronous Programming

The 5-Bit programmable counter counts-down from the programmed value of the data bits to zero and issues an output pulse at the end of each cycle. Settling time of the programmable 5-Bit counter is defined as the maximum time required for the counter to change the division ratio N to a new value after the data bits have settled. The worst case settling time occurs if the data bits A0 thru A4 are changing during the load cycle. Under this condition, the data bits may potentially be erroneous when they are clocked in and in the worst case could be all 1's, requiring 32 clock cycles until the correct data is re-loaded into the flip flops. The worst case asynchronous settling time can be calculated as follows:

$$T_{SETTLING\ MAX} = 32/f_{IN}$$ (For Asynchronous Programming)

As an example, if the input frequency is 1 GHz, the maximum settling time is 32 nS

Synchronous Programming

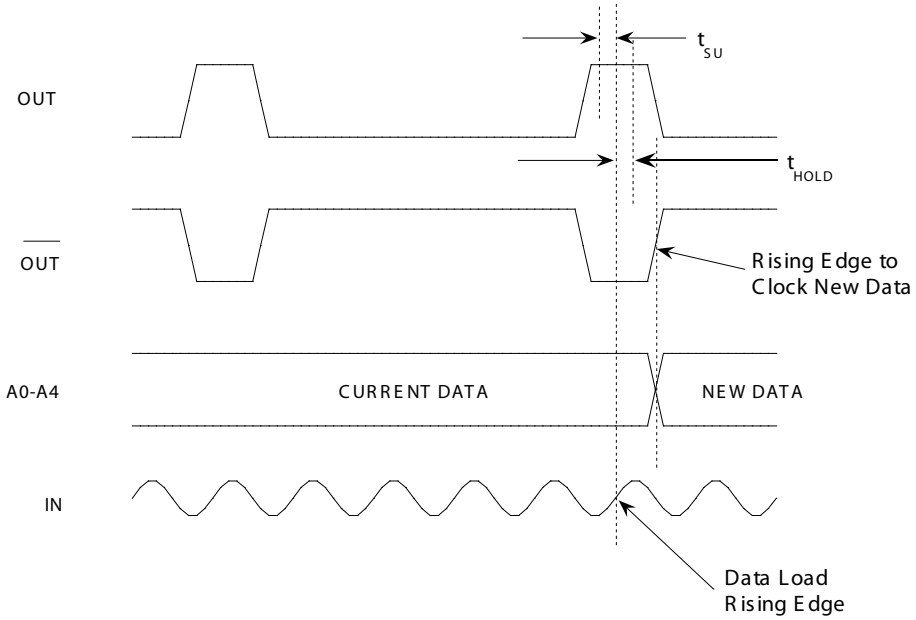
For applications which can not tolerate a momentary undefined division ratio, which normally occurs while changing the data bits (A0-A4) at random, synchronous programming can be used. Data is loaded into the counter on every rising edge of the clock which occurs while the output (OUT) is "HIGH". The typical minimum setup and hold times are shown in the table below as a function of frequency. For precision applications, the rising edge of the complementary output may be used to latch the new data bits (A0-A4), so that all bits are settled before the next load cycle.

$$T_{SETTLING\ MAX} = N/f_{IN}\ \text{(For Synchronous Programming)}$$

Where N is the desired division ratio, and f_{IN} = Input Frequency (Hz)

Parameter	0.5 GHz	1 GHz	2 GHz
t_{SETUP}	200 ps	200 ps	200 ps
t_{HOLD}	700 ps	300 ps	120 ps

Programmable Divider Timing Requirements for Synchronous Programming



CMOS/TTL Input Characteristics

Maximum Input Logic "0" Voltage ($V_{IL\ MAXIMUM}$) = 1.1V @ 1 µA.

Minimum Input Logic "1" Voltage ($V_{IH\ MINIMUM}$) = 1.8V @ 50 µA.

Input IV characteristics for the logic inputs (A0-A4) are shown below: