THCV219

V-by-One® HS High-speed video data transmitter

General Description

THCV219 is designed to support video data transmission between the host and display.

One high-speed lane can carry up to 32bit data and 3 bits of synchronizing signals at a pixel clock frequency from 7.5MHz to 75MHz.

It has one high-speed data lane and, maximum serial data rate is 3.0Gbps/lane.

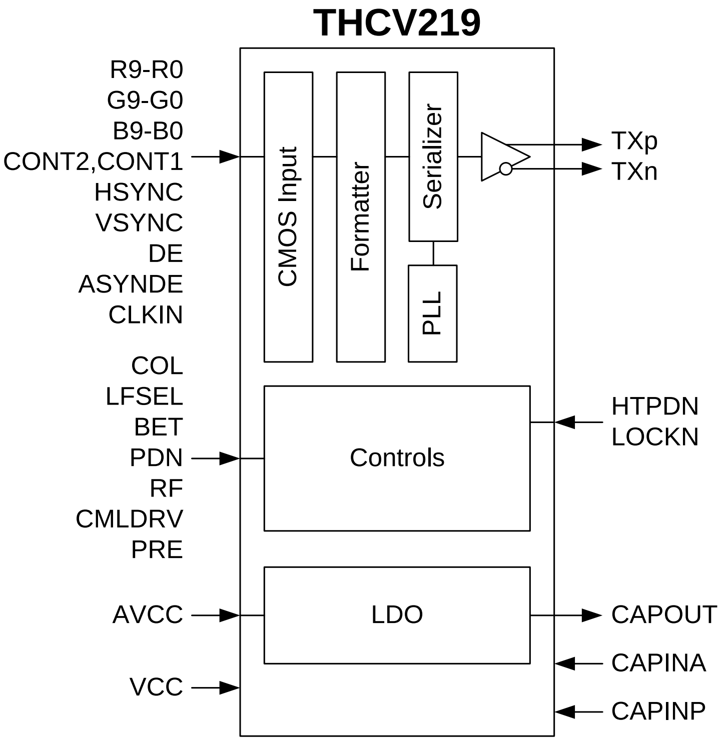
Width	Link	TTL Clock Freq.
24bit	Si/So	10MHz to 100MHz
32bit	Si/So	7.5MHz to 75MHz

Si/So : Single-in/Single-out,

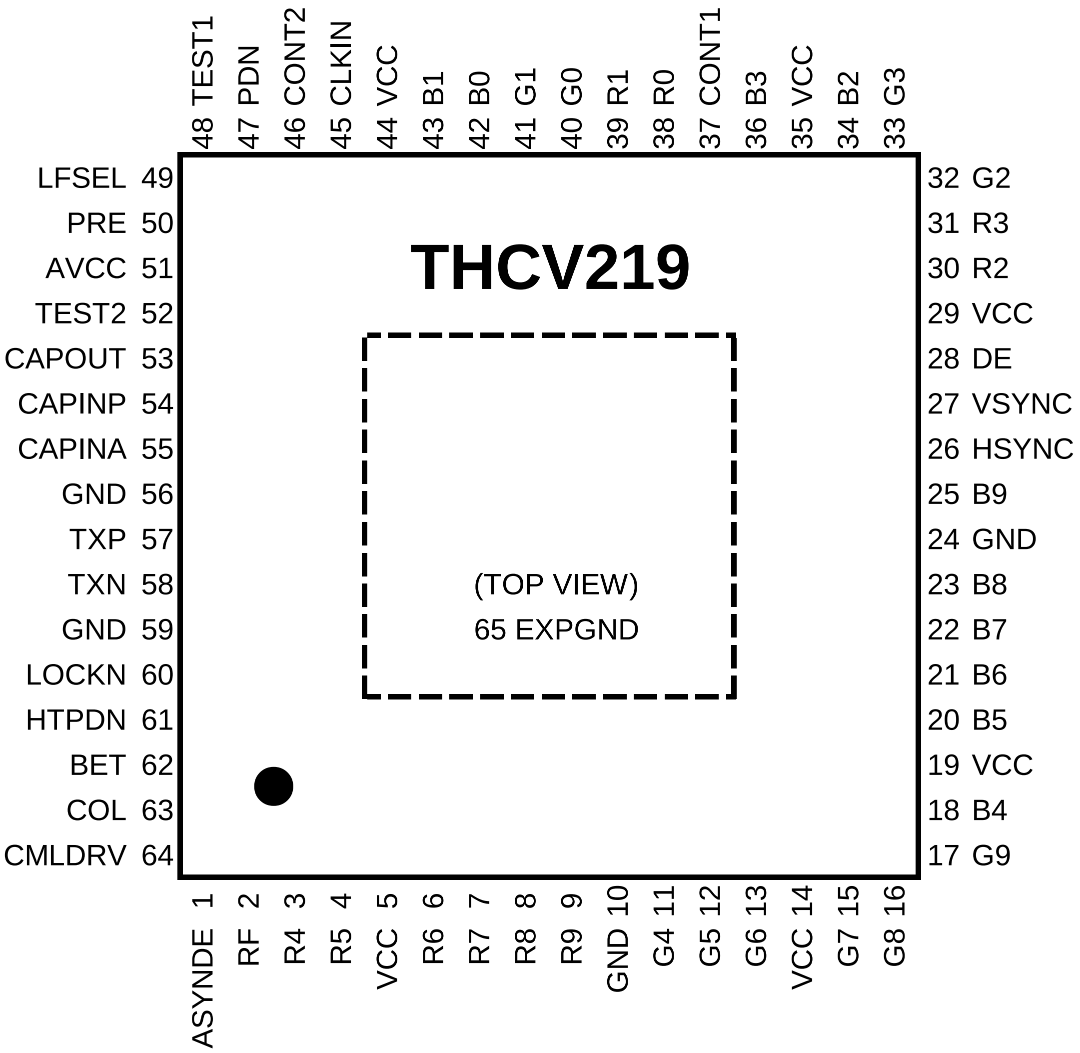
Features

- Color depth selectable: 24(8*3)/32(10*3)bit
- Single Link
- AC coupling for high speed lines
- Wide Range Supply Voltage 2.3~3.6V
- Package: 64 pin QFN
- Wide frequency range
- Spread Spectrum Clocking tolerant
  Up to 30kHz/±0.5% (center spread)
- V-by-One® HS standard Version1.4 compliant
- AEC-Q100 ESD Protection

Block Diagram



Pin configuration



Pin Description

Pin Name	Pin #	type*	Description
R9-R0	9,8,7,6,4, 3,31,30,39,38	I3	pixel data inputs
G9-G0	17,16,15,13,12, 11,33,32,41,40	I3	pixel data inputs
B9-B0	25,23,22,21,20, 18,36,34,43,42	I3	pixel data inputs
CONT1,2	37,46	I3	User defined data inputs. Active only in 32bit mode.
DE	28	I3	DE input
VSYNC	27	I3	Vsync input
HSYNC	26	I3	Hsync input
CLKIN	45	I3	Pixel clock input
TXN/P	58,57	CO	High-speed CML signal output.
LOCKN	60	I3L	Lock detect input. Must be connected to Rx LOCKN with a 10kΩ pull-up resistor.
HTPDN	61	I3L	Hot plug detect input. Must be connected to Rx HTPDN with a 10kΩ pull-up resistor.
PDN	47	I3L	Power down input. H: Normal operation L: Power down
PRE	50	I3	Pre-Emphasis level select input. H : Pre-Emphasis Enable L : Pre-Emphasis Disable
CMLDRV	64	I3	CML Outputs drive strength select input. H : Normal drive strength L : Weak drive strength
COL**	63	I3	Data width setting. H : 24bit L : 32bit
LFSEL**	49	I3	Frequency range setting. H: Low frequency operation L: Normal Operation
ASYNDE	1	I3	Asynchronous DE input. H: Normal operation (ASYNDE function disable) L: DE input invert operation (ASYNDE function enable)
RF	2	I3	Input clock triggering edge select input for latching input data H: Rising edge L: Falling edge
BET	62	I3	Field-BET entry. H : Field BET Operation L : Normal Operation
TEST1	48	-	Test pin, must be “L” for normal operation.
TEST2	52	-	Test pin, must be “L” for normal operation.
CAPOUT	53	-	Decoupling capacitor pins. This pin should be connected to external decoupling capacitors. Recommended Capacitance is 2.2uF
CAPINP	54	-	Reference Input for PLL circuit.Must be tied CAPOUT.
CAPINA	55	-	Reference Input for Analog circuit.Must be tied CAPOUT.
VCC	5,14,19,29, 35,44	PS	Digital Power supply Pins
AVCC	51	PS	Analog Power supply Pin
GND	10,24,56,59	PS	Ground Pins
EXPGND	65	PS	Exposed Pad Ground

*type symbol

I3=3.3v CMOS input, I3L=Low Speed 3.3v CMOS input

CO=CML output, PS=Power Supply

**COL, LFSEL pin

COL pin and/or LFSEL pin level shall not be changed during operation. If ether pin level is changed during operation, PDN shall be toggled (H-> L -> H) after the change.

Functional Description

Functional Overview

With V-by-One® HS proprietary encoding scheme and CDR (Clock and Data Recovery) architecture, THCV219 enables transmission of 8/10 bit RGB, 2bits of user-defined data (CONT), synchronizing signals HSYNC, VSYNC, and DE by a pair cable with minimal external components.

THCV219 inputs CMOS/TTL data (including video data, CONT, HSYNC, VSYNC, and DE) and serializes video data and synchronizing signals separately, depending on the polarity of DE. DE is a signal which indicates whether video or synchronizing data are active. When DE is high, it serializes video data inputs into differential data streams. And it transmits serialized synchronizing data when DE is low.

THCV219 can operate for a wide range of a serial bit rate from 600Mbps to 3.0Gbps.
It does not need any external frequency reference, such as a crystal oscillator.

Internal Reference Output/Input Function (CAPOUT,CAPINA,CAPINP)

An internal regulator produces the 1.2V (CAPOUT). This 1.2V linear regulator can not supply any other external loads. Bypass CAPOUT to GND with 2.2uF.

CAPINP supplies reference voltage for internal PLL, and CAPINA supplies reference voltage for any internal analog circuit. Bypass CAPINP/CAPINA to GND with 0.1uF to remove high frequency noise. CAPOUT, CAPINA and CAPINP must be tied together.

Analog power supply AVCC is supposed to be stabilized with de-coupling capacitor and series noise filter (for example, ferrite bead).

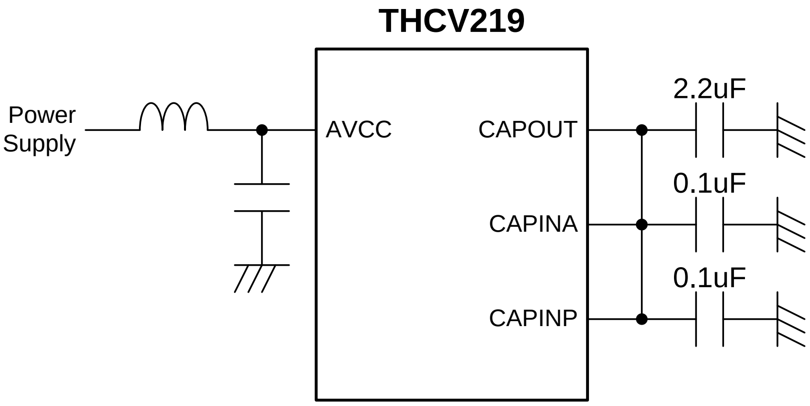
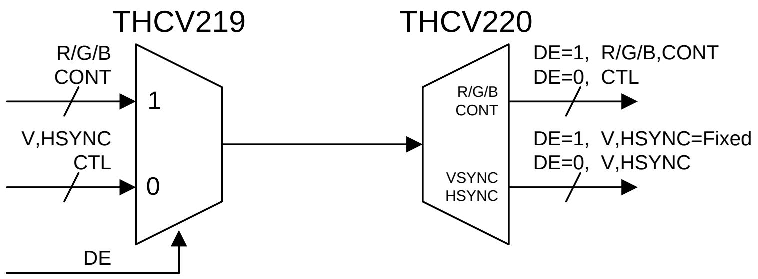


Figure 1. Connection of CAPOUT, CAPINA, CAPINP and Decoupling Capacitor

Data Enable

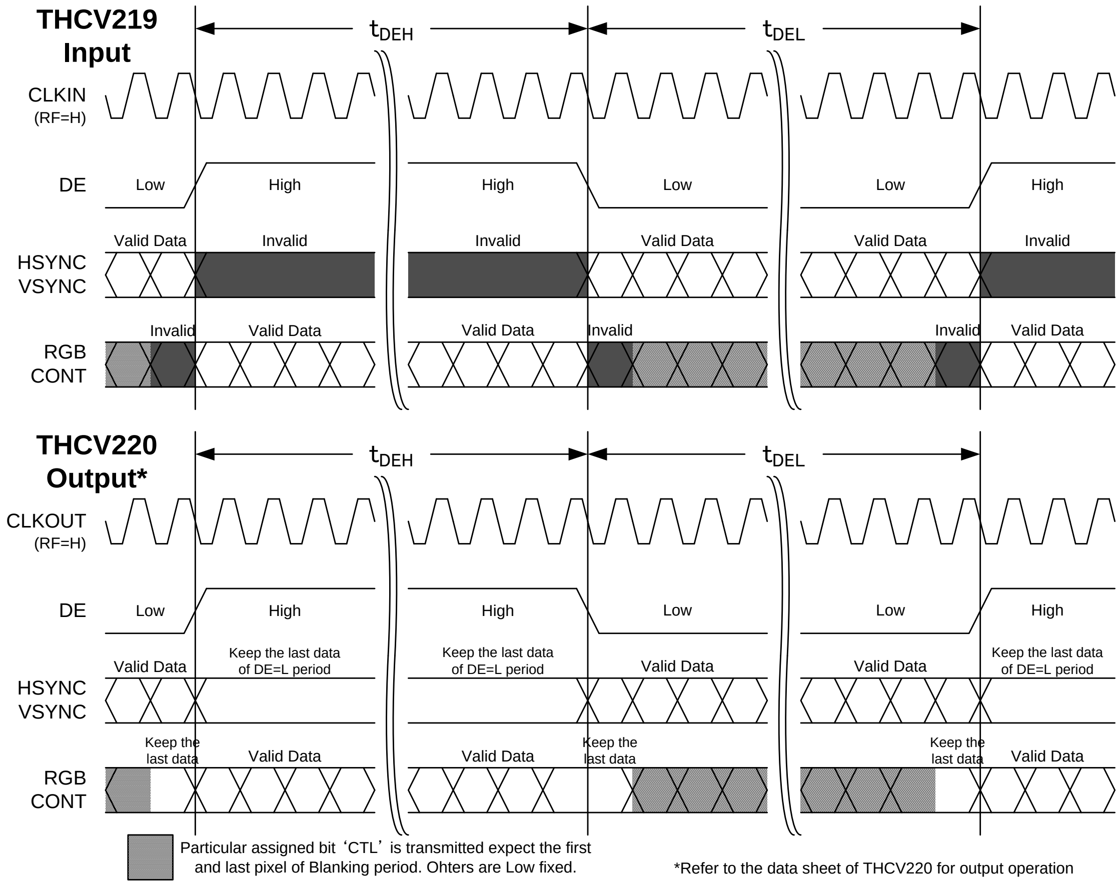
Figure 2 is the conceptual diagram of the basic operation of the chipset.THCV220 in Figure 2 is an example of V-by-One® HS Receiver.

There are some requirements for DE. Figure 3 shows the timing diagram of it.



CTL are particular assigned bit among R/G/B,CONT
that can carry arbitrary data during DE=0 period.

Figure 2. Conceptual diagram of the basic operation of the chipset



▨ Particular assigned bit ‘CTL’ is transmitted expect the first and last pixel of Blanking period. Ohters are Low fixed.

*Refer to the data sheet of THCV220 for output operation

Figure 3. Data and synchronizing signals transmission timing diagram

Table 1. DE requirement

symbol	Parameter	min.	typ.	max.	Unit
tDEH	DE=High Duration	2tTCIP			sec
tDEL	DE=Low Duration	2tTCIP			sec

ASYNDE

If ASYNDE input is Low, DE input is inverted before V-by-One® HS processing. RGB/CONT Data is transmitted during DE input=Low. Please be careful this inverted DE is outputted from V-by-One® HS receiver, which may cause polarity mismatch against following system requirement.

Color Depth and Frequency Range Select function

THCV219 supports a variety of data width and frequency range. Refer to Table 2 for details.

COL pin and/or LFSEL pin level shall not be changed during operation. If ether pin level is changed during operation, PDN shall be toggled (H-> L -> H) after the change.

Table 2. operation mode select

COL	LFSEL	Description	Freq. Range
L	L	32bit	15 to 75M
	H	32bit Low frequency mode	7.5 to 30M
H	L	24bit	20 to 100M
	H	24bit Low frequency mode	10 to 40M

Hot-Plug Function

HTPDN indicates connecting condition between the Transmitter and the Receiver. HTPDN of the transmitter side is high when the Receiver is not active or not connected. Then Transmitter can enter into the power down mode. HTPDN is set to Low by the Receiver when Receiver is active and connects to the Transmitter, and then Transmitter must start up and transmit CDR training pattern for link training. HTPDN is open drain output at the receiver side. Pull-up resistor is needed at the transmitter side.

HTPDN connection between the Transmitter and the Receiver can be omitted as an application option. In this case, HTPDN at the Transmitter side should always be taken as Low.

Lock Detect Function

LOCKN indicates whether the CDR PLL is in the lock state or not. LOCKN at the Transmitter input is set to High by pull-up resistor when Receiver is not active or at the CDR PLL training state. LOCKN is set to Low by the Receiver when CDR lock is done. Then the CDR training mode finishes and Transmitter shifts to the normal mode. LOCKN is open drain output at the receiver side. Pull-up resistor is needed at the transmitter side.

When HTPDN is included in an application, the LOCKN signal should only be considered when the HTPDN is pulled low by the Receiver.

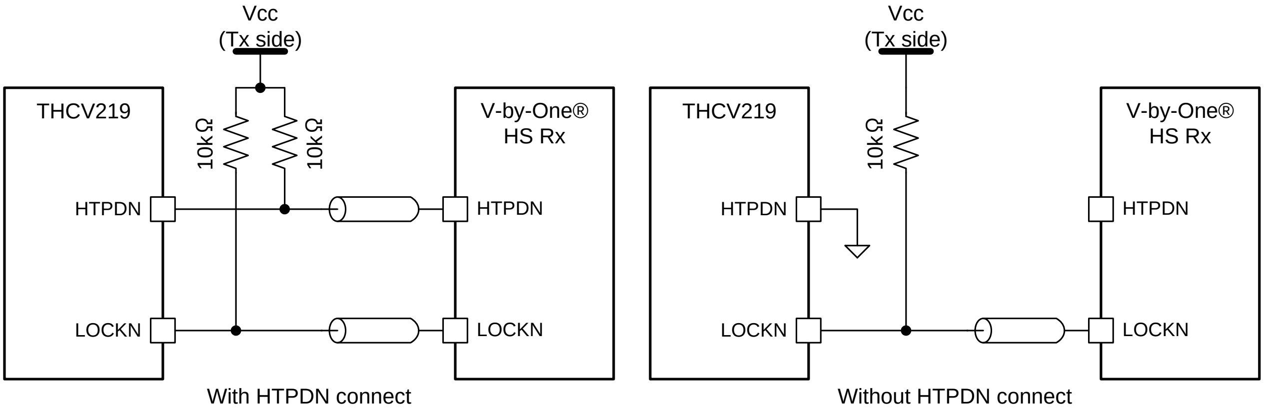


Figure 4. Hot-plug and Lock detect scheme

Pre-emphasis and Drive Select Function

Pre-emphasis can equalize severe signal degradation caused by long-distance or high-speed transmission. The PRE pin selects the strength of pre-emphasis.

CMLDRV controls CML output swing level. See Table 3.

Table 3. Pre-emphasis and Drive Select function table

PRE	CMLDRV	Description	
		Swing level	Pre-emphasis
L	L	400mV diff p-p	0dB
	H	600mV diff p-p	
H	L	400mV diff p-p	6dB
	H	600mV diff p-p	3.5dB

Power Down Function

Setting the PDN pin low places THCV219 in the power-down mode. Internal circuitry turns off and the TXP/N outputs turn to High level.

Table 4. Power Down function table

PDN	Description
L	Power Down
H	Normal Operation

Field BET Operation

In order to help users to check validity of CML high-speed serial line, THCV219 has an operation mode in which they act as a bit error tester (BET). In this mode, THCV219 internally generates test pattern which is then serialized onto the CML high-speed line. THCV220 which is an example or Rx device also has BET function mode. THCV220 receives the data stream and checks bit errors.

This "Field BET" mode is activated by setting BET= H both on THCV219 andTHCV220. The generated data pattern is then 8b/10b encoded, scrambled, and serialized onto the CML channel. As for THCV220, the internal test pattern check circuit gets enabled and reports result on a certain pin named BETOUT. The BETOUT pin goes LOW whenever bit errors occur, or it stays HIGH when there is no bit error. Please refer to Table 5.

Table 5. Field BET operation pin settings

THCV219	THCV220	Condition
BET	BET	
L	L	Normal Operation
H	H	Field BET Operation

Table 6. THCV220 Field BET result

BETOUT	Output
L	Bit error occurred
H	No error

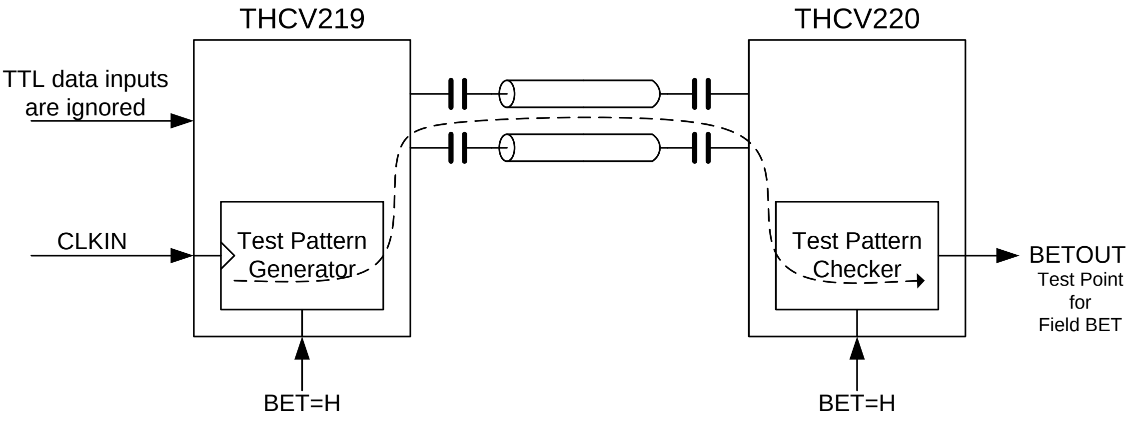


Figure 5. Field BET Configuration

Absolute Maximum Ratings*

Parameter	min.	typ.	max.	Unit
Supply Voltage(VCC,AVCC)	-0.3	-	+4.0	V
CMOS Input Voltage	-0.3	-	VCC+0.3	V
CML Transmitter Output Voltage	-0.3	-	CAPINA+0.3	V
Output Current	-30	-	30	mA
Storage Temperature	-55	-	+125	℃
Junction Temperature	-	-	+125	℃
Reflow Peak Temperature/Time	-	-	+260/10sec	℃
Maximum Power Dissipation @+25℃	-	-	3.9	W
ESD Protection AEC-Q100-002(HBM)	-	+/-2	-	kV
ESD Protection AEC-Q100-003(MM)	-	+/-200	-	V
ESD Protection AEC-Q100-011(CDM) (Corner.750)	-	+/-500	-	V

[*] “Absolute Maximum Ratings” are those values beyond which the safety of the device can not be guaranteed. They are not meant to imply that the device should be operated at these limits. The tables of “Electrical Characteristics” specify conditions for device operation.

Recommended Operating Conditions

Parameter	min.	typ.	max.	Unit
Supply Voltage（VCC,AVCC）	2.3	2.5	2.7	V
	2.6	2.8	3.0	V
	3.0	3.3	3.6	V
Operating Temperature	-40		85	℃

Electrical Specifications

CMOS DC Specifications

Over recommended operating supply and temperature ranges unless otherwise specified.

symbol	Parameter	conditions	min.	typ.	max.	Unit
IIH	Input Leak Current High		-10		+10	uA
IIL	Input Leak Current Low		-10		+10	uA
VCAPOUT	Regulator output Voltage			1.20		V

VCC=3.3±0.3V

symbol	Parameter	conditions	min.	typ.	max.	Unit
VIH	High Level Input Voltage	I3	2.0		VCC	V
		I3L	2.1		VCC	V
VIL	Low Level Input Voltage	I3	0		0.8	V
		I3L	0		0.7	V

VCC=2.8±0.2V

symbol	Parameter	conditions	min.	typ.	max.	Unit
VIH	High Level Input Voltage	I3	1.8		VCC	V
		I3L	1.9		VCC	V
VIL	Low Level Input Voltage	I3	0		0.7	V
		I3L	0		0.6	V

VCC=2.5±0.2V

symbol	Parameter	conditions	min.	typ.	max.	Unit
VIH	High Level Input Voltage	I3	1.7		VCC	V
		I3L	1.6		VCC	V
VIL	Low Level Input Voltage	I3	0		0.7	V
		I3L	0		0.5	V

CML DC Specifications

Over recommended operating supply and temperature ranges unless otherwise specified.

symbol	Parameter	conditions	min.	typ.	max.	Unit
VTOD	CML Differential Mode Output Voltage	CMLDRV=L	133	200	267	mV
		CMLDRV=H	200	300	400	mV
PRE	CML Pre-emphasis Level	PRE=L		0		%
		PRE=H, CMLDRV=L		100		%
		PRE=H, CMLDRV=H		50		%
VTOC	CML Common Mode Output Voltage	PRE=L		1.2 - VTOD		V
		PRE=H, CMLDRV=L		1.2 - 2 * VTOD		V
		PRE=H, CMLDRV=H		1.2 - 1.5 * VTOD		V
ITOH	CML Output Leak Current High	PDN=L, TXP/N=1.2V			±30	uA
ITOS	CML Output Short Circuit Current	PDN=L, TXP/N=0V	-80			mA

Supply Currents

Over recommended operating supply and temperature ranges unless otherwise specified.

symbol	Parameter	conditions	min.	typ.	max.	Unit
ITCCW	Transmitter Supply Current	COL=L PRE=H			100	mA
ITCCS	Transmitter Power Down Supply Current	PDN=L All Inputs =Fixed LorH		1.2	10	mA

Switching Characteristics

Over recommended operating supply and temperature ranges unless otherwise specified.

symbol	Parameter	conditions	min.	typ.	max.	Unit
tTRF	CML Output Rise and Fall Time(20%-80%)		50		150	ps
tTCIP	CLKIN Period	COL=H, LFSEL=L	10		50	ns
		COL=H, LFSEL=H	25		100	ns
		COL=L, LFSEL=L	13.34		66.66	ns
		COL=L, LFSEL=H	33.34		133.33	ns
tTCH	CLK IN High Time		0.35tTCIP	0.5tTCIP	0.65tTCIP	ns
tTCL	CLK IN Low Time		0.35tTCIP	0.5tTCIP	0.65tTCIP	ns
tTS	TTL Data Setup to CLK IN		2.0			ns
tTH	TTL Data Hold to CLK IN		0.6			ns
tTCD	Input Clock to Output Data Delay	COL=H	typ. - tTCIP	10.6tTCIP+1.7	typ. + tTCIP	ns
		COL=L	typ. - tTCIP	9.8tTCIP+1.7	typ. + tTCIP	ns
tTPD	Power On to PDN High Delay		0			ns
tTPLL0	PDN High to CML Output Delay				10	ms
tTPLL1	PDN Low to CML Output High Fix Delay				20	ns
tTNP0	LOCKN High to Training Pattern Output Delay				10	ms
tTNP1	LOCKN Low to Data Pattern Output Delay				10	ms

AC Timing Diagrams and Test Circuits

CMOS/TTL Input Switching Characteristics

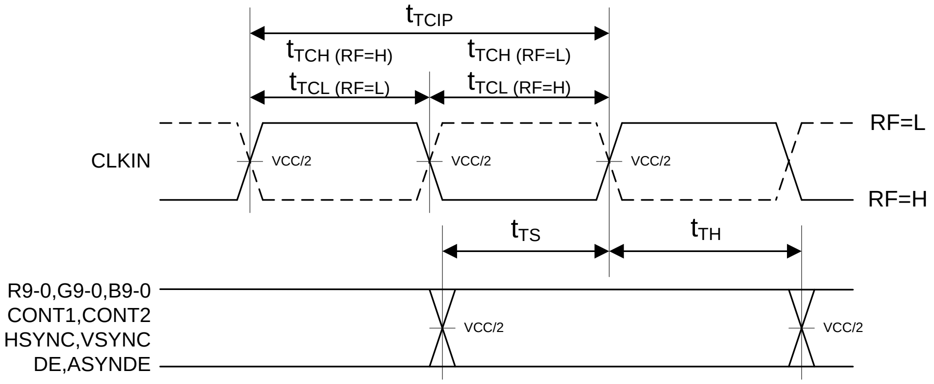
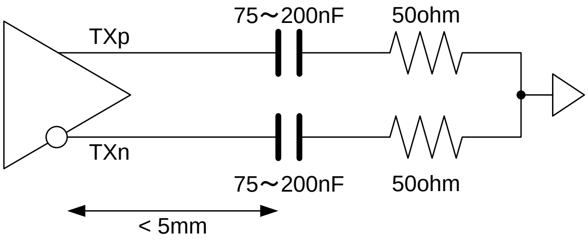


Figure 6. CMOS/TTL Input Switching Timing Diagrams

CML Output Switching Characteristics



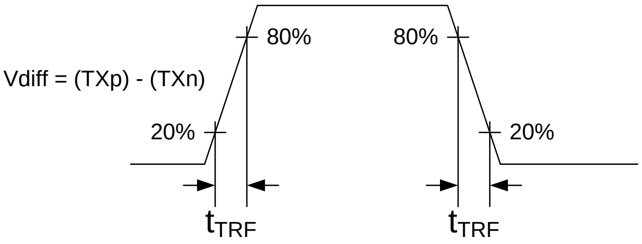


Figure 7. CML buffer Switching Timing Diagrams and Test Circuit

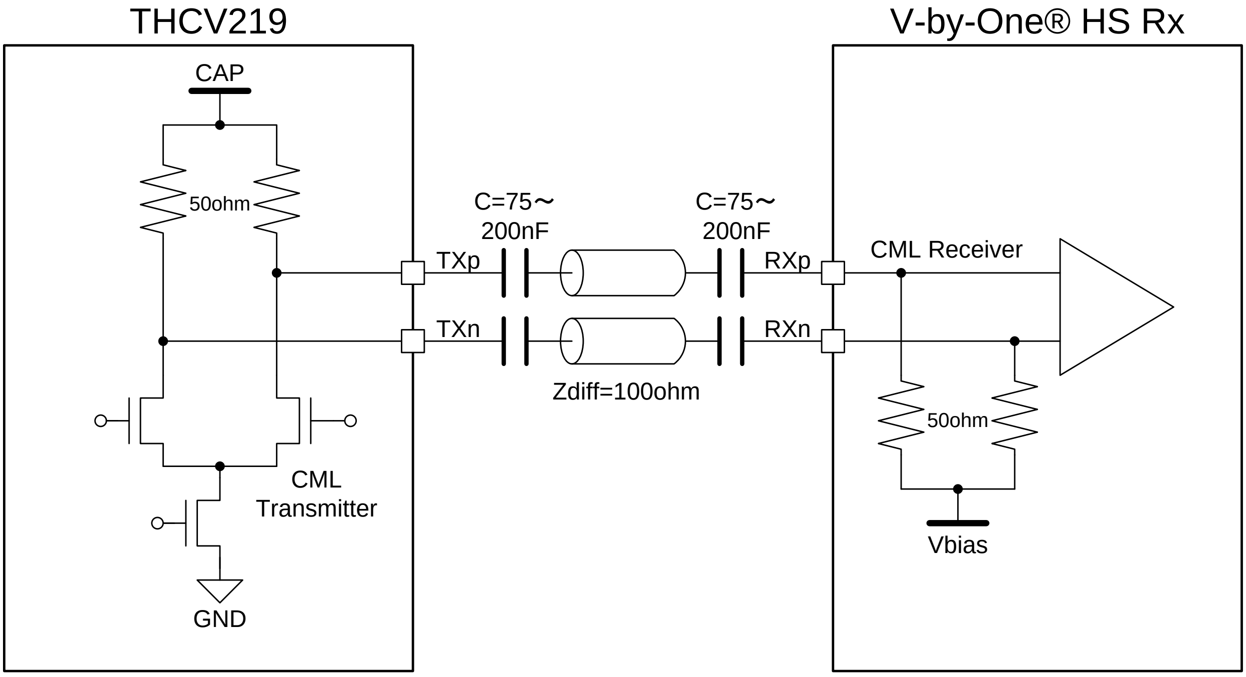


Figure 8. CML buffer scheme

Latency Characteristics

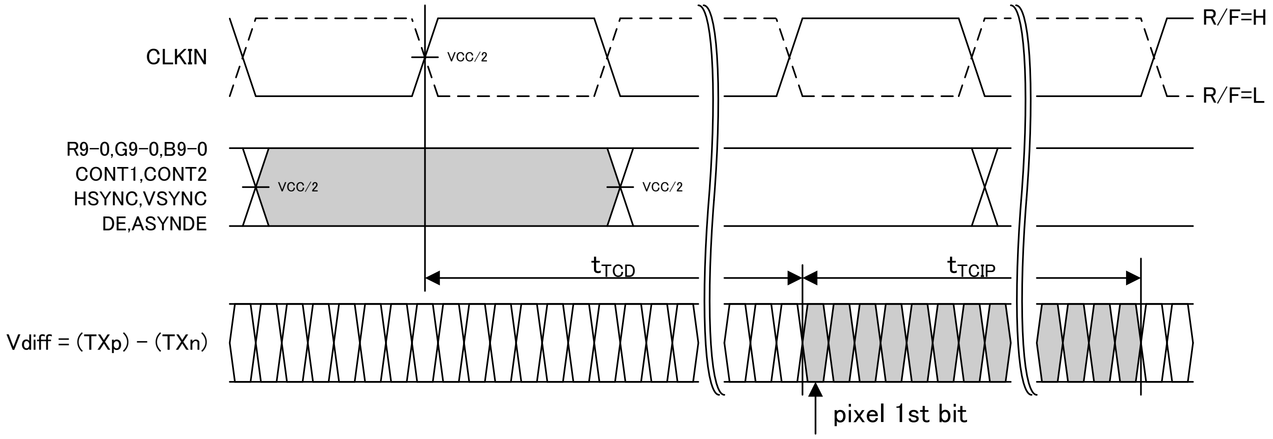


Figure 9. THCV219 Latency

Data output Sequence

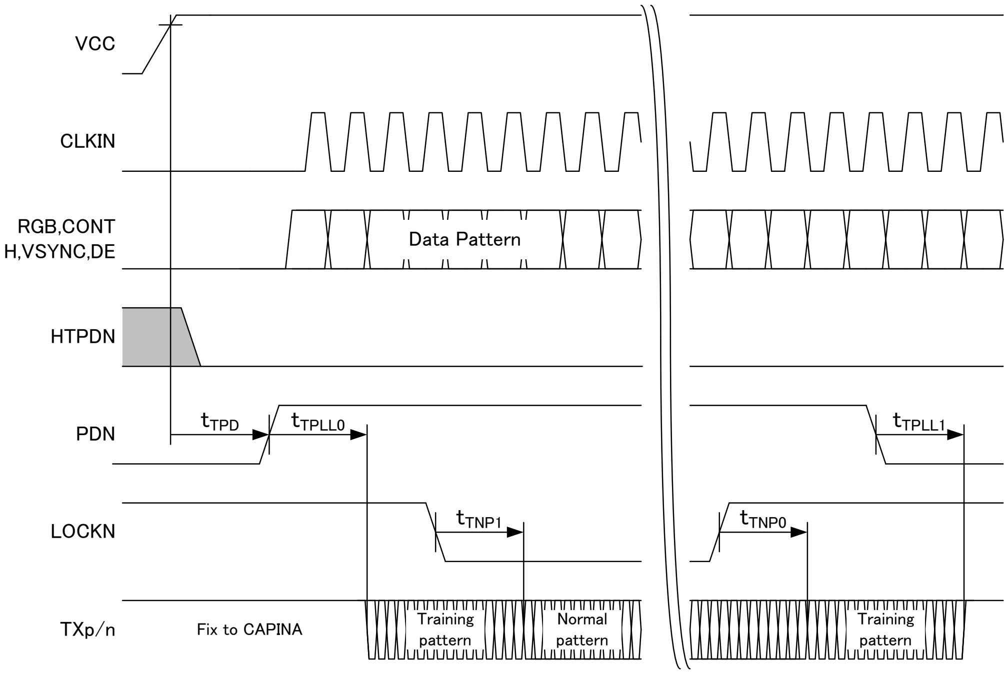


Figure 10. THCV219 Sequence

Input Data Mapping

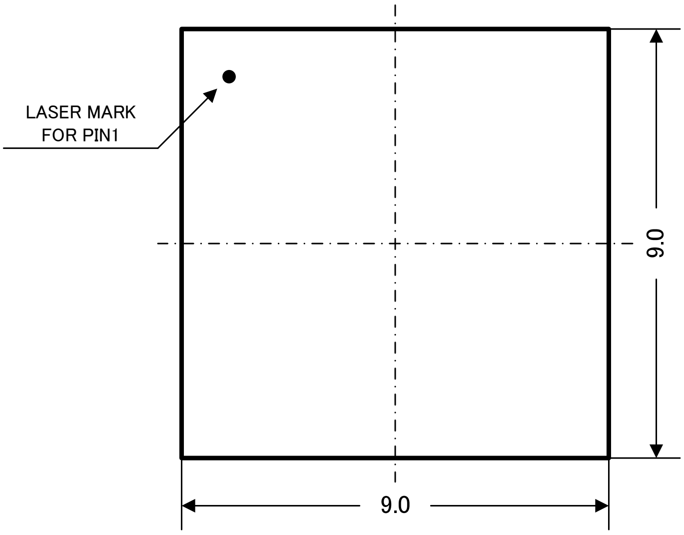
Table 7. CMOS/TTL Input Data Mapping

Data Signals		Transmitter Input Pin Name	
10bit (30bpp)	8bit (24bpp)	10bit (30bpp)	8bit (24bpp)
R0 *1	-	R0	-
R1 *1	-	R1	-
R2	R0	R2	R2
R3	R1	R3	R3
R4	R2	R4	R4
R5	R3	R5	R5
R6	R4	R6	R6
R7	R5	R7	R7
R8	R6	R8	R8
R9	R7	R9	R9
G0 *1	-	G0	-
G1 *1	-	G1	-
G2	G0	G2	G2
G3	G1	G3	G3
G4	G2	G4	G4
G5	G3	G5	G5
G6	G4	G6	G6
G7	G5	G7	G7
G8	G6	G8	G8
G9	G7	G9	G9
B0 *1	-	B0	-
B1 *1	-	B1	-
B2 *1	B0 *1	B2	B2
B3 *1	B1 *1	B3	B3
B4 *1	B2 *1	B4	B4
B5 *1	B3 *1	B5	B5
B6 *1	B4 *1	B6	B6
B7 *1	B5 *1	B7	B7
B8 *1	B6 *1	B8	B8
B9 *1	B7 *1	B9	B9
CONT1 *1	-	CONT1	-
CONT2 *1	-	CONT2	-
HSYNC	HSYNC	HSYNC	HSYNC
VSYNC	VSYNC	VSYNC	VSYNC
DE	DE	DE	DE

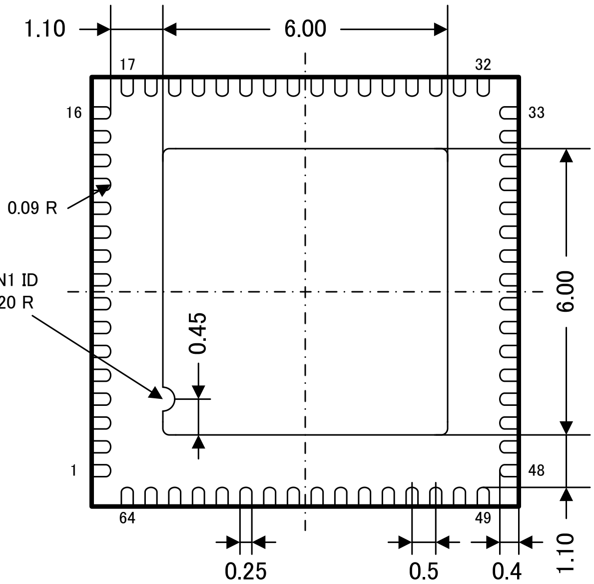
*1 CTL bits, which are carried during DE=Low except the 1st and the last pixel.

Package

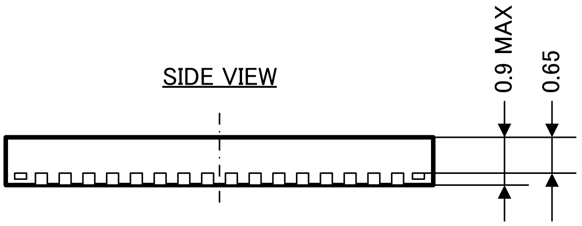
TOP VIEW



BOTTOM VIEW



SIDE VIEW



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1. The product specifications described in this material are subject to change without prior notice.

2. The circuit diagrams described in this material are examples of the application which may not always apply to the customer's design. We are not responsible for possible errors and omissions in this material. Please note if errors or omissions should be found in this material, we may not be able to correct them immediately.

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5. Product Application
   5.1 Application of this product is intended for and limited to the following applications: audio-video device, office automation device, communication device, consumer electronics, smartphone, feature phone, and amusement machine device. This product must not be used for applications that require extremely high-reliability/safety such as aerospace device, traffic device, transportation device, nuclear power control device, combustion chamber device, medical device related to critical care, or any kind of safety device.
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6. Despite our utmost efforts to improve the quality and reliability of the product, faults will occur with a certain small probability, which is inevitable to a semi-conductor product. Therefore, you are encouraged to have sufficiently redundant or error preventive design applied to the use of the product so as not to have our product cause any social or public damage.

7. Please note that this product is not designed to be radiation-proof.

8. Testing and other quality control techniques are used to this product to the extent THine deems necessary to support warranty for performance of this product. Except where mandated by applicable law or deemed necessary by THine based on the user's request, testing of all functions and performance of the product is not necessarily performed.

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10. The product or peripheral parts may be damaged by a surge in voltage over the absolute maximum ratings or malfunction, if pins of the product are shorted by such as foreign substance. The damages may cause a smoking and ignition. Therefore, you are encouraged to implement safety measures by adding protection devices, such as fuses.

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