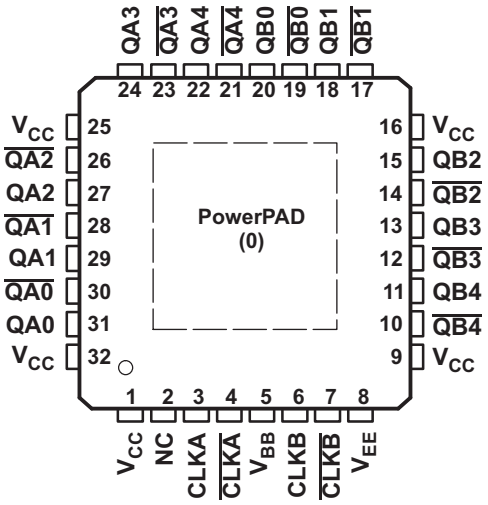
LOW-VOLTAGE DUAL DIFFERENTIAL 1:5 LVPECL CLOCK DRIVER

Check for Samples: CDCLVP215

FEATURES

- **2× One Differential Clock Input Pair LVPECL to 5 Differential LVPECL Clock Outputs**
- **Fully Compatible With LVPECL/LVECL**
- **Supports a Wide Supply Voltage Range From 2.375 V to 3.8 V**
- **Open Input Default State**
- **Low-Output Skew (Typ 15 ps) for Clock-Distribution Applications**
- **V_{BB} Reference Voltage Output for Single-Ended Clocking**
- **Available in the QFN32 Package**
- **Frequency Range From DC to 3.5 GHz**
- **Pin-to-Pin Compatible With the MC100 Series EP111, LVEP210, ES6111, LVEP111**

QFN32 PACKAGE
(TOP VIEW)



APPLICATIONS

- **Designed for Driving 50-Ω Transmission Lines**
- **High Performance Clock Distribution**

DESCRIPTION

The CDCLVP215 clock driver distributes two times one differential clock pair of LVPECL, (CLKA, CLKB) to 5 pairs of differential LVPECL clock (QA0..QA4, QB0..QB4) outputs with minimum skew for clock distribution. The CDCLVP215 specifies low output-to-output skew. The CDCLVP215 is specifically designed for driving 50-Ω transmission lines. When an output pair is not used, leaving it open is recommended to reduce power consumption. If only one of the output pairs is used, the other output pair must be identically terminated to 50 Ω.

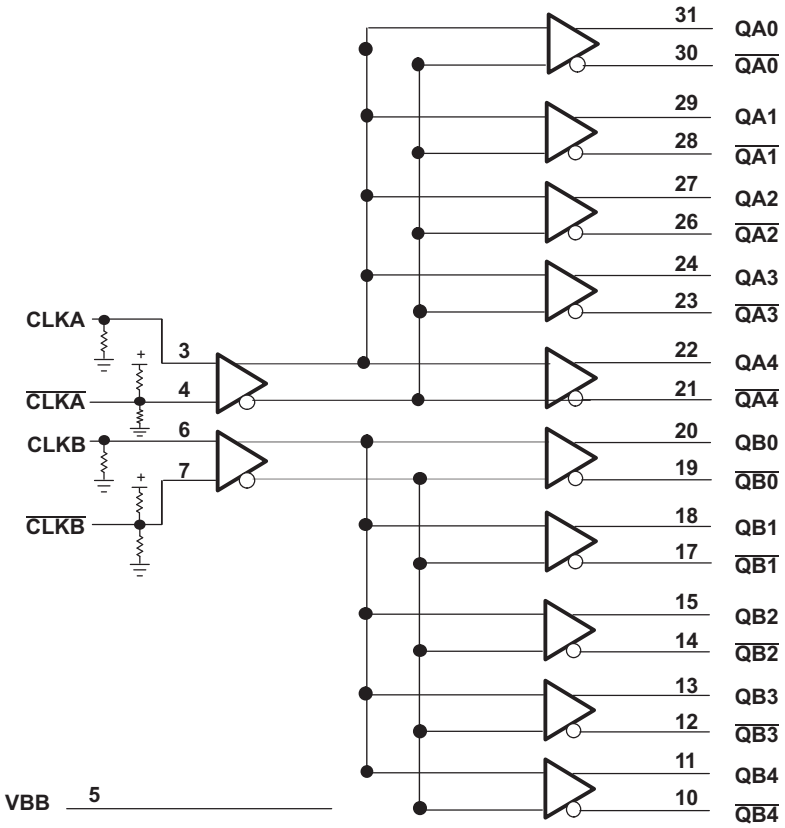
The V_{BB} reference voltage output is used if single-ended input operation is required. In this case, the V_{BB} pin should be connected to $\overline{CLKA}$ or $\overline{CLKB}$ and bypassed to GND via a 10-nF capacitor.

However, for high-speed performance up to 3.5 GHz, the differential mode is strongly recommended.

The CDCLVP215 is characterized for operation from –40°C to 85°C.

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.



PIN FUNCTIONS

PIN		DESCRIPTION
NAME	NO.	
NC	2	Not connected
CLKA, $\overline{\text{CLKA}}$	3, 4	Differential LVECL/LVPECL input pair
CLKB, $\overline{\text{CLKB}}$	6, 7	Differential LVECL/LVPECL input pair
Q [A0:A4]	22, 24, 27, 29, 31	LVECL/LVPECL clock outputs, these outputs provide low-skew copies of CLKA.
$\overline{\text{Q}}$ [A0:A4]	21,23, 26, 28, 30	LVECL/LVPECL complementary clock outputs, these outputs provide low-skew copies of $\overline{\text{CLKA}}$.
Q [B0:B4]	11, 13, 15, 18, 20	LVECL/LVPECL clock outputs, these outputs provide low-skew copies of CLKB.
$\overline{\text{Q}}$ [B0:B4]	10, 12, 14, 17, 19	LVECL/LVPECL complementary clock outputs, these outputs provide low-skew copies of $\overline{\text{CLKB}}$.
V_{BB}	5	Reference voltage output for single-ended input operation
V_{CC}	1, 9, 16, 25, 32	Supply voltage
V_{EE}	8	Device ground or negative supply voltage in ECL mode
PowerPAD™	0	The PowerPAD of the QFN32 package is thermally connected to the die to improve the heat transfer out of the package. This pad is connected to V_{EE}.

- CLKn pull down resistor 75 kΩ
- $\overline{\text{CLKn}}$ pull up resistor 37.5 kΩ
- $\overline{\text{CLKn}}$ pull down resistor 50 kΩ

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted)

		VALUE	UNIT
V_{CC}	Supply voltage (relative to V_{EE})	–0.3 to 4.6	V
V_I	Input voltage	–0.3 to V_{CC} + 0.5	V
V_O	Output voltage	–0.3 to V_{CC} + 0.5	V
I_{IN}	Input current	±20	mA
V_{EE}	Negative supply voltage (relative to V_{CC})	-4.6 to 0.3	V
I_{BB}	Sink/source current	–1 to 1	mA
I_O	DC output current	–50	mA
T_{stg}	Storage temperature range	–65 to 150	°C

RECOMMENDED OPERATING CONDITIONS

		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage (relative to V_{EE})	2.375	2.5/3.3	3.8	V
T_A	Operating free-air temperature	–40		85	°C

PACKAGE THERMAL IMPEDANCE

		TEST CONDITION	MIN	MAX	UNIT
θ_{JA}	Thermal resistance junction to ambient(1)	0 LFM		49	°C/W
		150 LFM		37	°C/W
		250 LFM		36	°C/W
		500 LFM		32	°C/W
θ_{JC}	Thermal resistance junction to case			19	°C/W

(1) According to JESD 51-7 standard.

LVECL DC ELECTRICAL CHARACTERISTICS

Vsupply: V_{CC} = 0 V, V_{EE} = –2.375 V to –3.8 V
over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
I_{EE}	Supply internal current	Absolute value of current	–40°C, 25°C, 85°C	40		90	mA
I_{CC}	Output and internal supply current	All outputs terminated 50 Ω to V_{CC} – 2 V	–40°C			354	mA
			25°C			380	
			85°C			405	
I_{IN}	Input current	Includes pullup/pulldown resistors V_{IH} = V_{CC}, V_{IL} = V_{CC} - 2 V	–40°C, 25°C, 85°C	–150		150	µA
V_{BB}	Internally generated bias voltage	For V_{EE} = –3 to –3.8 V, I_{BB} = –0.2 mA	–40°C, 25°C, 85°C	–1.45	–1.3	–1.15	V
		V_{EE} = –2.375 to –2.75 V, I_{BB} = –0.2 mA	–40°C, 25°C, 85°C	–1.4	–1.25	–1.1	
V_{ID}	Input amplitude (CLKn, $\overline{CLKn}$)	Difference of input | V_{IH} – V_{IL} | , See (1)	-40°C, 25°C, 85°C	0.5		1.3	V
V_{CM}	Common-mode voltage (CLKn, $\overline{CLKn}$)	DC offset relative to V_{EE}	-40°C, 25°C, 85°C	V_{EE} + 1		–0.3	V

(1) V_{ID} minimum and maximum is required to maintain ac specifications, actual device function tolerates a minimum V_{ID} of 100 mV.

LVECL DC ELECTRICAL CHARACTERISTICS (continued)

Vsupply: V_{CC} = 0 V, V_{EE} = –2.375 V to –3.8 V
over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{OH}	High-level output voltage	I_{OH} = –21 mA	–40°C	–1.26		–0.85	V
			25°C	–1.2		–0.85	
			85°C	–1.15		–0.85	
V_{OL}	Low-level output voltage	I_{OL} = –5 mA	–40°C	–1.85		–1.5	V
			25°C	–1.85		–1.45	
			85°C	–1.85		–1.4	
V_{OD}	Differential output voltage swing	Terminated with 50 Ω to V_{CC} – 2 V, See Figure 3	–40°C 25°C, 85°C	600			mV

LVPECL DC ELECTRICAL CHARACTERISTICS

Vsupply: V_{CC} = 2.375 V to 3.8 V, V_{EE}= 0 V
over operating free-air temperature range (unless otherwise noted)

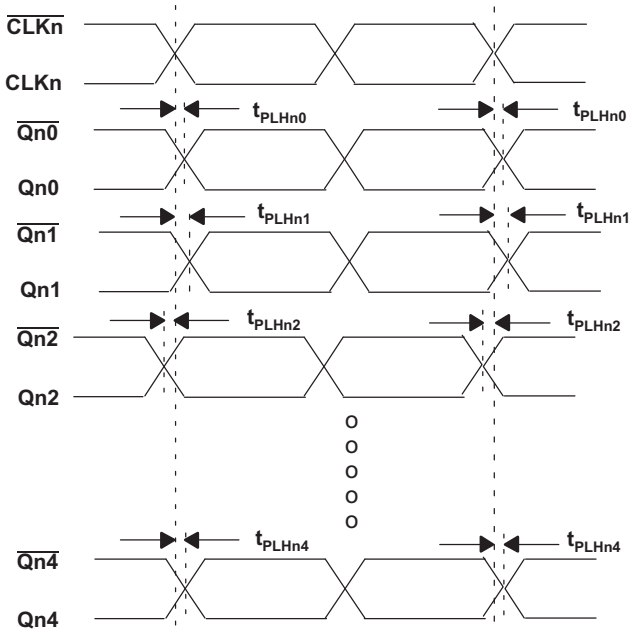
PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
I_{EE}	Supply internal current	Absolute value of current	–40°C, 25°C, 85C	40		90	mA
I_{CC}	Output and internal supply current	All outputs terminated 50 Ω to V_{CC} – 2 V	-40°C			354	mA
			25°C			380	
			85°C			405	
I_{IN}	Input current	Includes pullup/pulldown resistors V_{IH} = V_{CC}, V_{IL} = V_{CC} - 2 V	–40°C, 25°C, 85°C	–150		150	µA
V_{BB}	Internally generated bias voltage	V_{CC} = 3 to 3.8 V, I_{BB}= –0.2 mA	–40°C, 25°C, 85°C	V_{CC} – 1.45	V_{CC} – 1.3	V_{CC} – 1.15	V
		V_{CC} = 2.375 to 2.75 V, I_{BB} = –0.2 mA	–40°C, 25°C, 85°C	V_{CC} – 1.4	V_{CC} – 1.25	V_{CC} – 1.1	
V_{ID}	Input amplitude (CLKn, $\overline{CLKn}$)	Difference of input | V_{IH} – V_{IL}| , see (1)	–40°C, 25°C, 85°C	0.5		1.3	V
V_{CM}	Common-mode voltage (CLKn, $\overline{CLKn}$)	DC offset relative to V_{EE}	–40°C, 25°C, 85°C	1		V_{CC} – 0.3	V
V_{OH}	High-level output voltage	I_{OH} = –21 mA	–40°C	V_{CC} – 1.26		V_{CC} – 0.85	V
			25°C	V_{CC} – 1.2		V_{CC} – 0.85	
			85°C	V_{CC} – 1.15		V_{CC} – 0.85	
V_{OL}	Low-level output voltage	I_{OL} = –5 mA	–40°C	V_{CC} – 1.85		V_{CC} – 1.5	V
			25°C	V_{CC} - 1.85		V_{CC} – 1.45	
			85°C	V_{CC} – 1.85		V_{CC} – 1.4	
V_{OD}	Differential output voltage swing	Terminated with 50 Ω to V_{CC} – 2 V	–40°C, 25°C, 85°C	600			mV

(1) V_{ID} minimum and maximum is required to maintain ac specifications, actual device function tolerates a minimum V_{ID} of 100 mV.

AC ELECTRICAL CHARACTERISTICS

Vsupply: V_{CC} = 2.375 V to 3.8 V, V_{EE} = 0 V or LVECL/LVPECL input V_{CC} = 0 V, V_{EE} = -2.375 V to -3.8 V over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{pd}	Differential propagation delay CLKn, $\overline{CLKn}$ to all QA0, $\overline{QA0}$… QB4, $\overline{QB4}$	Input condition: V_{CM} = 1 V, V_{ID} = 0.5 V	135		300	ps
$t_{sk(o)}$	Output-to-output skew	See Note A of Figure 1		15	30	ps
$t_{sk(pp)}$	Part-to-part skew	See Note B of Figure 1			70	ps
t_{aj}	Additive phase jitter, rms	Integration bandwidth of 20 kHz to 20 MHz, fout = 125 MHz at 25°C			< 0.8	ps
$f_{(max)}$	Maximum frequency	Functional up to 3.5 GHz, timing specifications apply at 1 GHz, see Figure 3			3500	MHz
t_r/t_f	Output rise and fall time (20%, 80%)		90		200	ps



A. Output skew is calculated as the greater of: The difference between the fastest and the slowest t_{PLHn} (n = n0, n1,...n4) or the difference between the fastest and the slowest t_{PHLn} (n = n0, n1,...n4).

B. Part-to-part skew, is calculated as the greater of: The difference between the fastest and the slowest t_{PLHn} (n = n0, n1,...n4) across multiple devices or the difference between the fastest and the slowest t_{PHLn} (n = n0, n1,...n4) across multiple devices.

C. Output skew is measured per the output group.

Figure 1. Waveform for Calculating Both Output and Part-to-Part Skew

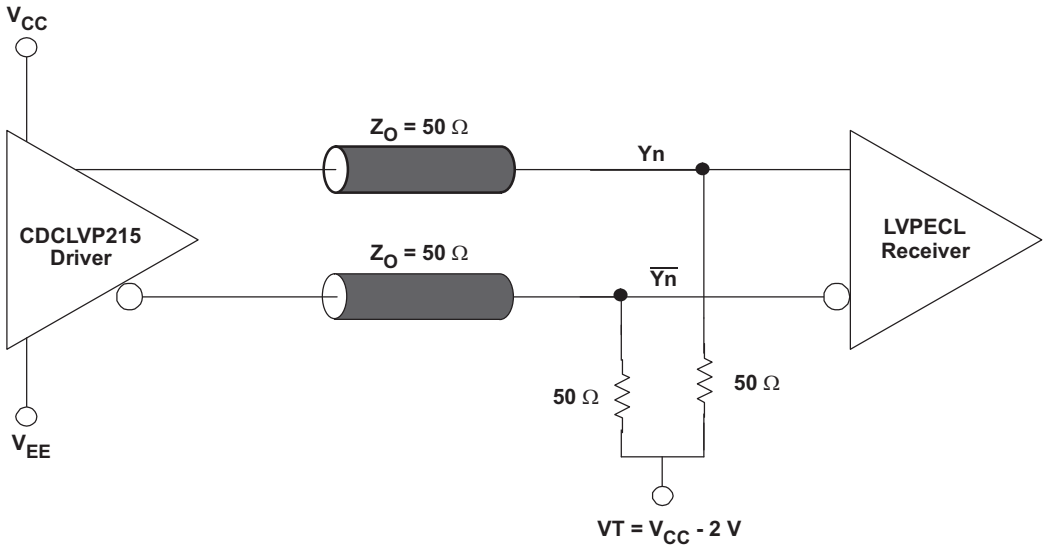


Figure 2. Typical Termination for Output Driver (See the Application Note *Interfacing Between LVPECL, LVDS, and CML*, Literature Number SCAA056)

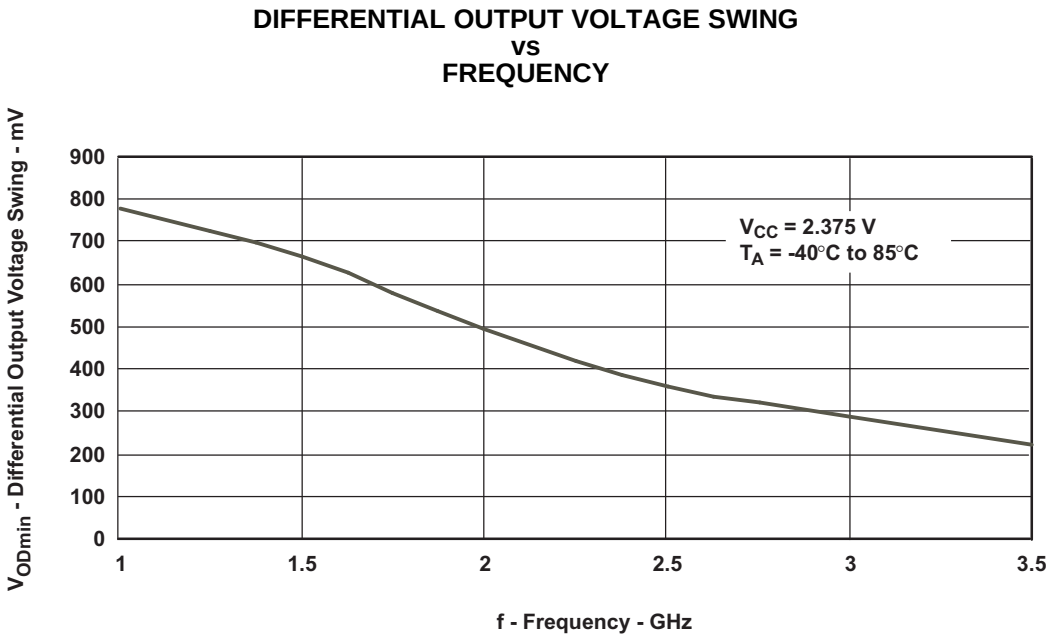


Figure 3. LVPECL Input Using CLKB Pair, V_{CM} = 1 V, V_{ID} = 0.5 V

REVISION HISTORY

Changes from Original (April 2008) to Revision A **Page**

- Changed Status from: Product Preview To: Production 1
- Changed Features bullet From: Fully Compatible With LVPECL/LVPECL To: Fully Compatible With LVPECL/LVECL 1
- Changed Features Bullet From: Single Supply Voltage Required ±3.3 V or ±2.5 V Supply To: Supports a Wide Supply Voltage Range From 2.375 V to 3.8 V 1
- Deleted PTN1111 from The Pin-to-Pin Features bullet 1
- Changed EP210 in The Pin-to-Pin Features bullet From: EP210 to LVEP210. 1
- Added Application bullet: High Performance Clock Distribution 1
- Changed paragraph - From: The bottom of the QFN32 To: The PowerPAD™ of the QFN32... 2
- Changed list item From: $\overline{\text{CLKn}}$ pull up resistor 31.4 kΩ To: $\overline{\text{CLKn}}$ pull up resistor 37.5 kΩ 2
- Changed Abs Max table - Negative supply voltage value From -0.3 to 4.6 To: -4.6 to 0.3 3
- Changed PACKAGE THERMAL IMPEDANCE max values. 3
- Changed LVECL DC ELECTRICAL CHARACTERISTICS values. 3
- Added to the input current Test Conditions: $V_{IH} = V_{CC}$, $V_{IL} = V_{CC}$ - 2V 3
- Changed From: Cross point of input 9 average (V_{IH}, V_{IL}) To: DC offset relative to V_{EE} 3
- Changed LVPECL DC ELECTRICAL CHARACTERISTICS values. 4
- Added to the input current Test Conditions: $V_{IH} = V_{CC}$, $V_{IL} = V_{CC}$ - 2V 4
- Changed From: Cross point of input 9 average (V_{IH}, V_{IL}) To: DC offset relative to V_{EE} 4
- Changed AC ELECTRICAL CHARACTERISTICS values. 5
- Changed From: Cycle to Cycle RMS jitter To: Additive phase jitter. 5
- Changed Output rise and fall time (20%, 80%) MIN Value From: 100 To: 90 5

Changes from Revision A (October 2008) to Revision B **Page**

- Added PowerPAD information to the Pinout Package 1
- Added PowerPAD information to the Pin Functions table 2
- Deleted The PowerPAD™ of the QFN32 2

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
CDCLVP215RHBR	ACTIVE	VQFN	RHB	32	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	LVP215	Samples
CDCLVP215RHBT	ACTIVE	VQFN	RHB	32	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	LVP215	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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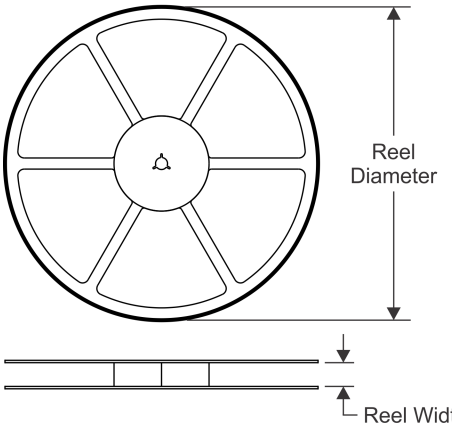
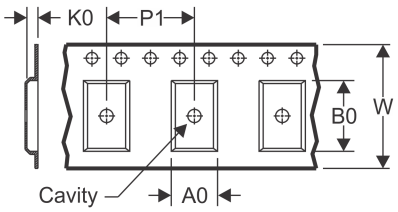
TAPE AND REEL INFORMATION

REEL DIMENSIONS

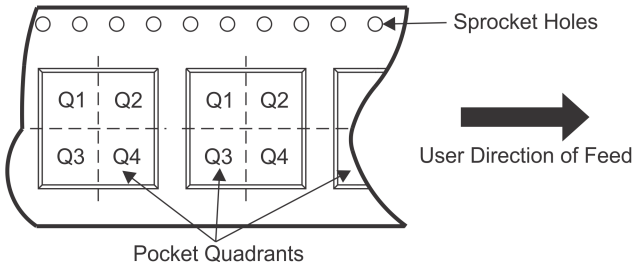


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

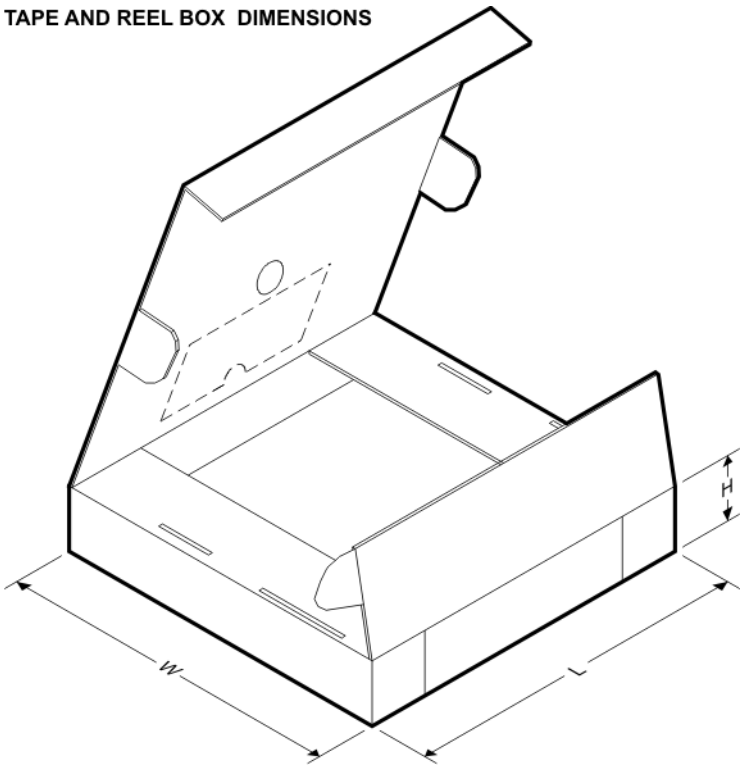
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CDCLVP215RHBR	VQFN	RHB	32	3000	330.0	12.4	5.3	5.3	1.5	8.0	12.0	Q2
CDCLVP215RHBT	VQFN	RHB	32	250	180.0	12.4	5.3	5.3	1.5	8.0	12.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CDCLVP215RHBR	VQFN	RHB	32	3000	336.6	336.6	28.6
CDCLVP215RHBT	VQFN	RHB	32	250	210.0	185.0	35.0

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