DRV8860x 38-V 8-Channel Serial Interface Low-Side Driver

1 Features

- 8-Channel Protected Low-side Driver
  - Eight NMOS FETs with Overcurrent Protection
  - Integrated Inductive Catch Diodes
  - Serial Interface
  - Open/Short Load Detection (DRV8860 only)
  - Configurable 100% Output Timing
  - Configurable PWM Duty Cycle
- Continuous Current Driving Capability
  - 560 mA (Single Channel on) PW and PWP
  - 200 mA (8 Channels on) PW
  - 330 mA (8 Channels on) PWP
  - Support Parallel Configuration
- 8 V to 38 V Supply Voltage Range
- Input Digital Noise Filter for Noise Immunity
- Internal Data Read Back Capability for Reliable Control
- Protection and Diagnostic Features
  - Overcurrent Protection (OCP)
  - Open Load Detection (OL)
  - Overtemperature Shutdown (OTS)
  - Undervoltage Lockout (UVLO)
  - Individual Channel Status Report
  - Fault Condition Alarm

2 Applications

- Relays, Unipolar Stepper Motors
- Solenoids, Electromagnetic Drivers
- General Low-side Switch Applications
- LED driver with dimmer functionality (DRV8860A)

3 Description

The DRV8860 provides an 8-channel low side driver with overcurrent protection and open/shorted load detection. It has built-in diodes to clamp turn-off transients generated by inductive loads, and can be used to drive unipolar stepper motors, DC motors, relays, solenoids, or other loads.

The PWP package can supply up to 330 mA × 8 channel and The PW package can supply up to 200 mA × 8 channel continuous output current. A single channel can deliver up to 560 mA continuous output current.

A serial interface is provided to control the DRV8860 output drivers, configure internal setting register and read the fault status of each channel. DRV8860 devices can be daisy-chained together to use a single serial interface. Energizing-time and holding-PWM-Duty cycles are configurable through serial interface as well. These functions allow for cooler running than always-on solutions.

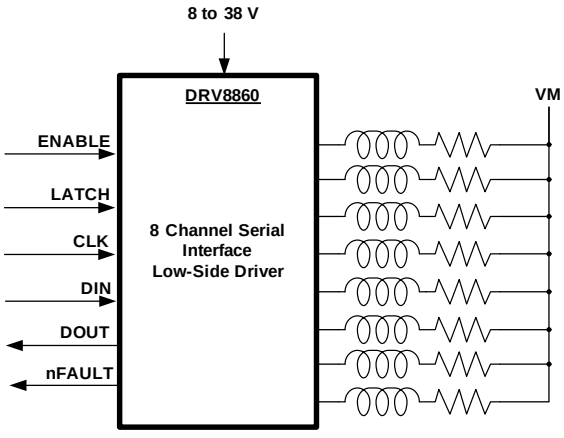
Internal shutdown functions are provided for overcurrent protection, short-circuit protection, undervoltage lockout, and overtemperature. DRV8860A does not include open load detection. Fault information for each channel can be read out through serial interface and indicated by an external fault pin.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
DRV8860	TSSOP (16)	5.00 mm × 6.40 mm
	HTSSOP (16)	5.00 mm × 4.40 mm
DRV8860A	TSSOP (16)	5.00 mm × 6.40 mm

(1) For all available packages, see the orderable addendum at the end of the datasheet.

4 Simplified Schematic



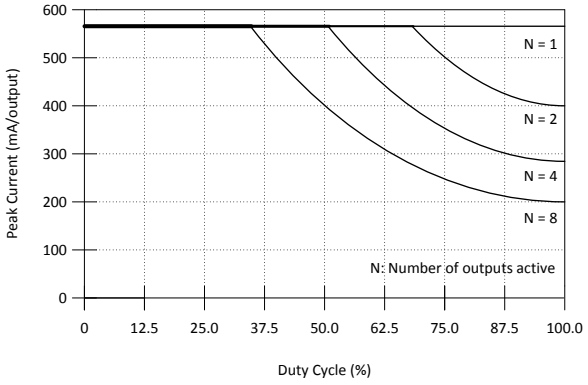


Table of Contents

5 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision D (October 2015) to Revision E — **Page**

- Added timing diagrams Figure 1, Figure 2 and Table 2, Table 3 ... 7

Changes from Revision C (October 2014) to Revision D — **Page**

- Added $I_{(VM)}$ MAX = 4.5 V ... 6
- Added I_{OFF} for DRV8860A ... 6
- Changed t_{OCP} From: MIN = 2.7 To: 2.0 µs ... 6
- Updated Functional Block Diagram ... 9

Changes from Revision B (July 2014) to Revision C — **Page**

- Added DRV8860A part to datasheet. ... 1
- Added caption to Figure 9 ... 14
- Added caption to Figure 10 ... 14
- Moved the Serial Control Interface information into the Programming section of the datasheet ... 16
- Moved the Register Maps information into the Detailed Description section of the datasheet ... 27
- Changed Figure 37 from a black background to a white background ... 29
- Added caption to Figure 39 ... 31
- Changed title From: Thermal Information To: Thermal Consideration ... 32

Changes from Revision A (November 2013) to Revision B **Page**

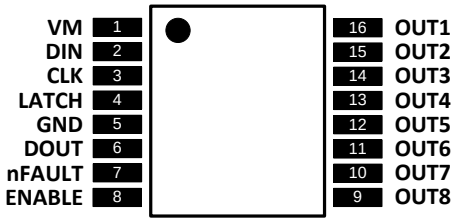
- Added Feature: Serial Interface ... 1
- Changed the Features list for: Continuous Current Driving Capability ... 1
- Deleted Features: Programmable Current Profile ... 1
- Updated the Application List ... 1
- Changed Description sentence From: These functions allow for lower temperature operation rather than traditional always-on solutions. To: These functions allow for cooler running than traditional always-on solutions ... 1
- Added the Handling Ratings table ... 5
- Changed the MIN value for VM in the Recommended Operating Conditions table From: 8.2 V To: 8 V ... 5
- Added HTTSSOP (PWP) to the Thermal Information table ... 5
- Changed V_{IL} From: MIN = - To: 0 V, TYP = 0.6 V To: - ... 6
- Changed V_{IH} From: MIN = 2 V To: 1.5 V, MAX = - To: 5.3 V ... 6
- Changed V_{HYS} From: MIN = - To: 100 mV, TYP = 0.45 V To: - ... 6
- Added the Timing Requirements table ... 6
- Added the Overview section ... 8
- Changed the description of the Recommended Output Current section ... 10
- Deleted the Example Output Configuration section. ... 12
- Changed the Serial Control Interface description text ... 16

Changes from Original (September 2013) to Revision A **Page**

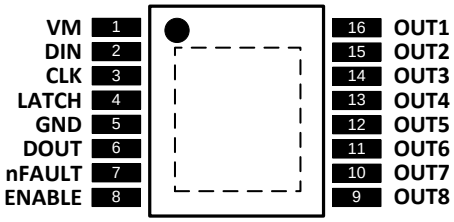
- Added Features: Programmable Current Profile ... 1
- Changed the MIN value for VM in the Recommended Operating Conditions table From: 8 V To: 8.2 V ... 5
- Added the Example Output Configuration section. ... 12

6 Pin Configuration and Functions

PW (TSSOP) PACKAGE
(TOP VIEW)



PWP (HTSSOP) PACKAGE
(TOP VIEW)



Pin Functions

NAME	PIN	I/O (1)	DESCRIPTION	EXTERNAL COMPONENTS OR CONNECTIONS
GND	5	—	Device ground	All pins must be connected to ground
VM	1	—	Motor power supply	Connect to motor supply voltage. Bypass to GND with a 0.1 µF ceramic capacitor plus a 10 µF electrolytic capacitor.
ENABLE	8	I	Output stage enable control input	Logic high to enable outputs, logic low to disable outputs. Internal logic and registers can be read and written to when ENABLE is logic low. Internal pulldown.
LATCH	4	I	Serial latch signal	Refer to serial communication waveforms. Internal pulldown.
CLK	3	I	Serial clock input	Rising edge clocks data into part for write operations. Falling edge clocks data out of part for read operations. Internal pulldown.
DIN	2	I	Serial data input	Serial data input from controller. Internal pulldown.
DOUT	6	O	Serial data output	Serial data output to controller. Open-drain output with internal pullup.
nFAULT	7	OD	Fault	Logic low when in fault condition. Open-drain output requires external pullup. Faults: OCP, OTS, UVLO, OL (DRV8860 only)
OUT1	16	O	Low-side output 1	NFET output driver. Connect external load between this pin and VM
OUT2	15	O	Low-side output 2	NFET output driver. Connect external load between this pin and VM
OUT3	14	O	Low-side output 3	NFET output driver. Connect external load between this pin and VM
OUT4	13	O	Low-side output 4	NFET output driver. Connect external load between this pin and VM
OUT5	12	O	Low-side output 5	NFET output driver. Connect external load between this pin and VM
OUT6	11	O	Low-side output 6	NFET output driver. Connect external load between this pin and VM
OUT7	10	O	Low-side output 7	NFET output driver. Connect external load between this pin and VM
OUT8	9	O	Low-side output 8	NFET output driver. Connect external load between this pin and VM

(1) Directions: I = input, O = output, OD = open-drain output

Table 1. External Components

COMPONENT	PIN 1	PIN 2	RECOMMENDED
$C_{(VM1)}$	VM	GND	0.1 µF ceramic capacitor rated for VM
			10 µF electrolytic capacitor rated for VM
$R_{(nFAULT)}$	V3P3 (1)	nFAULT	> 4.7 kΩ

(1) V3P3 is not a pin on the DRV8860, but a V3P3 supply voltage pullup is required for open-drain output nFAULT.

7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) (1) (2) (3)

		MIN	MAX	UNIT
Power supply voltage range	VM	–0.3	40	V
Digital input pin current range	ENABLE, LATCH, CLK, DIN	0	20	mA
Digital output pin voltage range	DOUT, nFAULT	–0.5	7	V
Digital output pin current	DOUT, nFAULT	–0.5	7	V
Output voltage range	OUTx	–0.3	40	V
Output current range	OUTx	Internally limited		A
Operating virtual junction temperature range, T_J		–40	150	°C

(1) Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute–maximum–rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to network ground terminal.
(3) Power dissipation and thermal limits must be observed

7.2 Handling Ratings

			MIN	MAX	UNIT
T_{stg}	Storage temperature range		–60	150	°C
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins (1)	–2	2	kV
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins (2)	–500	500	V

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
VM	Motor power supply voltage range	8		38	V
I_{OUT}	Low-side driver current capability			560	mA
T_A	Operating ambient temperature range	–40		85	°C

7.4 Thermal Information (1)

over operating free-air temperature range (unless otherwise noted)

THERMAL METRIC		TSSOP	HTSSOP	UNIT
		PW (16 PINS)	PWP (16 PINS)	
Θ_{JA}	Junction-to-ambient thermal resistance	103	40.9	°C/W
$R_{\theta JC(TOP)}$	Junction-to-case (top) thermal resistance	37.9	28.5	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	48	23.2	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	3	0.9	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	47.4	23.0	°C/W
$R_{\theta JC(BOTTOM)}$	Junction-to-case (bottom) thermal resistance	N/A	3.0	°C/W

(1) For more information about traditional and new thermal metrics, see the IC Package Thermal Metrics application report, SPRA953.

7.5 Electrical Characteristics

T_A = 25°C, over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
POWER SUPPLIES						
$I_{(VM)}$	VM operating supply current	VM = 24 V		3	4.5	mA
$V_{(UVLO)}$	VM undervoltage lockout voltage	VM rising			8.2	V
LOGIC-LEVEL INPUTS (DIN, CLK, LATCH, ENABLE)						
V_{IL}	Input low voltage		0		0.7	V
V_{IH}	Input high voltage		1.5		5.3	V
V_{HYS}	Input hysteresis		100			mV
I_{IL}	Input low current	V_{IN} = 0	–20		20	µA
I_{IH}	Input high current	V_{IN} = 3.3 V			100	µA
R_{PD}	Input pulldown resistance			100		kΩ
nFAULT, DOUT OUTPUTS (OPEN-DRAIN OUTPUTS)						
V_{OL}	Output low voltage	I_O = 5 mA			0.5	V
I_{OH}	Output high leakage current	V_O = 3.3 V, nFAULT	–1		1	µA
R_{PU}	Input pullup resistance	DOUT only (Pull up to internal 5.7 V)		1.4		kΩ
LOW-SIDE FET DRIVERS						
$R_{ds(on)}$	FET on resistance	VM = 24 V, I_O = 150 mA, T_J = 25°C		1.5		Ω
		VM = 24 V, I_O = 150 mA, T_J = 85°C		1.8		
I_{OFF}	Off-state leakage current	VM = 24 V, T_J = 25°C, DRV8860	0	30		µA
		VM = 24 V, T_J = 25°C, DRV8860A	-0.5		0.5	
HIGH-SIDE FREE-WHEELING DIODES						
V_F	Diode forward voltage	VM = 2 4V, I_O = 150 mA, T_J = 25°C		0.9		V
PROTECTION CIRCUITS						
I_{OCP}	Overcurrent protection trip level	Each channel separately monitored		620		mA
I_{OL}	Open load detect pull-down current	Per channel, DRV8860 only		30		µA
V_{OL}	Open load detect threshold voltage	Per channel, DRV8860 only		1.2		V
T_{TSD}	Thermal shutdown temperature	Die temperature	150	160	180	°C
T_{HYS}	Thermal shutdown hysteresis	Die temperature		35		°C
PWM CHOPPING FREQUENCY						
f_{PWM}	PWM chopping frequency	Duty cycle is > 25%	45	50	55	kHz
		Duty cycle is 25%	22	25	28	
		Duty cycle is 12.5%	11	12.5	14	

7.6 Timing Requirements

			MIN	TYP	MAX	UNIT
t_F	Fall time	I_O = 150 mA, VM = 24 V, resistive load	50		300	ns
t_{OCP}	Overcurrent protection deglitch time	VM = 24 V	2.0	3.0	3.85	µs
t_{OL}	Open load detect deglitch time	Each channel separately monitored	14	17	20	µs

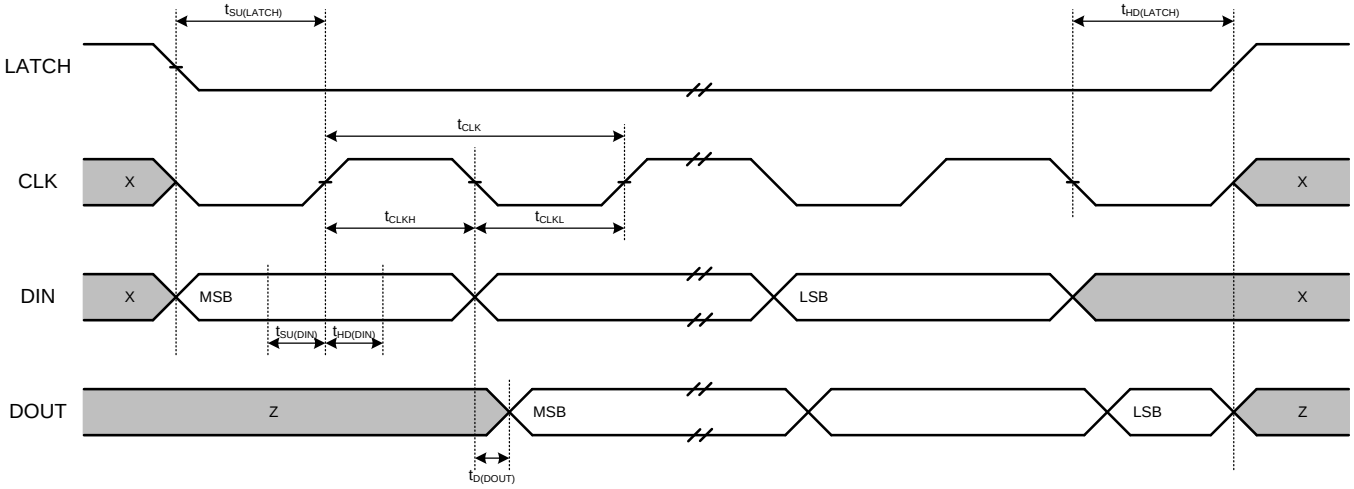


Figure 1. Serial Interface

Table 2. Serial Timing

NO.	REF DES	DESCRIPTION	MIN	TYP	MAX	UNIT
1	t_{CLK}	CLK cycle time	5			µs
2	t_{CLKH}	CLK high time	2.5			µs
3	t_{CLKL}	CLK low time	2.5			µs
4	$t_{SU(DIN)}$	Setup time, DIN to CLK	1			µs
5	$t_{H(DIN)}$	Hold time, DIN to CLK	1			µs
6	$t_{SU(LATCH)}$	Setup time, LATCH to CLK	1			µs
7	$t_{H(LATCH)}$	Hold time, LATCH to CLK	1			µs
8	$t_{OFF(LATCH)}$	Inactive time between writes and read	2			µs
9	$t_{D(DOUT)}$	Delay time, CLK to DOUT			1.5	µs

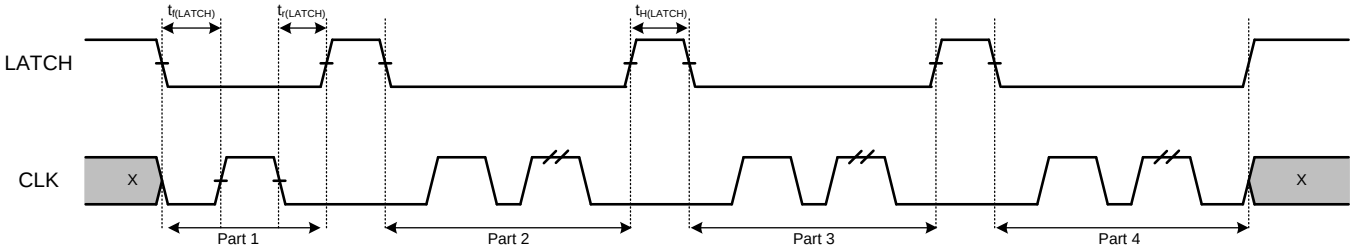


Figure 2. Special Commands

Table 3. Special Commands

NO.	REF DES	DESCRIPTION	MIN	TYP	MAX	UNIT
10	$t_{f(LATCH)}$	LATCH fall to CLK rise	1			µs
11	$t_{r(LATCH)}$	CLK fall to LATCH rise	1			µs
12	$t_{H(LATCH)}$	LATCH high time	2			µs

7.7 Typical Characteristics

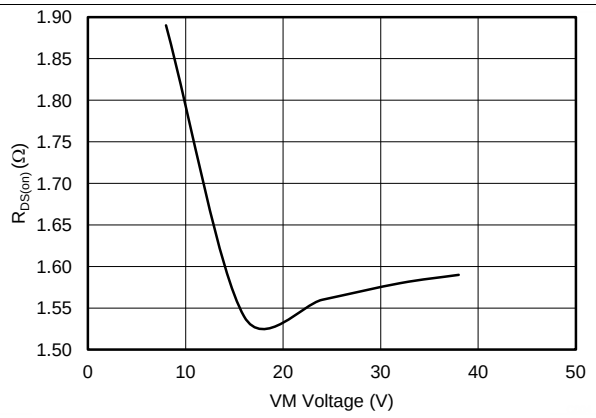


Figure 3. Output ON Resistance

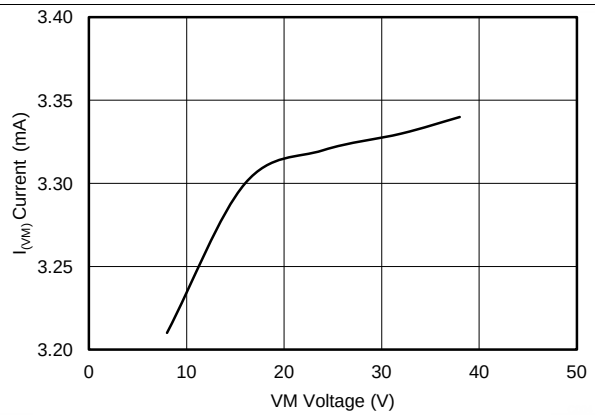


Figure 4. VM Operating Supply Current

8 Detailed Description

8.1 Overview

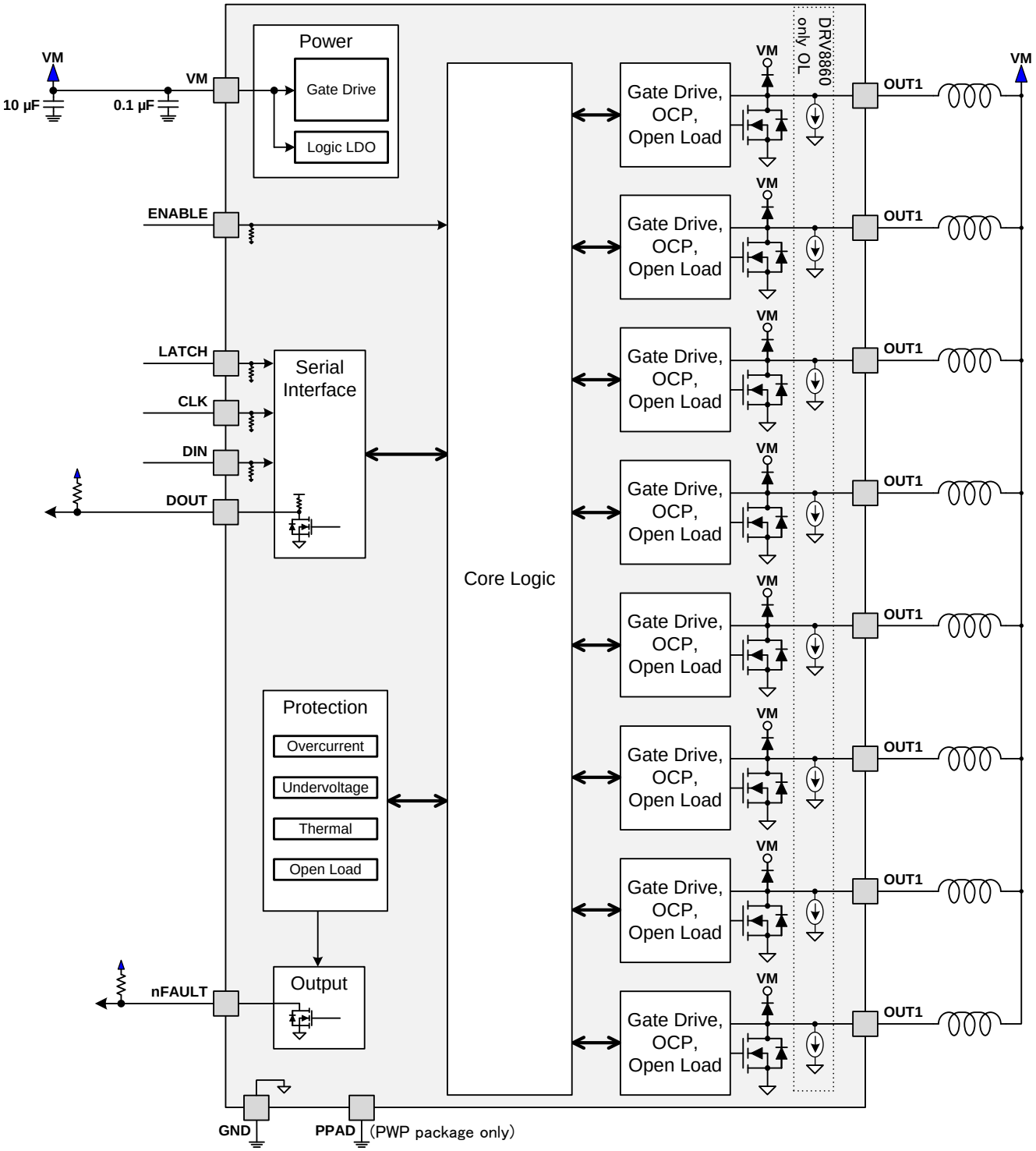
The DRV8860 is an integrated 8-channel low side driver with overcurrent protection and open/short detection. It has built-in diodes to clamp turn-off transients generated by inductive loads, and can be used to drive unipolar stepper motors, DC motors, relays, solenoids, or other loads.

DRV8860 can supply up to 200 mA x 8 channel continuous output current. The current driving capability increases with lower PWM duty cycle. A single channel can deliver up to 560 mA continuous output current. Refer to the current capability table for details.

A serial interface is provided to control the DRV8860 output drivers, configure internal register settings, and read the fault status of each channel. Multiple DRV8860 devices can be daisy-chained together to use a single serial interface. Energizing-time and holding-PWM-duty cycle are configurable through the serial interface as well. These functions allow for cooler running than traditional always-on solutions.

Internal shutdown functions are provided for overcurrent protection, short-circuit protection, under voltage lockout and over temperature. DRV8860 can diagnosis an open load condition. DRV8860A does not include open load detection. Fault information for each channel can be read out through serial interface and is indicated by an external fault pin.

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 Recommended Output Current

DRV8860 current capability will depend on several system application parameters such as system ambient temperature, maximum case temperature, and overall output duty cycle. The PWP package provides a better heatsinking capability through the PowerPAD™; and therefore, is cable of driving higher output current or operating at a slightly lower temperature than the device in PW package.

OUTPUT CURRENT RECOMMENDATION (PW PACKAGE) T_A = 25°C	
CONFIGURATION	**OUTPUT CURRENT CAPACITY**
1x output on (100% duty cycle)	566 mA
2x outputs on (100% duty cycle)	400 mA per output
4x outputs on (100% duty cycle)	283 mA per output
8x outputs on (100% duty cycle)	200 mA per output

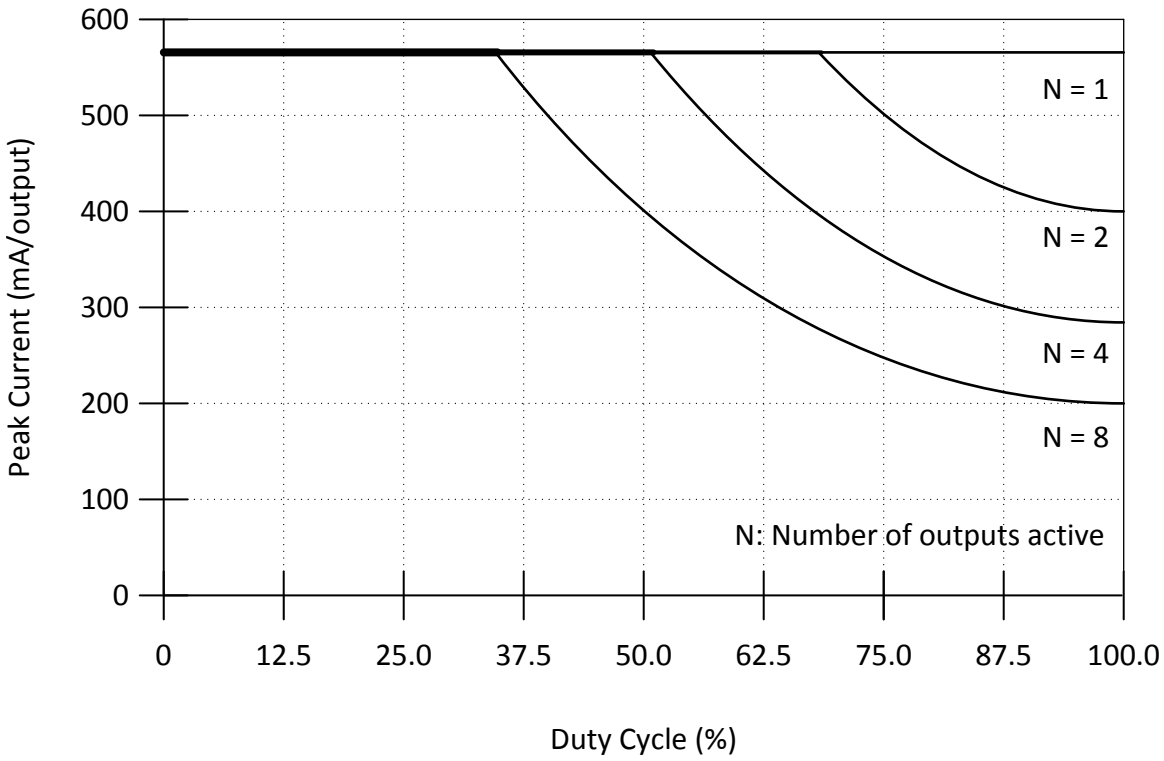


Figure 5. Output Current Capacity vs Duty Cycle for PW Package

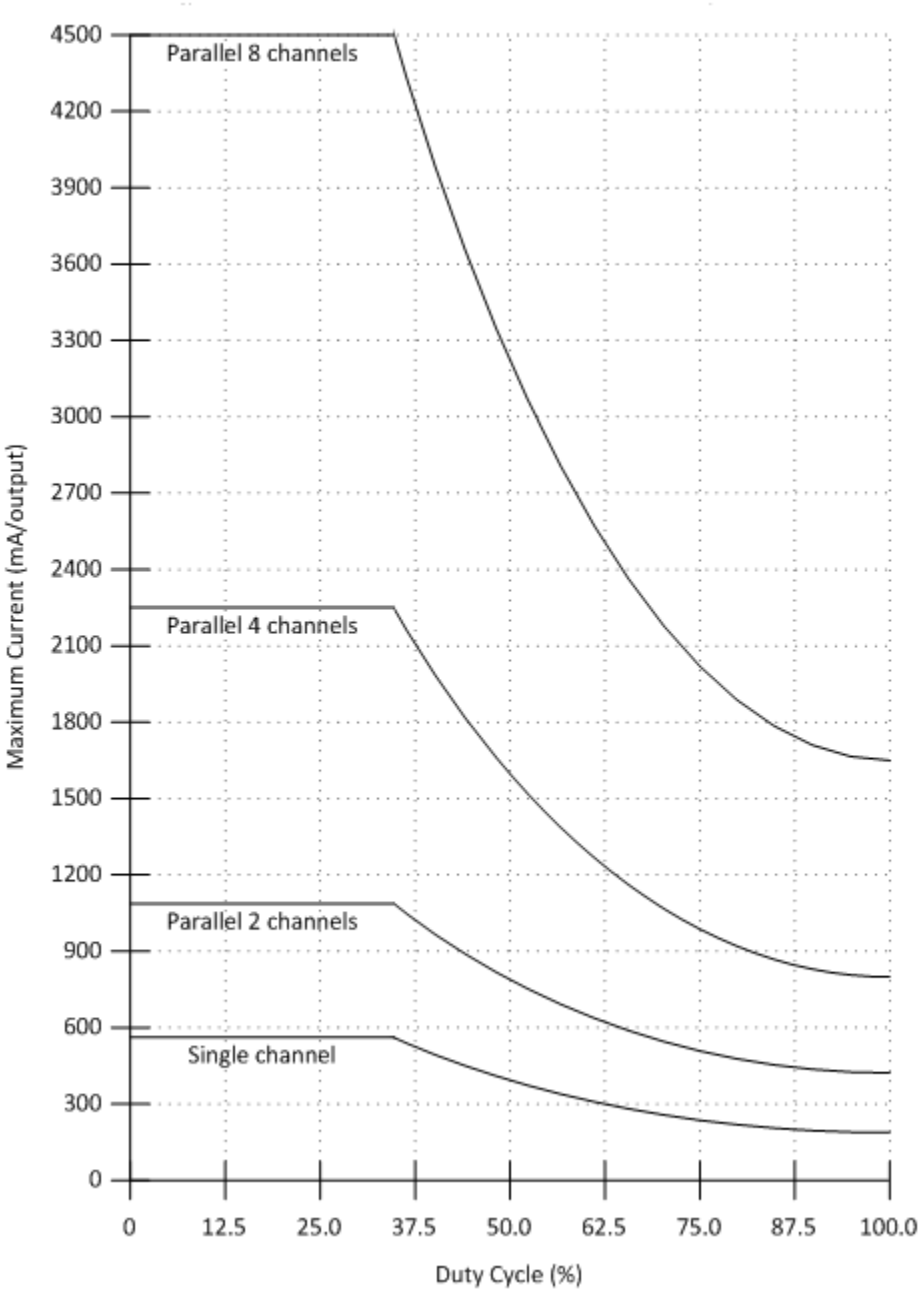


Figure 6. Maximum Current Capacity vs Duty Cycle when Paralleling Outputs for DRV8860PW

8.3.2 Daisy Chain Connection

Two or more DRV8860 devices may be connected together to use a single serial interface. The SDATOUT pin of the first device in the chain is connected to the SDATIN pin of the next device. The SCLK, LATCH, RESET, and nFAULT pins are connected together.

Timing diagrams are shown in Figure 7 and Figure 8 for the configuration of single devices, as well as two devices in daisy-chain connection.

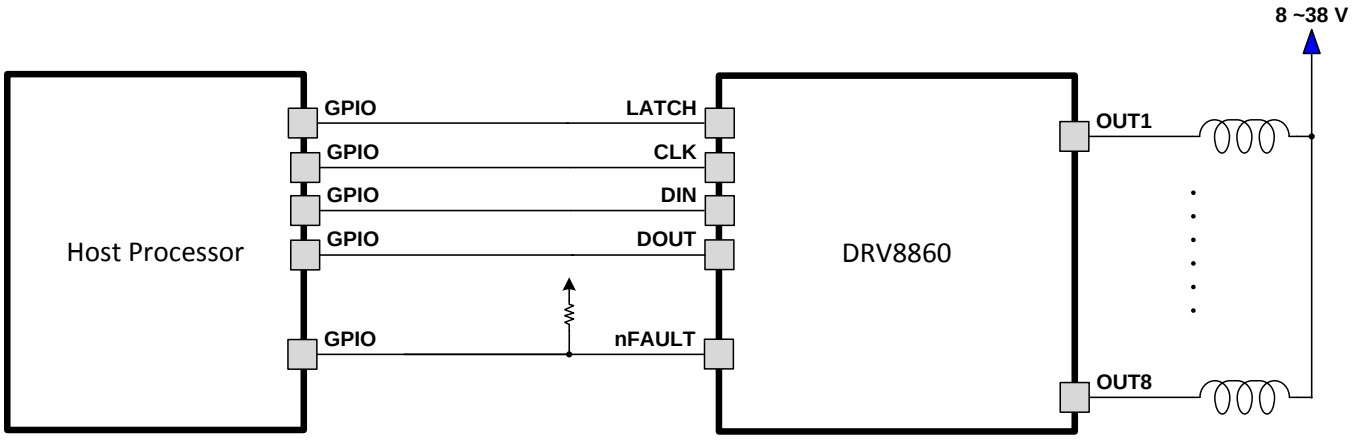


Figure 7. Single Device Connection

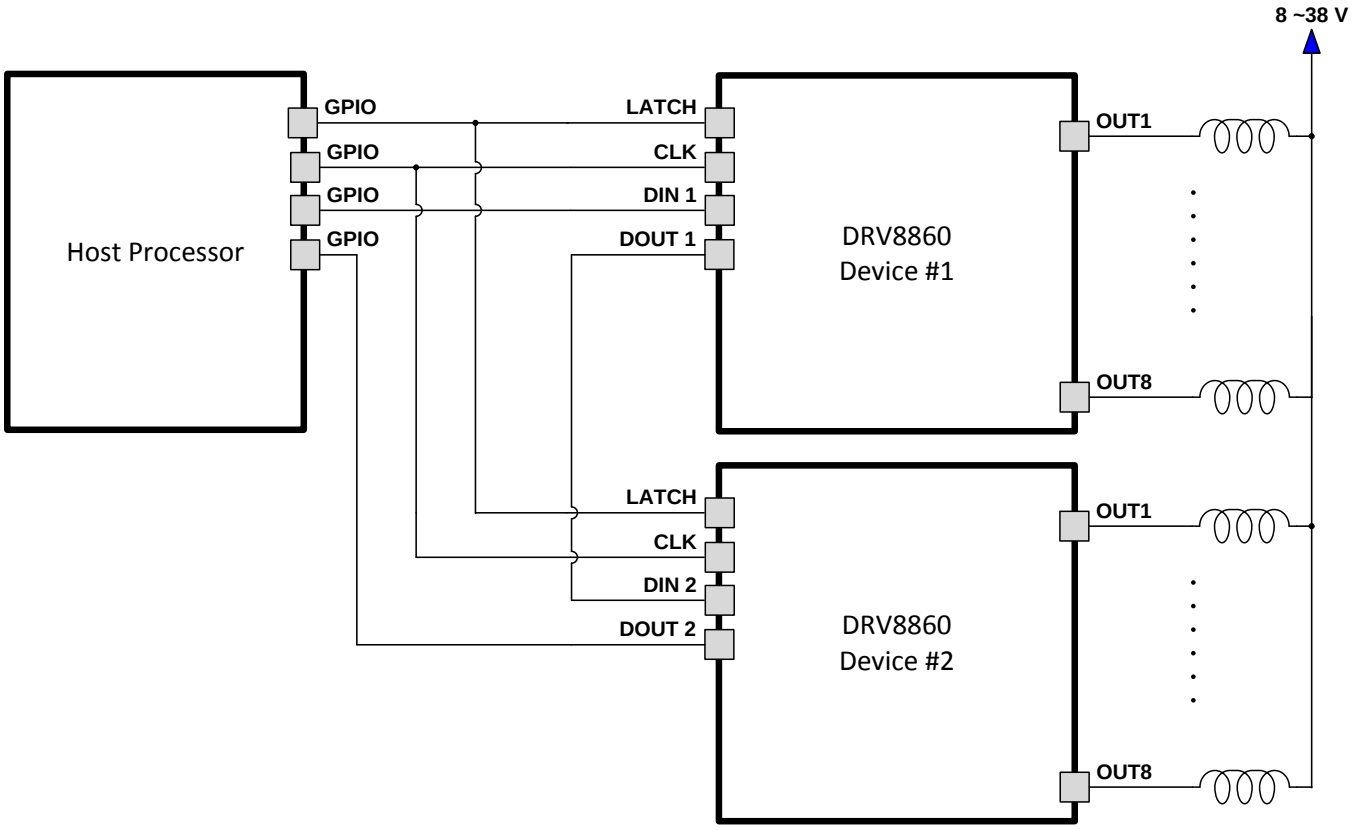


Figure 8. Daisy-Chain Connection

8.3.3 Protection Circuits

The DRV8860 is fully protected against undervoltage, overcurrent and overtemperature events.

8.3.3.1 Overcurrent Protection (OCP)

When output current exceeds OCP trigger level, corresponding channel will be automatically turned off. nFault pin will be set low and corresponding OCP flag in fault register will be set to 1.

Over current faults are automatically cleared whenever the corresponding output is turned off by setting the Data register bit to '0'. Alternatively, a Fault Reset special command will also clear this value. In either case, once all bits in the Fault register are clear, nFAULT is released.

8.3.3.2 Open Load Detection (OL) - DRV8860 only

When any output is in off status (the corresponding Data Register bit is set to '0'), a current sink pulls the node down with approximately 30 µA. If the voltage on the pin is sensed to be less than 1.2 V, then an open load condition is reported. nFAULT is driven low and the OL bit of the fault register (F8:F1) corresponding to the specific channel is set.

Open load faults are automatically cleared whenever the corresponding output is turned on by setting the Data register bit to '1'. Alternatively, a Fault Reset special command will also clear this value. In either case, once all bits in the Fault register are clear, nFAULT is released.

8.3.3.3 Thermal Shutdown (TSD)

If the die temperature exceeds safe limits, all outputs will be disabled, and the nFAULT pin will be driven low. Once the die temperature has fallen to a safe level, operation will automatically resume. The nFAULT pin will be released after operation has resumed.

8.3.3.4 Undervoltage Lockout (UVLO)

If at any time the voltage on the VM pin falls below the undervoltage lockout threshold voltage, all circuitry in the device will be disabled and internal logic will be reset. Operation will resume when VM rises above the UVLO threshold. nFAULT will not be asserted in this condition.

8.3.3.5 Digital Noise Filter

The DRV8860 features an internal noise filter on all digital inputs. In a noisy system, noise may disturb the serial daisy-chain interface. Without an input filter, this noise may result in an unexpected behavior or output state. The digital input filter is capable of removing unwanted noise frequencies while allowing fast communication over the serial interface.

8.4 Device Functional Modes

8.4.1 Internal Registers

The DRV8860 is controlled with a simple serial interface. There are three register banks that are used during operation: the Data register, the Control register, and the Fault register.

Register data movement flow and direction will be affected by special command.

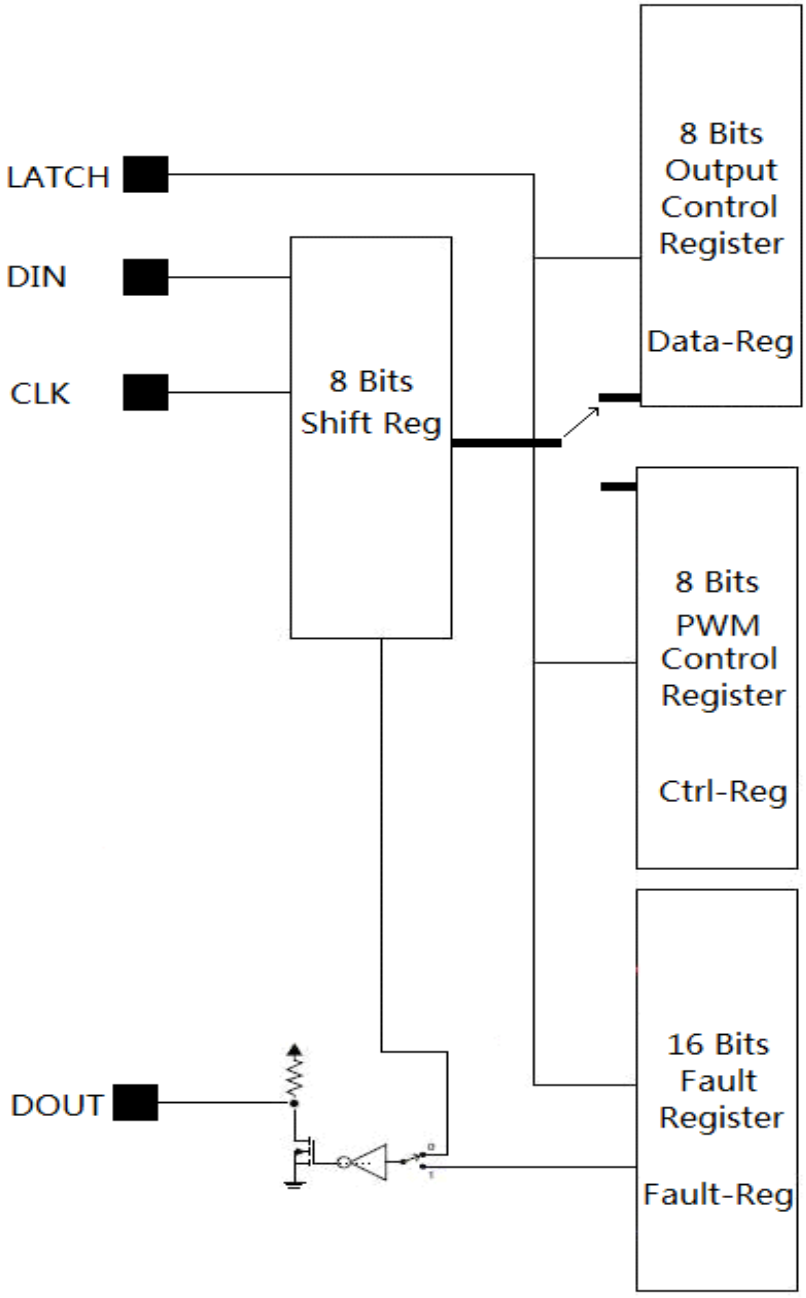


Figure 9. Register Data Movement

In default condition, 8 Bit shift register data moves into output control register DATA-REG.

Device Functional Modes (continued)

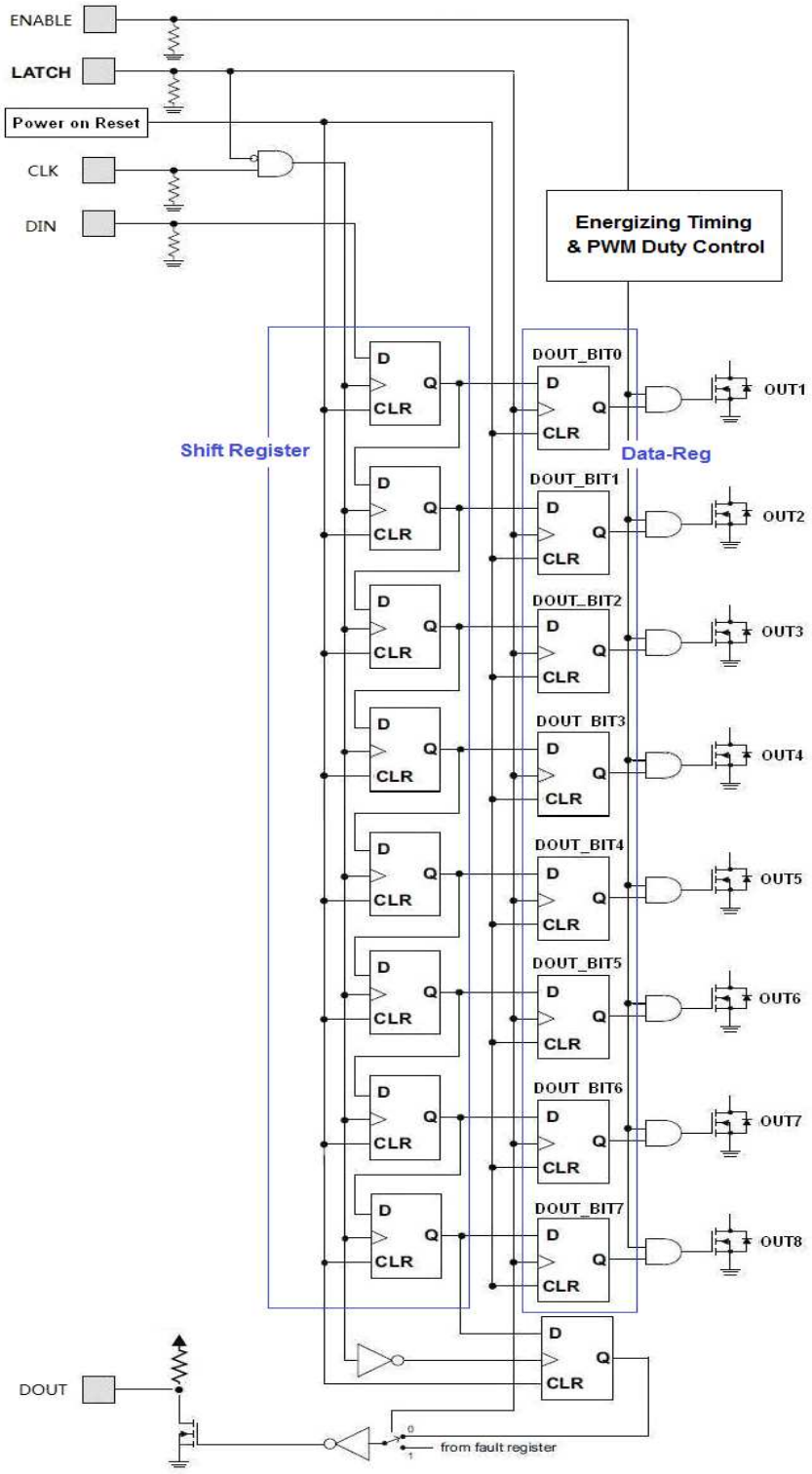


Figure 10. 8 Bit Shift Register Data Movement

8.5 Programming

8.5.1 Serial Control Interface

DRV8860 is using a daisy chain serial interface. Data is latched into the register on the rising edge of the LATCH pin. Data is clocked in on the rising edge of CLK when writing, and data is clocked out on the falling edge of CLK when reading.

8.5.1.1 Data Writing Waveform

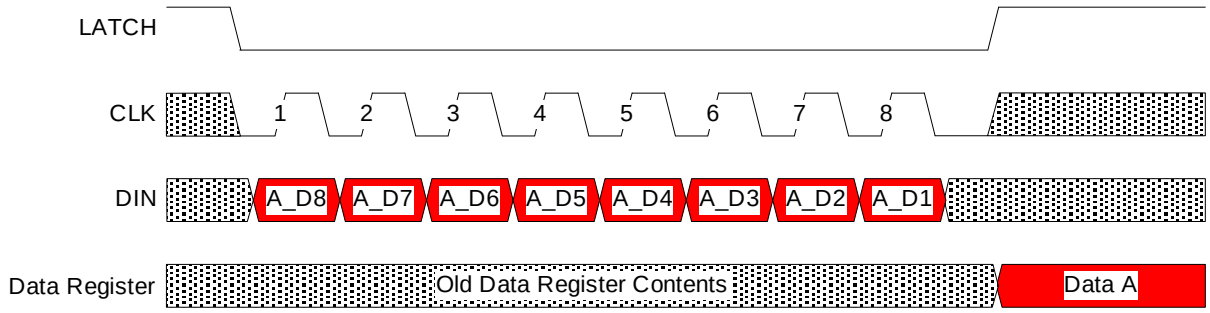


Figure 11. Writing Data Register – Single Device

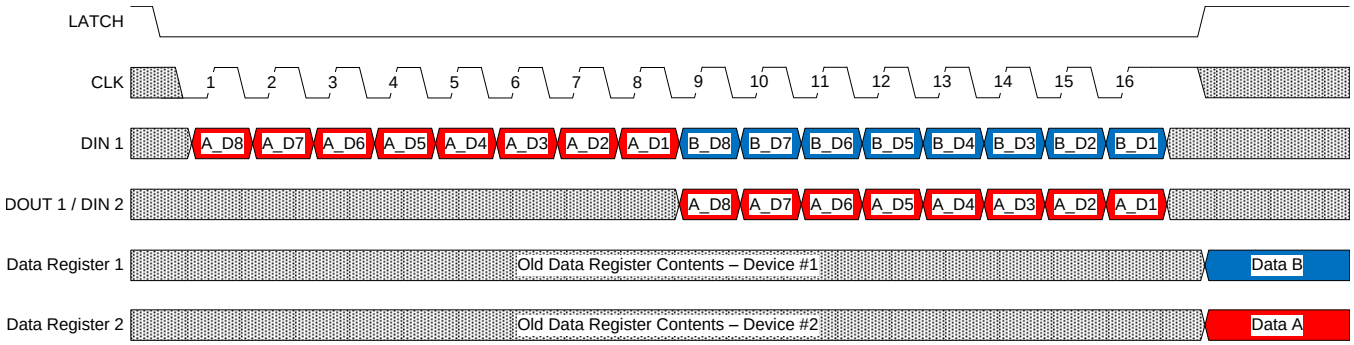


Figure 12. Writing Data Register – Daisy Chan

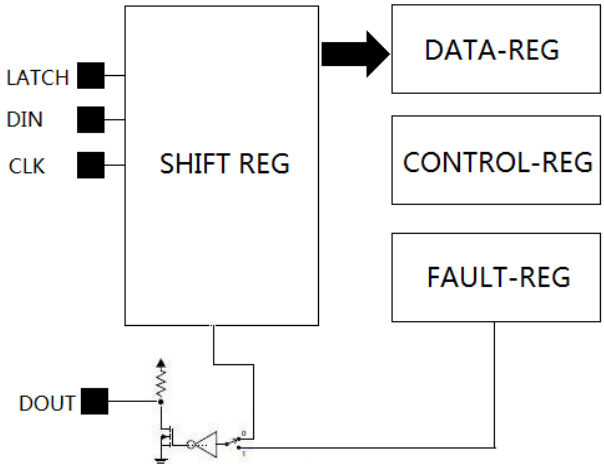


Figure 13. Writing Data Register – Data Flow

Programming (continued)

8.5.1.2 Fault Register Reading Waveform

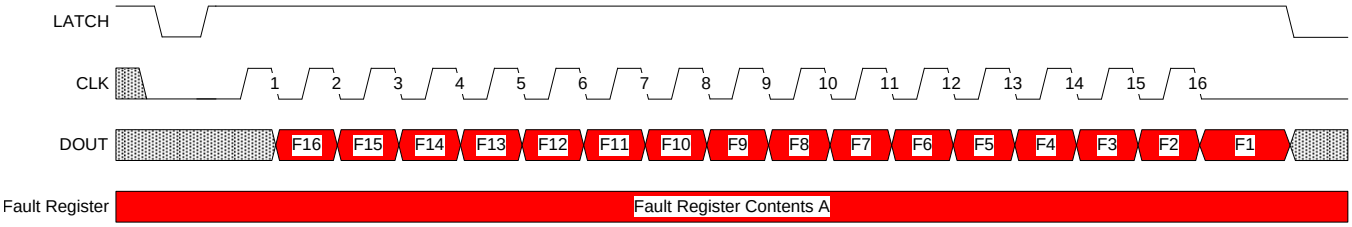


Figure 14. Reading Fault Register – Single Device

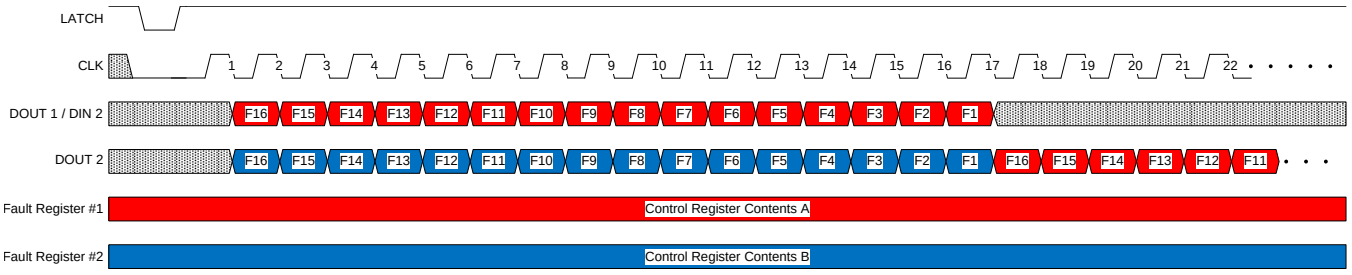


Figure 15. Reading Fault Register – Daisy Chain

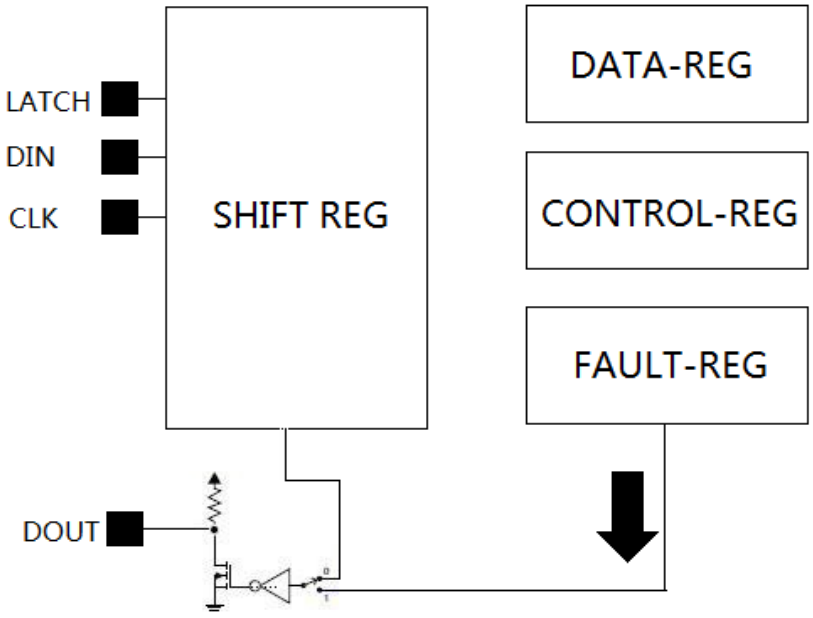


Figure 16. Reading Fault Register – Data Flow

Programming (continued)

8.5.1.3 Special Command

Besides output ON/OFF control and fault status reading back, DRV8860 has special functions to make system more robust or power efficient. These functions will need special command to initiate the device or configure the internal registers.

There are 5 Special Commands:

1. Write Control Register command
2. Read Control Register command
3. Read Data Register command
4. Fault Register Reset command
5. PWM Start command

Special wave form pattern on CLK and LATCH pin will issue the special command, as below

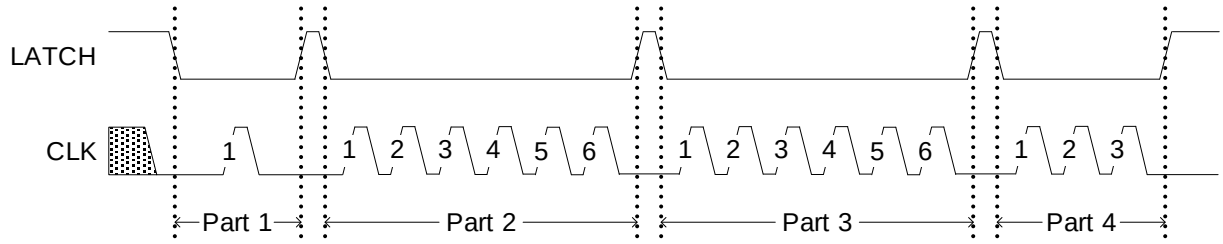


Figure 17. Special Command

SPECIAL COMMAND	CLK CYCLES IN EACH PART			
	Part 1	Part 2	Part 3	Part 4
Write Control Register	1	2	2	3
Read Control Register	1	4	2	3
Read Data Register	1	4	4	3
Fault Register Reset	1	2	4	3
PWM Start	1	6	6	3

8.5.1.3.1 Special command: Write Control Register

When Write-Control-Register command is issued, the following serial data will be latched into timing and duty control register.

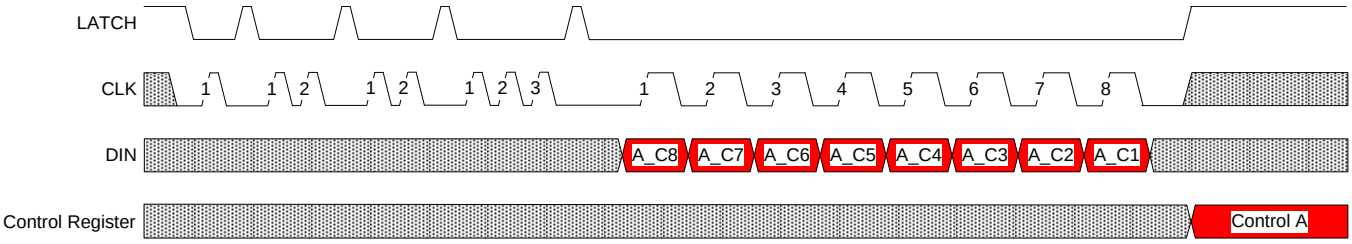


Figure 18. Writing Control Register – Single Device

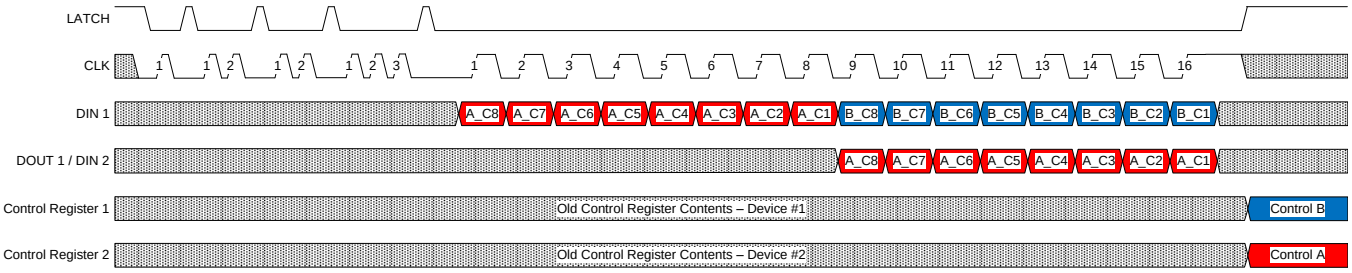


Figure 19. Writing Control Register – Daisy Chain

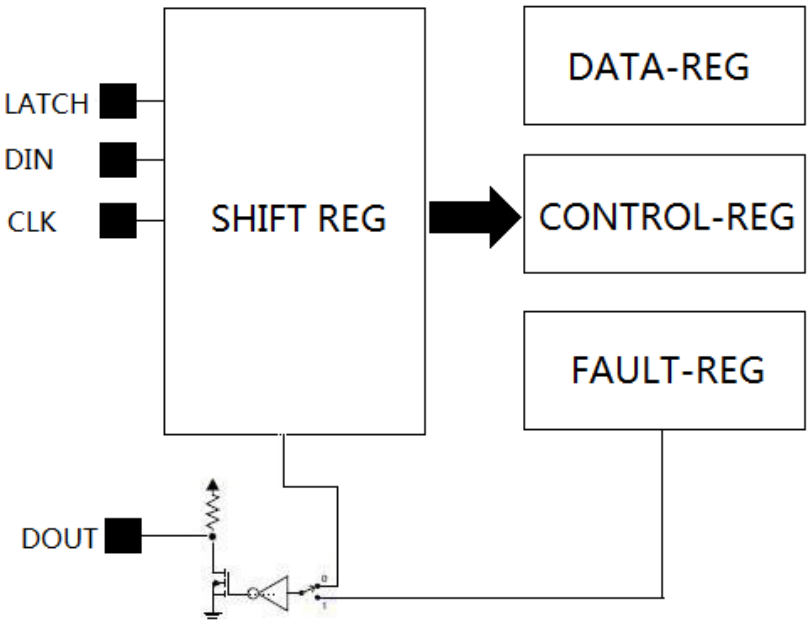


Figure 20. Writing Control Register – Data Flow

8.5.1.3.2 Special command: Read Control Register

When Read-Control-Register command is issued, control register content will be copied to internal shift register and following CLK will shift this content out from DOUT pin. This provides a mechanism for system to verify the control register is correctly programmed.

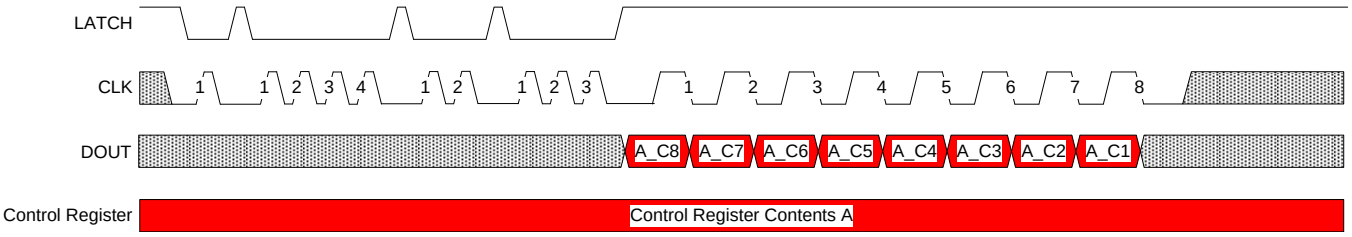


Figure 21. Read Control Register – Single Device

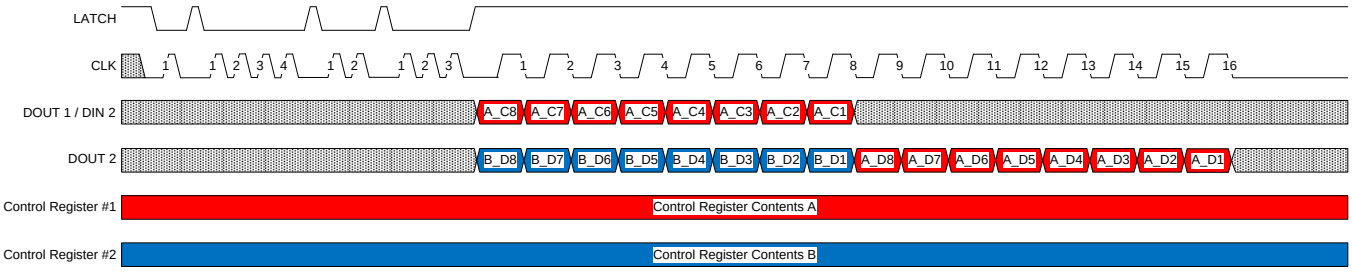


Figure 22. Read Control Register – Daisy Chain

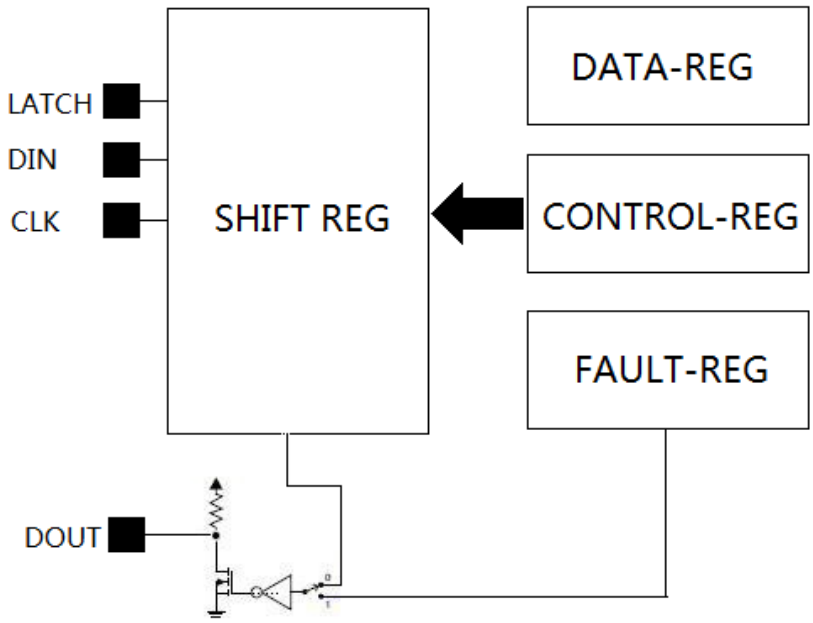


Figure 23. Read Control Register – Data Flow

8.5.1.3.3 Special command: Read Data Register

When Read-Data-Register command is issued, internal output data register content will be copied to internal shift register and following CLK will shift this content out from DOUT pin. This provides a mechanism for system to verify the output data is correctly programmed. It makes system more robust in noisy system.

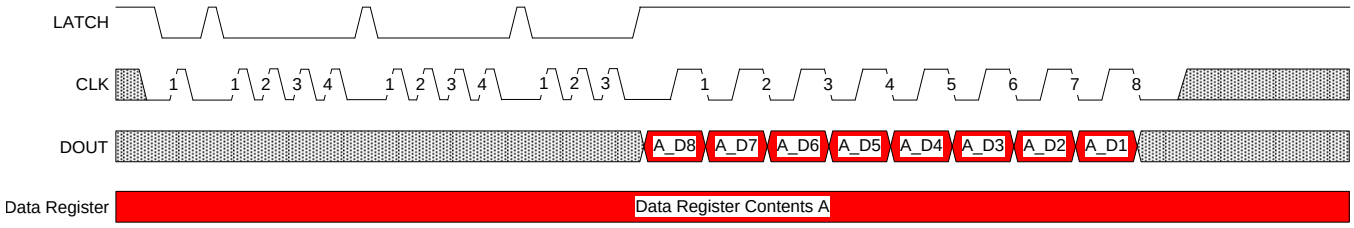


Figure 24. Reading Data Register – Single Device

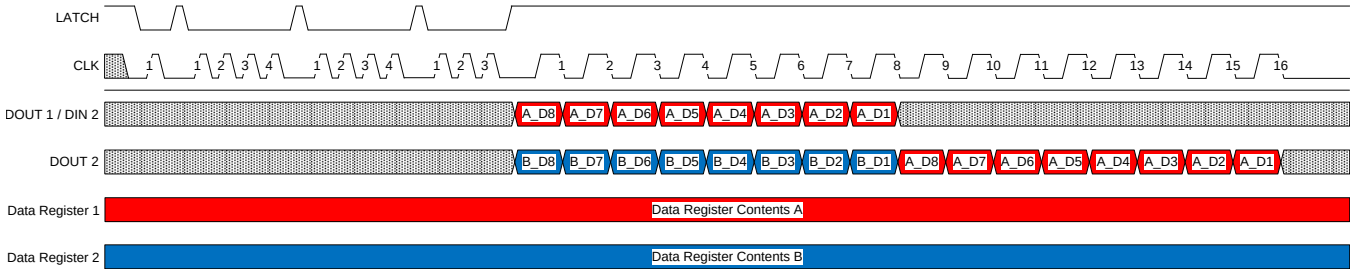


Figure 25. Reading Data Register – Daisy Chain

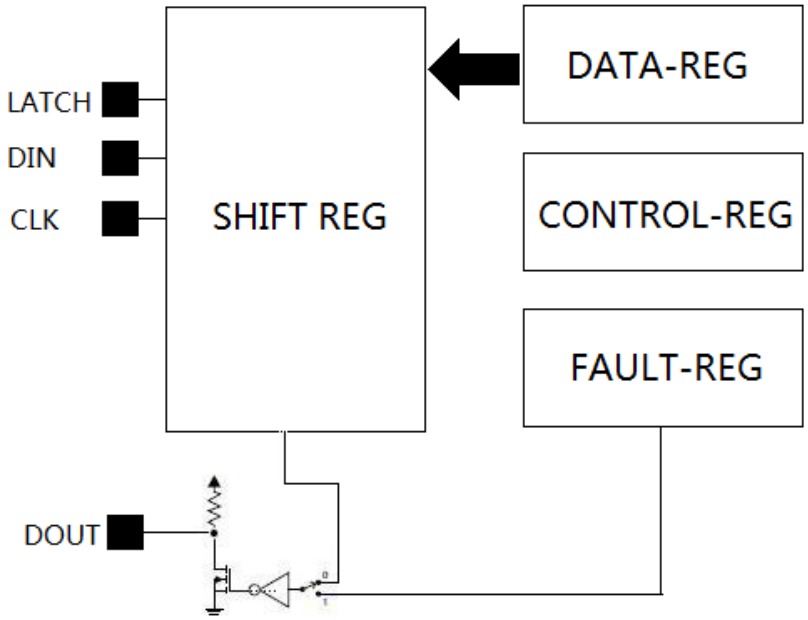


Figure 26. Reading Data Register – Data Flow

8.5.1.3.4 Special command: Fault Register Reset

When Fault-Register-Reset command is issued, internal 16bit fault register will be cleared. System can use this method to clear out all fault condition in every chained device at once.

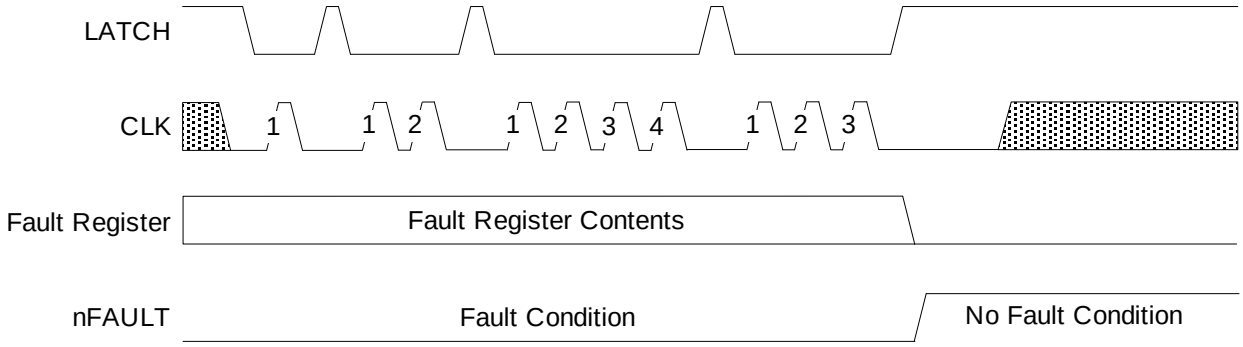


Figure 27. Fault Register Reset

8.5.1.3.5 Special command: PWM Start

When Fault-Register-Reset command is issued, output channel will ignore energizing time and directly enter into PWM mode following the setting in control register.

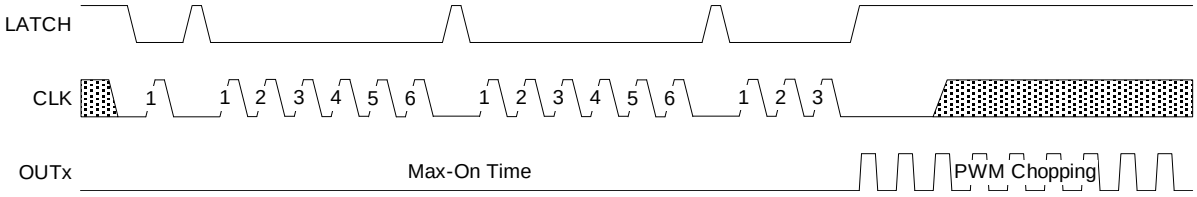


Figure 28. PWM Start Command

8.5.1.4 Output Energizing and PWM Control

The device output is defined by two stages: Energizing Phase and PWM Phase.

During the Energizing phase, the channel is turned on with 100% duty cycle for a duration set by Control register bits C4:C1.

In PWM chopping phase, with the PWM Duty Cycle defined by Control register bits C7:C5.

The behavior of each bit in the Control Register is described in Table 4.

Table 4. Control Register Settings

C8	C7	C6	C5	C4	C3	C2	C1	Value	DESCRIPTION	
0	X	X	X	X	X	X	X	N/A	Outputs always in Energizing mode	
1	X	X	X	0	0	0	0	0 ms	No Energizing, starts in PWM chopping	
1	X	X	X	0	0	0	1	3 ms	Sets the Energizing Time (100% duty cycle) before switching to PWM Phase	
1	X	X	X	0	0	1	0	5 ms		
1	X	X	X	0	0	1	1	10 ms		
1	X	X	X	0	1	0	0	15 ms		
1	X	X	X	0	1	0	1	20 ms		
1	X	X	X	0	1	1	0	30 ms		
1	X	X	X	0	1	1	1	50 ms		
1	X	X	X	1	0	0	0	80 ms		
1	X	X	X	1	0	0	1	110 ms		
1	X	X	X	1	0	1	0	140 ms		
1	X	X	X	1	0	1	1	170 ms		
1	X	X	X	1	1	0	0	200 ms		
1	X	X	X	1	1	0	1	230 ms		
1	X	X	X	1	1	1	0	260 ms		
1	X	X	X	1	1	1	1	300 ms		
1	0	0	0	X	X	X	X	0%	Output is off after Energizing Phase	
1	0	0	1	X	X	X	X	12.50%	12.5 kHz	Sets PWM chopping duty cycle. DC is the duty cycle that the low-side FET is on.
1	0	1	0	X	X	X	X	25.00%	25 kHz	
1	0	1	1	X	X	X	X	37.50%	50 kHz	
1	1	0	0	X	X	X	X	50.00%		
1	1	0	1	X	X	X	X	62.50%		
1	1	1	0	X	X	X	X	75.00%		
1	1	1	1	X	X	X	X	87.50%		

There are five operation cases as described in Figure 29 through Figure 33.

The output is turned on with 100% duty cycle.

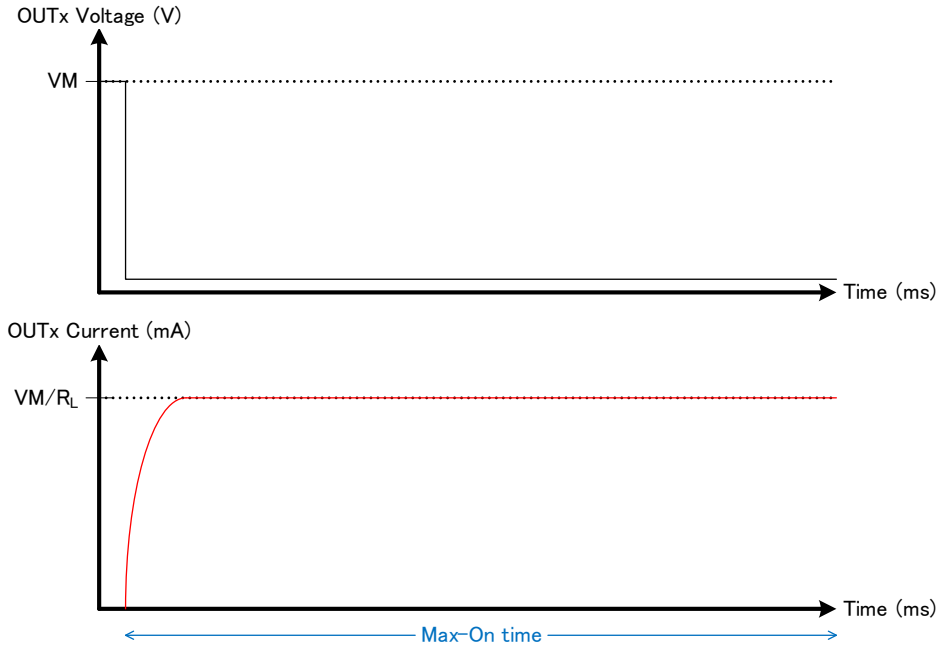


Figure 29. Case 1: Timer Enable Bit (C8) is 0 (Default Value)

The output is turned on in PWM chopping mode with duty cycle defined by Control register bits C7:C5.

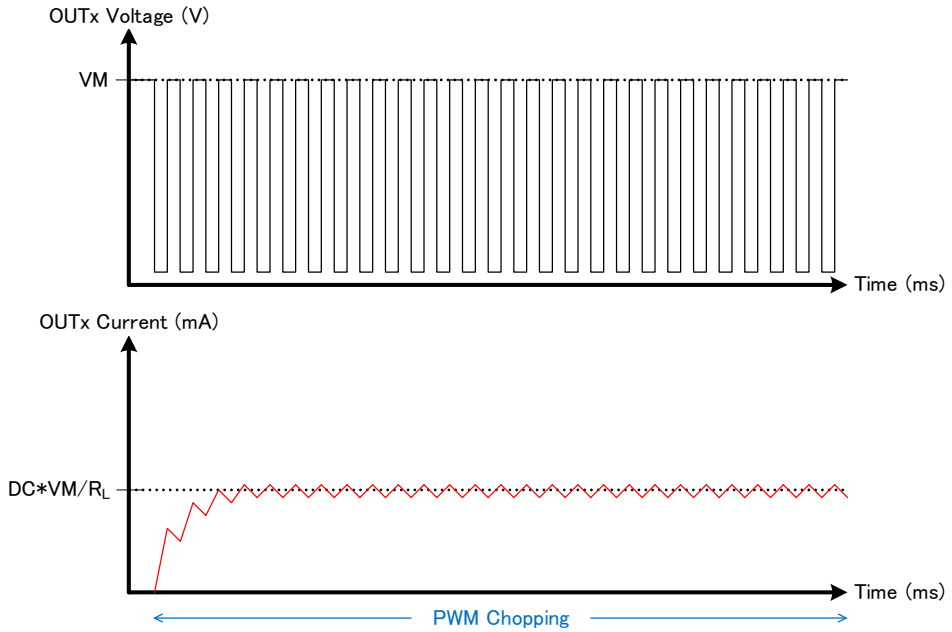


Figure 30. Case 2: Timer Enable Bit (C8) is 1 and Energizing Timing Bits (C4:C1) are 0000

The output is turned on in Energizing mode with 100% duty cycle for a duration set by Control register bits C4:C1. After the timer expires, the output switches to PWM chopping mode with PWM Duty Cycle defined by Control register bits C7:C5.

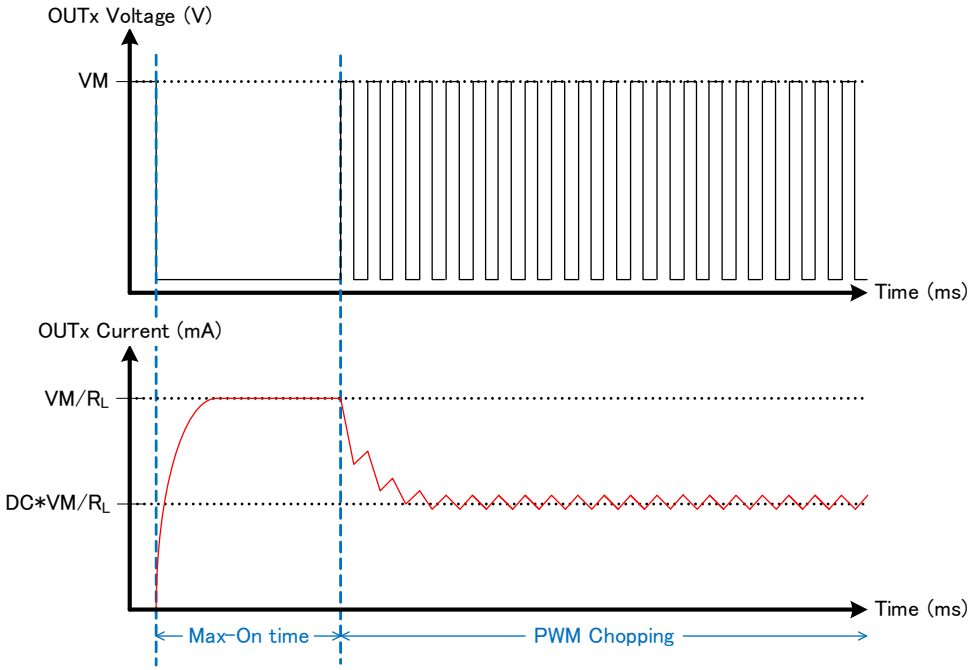


Figure 31. Case 3: Timer Enable Bit (C8) is 1, Energizing Timing Bits (C4:C1) are NOT 0000, and PWM Duty Bits (C7:C5) are NOT 000

The output is turned on in Energizing mode with 100% duty cycle for a duration set by Control register bits C4:C1. After the timer expires, the output is turned off.

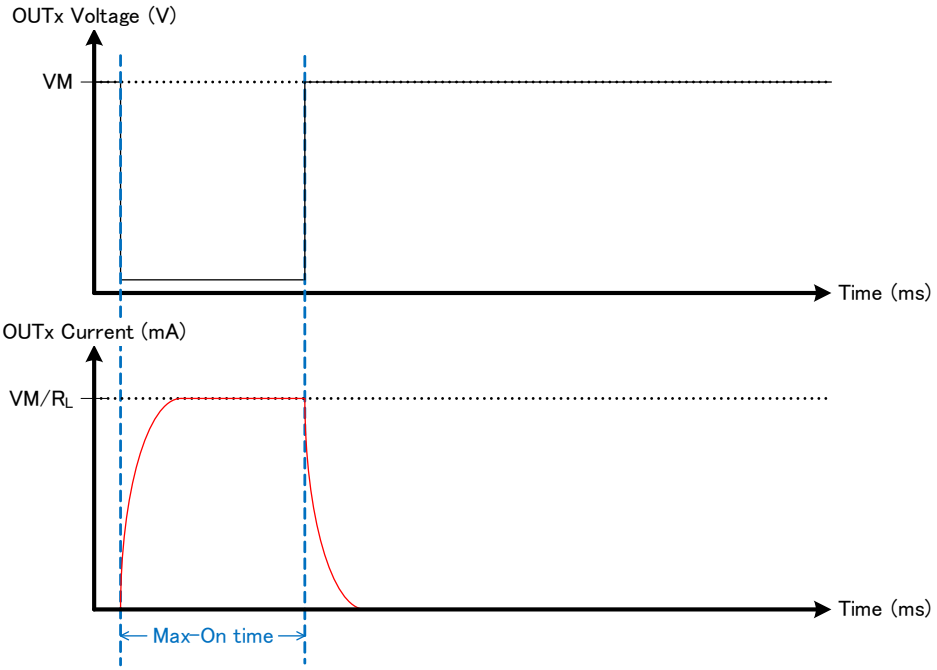


Figure 32. Case 4: Timer Enable Bit (C8) is 1, Energizing Timing Bits (C4:C1) are NOT 0000, and PWM Duty Bits (C7:C5) are 00

8.5.1.4.1 PWM Start Special Command Used

The output is turned on in Energizing mode with 100% duty cycle, and a timer is enabled with duration set by Control register bits C4:C1. If the PWM Start special command is received before the timer expires, then the output switches to PWM chopping mode with PWM Duty Cycle defined by Control register bits C7:C5. If the timer expires and no PWM Start is received, then the device will stay in Energizing mode regardless of other PWM Start commands.

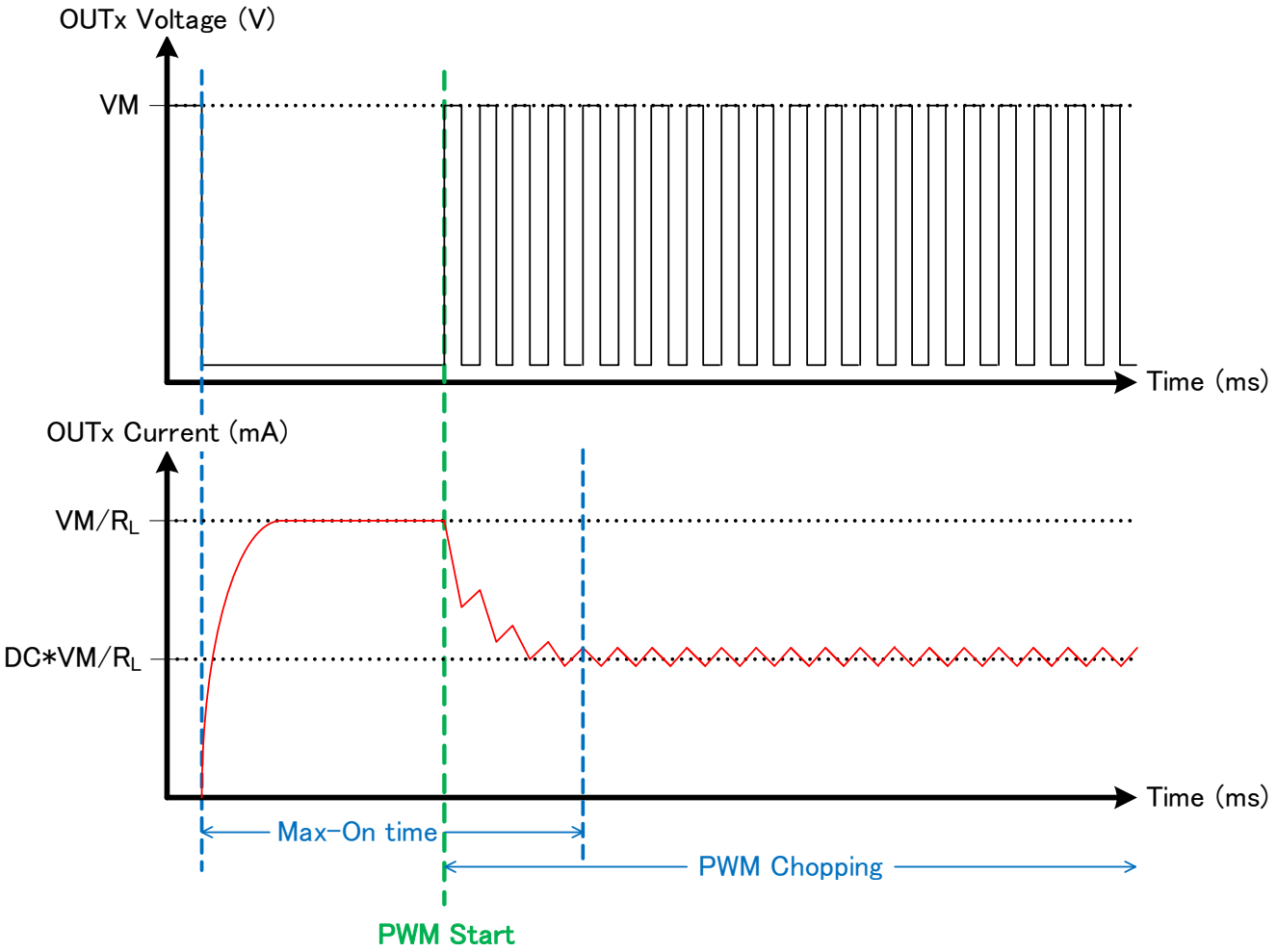


Figure 33. Case 5: Timer Enable Bit (C8) is 0, Energizing Timing Bits (C4:C1) are NOT 0000, and PWM Duty Bits (C7:C5) are NOT 000

8.6 Register Maps

8.6.1 Data Register

The Data register is used to control the status of each of the eight outputs:

Figure 34. Data Register

D8	D7	D6	D5	D4	D3	D2	D1
OUT8	OUT7	OUT6	OUT5	OUT4	OUT3	OUT2	OUT1
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

When any bit is '1', the corresponding output will be active. When any bit is '0', the output will be inactive.

The data register is the default write location for the serial interface. In order to read back data from this register, the Data Register Readout special command is used.

8.6.2 Fault Register

The Fault register can be read to determine if any channel exist fault condition. OCP is an overcurrent fault and OLD is an open load fault. OLD is not included on the DRV8860A

Figure 35. Fault Register

F16	F15	F14	F13	F12	F11	F10	F9
OUT8 OCP	OUT7 OCP	OUT6 OCP	OUT5 OCP	OUT4 OCP	OUT3 OCP	OUT2 OCP	OUT1 OCP
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
F8	F7	F6	F5	F4	F3	F2	F1
OUT8 OL	OUT7 OL	OUT6 OL	OUT5 OL	OUT4 OL	OUT3 OL	OUT2 OL	OUT1 OL
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

When any fault occurs, nFAULT pin will be driven low and corresponding Fault register bit will be set up as '1'. OCP is a flag indicating overcurrent fault. ODP is a flag indicating open load fault.

Fault bits can be reset by two approaches:

1. Special command 'FAULT RESET' clear all fault bits.
2. Setting Data register to ON will clear corresponding OLD bits (DRV8860 only)
   Setting Data register to OFF will clear corresponding OCP bits.

8.6.3 Control Register

The Control register is used to adjust the Energizing Time and PWM Duty Cycle of outputs:

Figure 36. Control Register

C8	C7	C6	C5	C4	C3	C2	C1
Over All Enable	PWM Duty Cycle control			Energizing Time control			
R/W	R/W			R/W			

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Special command 'WRITE CONTROL REGISTER' is used to program control register.

Special command 'READ CONTROL REGISTER' is used to read back control register content.

9 Application and Implementation

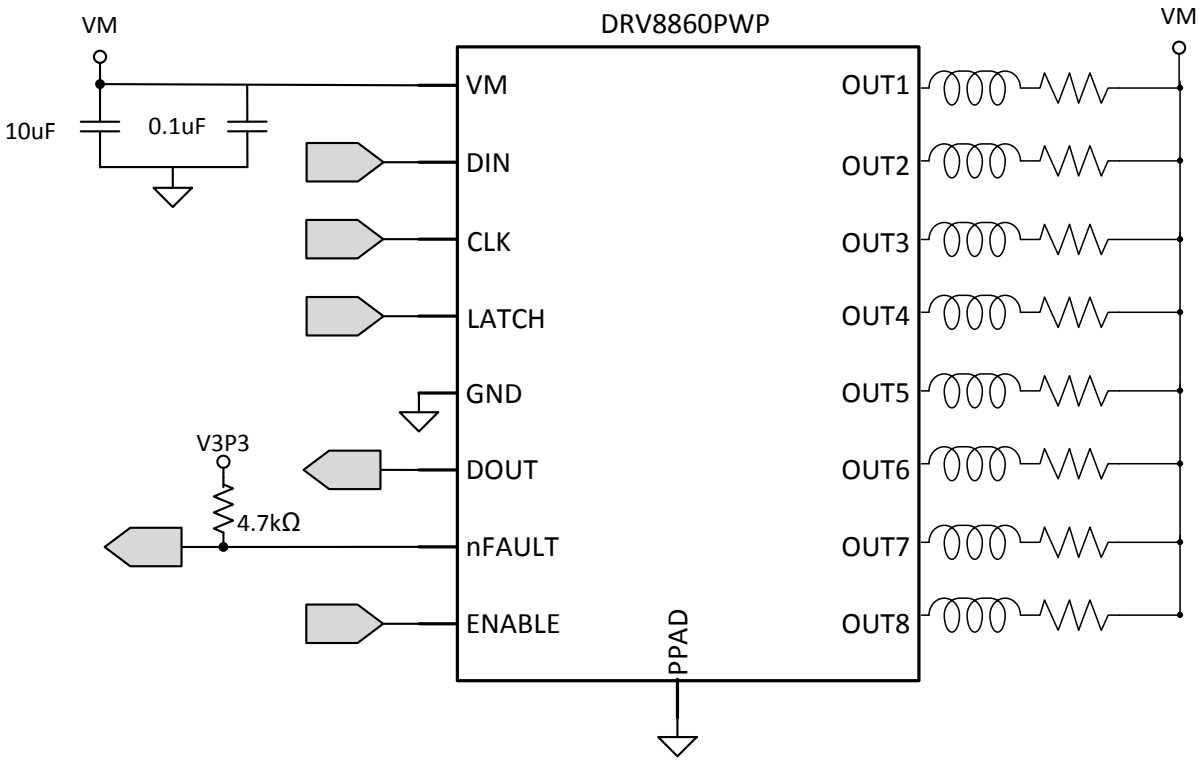
NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The DRV8860 is an eight channel low side driver with protection features. The following design is a common application of the DRV8860.

9.2 Typical Application



9.2.1 Design Requirements

Table 5. Design Parameters

Parameter	Value
Input voltage range	8 V – 38 V
Current	330 mA per channel

9.2.2 Detailed Design Procedure

9.2.2.1 Drive Current

The current path is from VM, through the load, into the low-side sinking driver. Power dissipation I^2R losses in one sink are calculated using Equation 1.

$$P_D = I^2 \times R_{DS(on)} \quad (1)$$

9.2.3 Application Curves

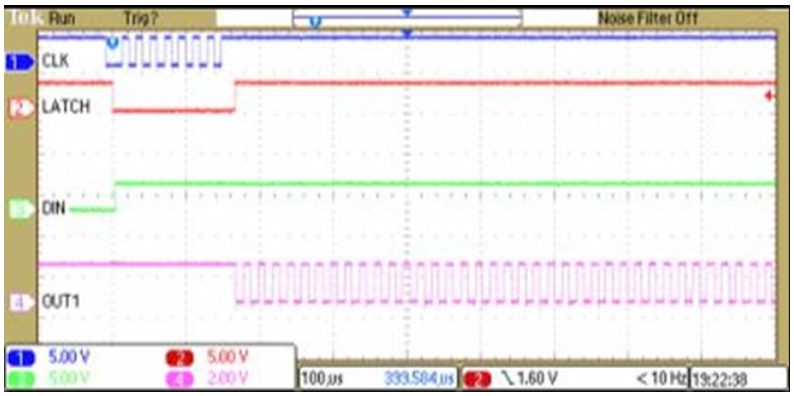


Figure 37. PWM Operation

10 Power Supply Recommendations

The DRV8860 is designed to operate from an input voltage supply (VM) range between 8 and 38 V. A 0.1-µF ceramic capacitor rated for VM must be placed as close as possible to the VM pin. In addition to the local decoupling cap, additional bulk capacitance is required and must be sized accordingly to the application requirements.

Bulk capacitance sizing is an important factor in motor drive system design. It is dependent on a variety of factors including:

- Type of power supply
- Acceptable supply voltage ripple
- Parasitic inductance in the power supply wiring
- Type of load
- Load startup current

The inductance between the power supply and motor drive system will limit the rate current can change from the power supply. If the local bulk capacitance is too small, the system will respond to excessive current demands or dumps from the motor with a change in voltage. The user should size the bulk capacitance to meet acceptable voltage ripple levels.

The datasheet generally provides a recommended value but system level testing is required to determine the appropriate sized bulk capacitor.

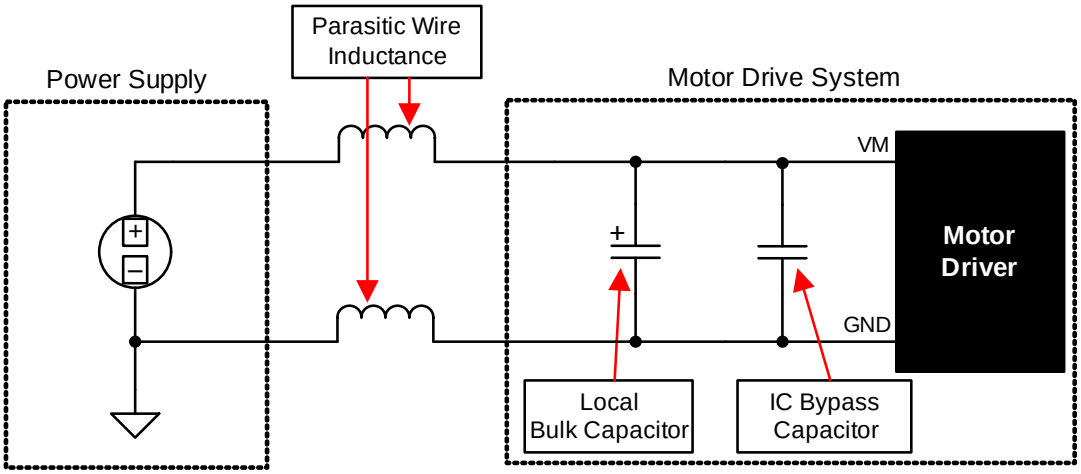


Figure 38. Example Setup of Motor Drive System with External Power Supply

10.1 Power Supply and Logic Sequencing

There is no specific sequence for powering-up the DRV8860. It is okay for digital input signals to be present before VM is applied. After VM is applied to the DRV8860, it begins operation based on the status of the control pins.

11 Layout

11.1 Layout Guidelines

- The VM pin should be bypassed to GND using a low-ESR ceramic bypass capacitor with a recommended value of 0.1-µF rated for VM.
- This capacitor should be placed as close as possible to the VM pin on the device with a thick trace or ground plane connection to the device GND pin.
- The VM pin must be bypassed to ground using and appropriate bulk capacitor. This component must be located close to the DRV8860.

11.2 Layout Example

Where the pull-up voltage (V3P3) is an external supply in the range of the recommended operating conditions for the digital open-drain outputs.

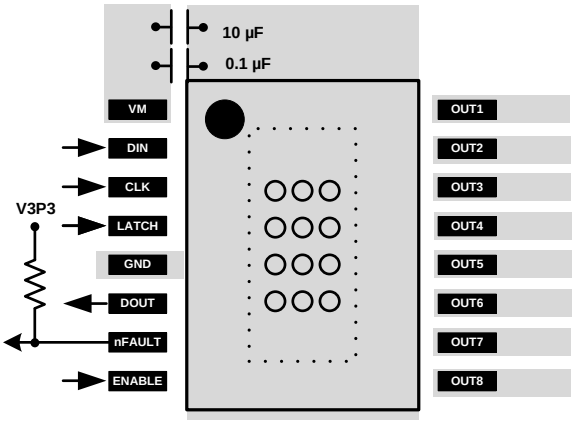


Figure 39. DRV8860 Layout

11.3 Thermal Consideration

The DRV8860 device has thermal shutdown (TSD) as described in the *Thermal Shutdown (TSD)* section. If the die temperature exceeds approximately 150°C, the device is disabled until the temperature drops to a safe level.

Any tendency of the device to enter TSD is an indication of either excessive power dissipation, insufficient heatsinking, or too high of an ambient temperature.

11.3.1 Power Dissipation

Power dissipation in the DRV8860 device is dominated by the power dissipated in the output FET resistance, $R_{DS(on)}$. Use the following equation to calculate the estimated average power dissipation of each output when running a driving a load.

$$P_D = R_{DS(on)} \times I_O^2 \quad (2)$$

where:

- P_D is the power dissipation of one channel
- $R_{DS(on)}$ is the resistance of each FET
- I_O is the RMS output current being applied to each channel

I_O is equal to the average current into the channel. Note that at startup, this current is much higher than normal running current; these peak currents and their duration must be also be considered.

The total device dissipation is the power dissipated in each channel added together.

The maximum amount of power that can be dissipated in the device is dependent on ambient temperature and heatsinking.

NOTE

$R_{DS(on)}$ increases with temperature, so as the device heats, the power dissipation increases. This fact must be taken into consideration when sizing the heatsink.

11.3.2 Heatsinking

The PowerPAD package uses an exposed pad to remove heat from the device. For proper operation, this pad must be thermally connected to copper on the PCB to dissipate heat. On a multi-layer PCB with a ground plane, this connection can be accomplished by adding a number of vias to connect the thermal pad to the ground plane.

On PCBs without internal planes, a copper area can be added on either side of the PCB to dissipate heat. If the copper area is on the opposite side of the PCB from the device, thermal vias are used to transfer the heat between top and bottom layers.

For details about how to design the PCB, refer to the TI application report, *PowerPAD™ Thermally Enhanced Package* (SLMA002), and the TI application brief, *PowerPAD Made Easy™* (SLMA004), available at www.ti.com. In general, the more copper area that can be provided, the more power can be dissipated.

12 Device and Documentation Support

12.1 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

12.2 Trademarks

PowerPAD, E2E are trademarks of Texas Instruments.
All other trademarks are the property of their respective owners.

12.3 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

12.4 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
DRV8860APW	ACTIVE	TSSOP	PW	16	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	8860A	Samples
DRV8860APWR	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	8860A	Samples
DRV8860PW	ACTIVE	TSSOP	PW	16	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	8860	Samples
DRV8860PWPR	ACTIVE	HTSSOP	PWP	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 85	8860PWP	Samples
DRV8860PWR	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	8860	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

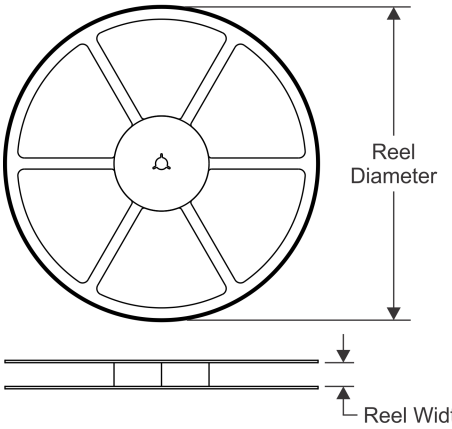
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

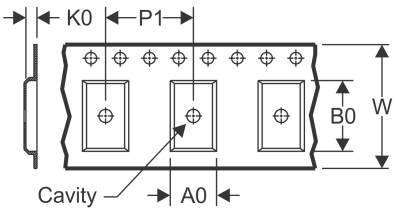
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

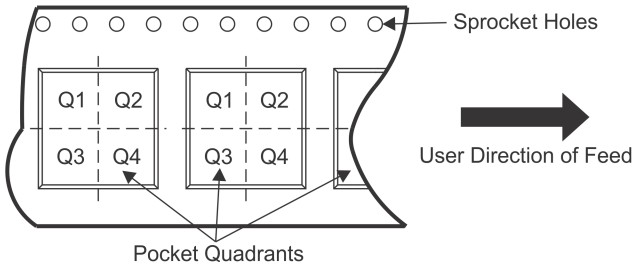


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

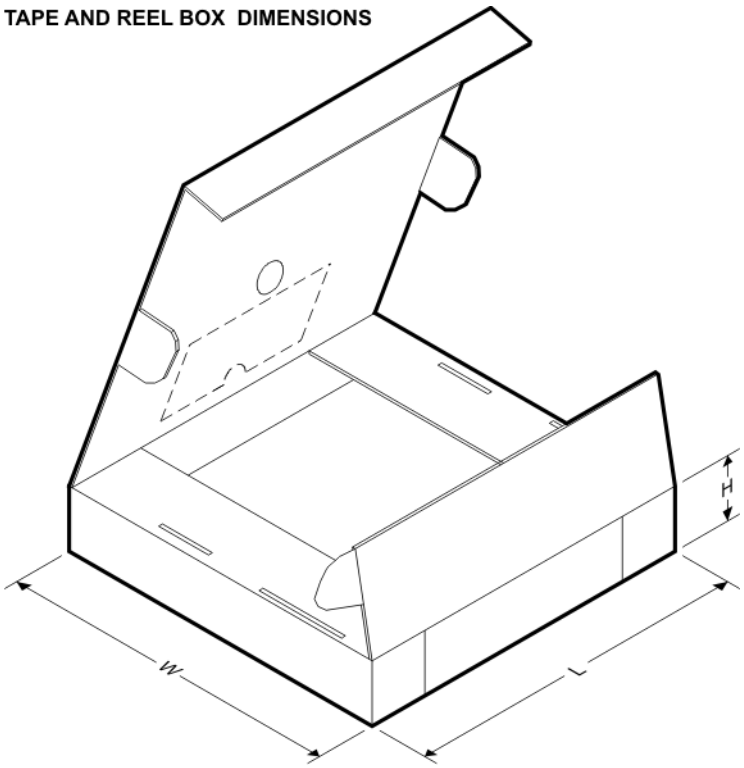
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
DRV8860APWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
DRV8860PWPR	HTSSOP	PWP	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
DRV8860PWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

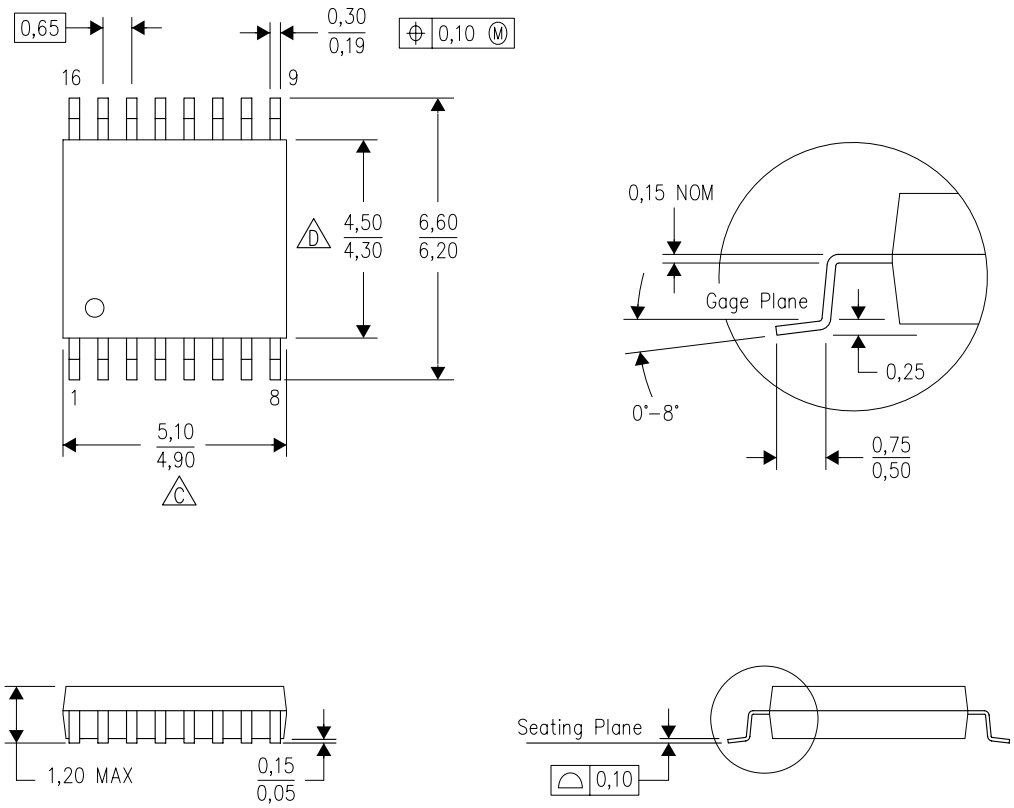
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
DRV8860APWR	TSSOP	PW	16	2000	367.0	367.0	38.0
DRV8860PWPR	HTSSOP	PWP	16	2000	367.0	367.0	38.0
DRV8860PWR	TSSOP	PW	16	2000	367.0	367.0	38.0

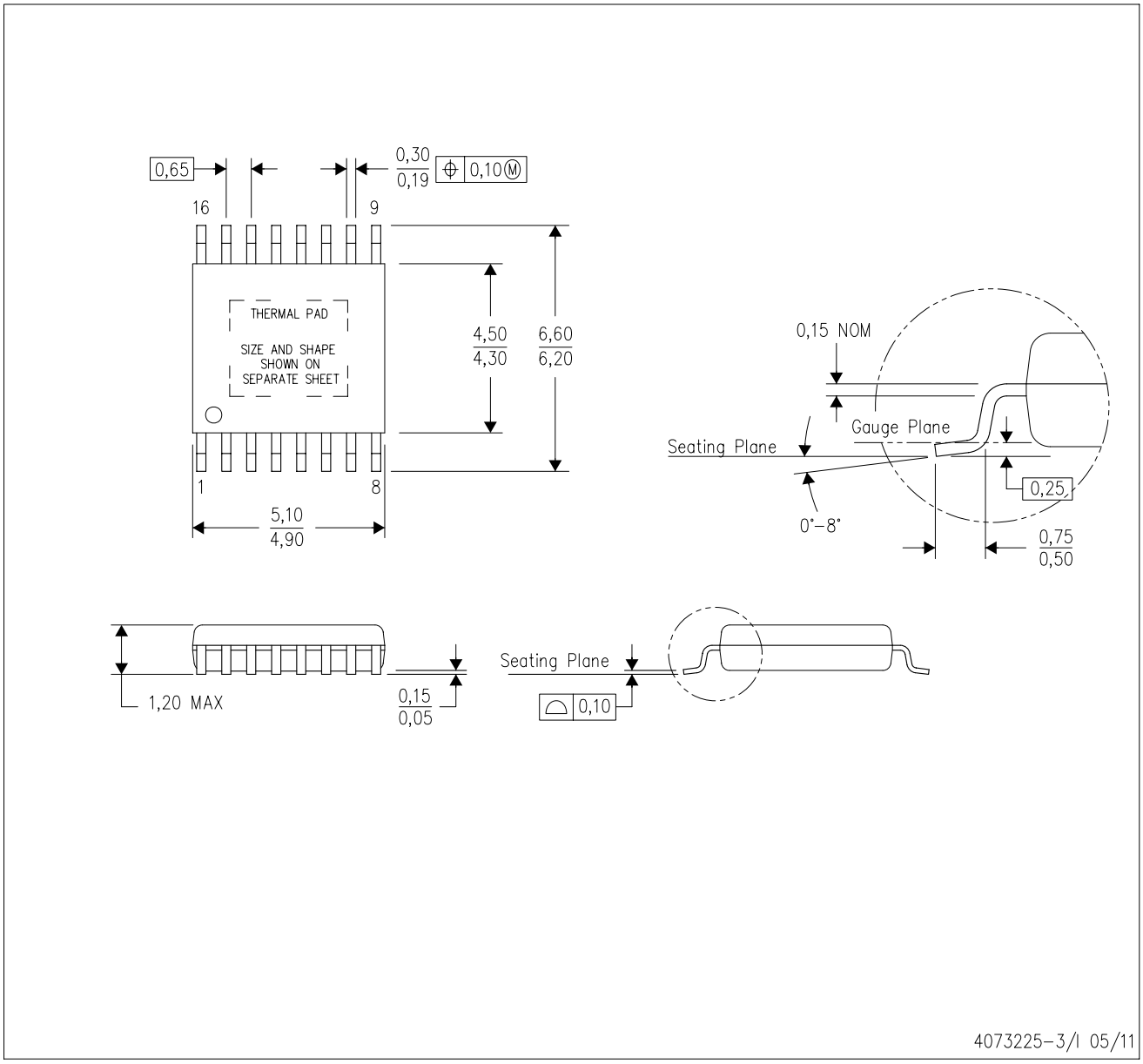
PW (R–PDSO–G16) PLASTIC SMALL OUTLINE



4040064–4/G 02/11

NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
E. Falls within JEDEC MO–153

PWP (R–PDSO–G16) PowerPAD™ PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusions. Mold flash and protrusion shall not exceed 0.15 per side.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 for information regarding recommended board layout. This document is available at www.ti.com <http://www.ti.com>.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
E. Falls within JEDEC MO–153

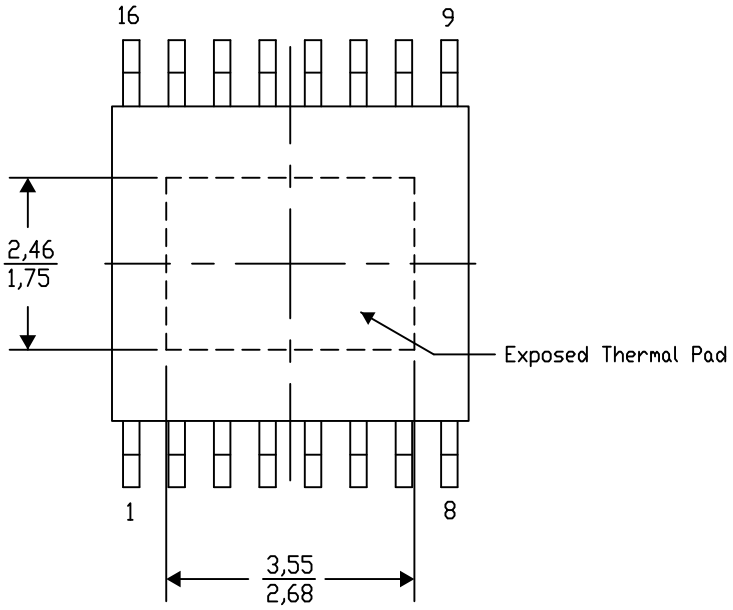
PWP (R–PDSO–G16) PowerPAD™ SMALL PLASTIC OUTLINE

THERMAL INFORMATION

This PowerPAD™ package incorporates an exposed thermal pad that is designed to be attached to a printed circuit board (PCB). The thermal pad must be soldered directly to the PCB. After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For additional information on the PowerPAD package and how to take advantage of its heat dissipating abilities, refer to Technical Brief, PowerPAD Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 and Application Brief, PowerPAD Made Easy, Texas Instruments Literature No. SLMA004. Both documents are available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



Top View

Exposed Thermal Pad Dimensions

4206332–51/AO 01/16

NOTE: A. All linear dimensions are in millimeters

PowerPAD is a trademark of Texas Instruments

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