# PRESSURE SENSOR SIGNAL CONDITIONER

## 1 DEVICE OVERVIEW

### 1.1 FEATURES

- Analog Features
  - Analog Front-End for Resistive Bridge Sensors
  - Self-Oscillating Demodulator for Capacitive Sensors
  - On-Chip Temperature Sensor
  - Programmable Gain
  - 16-Bit, 1MHz Sigma-Delta Analog-to-Digital Converter for Signal Channel
  - 10-Bit Sigma-Delta Analog-to-Digital Converter for Temperature Channel
  - Two 12–Bit DAC Outputs
- Digital Features
  - Microcontroller Core
    - 10 MHz 8051 WARP Core
      - 2 Clocks Per Instruction Cycle
    - On–Chip Oscillator
  - Memory
    - 8 KB of OTP Memory
    - 89 Bytes of EEPROM
    - 256 Bytes Data SRAM
- Peripheral Features
  - Serial Peripheral Interface (SPI™)
  - Inter-Integrated Circuit ($I^2C$™)
  - One-Wire Interface
  - Two Input Capture Ports
  - Two Output Compare Ports
  - Software Watchdog Timer
  - Oscillator Watchdog
  - Power Management Control
  - Analog Low-Voltage Detect
- General Features
  - Power Supply: 4.5 V to 5.5 V Operational, –5.5 V to 16 V Abs Max
  - PVQFN-36 package

### 1.2 APPLICATIONS

- Pressure Sensor Signal Conditioning
- Level Sensor Signal Conditioning
- Humidity Sensor Signal Conditioning

### 1.3 SUPPORTS INDUSTRIAL SENSING APPLICATIONS

- Controlled Baseline
- One Assembly and Test Site
- One Fabrication Site
- Extended Product Life Cycle
- Extended Product-Change Notification
- Product Traceability

### DEVICE OVERVIEW

The PGA400-EP is an interface device for piezoresistive, strain gauge and capacitive sense elements. The device incorporates the analog front end that directly connects to the sense element and has voltage regulators and oscillator. The device also includes sigma-delta analog-to-digital converter, 8051 WARP core microprocessor and OTP memory. Sensor compensation algorithms can be implemented in software. The PGA400-EP also includes 2 DAC outputs.

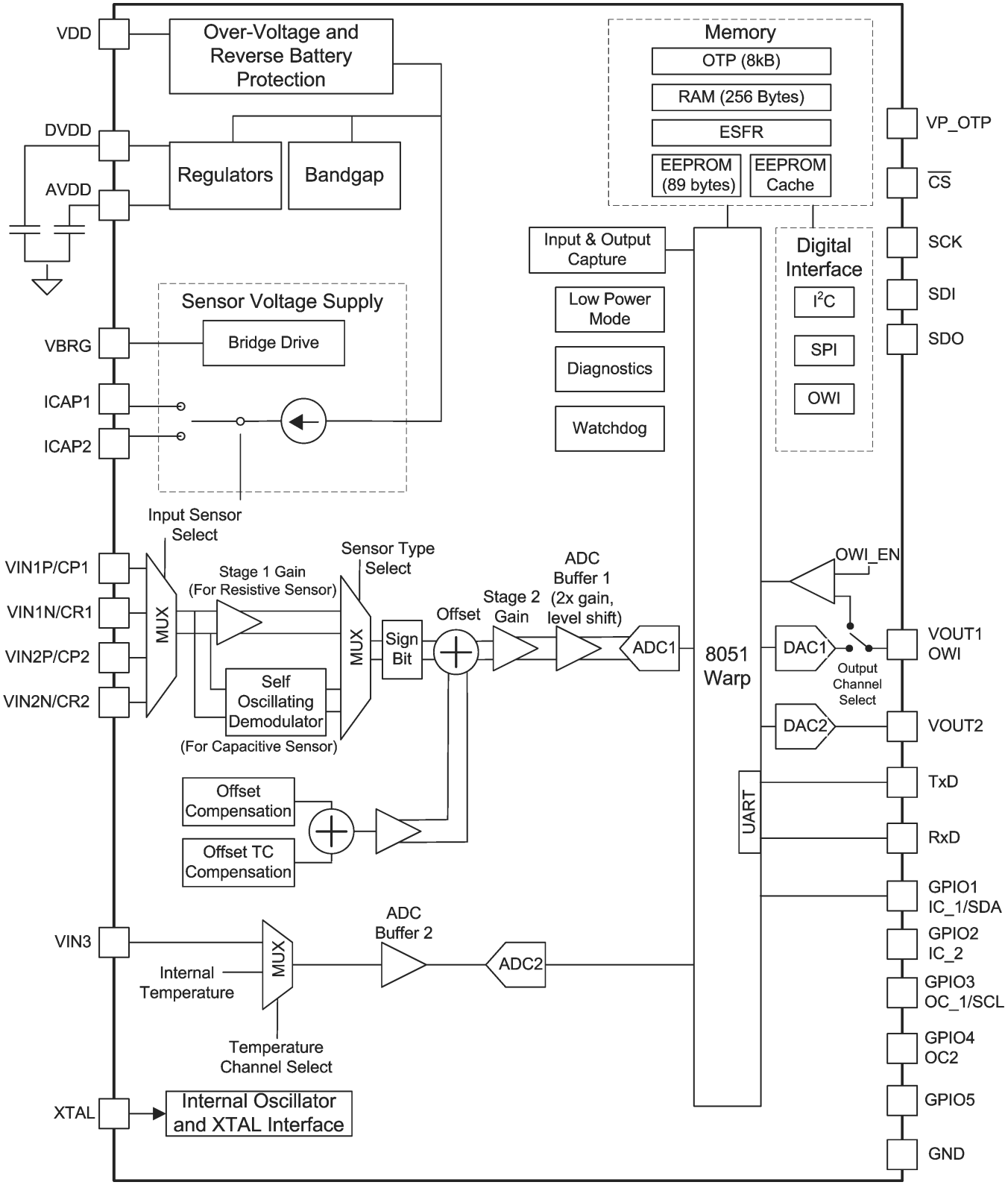
### 1.1 ORDERING INFORMATION(1)

| $T_A$ | PACKAGE(2) | ORDERABLE PART NUMBER | TOP-SIDE MARKING | VID NUMBER |
|---|---|---|---|---|
| –40°C to 125°C | PVQFN (RHH) | PGA400QRHHTEP | PGA400QRHH-EP | V62/13619-01XE |

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI website at www.ti.com.
(2) Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

## 2 FUNCTIONAL BLOCK DIAGRAM





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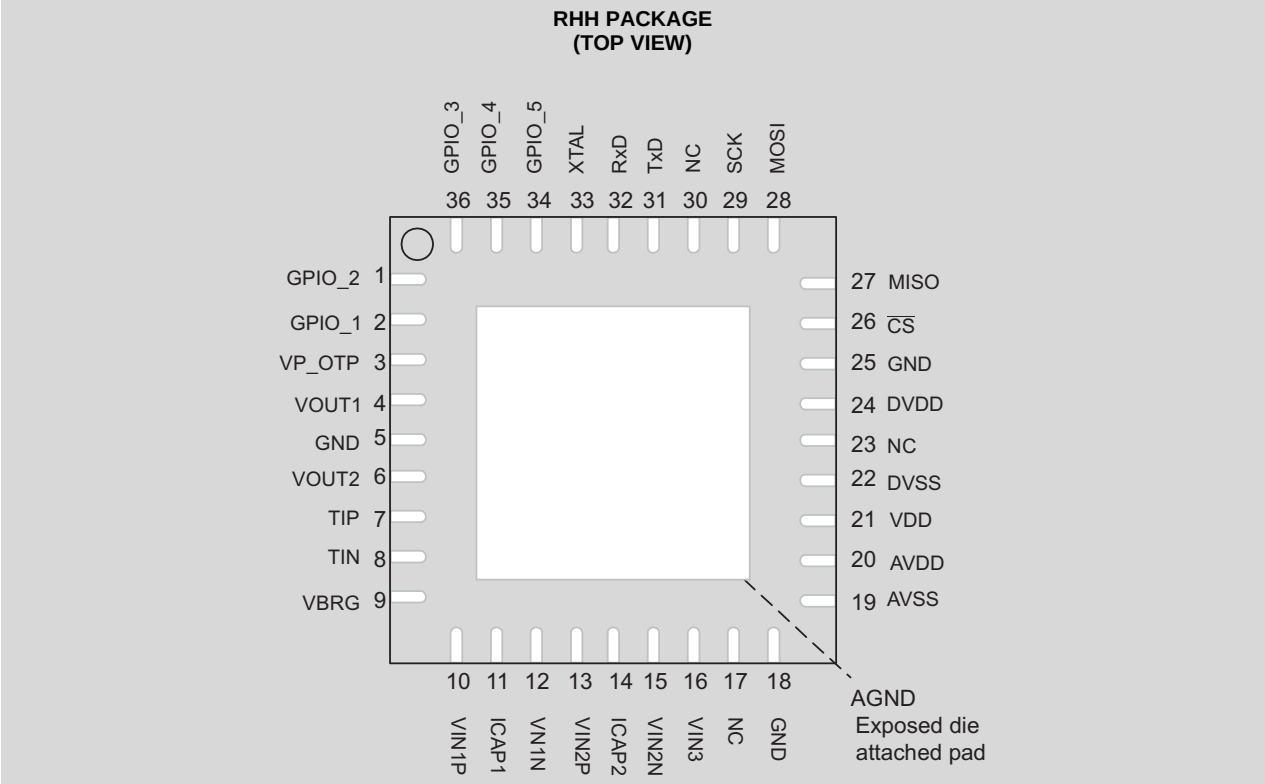
# 3 DEVICE INFORMATION




## PIN DESCRIPTIONS

| NAME | NO. | DESCRIPTION |
|---|---|---|
| GPIO_2 | 1 | General purpose IO 2 / input capture port 2 |
| GPIO_1 | 2 | General purpose IO 1 / input capture port 1 / I2C Data |
| VT_OTP | 3 | One-time programmable memory programming voltage |
| VOUT1 | 4 | DAC1 output / One-wire interface |
| GND | 5, 18, 25 | Ground |
| VOUT2 | 6 | DAC2 output |
| TIP | 7 | Test pin reserved |
| TIN | 8 | Test pin reserved |
| VBRG | 9 | Resistive bridge supply voltage |
| VIN1P | 10 | Resistive sensor 1 positive input / capacitive sensor 1 positive input |
| ICAP1 | 11 | Capacitive sensor drive current 1 |
| VIN1N | 12 | Resistive sensor 1 negative input / capacitive sensor 1 reference input |
| VIN2P | 13 | Resistive sensor 2 positive input / capacitive sensor 2 positive input |
| ICAP2 | 14 | Capacitive sensor drive current 2 |
| VIN2N | 15 | Resistive sensor 2 negative input / capacitive sensor 2 reference input |
| VIN3 | 16 | External temperature sensor input |
| NC | 17, 23, 30 | No connect |
| AVSS | 19 | Ground |
| AVDD | 20 | Linear regulator output for internal analog circuit supply |
| VDD | 21 | Input power supply |
| DVSS | 22 | Ground |
| DVDD | 24 | Linear regulator output for internal digital circuit supply |
| $\overline{CS}$ | 26 | Serial peripheral interface chip select |

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## PIN DESCRIPTIONS (continued)

| NAME | NO. | DESCRIPTION |
|---|---|---|
| MISO | 27 | Serial peripheral interface slave data out |
| MOSI | 28 | Serial peripheral interface slave data in |
| SCK | 29 | Serial peripheral interface clock |
| TxD | 31 | 8051 UART Tx (Port 3_1) |
| RxD | 32 | 8051 UART Rx (Port 3_0) |
| XTAL | 33 | XTAL External crystal input |
| GPIO5 | 34 | General purpose IO 5 |
| GPIO4 | 35 | General purpose IO 4 / output compare port 2 |
| GPIO3 | 36 | General purpose IO 3 / output compare port 1 / I2C Clock |


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# 4 ABSOLUTE MAXIMUM RATINGS

## 4.1 ABSOLUTE MAXIMUM RATINGS(1)

| PARAMETER | | MIN | MAX | UNIT |
|---|---|---|---|---|
| VDD, Continuous | Power Supply Voltage | –5.5 | 16 | V |
| | Voltage at VP_OTP | –0.3 | 8.0 | V |
| | Voltage at sensor input and drive pins | –0.3 | 3.6 | V |
| | Voltage at any IO pin except at VOUT1/OWI | –0.3 | VDD + 0.3 | V |
| | Voltage at VOUT1/OWI pin | –0.3 | 7.5 | V |
| $I_{DD}$, Short on VOUT1 or VOUT2 | Supply Current | –45 | 45 | mA |
| Iout1, Iout2 | Output Current | –30 | 30 | mA |
| ESD | Human Body Model (HBM) | ±2 | | KV |
| | Field Induced Charge Device Model (CDM) | ±500 | | V |
| $T_{jmax}$ | Maximum Junction Temperature | | 150 | °C |
| $T_{stg}$ | Storage Temperature | –40 | 150 | °C |

(1) Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "Recommended Operating Conditions" are not implied. Exposure to Absolute-Maximum-Rated conditions for extended periods may affect device reliability.

## 4.2 THERMAL INFORMATION

| THERMAL METRIC | | PGA400-EP RHH 36 PINS | UNITS |
|---|---|---|---|
| $\theta_{JA}$ | Junction-to-ambient thermal resistance(1) | 30.6 | °C/W |
| $\theta_{JCtop}$ | Junction-to-case (top) thermal resistance(2) | 16.4 | |
| $\theta_{JB}$ | Junction-to-board thermal resistance(3) | 5.4 | |
| $\psi_{JT}$ | Junction-to-top characterization parameter(4) | 0.2 | |
| $\psi_{JB}$ | Junction-to-board characterization parameter(5) | 5.4 | |
| $\theta_{JCbot}$ | Junction-to-case (bottom) thermal resistance(6) | 0.7 | |

(1) The junction-to-ambient thermal resistance under natural convection is obtained in a simulation on a JEDEC-standard, high-K board, as specified in JESD51-7, in an environment described in JESD51-2a.
(2) The junction-to-case (top) thermal resistance is obtained by simulating a cold plate test on the package top. No specific JEDEC-standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.
(3) The junction-to-board thermal resistance is obtained by simulating in an environment with a ring cold plate fixture to control the PCB temperature, as described in JESD51-8.
(4) The junction-to-top characterization parameter, $\psi_{JT}$, estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining $\theta_{JA}$, using a procedure described in JESD51-2a (sections 6 and 7).
(5) The junction-to-board characterization parameter, $\psi_{JB}$, estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining $\theta_{JA}$ , using a procedure described in JESD51-2a (sections 6 and 7).
(6) The junction-to-case (bottom) thermal resistance is obtained by simulating a cold plate test on the exposed (power) pad. No specific JEDEC standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.

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## 4.3 RECOMMENDED OPERATING CONDITIONS

over operating free-air temperature range (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $V_{DD}$ | Power supply voltage | | 4.5 | 5 | 5.5 | V |
| $I_{DD}$ | Power supply current - normal mode | $V_{DD}$ = 5V, No load on VBRG, No load on DAC1 and DAC2 | | | 13.6 | mA |
| | Power supply current - low power mode | $V_{DD}$ = 5.5V, No load on VBRG, No load on DAC1 and DAC2, AFE turned OFF | | | 9.5 | mA |
| VP_OTP | OTP programming voltage | | 7.0 | 7.4 | 7.8 | V |
| I_VP_OTP | OTP programming current | During OTP Programming | | | 3 | mA |
| tprog_OTP | OTP programming timing per byte | | 120 | | | µs |
| $T_A$ | Operating ambient temperature | | –40 | | 125 | °C |
| | Programming temperature | OTP or EEPROM | –40 | | 140 | °C |
| | Micro start-up time | VDD ramp rate 1V/µs | | | 250 | µs |


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# 5 ELECTRICAL CHARACTERISTICS

## 5.1 Overvoltage Protection

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| OV | Overvoltage protection threshold | | 5.5 | 6.1 | 7.0 | V |
| $OV_{hyst}$ | Overvoltage protection hysteresis | | | 410 | | mV |

## 5.2 Regulators

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $V_{AVDD}$ | AVDD voltage | $C_{AVDD}$ = 100 nF | | 3.3 | | V |
| I_AVDD | AVDD current | $V_{AVDD}$ = 3.3 V | | | 5 | mA |
| $V_{DVDD}$ | DVDD voltage | No EEPROM Programming | | 3.3 | | V |
| | | EEPROM Programming | | 3.6 | | V |

## 5.3 Internal Oscillator and External Crystal Interface

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| **INTERNAL OSCILLATOR** | | | | | | |
| | Internal Oscillator frequency | $T_{amb}$ = 25 °C | 38.4 | 40 | 41.6 | MHz |
| | Internal Oscillator frequency | Accross operating temperature | 36.3 | | 43.7 | MHz |
| **EXTERNAL 40-MHZ CRYSTAL** | | | | | | |
| | Low-level input voltage on XTAL | | –0.3 | | 0.1× VDD | V |
| | High-level input voltage on XTAL | | 0.7 × VDD | | VDD + 0.3 | V |

## 5.4 Sensor Supply

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| **VBRG SUPPLY FOR RESISTIVE BRIDGE SENSORS** | | | | | | |
| $V_{BRG}$ | Supply Voltage | 0.44 kΩ ≤ $R_{BRG}$ ≤ 20 kΩ | 3.2 | 3.33 | 3.4 | V |
| $R_{BRG}$ | Resistive Bridge Resistance | | 0.44 | | 20 | KΩ |
| $C_{BRG}$ | Capacitive Load | $R_{BRG}$ = 20 kΩ | | | 500 | pF |
| | Line regulation | $V_{DD}$ = 4.5V, 5.5V, $R_{BRG}$ = 0.44 kΩ | -40 | | 40 | mV |
| | Load regulation | $V_{DD}$ = 5.0 V, 10 µA ≤ $I_{LOAD}$ ≤ 10 mA | -40 | | 40 | mV |
| **ICAPx SUPPLY FOR CAPACITIVE SENSORS** | | | | | | |
| ICAP_A | Supply Current Amplitude on ICAP, $T_A$ = 25°C | CI[2:0] = 000, ICAP_V = 100 mV | -5.3 | | -4.3 | µA |
| | | CI[2:0] = 001, ICAP_V = 100 mV | -8 | | -6.6 | |
| | | CI[2:0] = 010, ICAP_V = 100 mV | -10.8 | | -8.8 | |
| | | CI[2:0] = 011, ICAP_V = 100 mV | -13.5 | | -11.1 | |
| | | CI[2:0] = 100, ICAP_V = 100 mV | -16.2 | | -13.3 | |
| | | CI[2:0] = 101, ICAP_V = 100 mV | -18.9 | | -15.5 | |
| | | CI[2:0] = 110, ICAP_V = 100 mV | -21.6 | | -17.8 | |
| | | CI[2:0] = 111, ICAP_V = 100 mV | -24.4 | | -20.1 | |
| | | CI[2:0] = 000, ICAP_V = 3.2 V | 4.5 | | 5.6 | |
| | | CI[2:0] = 001, ICAP_V = 3.2 V | 6.9 | | 8.5 | |
| | | CI[2:0] = 010, ICAP_V = 3.2 V | 9.2 | | 11.3 | |
| | | CI[2:0] = 011, ICAP_V = 3.2 V | 11.5 | | 14.1 | |
| | | CI[2:0] = 100, ICAP_V = 3.2 V | 13.6 | | 16.7 | |
| | | CI[2:0] = 101, ICAP_V = 3.2 V | 15.8 | | 19.2 | |
| | | CI[2:0] = 110, ICAP_V = 3.2 V | 18.1 | | 22.1 | |
| | | CI[2:0] = 111, ICAP_V = 3.2 V | 20.4 | | 24.8 | |
| | Variation over temperature | | -5.0 | | +5.0 | % |
| CPx_V, CRx_V | Capacitive Sensor Drive - Voltage at CPx and CRx pins | CV[1:0] = 00 | 70 | 90 | 110 | mV |
| | | CV[1:0] = 01 | 255 | 300 | 345 | |
| | | CV[1:0] = 10 | 425 | 500 | 575 | |
| | | CV[1:0] = 11 | 595 | 700 | 805 | |
| **SELF OSCILLATING CURRENT MODE DEMODULATOR FOR CAPACITIVE SENSORS** | | | | | | |
| $R_F$ / $R_{REF}$ | Gain in Transimpedance amplifier | CR[1:0] = 00, $R_{REF}$ = 78 kΩ | -1.07 | -1.01 | -0.94 | V/V |
| | | CR[1:0] = 01, $R_{REF}$ = 78 kΩ | -2.13 | -1.97 | -1.82 | |
| | | CR[1:0] = 10, $R_{REF}$ = 78 kΩ | -4.24 | -3.93 | -3.63 | |
| | | CR[1:0] = 11, $R_{REF}$ = 78 kΩ | -8.45 | -7.85 | -7.26 | |
| Cf | Feedback Capacitor in Transimpedance amplifier | | 14 | 16 | 18 | pF |

## 5.5 Temperature Sensor

| PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|
| Temperature Range | | –55 | | 125 | °C |
| Temperature ADC Resolution | | | 10 | | bits |
| Temperature ADC Update Rate | | | 8 | | ms |
| Gain (1) | | 2.7 | 2.8 | 2.9 | LSB/°C |
| Offset (1) | | -105 | | -66 | LSB |
| Total Error | | -4 | | 4 | °C |

(1) The Temperature ADC Value is given by the equation: ADC Code = Gain*Temperature (in °C) + Offset


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## 5.6 Analog Front Ends

| PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|
| **STAGE 1 GAIN FOR RESISTIVE BRIDGE SENSORS** | | | | | |
| Gain Steps | Sx_G1[2:0] = 000 | | 3.0 | | V/V |
| | Sx_G1[2:0] = 001 | | 4.4 | | |
| | Sx_G1[2:0] = 010 | | 6.8 | | |
| | Sx_G1[2:0] = 011 | | 10.2 | | |
| | Sx_G1[2:0] = 100 | | 14.6 | | |
| | Sx_G1[2:0] = 101 | | 25.5 | | |
| | Sx_G1[2:0] = 110 | | 34.0 | | |
| | Sx_G1[2:0] = 111 | | 51.0 | | |
| Bandwidth | –3 dB, Gain = 111 | | 7 | | KHz |

## 5.7 Stage 2 Gain

| PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|
| Gain Steps | Sx_G2[4:0] = 00000 | 0.97 | 1.01 | 1.05 | V/V |
| | Sx_G2[4:0] = 00001 | 1.06 | 1.11 | 1.16 | |
| | Sx_G2[4:0] = 00010 | 1.18 | 1.23 | 1.28 | |
| | Sx_G2[4:0] = 00011 | 1.31 | 1.37 | 1.42 | |
| | Sx_G2[4:0] = 00100 | 1.45 | 1.52 | 1.58 | |
| | Sx_G2[4:0] = 00101 | 1.61 | 1.68 | 1.76 | |
| | Sx_G2[4:0] = 00110 | 1.79 | 1.87 | 1.94 | |
| | Sx_G2[4:0] = 00111 | 1.98 | 2.07 | 2.16 | |
| | Sx_G2[4:0] = 01000 | 2.20 | 2.29 | 2.39 | |
| | Sx_G2[4:0] = 01001 | 2.44 | 2.55 | 2.65 | |
| | Sx_G2[4:0] = 01010 | 2.71 | 2.83 | 2.94 | |
| | Sx_G2[4:0] = 01011 | 3.00 | 3.13 | 3.26 | |
| | Sx_G2[4:0] = 01100 | 3.34 | 3.48 | 3.62 | |
| | Sx_G2[4:0] = 01101 | 3.74 | 3.90 | 4.06 | |
| | Sx_G2[4:0] = 01110 | 4.12 | 4.30 | 4.48 | |
| | Sx_G2[4:0] = 01111 | 4.61 | 4.81 | 5.01 | |
| | Sx_G2[4:0] = 10000 | 5.09 | 5.31 | 5.54 | |
| | Sx_G2[4:0] = 10001 | 5.67 | 5.92 | 6.16 | |
| | Sx_G2[4:0] = 10010 | 6.26 | 6.52 | 6.79 | |
| | Sx_G2[4:0] = 10011 | 6.93 | 7.23 | 7.53 | |
| | Sx_G2[4:0] = 10100 | 7.70 | 8.04 | 8.37 | |
| | Sx_G2[4:0] = 10101 | 8.57 | 8.95 | 9.32 | |
| | Sx_G2[4:0] = 10110 | 9.54 | 9.96 | 10.37 | |
| | Sx_G2[4:0] = 10111 | 10.62 | 11.06 | 11.51 | |
| | Sx_G2[4:0] = 11000 | 11.76 | 12.27 | 12.79 | |
| | Sx_G2[4:0] = 11001 | 13.02 | 13.58 | 14.15 | |
| | Sx_G2[4:0] = 11010 | 14.48 | 15.10 | 15.72 | |
| | Sx_G2[4:0] = 11011 | 16.03 | 16.71 | 17.40 | |
| | Sx_G2[4:0] = 11100 | 17.72 | 18.53 | 19.34 | |
| | Sx_G2[4:0] = 11101 | 19.61 | 20.49 | 21.37 | |
| | Sx_G2[4:0] = 11110 | 21.72 | 22.70 | 23.68 | |
| | Sx_G2[4:0] = 11111 | 23.85 | 25.06 | 26.28 | |
| Bandwidth | –3 dB, Gain Setting = 11111 | 120 | | | KHz |

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## 5.8 Offset and Offset TC Compensation

| PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|
| Offset Compensation Low | Offset Setting = 0x000, Stage 1 Gain Setting = 0b000 | -385 | -324 | -279 | mV |
| Offset Compensation High | Offset Setting = 0x3FF, Stage 1 Gain Setting = 0b000 | 279 | 324 | 385 | mV |
| Offset Compensation Resolution | Stage 1 Gain Setting = 0b000 | 0.59 | | 0.72 | mV/step |
| Offset TC Compensation Low | Offset TC Setting = 0x00, Stage 1 Gain Value = 0b000 | | -371 | | µV/°C |
| Offset TC Compensation H igh | Offset TC Setting= 0x3F, Stage 1 Gain Value = 0b000 | | 361 | | µV/°C |
| Offset TC Compensation Resolution | Stage 1 Gain Value = 0b000 | | 11.6 | | µV/V/°C/step |
| Reference Temperature | | | 22 | | °C |

## 5.9 Analog to Digital Converter

| PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|
| **ADC BUFFER FOR 16-BIT AD CONVERTER 1** | | | | | |
| Gain | | 1.9 | 2 | 2.1 | V/V |
| DC Level Shift | ADC_BUF bit = 1 | -1.74 | –1.65 | -1.55 | V |
| DC Offset | | -15 | | 15 | mV |
| **ADC BUFFER FOR 10-BIT AD CONVERTER 2** | | | | | |
| VIN3 Input Voltage Range | | 0.425 | | 1.7 | V |
| Gain | | 1.09 | 1.15 | 1.21 | V/V |
| DC Offset | | -15 | | 15 | mV |
| **VIN3 VOLTAGE VERSUS ADC CODE** | | | | | |
| Gain (1) | | 740 | 760 | 780 | LSB/V |
| Offset (1) | | -850 | -820 | -790 | LSB |
| Gain Temperature Coefficient | $T_{amb}$ = 25 °C | | 0.02 | | LSB/V/°C |
| Offset Temperature Coefficient | $T_{amb}$ = 25 °C | | -0.02 | | LSB/°C |
| Integral Nonlinearity | | -1 | | 1 | LSB |

(1) ADC Code = Gain*VIN3+Offset

## 5.10 One Wire Interface

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| | Communication Baud Rate | | 2400 | | 115000 | Bits Per Second |
| OWI_EN | OWI Enable | | 6.5 | | 7.0 | V |
| $OWI_EN_{hys}$ | OWI Enable Hysteresis | | | 50 | | mV |
| | Internal Pullup | | | 10 | | KΩ |
| | Activation Signal Pulse Low time | | 12 | | | ms |
| | Activation Signal Pulse High time | | 12 | | | ms |
| OWI_VIH | OWI Transceiver Rx Threshold | | 0.7 × VDD | | VDD + 0.3 | V |
| OWI_VIL | OWI Transceiver Rx Threshold | | –0.3 | | 0.3 × VDD | V |
| OWI_VOH | OWI Transceiver Tx Threshold | VDD = 5 V | 4.0 | | | |
| OWI_VOL | OWI Transceiver Tx Threshold | VDD = 5 V | | | 0.8 | V |

## 5.11 Serial Peripheral Interface (SPI) Interface

over operating free-air temperature range (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $V_{IH}$ | High-level input voltage | | 0.7 × VDD | | VDD + 0.3 | V |


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## Serial Peripheral Interface (SPI) Interface *(continued)*

over operating free-air temperature range (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $V_{IL}$ | Low-level input voltage | | –0.3 | | 0.3 × VDD | V |
| $V_{OH}$ | High-level output voltage | | 4.0 | | | V |
| $V_{OL}$ | Low-level output voltage | | | | 0.8 | V |
| $f_{SCK}$ | SPI Frequency | | | | 4 | MHz |
| $t_{CSSCK}$ | $\overline{CS}$ Low to First SCK Rising Edge | | 25 | | | ns |
| $t_{SCKCS}$ | Last SCK Rising Edge to $\overline{CS}$ Rising Edge | | 125 | | | ns |
| $t_{CSD}$ | $\overline{CS}$ Disable Time | | 500 | | | ns |
| $t_{DS}$ | SDI Setup Time | | 25 | | | ns |
| $t_{DH}$ | SDI Hold Time | | 25 | | | ns |
| $t_{SDIS}$ | SDI Fall/Rise Time | | | | 7 | ns |
| $t_{SCKR}$ | SCK Rise Time | | | | 7 | ns |
| $t_{SCKF}$ | SCK Fall Time | | | | 7 | ns |
| $t_{SCKH}$ | SCK High Time | | 125 | | | ns |
| $t_{SCKL}$ | SCK Low Time | | 125 | | | ns |
| $t_{SDOE}$ | SDO Enable Time | | 15 | | | ns |
| $t_{ACCS}$ | SCK Rising Edge to SDO Data Valid | | 15 | | | ns |
| $t_{SDOD}$ | SDO Disable Time | | | | 15 | ns |
| $t_{SDOS}$ | SDO Rise/Fall Time | | 3 | | 11 | ns |
| $C_{L(SDO)}$ | Capacitive Load for Data Output (SDO) | | | 10 | | pF |

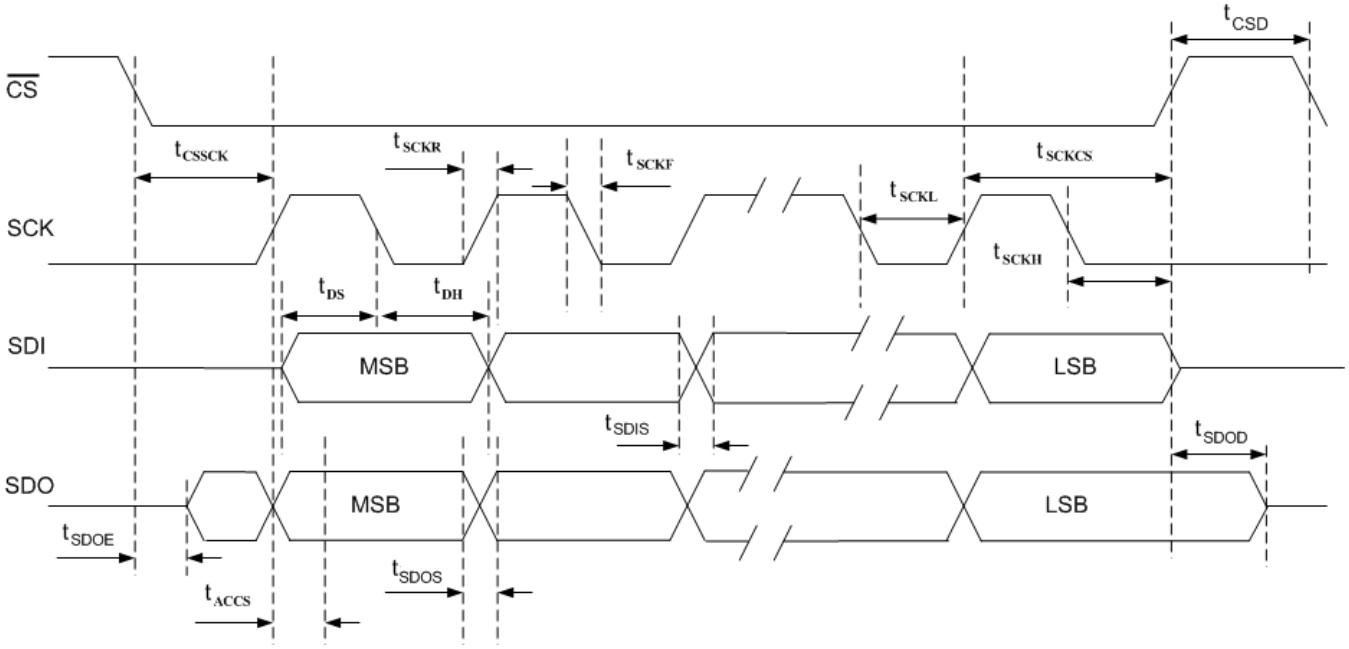


**Figure 5-1. SPI Timing**

## 5.12 I2C Interface

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $V_{IH}$ | High-level input voltage | | 0.7 × VDD | | VDD + 0.3 | V |
| $V_{IL}$ | Low-level input voltage | | –0.3 | | 0.3 × VDD | V |

## I2C Interface *(continued)*

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $V_{OH}$ | High-level output voltage | | 4.0 | | | V |
| $V_{OL}$ | Low-level output voltage | | | | 0.8 | V |
| $f_{SCL}$ | SCL clock frequency | | | | 400 | KHz |
| $t_{STASU}$ | START condition set-up time | | 500 | | | ns |
| $t_{STAHD}$ | START condition hold time | | 500 | | | ns |
| $t_{LOW}$ | SCL low time | | 1.25 | | | µs |
| $t_{HIGH}$ | SCL high time | | 1.25 | | | µs |
| $t_{RISE}$ | SCL and SDA rise time | | | | 7 | ns |
| $t_{FALL}$ | SCL and SDA fall time | | | | 7 | ns |
| $t_{DATSU}$ | Data setup time | | 500 | | | ns |
| $t_{DATHD}$ | Data hold time | | 500 | | | ns |
| $t_{STOSU}$ | STOP condition set-up time | | 500 | | | ns |

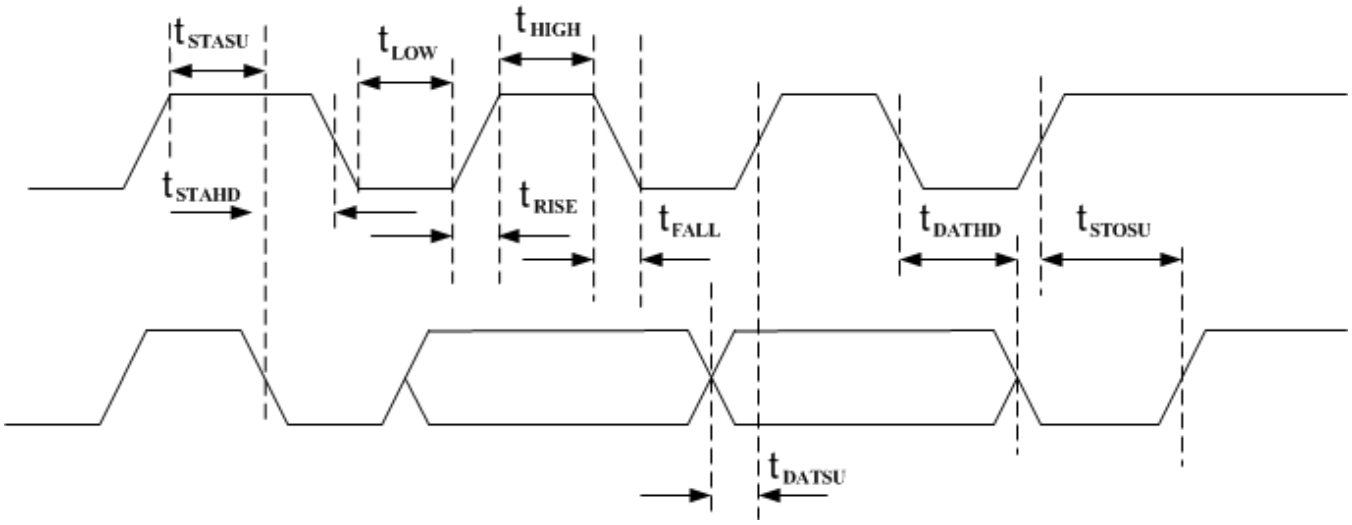


**Figure 5-2. I²C Timing**

## 5.13 Non-Volatile Memory

| PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|
| OTP | | | 8 | | KB |
| OTP Number of Erase/Write Cycles | Erase using UV light | | | 10 | Cycles |
| EEPROM | Programmable using SPI or OWI | | 89 | | Bytes |
| | Number of bytes writeable by 8051 | | 16 | | Bytes |
| EEPROM Erase/Write Cycles | | | | 1000 | Cycles |


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## 5.14 GPIO

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $V_{IH}$ | High-level input voltage | $R_{LOAD}$ ≥ 10 kΩ to $V_{DD}$ or to 0 V | 0.7 × VDD | | VDD + 0.3 | V |
| $V_{IL}$ | Low-level input voltage | $R_{LOAD}$ ≥ 10 kΩ to $V_{DD}$ or to 0 V | –0.3 | | 0.3 × VDD | V |
| $V_{OH}$ | High-level output voltage | $I_{OH}$ = 1 mA | 4.0 | | | V |
| $V_{OL}$ | Low-level output voltage | $I_{OL}$ = –1 mA | | | 0.8 | V |
| $I_{OH}$ | High-level output current | $V_{OH}$ = 4.5 V | | | 1 | mA |
| $I_{OL}$ | Low-level output current | $V_{OL}$ = 0.5 V | | | 1 | mA |
| $R_{PU}$ | Pull-up resistance | | | 160 | | kΩ |

## 5.15 DAC1 and DAC2 Output

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| | Settling time | DAC Code 000h to FFFh step.Output is 90% of Full Scale. $R_{LOAD}$ = 5 kΩ, $C_{LOAD}$ = 500 pF | | | 7 | µs |
| | Zero scale error | DAC code = 000h, $I_{DAC}$ = 1.5 mA | | | 46 | mV |
| | Full scale voltage | Output when DAC code is FFFh, $I_{DAC}$ = - 1.5 mA | 4.85 | | 4.95 | V |
| | Output current amplitude | DAC Code = 0FFFh , DAC Code = 0000h | | | 1.5 | mA |
| | Short circuit source current | VDD = 5V, DAC code = 000h | -34 | | -10 | mA |
| | Short circuit sink current | VDD = 5V, DAC code = FFFh | 10 | | 34 | mA |
| | INL (best-fit line) | | -3.5 | | 3.5 | LSB |

## 5.16 Input Capture and Output Compare

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| **INPUT CAPTURE PORTS** | | | | | | |
| $V_{IH}$ | High-level input voltage | $R_{LOAD}$ ≥ 10 kΩ to $V_{DD}$ or to 0 V | 0.7 × VDD | | VDD + 0.3 | V |
| $V_{IL}$ | Low-level input voltage | $R_{LOAD}$ ≥ 10 kΩ to $V_{DD}$ or to 0 V | –0.3 | | 0.3 × VDD | V |
| | Input capture timer clock frequency | 10_20_MHZ bit = 1 | | 10 | | MHz |
| | | 10_20_MHZ bit = 0 | | 20 | | |
| | Input capture timer bits | | | 16 | | Bits |
| **OUTPUT COMPARE PORTS** | | | | | | |
| $V_{OH}$ | High-level output voltage | $I_{OH}$ = 1 mA | VDD – 1.0 | | | V |
| $V_{OL}$ | Low-level output voltage | $I_{OL}$ = -1 mA | | | 0.8 | V |
| | Output compare timer frequency | 10_20_MHZ bit = 1 | | 10 | | MHz |
| | | 10_20_MHZ bit = 0 | | 20 | | |
| | Output compare timer bits | | | 16 | | Bits |
| $I_{OH}$ | High-level output current | | | | 1 | mA |
| $I_{OL}$ | Low-level output current | | | | 1 | mA |

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## 5.17 Diagnostics

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| | 8051 Software watchdog | | | 500 | | ms |
| | Main clock normal operation range | | 35 | 40 | 45 | MHz |
| VBRG_OV | Sensor supply over voltage threshold | | 3.55 | 3.65 | 3.75 | V |
| VBRG_UV | Sensor supply under voltage threshold | | 2.9 | 3.0 | 3.11 | V |
| | AVDD OV threshold | | 3.7 | | 3.95 | V |
| | AVDD UV threshold | | 2.72 | | 3.1 | V |
| $Sensor_{OV}$ | Output overvoltage threshold for gain stage 1 and 2 | | 2.3 | 2.5 | 2.6 | V |
| $Sensor_{UV}$ | Output undervoltage threshold for gain stage 1 and 2 | | 0.7 | .85 | 1.0 | V |
| $f_cap_{High}$ | Capacitive sensor interface clock high frequency fault threshold | | 1.5 | | 2.5 | MHz |
| $f_cap_{Low}$ | Capacitive sensor interface clock low frequency fault threshold | | 30 | | 50 | kHz |
| | EEPROM CHG PUMP overvoltage threshold | | | 14.65 | | V |
| | EEPROM CHG PUMP undervoltage threshold | | | 11.45 | | V |
| | DAC loop back voltage gain | | 0.537 | 0.545 | 0.557 | V/V |
| | Open wire leakage current 1 - open VDD with pull-up on VOUT1 | | | | 2 | µA |
| | Open wire leakage current 2 - open GND with pull-down on VOUT1 | | | | 20 | µA |

# 6 FUNCTIONAL DESCRIPTIONS

In this section, individual blocks in the Section 2 are described in more detail.

## 6.1 Overvoltage / Reverse Voltage Protection Block

The PGA400-EP includes an Overvoltage and Reverse Voltage Protection block. This block protects the device from overvoltage and reverse-battery conditions on the external power supply. In this block, a control circuit monitors the input supply line for reverse-battery and overvoltage fault conditions protects the device if these voltage conditions occur on the external power supply.

## 6.2 Linear Regulators and Bandgap + Current Blocks

The PGA400-EP contains two precision low-drift bandgap supply voltage references for other blocks of the device. One bandgap provides the reference voltage for internal linear regulators that supply AVDD and DVDD. The other bandgap reference provides the voltage reference for the all the other internal circuitry, including sensor supply regulators, sensor offset compensation, etc.

The PGA400-EP has two main linear regulators: AVDD Regulator and DVDD Regulator. The AVDD regulator provides the 3.3 V voltage source for internal analog circuitry while the DVDD regulator provides the 3.3 V regulated voltage for the digital circuitry. The user needs to connect bypass capacitors of 100nF on both the AVDD and DVDD pins of the device.

Figure 6-1 shows the Power-On Reset sequence for AVDD and DVDD with respect to the voltage applied to the VDD pin.


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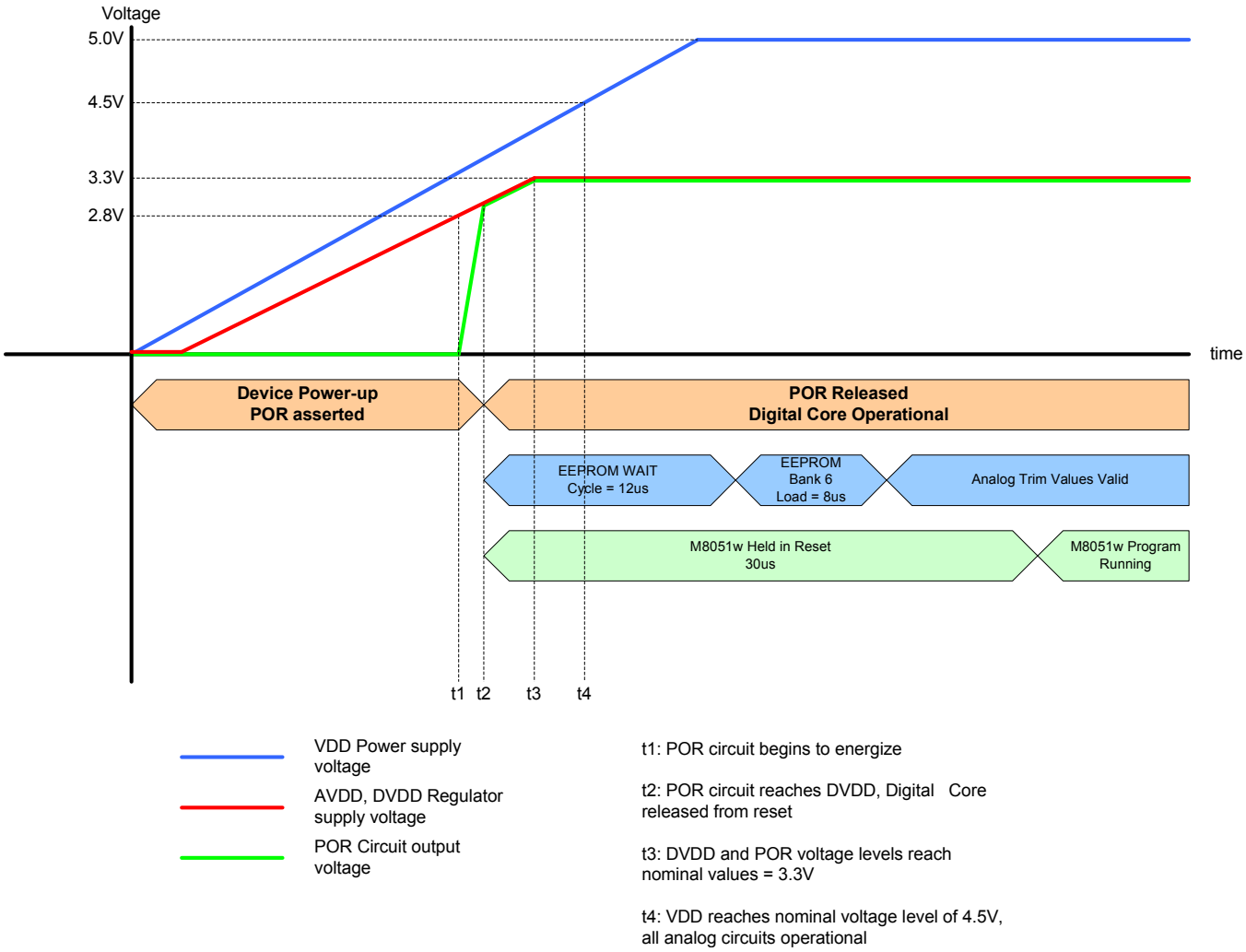


**Figure 6-1. POR Sequence Diagram**

## 6.3 Internal OSC/XTAL I/F Block

The device includes an internal 40 MHz oscillator, which by default provides the internal clocks required. The device can also be configured to use an external 40-MHz crystal as a time base via the XTAL_EN bit in the Sensor Control Register (SENCTRL). When the XTAL_EN bit is set high, the internal 40-MHz oscillator is disabled and control of the main system clock is driven by the external clock source connected to the XTAL pin.

**NOTE**

Do not use the XTAL pin as an output for sourcing a clock signal to other devices.

## 6.4 Sensor Voltage Supply Block

The Sensor Voltage Supply block of the PGA400-EP supplies both the VBRG output for resistive bridge sensors and the ICAP supply for capacitive sensors.

### *6.4.1 VBRG Supply for Resistive Bridges*

The VBRG pin on the PGA400-EP is a 3.3-V nominal output supply from a linear regulator with a precise internal temperature independent band-gap reference.

### 6.4.2 ICAP Supply for Capacitive Sensors

A functional schematic of the capacitive sensor drive circuit is shown in Figure 6-2. The common node of the sensor capacitances is tied to the ICAP pin and the current and voltage at this point are referred to as $I_X$ and $V_X$ respectively. For the sake of understanding the operation of the drive circuit by itself, the other terminals of the sensor may be treated as if they were tied to ground, because the sensor signal measurement circuit regulates the voltage at these nodes. This circuit is essentially a relaxation oscillator where the capacitance of the sensor, the charging current $I_C$, and the comparator hysteresis $V_H$ determine the frequency of oscillation.

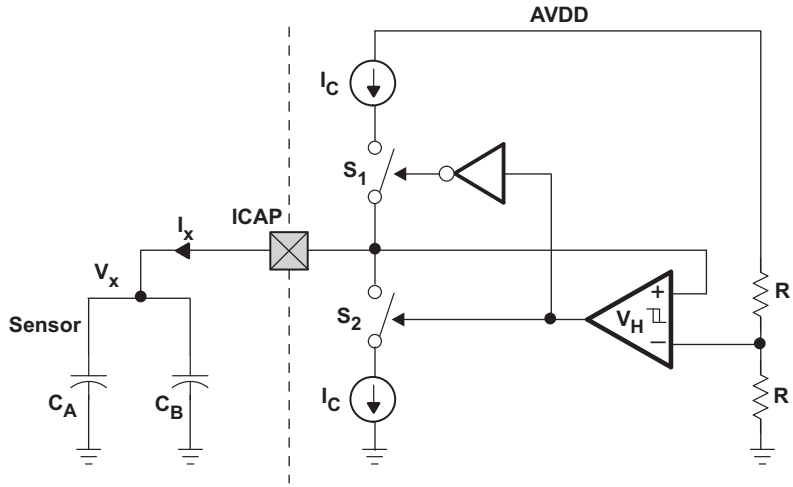


**Figure 6-2. Capacitive Sensor Drive Circuit**

To illustrate the circuit operation, the sensor voltage $V_X$ is initially set to 0 V. In this state, the positive terminal of the hysteretic comparator is lower than its negative reference terminal, producing a logical zero at the output. This results is switch S2 is open and switch S1 is closed, allowing the upper current source to charge the sensor capacitance. Figure 6-3 shows the resulting waveform. Equation 1 calculates the linear ramp up slope of the voltage, $V_X$:

$$\frac{dV_x}{dt} = \frac{1_C}{C_A + C_B} \tag{1}$$

After $V_X$ is charged up to the high threshold of the comparator, the circuit inverts the states of switches $S_1$ and $S_2$. By closing $S_2$ and opening $S_1$ the lower current source begins to discharge the sensor capacitances, making $V_X$ ramp down with an equal but opposite rate as before. Once $V_X$ reaches the low threshold of the comparator, the circuit again inverts the states of the switches and returns to the positive charging state. This process of charging and discharging repeats with a period characterized as shown in Equation 2.

$$T = \frac{2 \bullet V_H}{I_C} \bullet (C_A + C_B) \tag{2}$$

Both the comparator hysteresis voltage $V_H$ and capacitor charging current $I_C$ are configurable to allow control of the oscillation period for a particular sensor. Bits CV[1..0] in the Capacitive Sensor Settings Register (CAPSEN) can be used to set $V_H$. $V_H$ can be set between 100 mV and 700 mV with four possible steps. Bits CI[2..0] in the Capacitive Sensor Settings Register (CAPSEN) can be used to set $I_C$, with possible values between 5 µA and 22 µA with eight possible steps.

**NOTE**

For capacitive sensors, one common set of configurations registers are implemented. If different settings are needed for the two capacitive sensors, then the software must dynamically update the register values.


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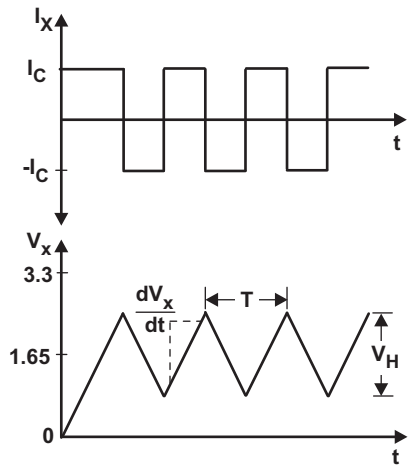


**Figure 6-3. Capacitive Sensor Drive Waveforms**

## 6.5 Internal Temperature Block and External Temperature Sensing

The device has the ability to perform temperature compensation via an internal or external temperature sensor. The user can select the source of the sensor with the TEMP_SEN bit in the Sensor Control Register (SENCTRL). When the TEMP_SEN bit is set to "0" the internal temperature sensor is used, and when the TEMP_SEN bit is set to "1" the external temperature sensor is used.

### *6.5.1 Internal Temperature Sensor*

The device contains an internal temperature sensor which is converted by an ADC and made available to the 8051 microprocessor so that appropriate temperature compensation algorithms can be implemented in software. The nominal relationship between the device temperature and the ADC Code is shown in Equation 3.

ADC Code = *2.8* TEMP -80*, *TEMP* is temperature in °C. (3)

### *6.5.2 External Temperature Sensor*

The device accepts a temperature from an external temperature sensor via the VIN3 pin. The input temperature needs to be in the form of a voltage.

**NOTE**

The Offset TC block has been configured to operate with the internal temperature sensor transfer function. If an external temperature sensor is used and the user needs to use Offset TC compensation, then the temperature-to-voltage transfer function of the external temperature sensor has to match the transfer function of the internal temperature sensor.

## 6.6 Using the Analog Front End

The PGA400 can be used to interface with Resistive Bridge Sensors as well as Capacitive Sensors. To enable multiple sensors of either type a series of muxes are used. These muxes are controlled by the Sensor Control Register (SENCTRL) and Capacitve Sensor Setting Register (CAPSEN).

The SEN_TYP bit of the Capacitive Sensor Settings Register (CAPSEN) configures the device to be used with either resisitive or capacitve sensor types. When this bit is set to ‘0’, the device is configured for capacitive sensors and when the bit is set to "1" the device is configured for resistive bridge sensors. When either front-end is selected, the other option is disabled and placed in a low quiescent current state.

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The Analog Front End (AFE) can also be configured to measure two sensors sequentially. This is controlled via the SEN_CHNL bit in the Sensor Control Register (SENCTRL). When this bit is set to '0', the analog MUX at the input of the AFE is switched to pass the signals present at VIN1P and VIN1N pins. For capacitive sensors, the capacitive sensor drive current is also applied to the ICAP1 pin. When this bit is set to '1', the VIN2P, VIN2N and ICAP2 pins become active. The SEN_CHNL bit also controls which External Special Function Registers (ESFRs) are applied to the Stage 1 Gain, Stage 2 Gain, Offset, Offset TC and the Sign bits.

In addition the sensor supply regulator can be independently enabled or disabled via the VBRG_EN bit in the Sensor Control Register (SENCTRL). This allows the VBRG 3.3 V output to be used with external temperature sensors while the AFE is configured in capacitive sensor mode. For more information on programming the PGA400-EP please refer to the

## 6.7 Stage 1 Gain Block

When the device is configured to interface with resistive sensors, the first gain block that the signal passes through in the AFE is the Stage 1 Gain block. This gain block is designed with precision, low drift, low flicker noise amplifiers.

The gain of this stage is adjustable to accommodate sensors with a wide-range of signal spans and can be set from 3V/V to 51V/V in 8 possible steps. The Stage 1 Gain has two independent registers, Sensor 1 Gain Register (SEN1GAIN) and Sensor 2 Gain Register (SEN2GAIN), so that two different resistive sensors can be connected with different gain settings. For Stage 1 Gain settings use either the S1_G1 bits or the S2_G2 bits in the registers mentioned above. The gain setting that is used depends on the SEN_CHNL bit in Sensor Control Register (SENCTRL).

Table 6-1 outlines the ranges of of resistive bridge sensor characteristics that are compatible.

**Table 6-1. Target Resistive Bridge Sensors**

| PARAMETER | CONDITION | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|
| Resistive bridge resistance | $-40°C \le T_A \le 150°C$ | 2 | | 20 | KΩ |
| Resistive bridge resistance TC | | –350 | | 4800 | PPM/°C |
| Resistive bridge offset (compensated in Analog Front End) | $T_A = 25°C$ | –33 | | 33 | mV/V |
| Resistive bridge offset TC (compensated in Analog Front End) | | –40 | | 40 | µV/V/°C |
| Resistive bridge span | $T_A = 25°C$ | 1.4 | | 75 | mV/V |

## 6.8 Self Oscillating Demodulator Block

Figure 6-4 shows an essential schematic of the capacitive sensor signal measurement circuit. . The Sensor Voltage Supply block discussed in is depicted only as a functional block called Sensor Drive that provides the sensor drive current via the ICAPx pin and the clock signals $S_1$ and $S_2$ that are used by the synchronous demodulator in the measurement circuit. As with the ICAP supply circuitry the demodulator block circuitry toggles between two states during normal operation. In one state the $S_1$ switches are closed while the $S_2$ switches are open and in the other state the $S_1$ switches are open while the $S_2$ switches are closed.


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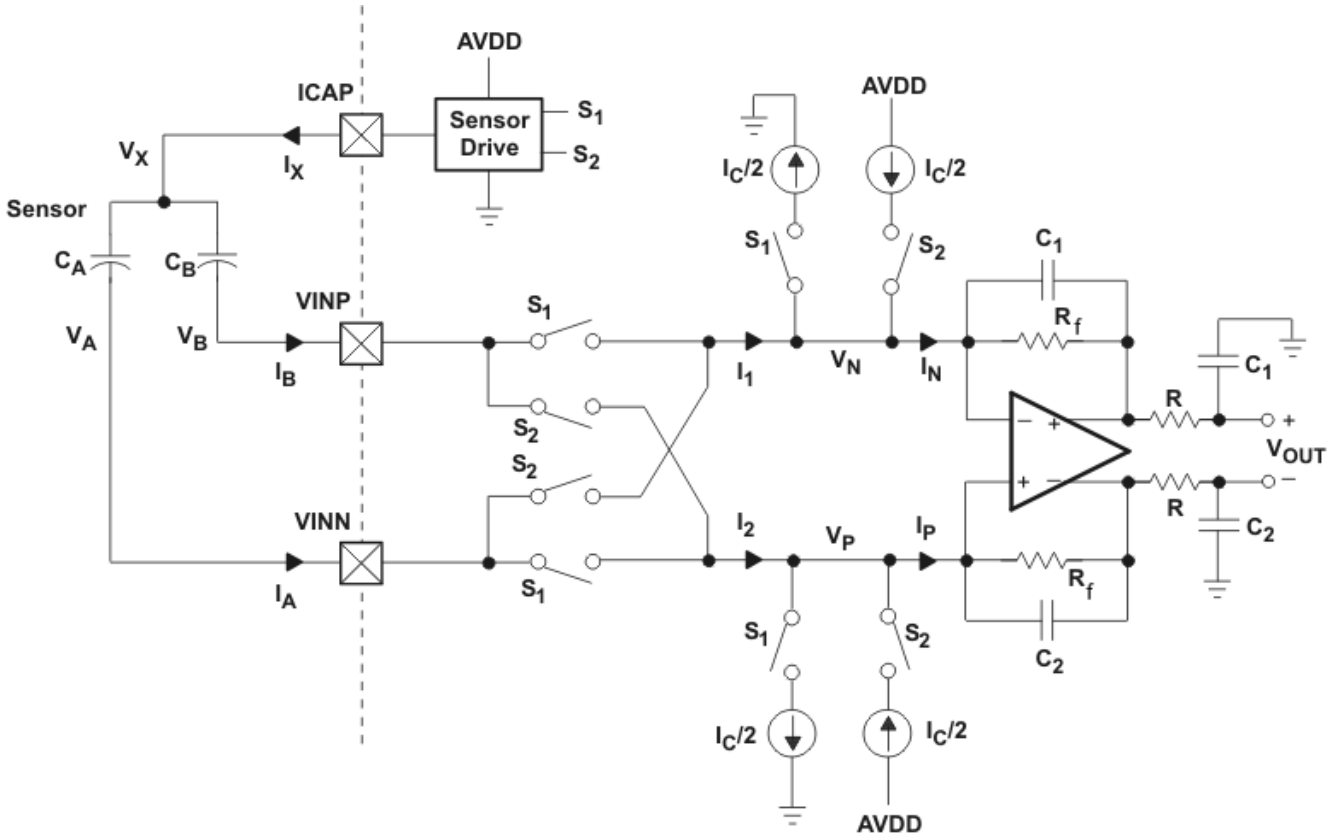


**Figure 6-4. Capacitive Sensor Signal Measurement Circuit**

To illustrate the operation of the circuit, assume that it has been given sufficient time to settle and is now operating in its normal steady-state mode of operation. During the positive charging phase, $I_X$ is positive and the $S_1$ switches are closed. In this state, the amplifier seeks to regulate its input terminals to the same potential, creating a virtual ground at the VINP and VINN pins. This allows $I_X$ to be expressed in Equation 4 as:

$$I_X = (C_A + C_B) \bullet \frac{dV_X}{dt} \tag{4}$$

In a similar manner, Equation 5 describes the currents through $C_A$ and $C_B$ and the difference between these currents.

$$I_A = C_A \bullet \frac{dV_X}{dt} \tag{5}$$

$$I_B = C_B \bullet \frac{dV_X}{dt} \tag{6}$$

$$\Delta I = (I_A - I_B) = (C_A - C_B) \bullet \frac{dV_X}{dt} = I_X \bullet \left(\frac{C_A - C_B}{C_A + C_B}\right) \tag{7}$$

The drive current is split between the capacitors in proportion to their relative difference. Measuring ΔI provides a means to infer the value of the difference in capacitance ($C_A$ – $C_B$) or the value of one of the capacitors if the other is known. Also, driving the sensor with a current source and measuring the resulting difference in current has the benefit of being fully differential and thus less susceptible to common-mode disturbances and non-idealities. Note that the expressions for $I_A$ and $I_B$ may are rewritten in terms of common-mode and differential-mode components in Equation 8 and Equation 9.

$$I_A = \frac{I_X}{2} + \frac{\Delta I}{2} \tag{8}$$

$$I_B = \frac{I_X}{2} - \frac{\Delta I}{2} \tag{9}$$

The capacitive sensor signal measurement circuit extracts and amplifies ΔI. Figure 6-5 illustrates the current waveforms at different points in the circuit of Figure 6-4. The currents into and out of the sensor are shown on axis (a). Initially, the circuit is in the discharge phase where $I_X$ is negative and $S_2$ switches are closed. After some time, the state switches to the charge phase where the $S_1$ switches are closed. This process of changing the state of the circuit continues periodically with a frequency set by the sensor drive circuit.

During each half cycle the $I_X$ current is split into the individual capacitor currents $I_A$ and $I_B$. As shown in Figure 6-5(b), while the $S_1$ switches are closed $I_2 = I_A$ and $I_1 = I_B$, but when the $S_2$ switches are closed the currents are inverted such that $I_2 = I_B$ and $I_1 = I_A$. Because the sign of $I_X$ is also changing, the difference between $I_2$ and $I_1$ remains constant and equal to ΔI (ignoring the glitches that occur at phase transitions).

While the $S_1$ switches are closed, half the sensor drive current ($I_C/2$) is subtracted from $I_2$ and $I_1$ and while the $S_2$ switches are closed, half the sensor drive current is added to them. This removes the cycle-to-cycle offset in Figure 6-5(b), delivering the DC currents $I_P$ and $I_N$ to the trans-impedance amplifier, as shown in Figure 6-5(c) where $I_P$ – $I_N$ = ΔI. For low frequency signals, the output voltage of the amplifier is shown in Equation 10.

$$V_{out} = R_f \cdot \Delta I = R_f \cdot I_C \cdot \left( \frac{C_A - C_B}{C_A + C_B} \right) \tag{10}$$

For a given sensor, the drive current $I_C$ should be adjusted to keep $V_{OUT}$ < 1.65 V over the expected operating conditions of the sensor to avoid saturating the ADC input.

**NOTE**

for some types of wide span sensors, it may be necessary to reduce the gain set by the value of $R_f$ in the transimpedance amplifier. The drive current $I_C$ and feedback resistance $R_f$ can be adjusted via Capacitive Sensor Settings Register (CAPSEN).


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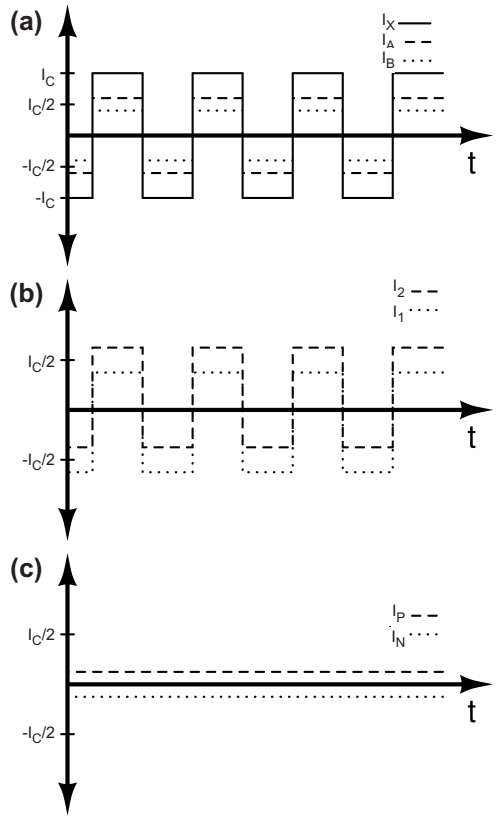


**Figure 6-5. Current Waveforms in the Sensor Signal Measurement Circuit**

This process of changing the state of the circuit continues periodically with a frequency set by the sensor drive circuit described in Equation 11.

$$f = \frac{I_C}{2 \cdot V_H \cdot (C_A + C_B)} \tag{11}$$

BEcause the op-amp must settle at each switching cycle, there is an upper bound imposed on the sensor drive frequency. Using a minimum half-cycle time of seven times the op-amp settling time and a minimum op-amp GBW of 7 MHz, shows the following upper bound on the switching frequency:

$$f_{MAX} \leq 800 \text{ kHz}$$

In reality, there are glitches and residual up-converted noise in the $I_P$ and $I_N$ signals. For this reason, the trans-impedance amplifier has a low-pass characteristic, with one pole set by the feedback elements $R_f$ and $C_f$, and a second pole at the output set by R and the same capacitance $C_f$. For most sensor types, R is equal to $R_f$. In this case, the frequency dependent trans-impedance may be expressed as shown in Equation 12.

$$Z(s) = \frac{R_f}{1 + s \cdot R_f \cdot C_f)^2} \ \Omega \tag{12}$$

Where with nominal values of $R_f$ = 625 kΩ and $C_f$ = 16 pF, the corner frequency of the filter is 15.9 kHz. If the minimum permissible ripple suppression is chosen to be 40 dB at the switching frequency, and the corner frequency is rounded up to 20 kHz, illustrates the lower bound on the switching frequency:

$$f_{min} \geq 200 \text{ kHz}$$

For a given sensor, the drive circuit comparator hysteresis value $V_H$ and the drive current $I_C$ should be chosen so that the switching frequency remains within the range of 200 to 800 kHz as the sensor capacitance varies within its expected range.

Table 6-2 outlines the ranges of compatible capacitive bridge sensor characteristics.

**Table 6-2. Target Capacitive Sensors**

| PARAMETER | CONDITION | MIN | MAX | UNIT |
|---|---|---|---|---|
| Capacitive sensor initial capacitance (Cp+Cr) | | 10 | 310 | pF |
| Capacitive sensor offset (compensated in Analog Front End) | (Cp,0 – Cr,0)/(Cp,0 + Cr,0) | –0.16 | 0.16 | |
| Capacitive sensor span | (Cp,100 – Cr,100)/(Cp,100 + Cr,100) | 0.04 | 1.00 | |
| Capacitive sensor offset TC | | | 0.8 | %Cv,0/ °C |

### *6.8.1 Configuring the Capacitive Sensor Interface for a Particular Sensor*

A general procedure for choosing what values to use for the capacitive sensor drive current ($I_C$), drive voltage comparator hysteresis ($V_H$) and trans-impedance ($R_f$) is the following:

- Find the values of $I_C$ that maintain $V_{OUT}$ below 1.65 V for the maximum sensor span plus offset
- Using the largest allowed value for $I_C$ and the minimum and maximum total sensor capacitance ($C_A$+$C_B$), find a value for $V_H$ that maintains the switching frequency within the range of 200 kHz to 800 kHz
- If the frequency constraints cannot be met, reduce the value of $I_C$ and iterate to find an optimal solution

This procedure can be applied to configure the capacitive sensor interface with total capacitances ranging from 10 pF to 300 pF and span plus offset ratios ($C_A$–$C_B$)/($C_A$+$C_B$) up to 0.36.

The Stage 1 gain has two independent registers for the two sensors that can be potentially connected. The Stage 1 gain setting used depends on the SEN_CHNL bit in the Sensor Control Register.

## 6.9 Sign Bit Block

The device has a sign bit block that is used for span sign compensation. This block is used to change the polarity of the first stage output, and it is implemented through the use of four switches. The switches are set through the use of the S1_INV bit for sensor 1 and the S2_INV bit for sensor 2 in the Sensor Control Register (SENCTRL). There are two independent sign bit settings to accommodate configuring the polarity for two independent sensors. The sensor sign bit used is based on the SEN_CHNL bit in the Sensor Control Register.

## 6.10 Offset and Offset TC Compensation Blocks

The offset compensation circuit can be configured to null out the sensor offset and first order offset temperature coefficient. The offset compensation block is located between the Sign Bit block and the Stage 2 Gain block as shown in the Section 2.

The offset compensation, $V_{COMP}$, is a value that is subtracted from the output of the sign bit block. This offset provides a means to null the sensor offset prior to Stage 2 Gain. The offset compensation circuit block provides ten bits of zero-order compensation and six bits of first-order TC compensation.


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A more detailed block diagram of the offset compensation subsystem is shown in Figure 6-6. As shown $V_{comp}$ is derived from two references, $V_{BG}$ and $V_{PTAT}$. Where $V_{BG}$ is a precise temperature independent band-gap reference voltage, and $V_{PTAT}$ is a proportional-to-absolute-temperature voltage. In PGA400-EP, the gains in the offset compensation circuitry (A, B, C) have been designed assuming the following characteristics about the reference signals:

$$V_{BG} = 1.23\ V \tag{13}$$

$$V_{PTAT}(T) = k_{PTAT} \bullet (T + 273) + \xi_{PTAT} \tag{14}$$

where

$$k_{PTAT} = 3.7\ mV/°C \text{ and } \xi_{PTAT} = -47\ mV \tag{15}$$

**NOTE**

If an external temperature sensor is used, the signal applied to the VIN3 pin must have the same temperature dependency as the above mentioned $V_{PTAT}$ signal or else the offset TC compensation does not work as intended.

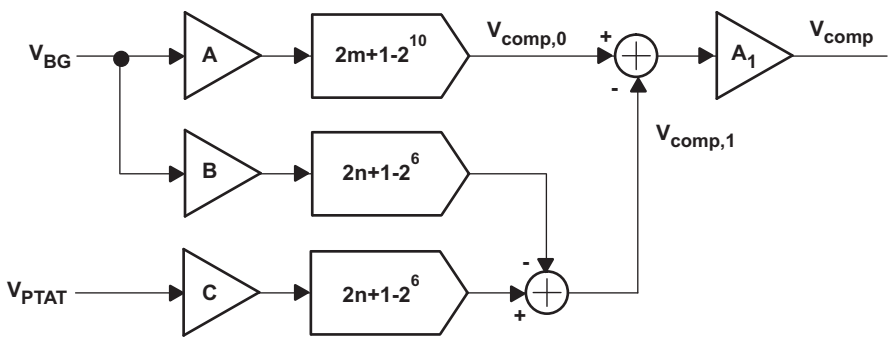


**Figure 6-6. Block Diagram of Offset Compensation Circuit**

The zero-order portion of $V_{COMP}$ is produced by scaling $V_{BG}$ by the gain A to generate the reference for a 10-bit DAC. The DAC scales this reference by $2m+1-2^{10}$, where m is decimal equivalent of the DAC's digital input and ranges from 0 to 1023. The zero-order portion of the compensation voltage is expressed as a function of m as shown in Equation 16.

$$V_{COMP,0}(m) = V_{BG} \bullet A \bullet (2 \bullet m + 1 - 2^{10})\ V \tag{16}$$

The first order portion of $V_{COMP}$ is constructed from the difference between scaled versions of $V_{PTAT}$ and $V_{BG}$. The reason for this is that the temperature compensation signal should pivot about a particular reference temperature, which ideally would be the same temperature at which the zero-order portion of the sensor offset is calibrated out. Because $V_{PTAT}$ pivots about 0 K, a temperature independent offset must be introduced to shift the pivot temperature up to a practical value like 22°C. The first-order portion of the compensation voltage is expressed in Equation 17.

$$Vcomp,1\ (n,T) = (C \bullet [k_{PTAT} \bullet (T + 273) + \xi_{PTAT}] - B \bullet V_{BG}) \bullet (2 \bullet n + 1 - 2^{6})\ V \tag{17}$$

Where the reference temperature about which this function pivots may be expressed in terms of the other variables as shown in Equation 18.

$$T_R = \frac{1}{k_{PTAT}} \bullet \left( \frac{V_{BG} \bullet B}{C} - \varepsilon_{PTAT} \right) - 273°C \tag{18}$$

The gains B and C are set to produce a reference temperature of approximately 22°C.

When Equation 17 and Equation 18 are combined and consolidate the values of the constants, the final output voltage of the offset compensation circuit is expressed as a function of m, n, T, and $A_1$ in the following way:

$$V_{comp}(m, n, T, A1) = A_1 \bullet \frac{1277}{3} \bullet \left[250 \bullet (2 \bullet m + 1 - 2^{10}) + 4.921 \bullet (T-22) g (2 \bullet n + 1 - 2^{6})\right] nV \tag{19}$$

For resistive sensors, the gain used for the offset compensation calculation is always the same as the first stage gain in the AFE and is controlled by the same registers. For capacitive sensors, $A_1$ is an independent variable that may be set to meet a specific sensor or noise requirements.

**NOTE**

The above voltage $V_{comp}$ is subtracted (differentially) from the output of the first stage.

The Offset and Offset TC has two independent registers, Sensor 1 Offset Register (SEN1OFF1 and SEN1OFF2) and Sensor 2 Offset Register (SEN2OFF1 and SEN2OFF2), to accomodate for two independent sensors that can be potentially connected. The sensor offset value used is based on the SEN_CHNL bit in the Sensor Control Register (SENCTRL).

## 6.11 Stage 2 Gain Block

The Stage 2 Gain block is contructed with a low flicker noise, low offset amplifier. Both resistive bridge sensors and capacitive sensors share this gain stage. The gain setting for this stage ranges from 1 V/V to 25 V/V in 32 possible steps.

The Stage 2 Gain block has two independent registers, Sensor 1 Gain Register (SEN1GAIN) and Sensor 2 Gain Register (SEN2GAIN). This accomodates two different sensors that can be connected with different gain settings. The Stage 2 gain is determined by the SEN_CHNL bit in Sensor Control Register.

## 6.12 ADC Buffer Blocks

The device has two buffer blocks, one for the pressure signal path and one for the temperature signal path.

### *6.12.1 Analog to digital Converter Buffer 1*

The ADC Buffer 1 is a differential amplifier with 2X gain that is used to condition the pressure signal before reaching the Analog to Digital Converter (ADC).

In addition to gain this block can be configured to provide a level shift using the ADC_BUF bit in Sensor Control Register (SENCTRL). When this bit is set to ‘0’, no offset is introduced to the signal, and the output of the ADC buffer is simply two times the output of Gain Stage 2. When this bit is set to ‘1’, a –1.65 V offset is introduced such that the output of the ADC buffer is equal to two times the output of Gain Stage 2 minus 1.65 V. The Level Shift feature of the ADC Buffer shifts the output of the Stage 2 Gain so that the full dynamic range of the sigma-delta modulator can be used.

### *6.12.2 Analog to digital Converter Buffer 2*

The ADC Buffer 2 is a unity gain differential amplifier. This buffer block conditions the temperature signal before reaching the ADC.

## 6.13 Sigma Delta Modulator Blocks

There are two independent Sigma Delta Modulator ADCs, one for the pressure signal and another for the temperature signal.

### *6.13.1 Sigma Delta Modulator for AD Converter 1*

The Sigma Delta Modulator 1 block is a 1-bit 1MHz sigma-delta modulator for the pressure sensor signal. To further condition the signal this stage is followed by two stages of digital decimation filters.

### *6.13.2 Sigma Delta Modulator for AD Converter 2*

The Sigma Delta Modulator 2 block is a 1-bit 128kHz sigma-delta modulator for the temperature signal. The input signal to the sigma-delta modulator can come from either the internal or external temperature. The output of this ADC is followed by a single decimation filter.


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## 6.14 Decimation Filter Blocks

The device contains three Signal Decimation FIlters. Two back to back decimation filters for the pressure sensor signal path and one decimation filter for the termperature path.

### *6.14.1 ADC1 Decimation Filter Blocks*

The sensor signal path contains two decimation filters in series with each other. The first decimation filter has a fixed decimation ratio and a second decimation filter that has a variable decimation ratio.

The 1st Stage Decimator Filter has a fixed decimation ratio of 32. Based on the 1MHz sampling frequency of the sigma-delta modulator, the output rate of the 1st stage decimator is fixed at 32 µs per sample.

The 2nd Stage Decimator has a variable decimation ratio. This filter further decimates the output of the first stage decimator. The decimation ratios of the second stage can be configured for a decimation ratio of 2, 4, or 8 using the OSR[1..0] bits in the Decimator and Low Power Control Register (DECCTRL).

The output of the second decimation filter in the sensors signal path is a 16 bit **signed** value. Some example second stage decimation output codes for given differential voltages at the input of the sigma delta modulator are shown in Table 6-3:

**Table 6-3. Input Voltage to Output Counts for the Signal Channel ADC**

| SIGMA DELTA MODULATOR DIFFERENTIAL INPUT VOLTAGE | NOISE-FREE OUTPUT |
|---|---|
| –3.3V | –32768 |
| –1.65V | –16384 |
| 0 | 0 |
| 1.65V | 16383 |
| 3.3V | 32767 |

### *6.14.2 Decimation Filters for AD Converter 2*

The temperature path contains one fixed ratio decimation filter block after the sigma delta modulator. The filter is 10-bit with fixed decimation ratio of 1024. Based on the 128-kHz sampling frequency, the output rate of the fixed ratio decimation filter is fixed at 8 ms per sample.

The output of the temperature channel decimation filter is a 10 bit **signed** value. The equation to calculate the relationship between the input voltage at VIN3 and the output of the decimator block is shown below.

ADC Code = *760* VIN3 -820*, *VIN3* is voltage at the input of the buffer in volts. (20)

Table 6-4 summarizes the relationship between the internal temperature sensor and the decimator output.

**Table 6-4. Input Voltage to Output Counts for the Temperature Channel ADC**

| INTERNAL TEMPERATURE | NOISE-FREE OUTPUT OF TEMPERATURE CHANNEL DECIMATOR |
|---|---|
| –40°C | -196 |
| –20°C | -140 |
| 0°C | -83 |
| 20°C | -27 |
| 40°C | 28 |
| 150°C | 338 |

### 6.14.3 Accessing the ADC Values for the 8051

the ADC Decimator Output Register (ADCMSB and ADCLSB) makes available the output of all three decimators that are available to the microprocessor.

The microprocessor specifies which decimator is loaded by writing a "1" to the appropiate bit in the Load ADC Decimator Shadow Register (LD_DEC).

If more than 1 bit in the LD_DEC register is set to 1 simultaneously, then only one decimator output is loaded into ADCMSB and ADCLSB register. The priority used to determine which decimator output gets loaded is as follows:

- Decimator 1 Output
- Decimator 2 Output
- Temperature Decimator

## 6.15 8051 WARP Microprocessor Block

The 8051 WARP microprocessor is an exceptionally high-performance version of this popular 8-bit microcontroller, requiring only 2 clocks per machine cycle rather than the 12 clocks per cycle of the industry standard device while it maintains functional compatibility with the standard device

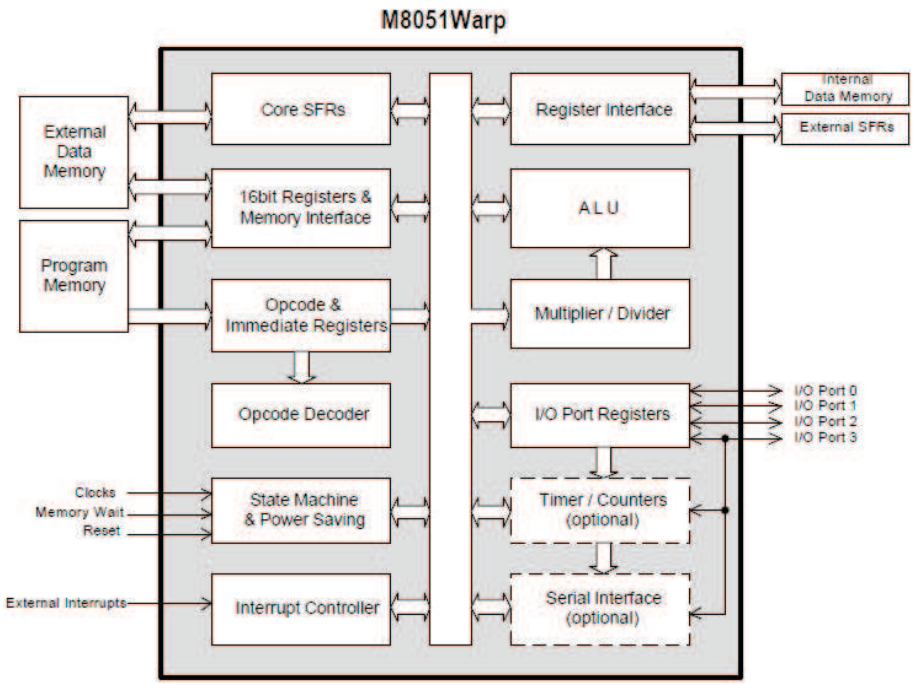


**Figure 6-7. 8051W Core. The 8051W core includes two 16-bit timers and serial interface.**

## 6.16 Digital Interface

The digital interfaces are used to access (read as well as write) the internal memory spaces described in Section 6.20. Each interface uses different pin(s) for communication. The device has three separate modes of communication:

1. One-Wire Interface (OWI)
2. Serial Peripheral Interface (SPI)
3. Inter-Integrated Circuit ($I^2C$)

Each communication mode has its own protocol of communication, but all three access the same memory elements within the device. For all three communication modes the PGA400-EP device operates as a slave device.


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Figure 6-8 shows the interface between the 8051W, the Memory block and the Digital Interface. **In the PGA400-EP, only the Digital Interface OR the 8051W can access can access the internal memory spaces.** It is not possible for both 8051W and the Digital Interface to access the memory spaces simultaneously. Therefore there is an access selection bit called IF_SEL in the Micro/Interface Control Register (MICRO_IF_SEL_T) that allows either the 8051W microprocessor or the digital interfaces to have access to the OTP, EEPROM, ESFR and RAM memory spaces.

Figure 6-8 also shows that a special memory space called the Test Registers are only accessible only via the Digital interface. Since the Micro/Interface Control Register is in the Test Register memory block which is only accessible via the digital interface, only the digital interfaces can change the memory access selection.

To select the specific digital interface that is used for communication the DI_CTRL[1:0] bits in the Digital Interface Control Register (DI_CTRL) need to be set. If DI_CTRL is configured for I2C, then GPIO1 and GPIO3 automatically configures for $I^2C$ operation.

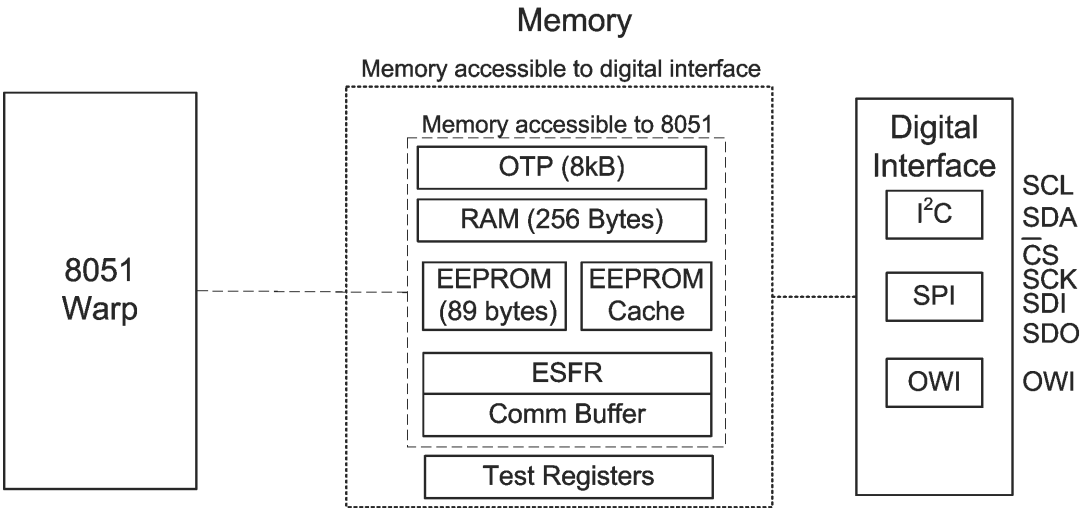


**Figure 6-8. Digital Interface**

**NOTE**

If Digital Interface is used to access the internal memory, the 8051W must enter reset state (to prevent the 8051W from accessing the memory. The 8051W operates in reset state using the "MICRO_RESET" bit in the Micro/Interface Control Register (MICRO_IF_SEL_T).

**NOTE**

The internal memory space internal is accessible via the Digital Interface without the need for the user to implement any communication software in the 8051W. The user must implement communication software, in the form of an interupt service routine, only if the user wishes to communicate with the PGA400-EP while 8051W is not in reset state. This interupt service routine is used in conjuction with a communication buffer interface, that is available in both the ESFR and Test Memory address spaces.

**NOTE**

While the 8051W is not in a reset state, it transfers data to the internal memory space using the Digital Interface. This transfer is accomplished using the communication buffer that exists between the Test Register memory space and the ESFR memory space (shown as COMM BUFFER in Figure 6-8).

## 6.17 One-Wire Interface (OWI)

The device includes a One-Wire Interface (OWI) digital communication interface. The main function of the OWI is to enable writes to and reads from all addresses available for OWI access. These include access to most Test Register and ESFR memory locations.

### *6.17.1 Overview of OWI Interface*

The OWI digital communication is a master-slave communication link in which the PGA400-EP operates as a slave device only. The master device controls when data transmission begins and ends. The slave device does not transmit data back to the master until it is commanded to do so by the master. A logic 1 (high) value on the one wire interface is defined as a *recessive* value, while a logic 0 (low) value on the one-wire interface is defined as a *dominant* value.

The VOUT1/OWI pin acts as both an analog DAC output and the interface communication pin, so that when the device is embedded inside of a system module only three pins are needed (VOUT1/OWI pin, VDD and GND). The 8051 microprocessor has the ability to control the activation and deactivation of the OWI interface based upon the signal driven into the VOUT1/OWI pin.

During normal operation the DAC is the last stage of the sensor signal path, and drives data out on the VOUT1/OWI pin in the form of an analog signal. To change to OWI communication mode this pin must be driven with an appropiate activation signal described in Section 6.17.2.

Figure 6-9 shows a functional equivalent circuit for the structure of the OWI and DAC circuitry.

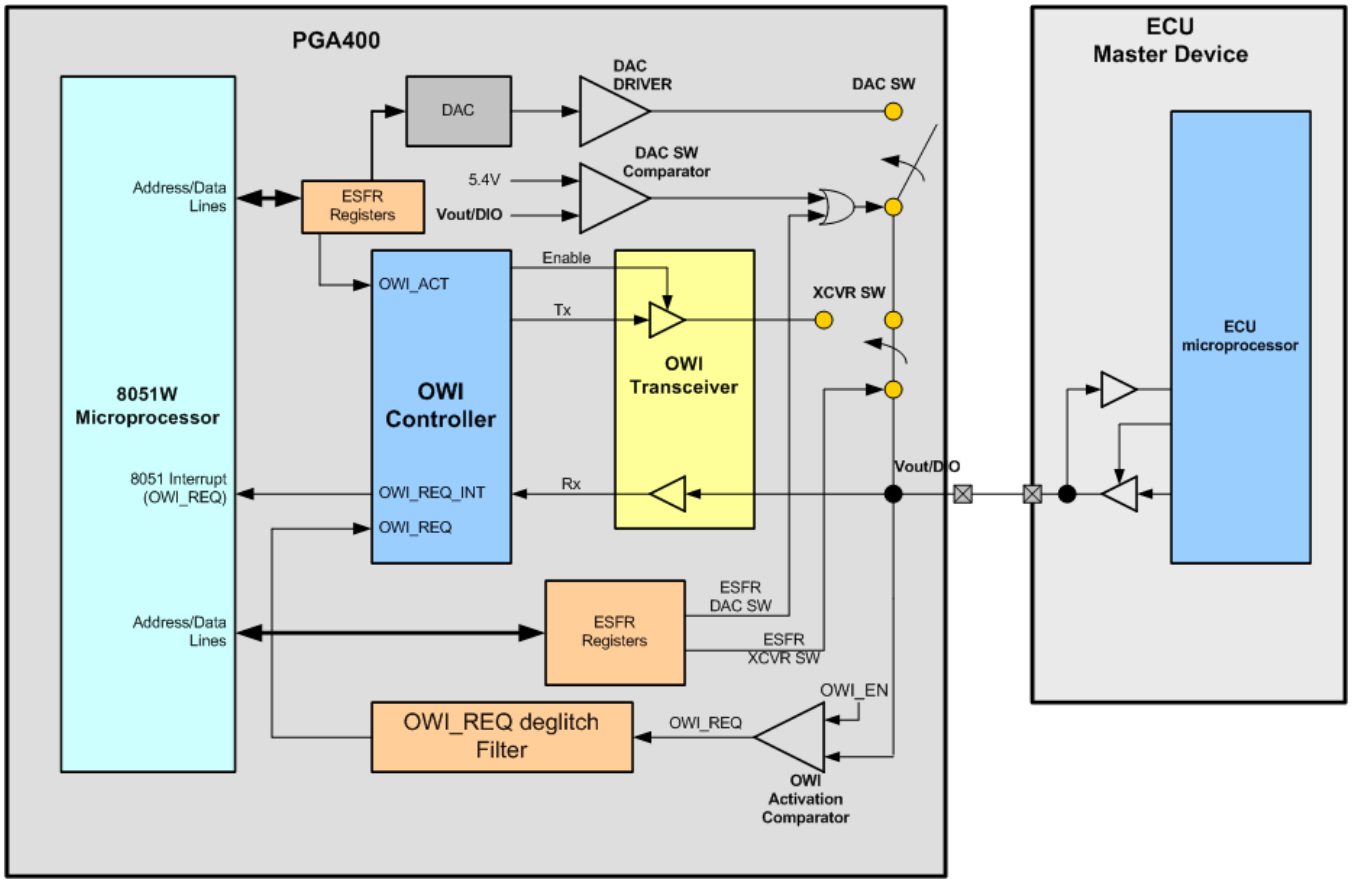


**Figure 6-9. OWI System Components**


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### 6.17.2 Activating and Deactivating the OWI Interface

#### 6.17.2.1 OWI Activation Procedure

Figure 6-10 shows the sequence diagram for the OWI activation procedure. This figure shows that the OWI master initiates the switching of the VOUT1/OWI pin from DAC output mode to OWI mode by generating an OWI activation signal. Upon receiving the OWI activation signal, the PGA400 OWI controller generates OWI_ACTIVATION interrupt to the 8051W. The user interrupt service routine switches the VOUT1/OWI mode by writing to the appropriate registers.

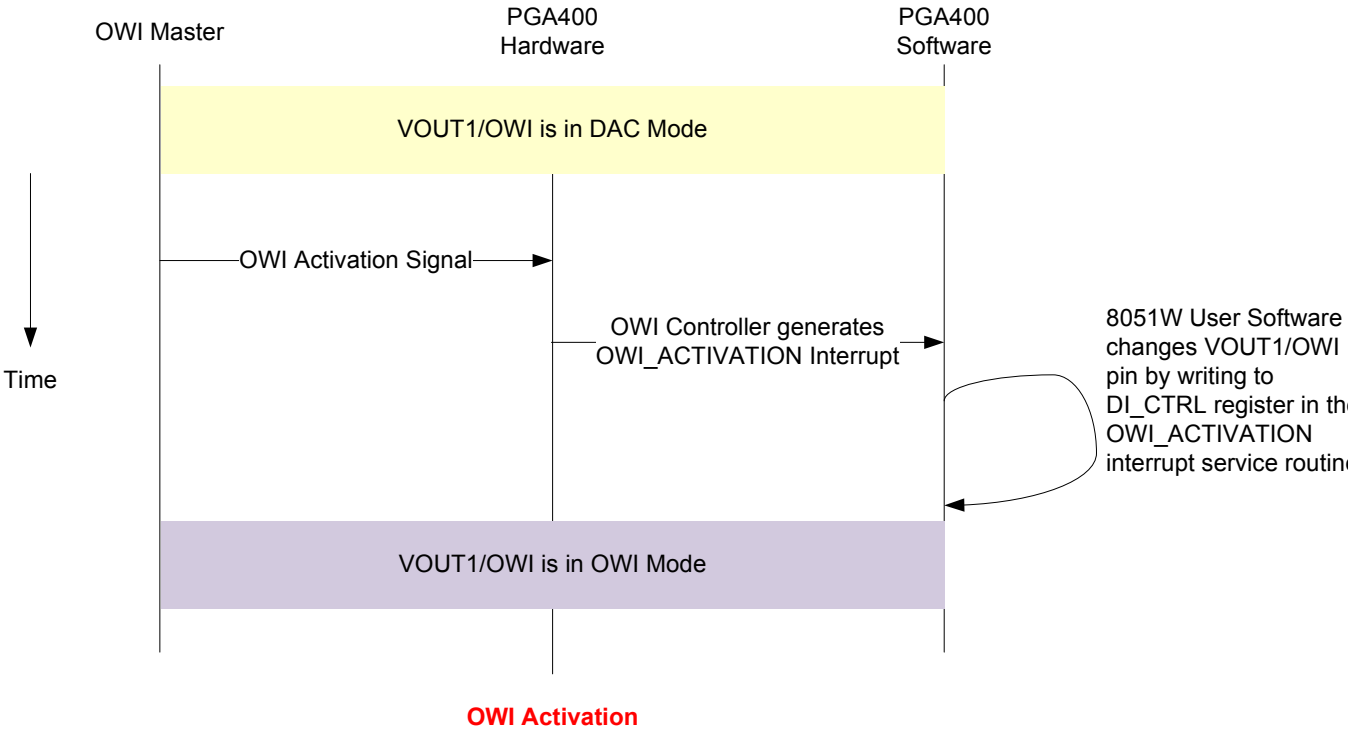


**Figure 6-10. OWI Activation Sequence**

#### 6.17.2.2 OWI Activation Signal

If the device is operating in the normal operation where the DAC is active and I2C or SPI communication modes are not enabled the following activation signal can be driven into the VOUT1/OWI pin to place it into OWI communication mode. The process begins with driving the OWI_EN voltage on the VOUT1/OWI pin. As soon as the DAC voltage exceeds 5.4 volts the DAC is switched off by by a comparator. Once the pin voltage reaches the OWI_EN voltage threshold a deglitch timer begins. Once the pin voltage has been asserted for a time greater than the deglitch time the OWI Activation Comparator transmits a logic 1 value to the OWI Controller. Figure 6-11 illustrates the activation of the OWI interface.

This deglitch time is set by the OWI_DEGLITCH_SEL bit in the Digital Interface Control Register (DI_CTRL), and has the following properties:

- OWI_DEGLITCH_SEL = ‘0’ → OWI Activation deglitch time = 1ms
- OWI_DEGLITCH_SEL = ‘1’ → OWI Activation deglitch time = 10ms
- The default value for OWI_DEGLITCH_SEL bit is ‘0’, which corresponds to deglitch time of 1ms.

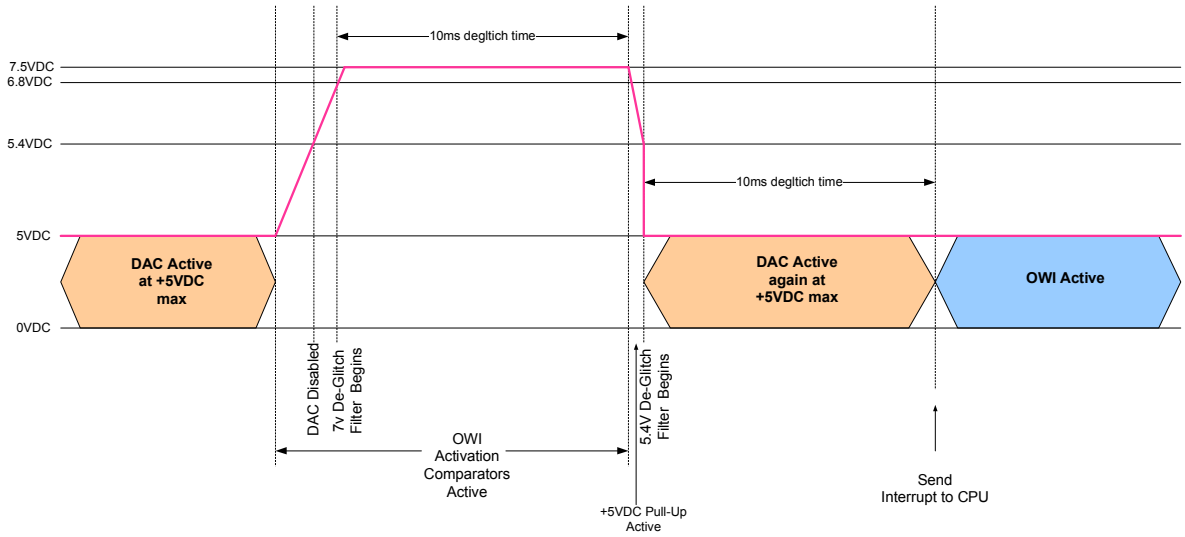


**Figure 6-11. OWI Activation Using Overvoltage Drive. Deglitch is assumed to be 10ms.**

When the high voltage has been maintained for the proper deglitch time, the pin must then be driven back to the standard 5V IO voltage for an additional deglitch time set by the same bit as before. During this second deglitch time the DAC becomes active again only until the the second deglitch time has passed. Once this second deglitch period is over the OWI controller generates an OWI activation interrupt that is sent to the 8051. This user interrupt service routine switches the VOUT1/OWI pin's mode by writing to the appropriate registers. The OWI transceiver is switched to the VOUT1/OWI pin and the DAC is placed back into the OFF state. The capability to drive the appropiate OWI_EN voltage must be provided in the test environment.

The XCVR switch, controlled by an ESFR register, changes the output drive from the unidirectional DAC analog signal to the bi-directional OWI digital signal interface. Once this switch is selecting the OWI transceiver, OWI data can be transmitted and received through the VOUT1/OWI pin. The OWI transceiver is responsible for translating voltage levels to appropriate logic levels so that the OWI controller may process the OWI data. The OWI_REQ deglitch filter ensures that no invalid activation signals are transmitted from the analog OWI Activation Comparator to the 8051 interrupt input. Both the DAC switch ESFR and the XCVR switch ESFR must be set via the OWI interrupt service routine. It is recommended to set the DAC switch to the OFF position before setting the XCVR switch to the OWI mode.

If the device is already in SPI communication mode or $I_2C$ communication mode, enabling OWI communication changing the DAC enable bit and the OWI transceiver enable bit in the Digital Interface Control Register (DI_CTRL) is the only requirement. The register bits can be set manually in the following order.

1. The register bits DI_CTRL[1:0] in the Digital Interface Control Register (DI_CTRL) need to be set to 0b10. This activates the OWI controller and deactivates the DAC via the DAC switch.
2. The OWI_XCR_EN bit in the Digital Interface Control Register (DI_CTRL) must be set to 1. This turns on the OWI transceiver and switches the VOUT1/OWI pin to the OWI transceiver.

**NOTE**

Note that DI_CTRL[1:0] and OWI_XCR_EN bits can be written simultaneously (in 1 write command). However, because the state of the VOUT1/OWI is unknown during the transition from VOUT1 to OWI, it is recommended that the master wait at least 15 ms before transmitting the OWI command.

### 6.17.2.3 Deactivating OWI Communication

In order to deactivate the OWI communication the following two steps must be performed in any order.


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- The OWI_XCR_EN bit in the Digital Interface Control Register (DI_CTRL) must be set to 0. This turns off the OWI transceiver and switch the VOUT1/OWI pin to the DAC driver.
- The register bits DI_CTRL[1:0] in the Digital Interface Control Register (DI_CTRL) must to be a value other than 0b10. This selects a different Digital Interface (either I2C or SPI) and it also switchs on the DAC driver.

### 6.17.3 OWI Communication Error Status

The device has the ability to detect and report errors in OWI communication. The OWI Error Status 1 Register (OWI_ERR_1), and OWI Error Status 2 Register (OWI_ERR_2) contain the error bits. The communication errors that are reported with the registers include

- Out of range communication baud rate
- Invalid SYNC field
- Invalid STOP bits in command and data
- Invalid OWI command

## 6.18 Serial Peripheral Interface (SPI) Interface

The device includes a Serial Peripheral Interface (SPI) digital communication interface. The main function of the SPI is to enable writes to and reads from all addresses available for SPI access.

### 6.18.1 Overview of SPI Interface

SPI is a synchronous, serial, master-slave, communication standard that requires the following four pins:

- SDI: SPI slave in master out, serial input pin.
- SDO:SPI slave out master in, serial output pin (tri-state output)
- SCK: SPI clock which controls the communication.
- $\overline{CS}$: chip select (active low)

SPI comminucates in a master/slave style where only one device, the master, can initiate data transmissions. The PGA400-EP always acts as the slave in SPI communication, where whatever external device that is communicating to it becomes the master mode. Both devices begin data transmission with the most significant bit (MSB) first.

Because multiple slave devices can exist on one bus, the master node is able to notify the specific slave node that it is ready to begin communicating with by driving the $\overline{CS}$ line to a low logic level. In the absence of active transmission, the master SPI device places the device in reset by driving the $\overline{CS}$ pin to a high logic level. During a reset state the SDO pin operates in tri-state mode. For the SPI interface to have access to memory locations other than test register space, the IF_SEL bit in the Micro/Interface Control Test register (MICRO_IF_SEL_T) has to be set to ‘1’.

### 6.18.2 Activating the SPI Interface

To activate SPI communication the following steps must be made in order:

1. Place the 8051W in reset by setting the MICRO_RESET bit in the Micro/Interface Control Register (MICRO_IF_SEL_T) to logic "high"
2. Give control of the memory block to the digital interface by setting the IF_SEL bit in the Micro/Interface Control Register (MICRO_IF_SEL_T)to logic "high"
3. Set the DI_CTRL bits in the Digital Interface Control Register (DI_CTRL) to 0b00 for SPI interface

### 6.18.3 Clocking Details of SPI Interface

Input data on the SDI pin must be valid on the rising edge of the SCK clock, whereas output data on the SDO pin changes during the rising edge of the SCK clock. For SPI timing information the SPI Timing diagram is shown in Figure 5-1.

## 6.19 Inter-Integrated Circuit Interface

The device includes an Inter-Integrated Circuit ($I^2C$) digital communication interface. The main function of the $I^2C$ is to enable writes to, and reads from, all addresses available for $I^2C$ access.

### 6.19.1 Overview of I2C Interface

$I^2C$ is a synchronous serial communication standard that requires the following two pins for communication:

- GPIO_1/IC_1/SDA: $I^2C$ Serial Data Line (SDA)
- GPIO_3/OC_1/SCL: $I^2C$ Serial Clock Line (SCL)

$I^2C$ communicates in a master/slave style communication bus where one device, the master, can initiate data transmission. The device always acts as the slave device in $I^2C$ communication, where the external device that is communicating to it acts as the master node. The master device is responsible for initiating communication over the SDA line and supplying the clock signal on the SCL line. When the $I^2C$ SDA line is pulled low it is considered a logical zero, and when the $I^2C$ SDA line is floating high it is considered a logical one. For the $I^2C$ interface to have access to memory locations other than test register space, the IF_SEL bit in the Micro/Interface Control Test register (MICRO_IF_SEL_T) has to be set to logic one.

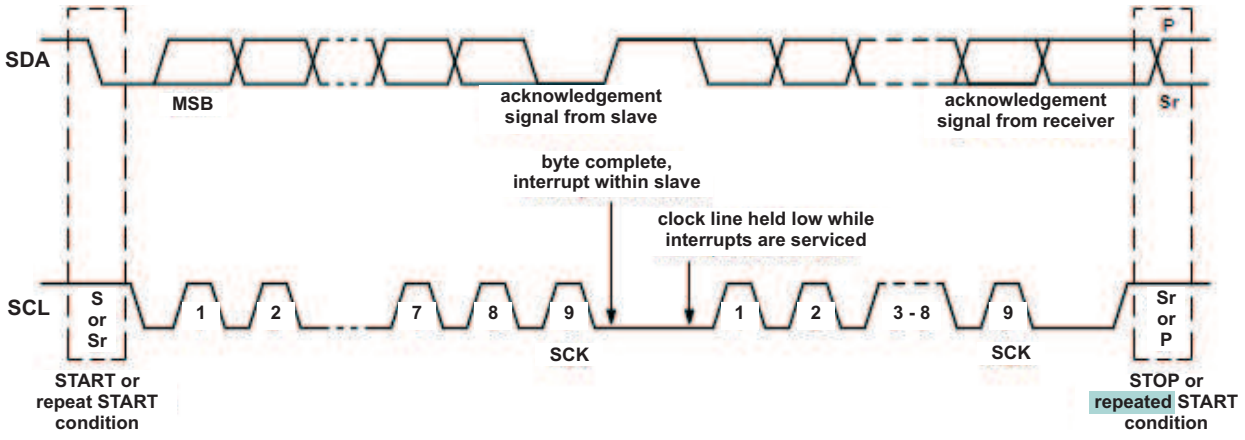
### 6.19.2 Activating the $I^2C$ Interface

To activate $I^2C$ communication the following steps must be made in order:

1. Place the 8051W into a reset state by setting the MICRO_RESET bit in the Micro/Interface Control Register (MICRO_IF_SEL_T) to logic "high"
2. Give control of the memory to digital interface by setting the IF_SEL bit in the Micro/Interface Control Register (MICRO_IF_SEL_T)to logic "high"
3. Set the DI_CTRL bits in the Digital Interface Control Register (DI_CTRL) to 0b01 for $I^2C$ interface

### 6.19.3 Clocking Details of I2C Interface

The device samples the data on the SDA line when the rising edge of the SCL line is high, and is changed when the SCL line is low. The only exceptions to this indication a start, stop or repeated start condition as shown in Figure 6-12





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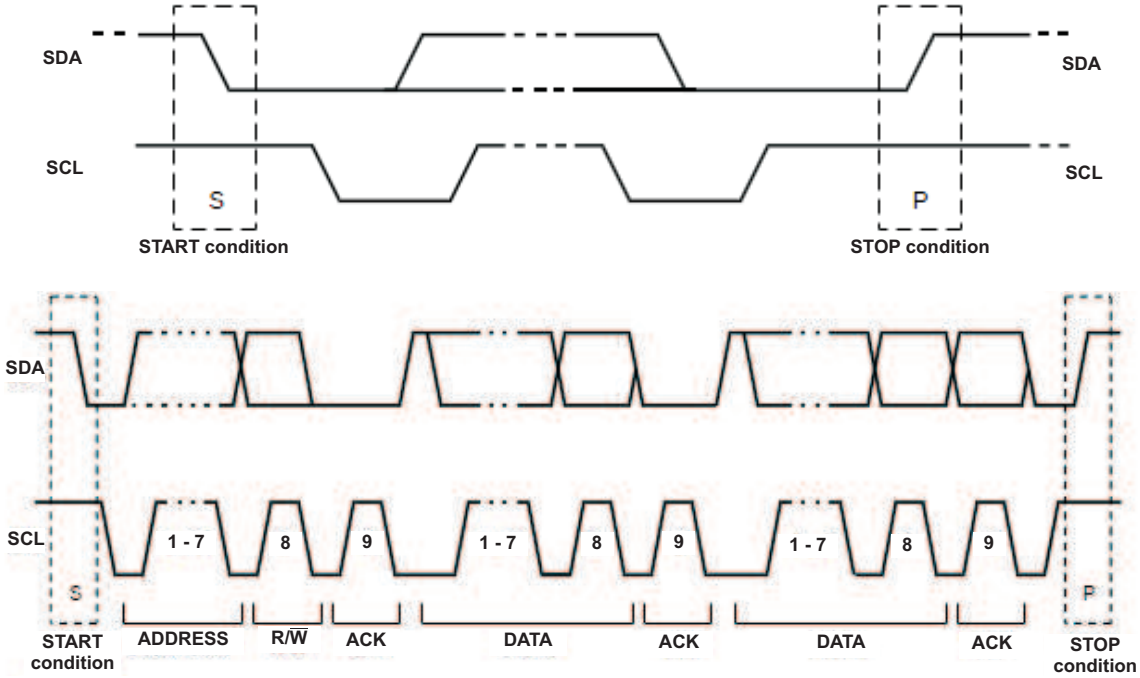


**Figure 6-12. I2C Clocking Details**

## 6.20 Memory

### *6.20.1 OTP Memory*

The OTP Memory space is 8 kB and is located at memory pages 3 and 4. This memory space contains program instructions for the 8051W microprocessor. To program the OTP memory an external VP_OTP voltage needs to be applied to the VP_OTP pin.

The device has the ability to lockout access to all memory spaces except the Test Register space from the digital interface. This helps protect firmware intellectual property. The locking/unlocking of the access to the OTP memory is achieved using 8051W Port 0 in the SFR memory space (P0[7:0]) in the following way:

- If P0(7:0) is set to 0xAA, the Digital Interface is in locked state. In this state, memories cannot be read via Digital Interface. Note that once the Digital Interface is locked, the Micro/Interface Control Test register is also not accessible via the Digital Interface.
- If P0(7:0) is set to 0x00 while the Digital Interface is in locked state, then the memories are accessible via Digital Interface.

The 8051W microprocessor can access all memories even when the memories are in locked state, allowing software programs to execute. If the Digital Interface is in locked state and the CPU watchdog causes a 8051W reset, the Digital Interface maintains the lockout state.

### *6.20.2 EEPROM Memory*

Figure 6-13 shows the EEPROM Bank structure. EEPROM cells within a bank are activated only when reading from or writing to their specific EEPROM bank. Therefore the contents of each EEPROM must be transferred to the EEPROM Cache before reads and writes can occur to that bank. There are a total of six banks of EEPROM, and they are located at memory page 5.

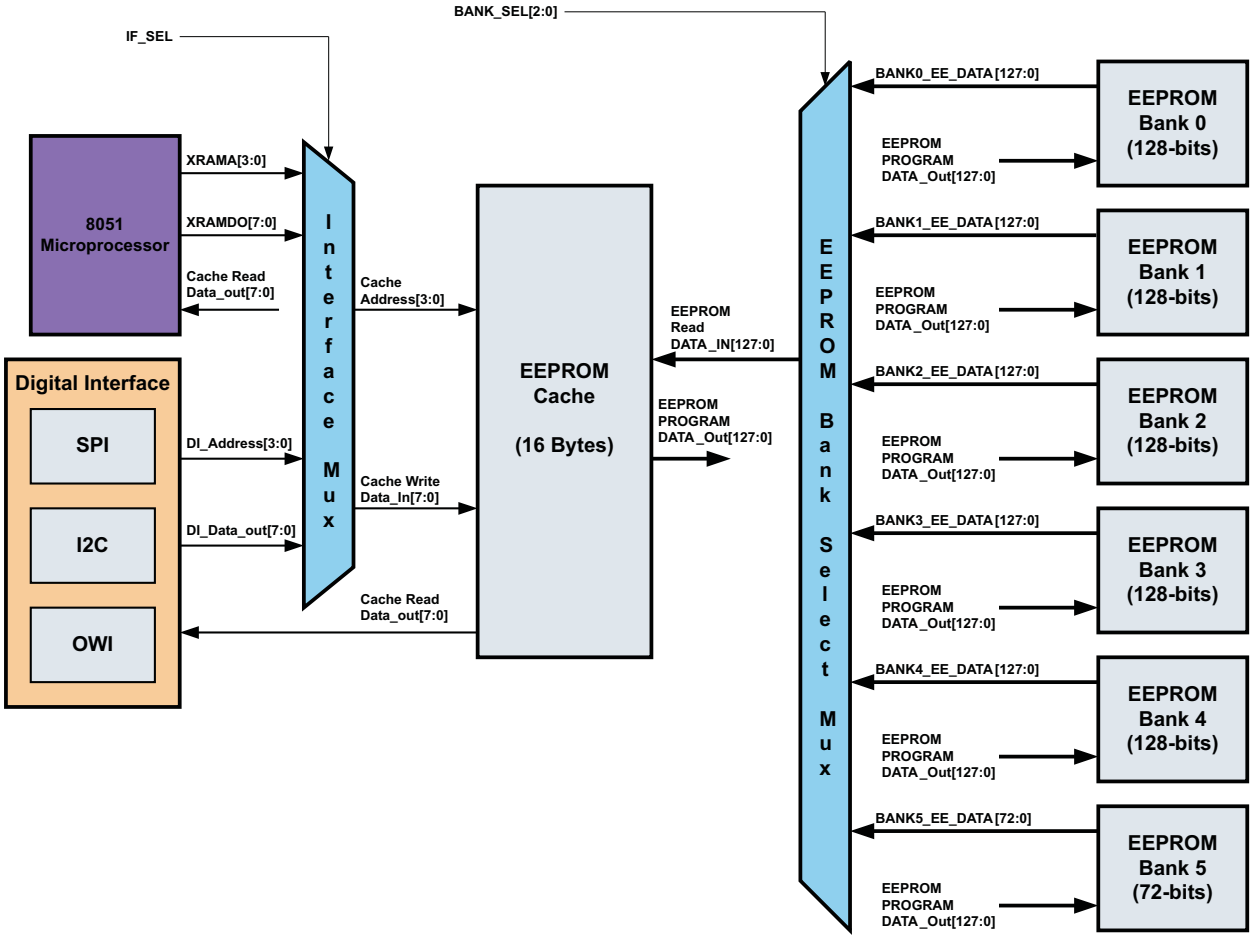


**Figure 6-13. Structure of EEPROM Interface**

### 6.20.2.1 EEPROM Memory Organization

#### *6.20.2.1.1 EEPROM Cache*

The EEPROM Cache serves as temporary storage of data being transferred to/from a selected EEPROM bank. Data transferred to the EEPROM cache from either a digital interface or from the M8051 is byte addressable and one byte at time can be written to or read from. The only exception being a special OWI burst write/read access in which 8 bytes of data can be accessed at a time. Selection of the EEPROM Cache interface is determined by the IF_SEL bit in the EEPROM Access Control register.

Data transferred to the Cache from an EEPROM bank is loaded 128-bits at a time during the EEPROM Cache load cycle. EEPROM Bank selection is determined by the value placed in the BANK_SEL bits in the EEPROM Access Control Register. When programming an EEPROM bank, the EEPROM Cache holds the programming data for the amount of time necessary to complete the EEPROM programming process.

#### *6.20.2.1.2 Bank 0*

Bank 0 is used for storage of customer data and is the only bank which can be programmed by both the 8051W and the Digital Interface. 16 bytes of EEPROM data are provided in bank 0. No CRC validation against a pre-stored CRC value occurs when Bank 0 is programmed, and thus, there are no dedicated EEPROM Cells used for CRC storage.


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Due to limited number of erase/write cycles, the user has to keep track of the number of writes to EEPROM Bank 0 and store the value inside the bank because it is the only bank that is accessable when the write is occuring.

#### 6.20.2.1.3 Banks 1-4

Banks 1–4 are used for storage of customer data. Each bank 1 through 4 provides 128-bits of data storage for a total of 512 bits (64 bytes) of storage data. Since the 8051W does not have access to these banks, only the digital interfaces can program them. Each time one of these banks is programmed a CRC is calculated based upon the data held in the EEPROM Cache during program. This calculated CRC value is stored internally and validated after bank programming is complete.

#### 6.20.2.1.4 Bank 5

The firse 64-bits (8 bytes) of Bank 5 are provided to the customer for calibration value and/or general storage. Byte 9 is used for the storage of the cummulative CRC values for banks 1-4 and the first half of Bank 5. When programming Bank 5 it is required to place the cumulative CRC value for banks 1–5 in the EEPROM Cache Address 0x558. This CRC value covers all data in banks 1 through 4 and the first 64-bits of data in bank 5. Everytime programming of Bank 5 is completed the CRC value is validated. The remaining 7 bytes of Bank 5 (0x559 - 0x55F) are not used.

### 6.20.3 RAM Memory

This memory space is used for 8051W scratchpad memory, such as intermediate calculation results. It is a 256 byte memory space, and located at memory page 1.

### 6.20.4 SFR/ESFR Memory

The 8051W uses two types of memory storage, Special Function Registers (SFR) and External Special Function Registers (ESFR). The SFR registers are used for 8051W internal operations, and cannot be accessed external to the 8051W. The ESFR register exists on the same address space as the SFR, however these registers can be accessed via the digital interface. The ESFR registers are used for calibration, configuration, fault reporting and memory storage. The SFR/ESFR total memory space is 256 bytes, and they are located at memory page 2.

### 6.20.5 Test Register Memory

The test register memory space is used for diagnostic configuration, and testing for sensor calibration. The test registers are located at memory page 0, and can only be accessed by the Digital Interface.

## 6.21 General Purpose Input Output (GPIO) Pins

The GPIO_x pins have multiple functions, including general purpose inputs/outputs (GPIO), input capture, output compare or I2C. In the GPIO mode, the GPIO_x pins are connected directly to 8051W port pins. The state of the pins can then be controlled through software by setting the appropriate I/O port SFRs in the 8051W. Table 6-5 shows the mapping of the GPIO_x pins to specific 8051W ports.

### 6.21.1 Setting the GPIO Functions

**Table 6-5. GPIO_x Pin Functionality**

| PIN | 8051W PORT | ALTERNATE FUNCTION 1 | ALTERNATE FUNCTION 2 |
|---|---|---|---|
| GPIO_1/IC_1/SDA | 2.0 | Input Capture 1 | I2C Data |
| | Default | Set IC1_ACT to 1 in IC_OC_GPIO | Set DI_CTRL[1:0] = 0b01 in DI_CTRL |
| GPIO_2/IC_2 | 2.1 | Input Capture 2 | - |
| | Default | Set IC2_ACT to 1 in IC_OC_GPIO | |

**Table 6-5. GPIO_x Pin Functionality (continued)**

| PIN | 8051W PORT | ALTERNATE FUNCTION 1 | ALTERNATE FUNCTION 2 |
|---|---|---|---|
| GPIO_3/OC_1/SCL | 2.2 | Output Compare 1 | I2C Clock |
| | Default | Set OC1_ACT to 1 in IC_OC_GPIO | Set DI_CTRL[1:0] = 0b01 in DI_CTRL |
| GPIO_4/OC_2 | 2.3 | Output Compare 2 | |
| | Default | Set OC2_ACT to 1 in IC_OC_GPIO | |
| GPIO_5 | 3.2 | - | - |
| | Default | | |

After power up or reset, the default configuration for all of these pins is the input GPIO function. To change the function of a pin a write command to the appropriate ESFR will automatically reconfigure it. Table 6-5 shows the appropiate bits in each ESFR that need to be set to enable different functions for each GPIO pin.

As Table 6-5 shows, some GPIOx pins can be configured for multiple alternate functionalities and therefore the device implements a priority level for each GPIO configuration. The priority level is as follows:

1. $I^2C$
2. Input Capture / Output Compare
3. General Purpose I/Os

This means that if the IC1_ACT bit is set to 1 (enabling Input Capture 1 functionality on GPIO_1 pin) and the DI_CTRL[1:0] bits are set to 0x01 (enabling I2C functionality on GPIO_1) then the GPIO_1 pin is configured as I2C pin.

### *6.21.2 GPIO Buffers*

The device includes five general purpose digital input/output buffers, one for each of the GPIO_x pin. The buffers can be configured to operate as standard 8051W I/O buffers or other alternate functions such as I2C and input capture/output compare. The direction of the buffers are controlled digitally depending on the mode of the GPIO_x pin.

The device also offers a strong drive mode which allows the user to override the digital control signals generated by the 8051W GPIO interface. This mode is set for a given IO buffer via the GPIO Strong Output Drive Mode ESFR. When a ‘1’ is written to the ST_GPOx bit, a switch at the output of the Output buffer is always closed, providing a means to strongly pull up or down the voltage on the GPIO_x pin regardless of whether output data is low or high. It is important to note that the *GPIO Strong Output Drive Mode* ESFR can be set independent of the function assigned to the GPIO buffers. Strong drive mode should be disabled if the buffer should operate as an input or in I2C mode.

## 6.22 8051W UART

The TxD and RxD pins are connected to the 8051W UART. These pins can either be used for software debugging or for implementing application-specific protocols. Both the TxD and RxD pins have their respective unidirectional buffers.

## 6.23 DAC Output

The device includes two 12-bit digital to analog converters that produce a ratiometric output voltage with respect to the VDD supply. The digital input comes from the DAC 1 or DAC 2 registers, where the 4 MSBs reside in a separate address from the 8 LSBs. **In order to update the analog outputs on the VOUTx pins in a coherent manner, the software must update the MSBs first, followed by the LSBs.**


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**NOTE**

Changes in the VDD voltage result in a proportional change in the output voltage because the current reference for the DAC is derived from VDD.

## 6.24 Input Capture and Output Compare

The device has two Input Capture and two Output Compare ports. Table 6-5 shows the GPIO pins of the device that can be used for Input Capture and Output Compare ports. The capture and compare functionality uses a 16-bit Free Running Timer for the events.

### *6.24.1 Free Running Timer*

The Free Running Timer is a 16-bit timer that is different from the 8051W native timers. The resolution of the Free Running Timer can be set to either 1µs/bit or 0.5µs/bit using 10_20_MHZ bit in Input Capture/Output Compare Control Register (IC_OC_CTRL) in the ESFR memory spacer.

The current value of the Free Running Timer can be accessed using the Free Running Timer Shadow Registers (FRTMSB & FRTLSB). This register in only updated upon request, it is not continuously updated. When the IC_OC_TIM_LAT bit in the Input Capture/Output Compare Control Register (IC_OC_CTRL) is set to logic 1, the current value of the Free Running Timer is written to the Free Running Timer Shadow registers.

### *6.24.2 Input Capture*

The device has 2 Input Capture ports. The Input Capture functionality can be enabled when the pin is configured to be a GPIO by setting ICx_ACT (x = 1,2) bits in the Input Capture/Output Compare GPIO Register (IC_OC_GPIO) in the ESFR memory space. When the user sets the corresponding bit to logic high, the GPIO pin is configured for Input Capture functionality automatically.

The Input Capture port can be configured to either capture the Free Running Timer value on a rising edge or falling edge using the ICx_EDGE bits in the Input Capture/Output Compare Control Register (IC_OC_CTRL) in the ESFR memory space. Both IC_1 and IC_2 each have unique 16-bit timer capture registers associated with them called Input Capture 1 Register and Input Capture 2 Register respectively. When the corresponding rising or falling edge occurs the Input Capture peripheral transfers the value of the Free Running Timer into the corresponding capture register and generates an interrupt to the 8051W.

### *6.24.3 Output Compare*

The device has 2 Output Compare ports. The Output Compare functionality can be enabled when the pin is configured to be a GPIO by setting OCx_ACT (x = 1,2) bits in the Input Capture/Output Compare GPIO Register (IC_OC_GPIO) in the ESFR memory space.

The Output Compare port can be configured to either (1) Set the pin to High level when the match occurs or (2) Set the pin to Low level when the match occurs. The user can configure the desired state of the OC_1 and OC_2 pins at match using OC1_LVL and OC2_LVL bits in the Input Capture/Output Compare Control Register (IC_OC_CTRL) .

Each Output Compare port has a unique 16-bit timer compare register associated with it. When the value programmed in the compare register matches the value of the Free Running Timer, the Output Compare peripheral changes the state of the corresponding pin to the configured value and generates a unique interrupt to the 8051W. This occurs every time the value in the Compare register matches the value of the Free Running Timer.

**NOTE**

For correct function of the output compare it is recommended that the MSB be updated first and then the LSB.

## 6.25 Diagnostics

This section describes the diagnostics.

### 6.25.1 Power Supply Diagnostics

The device includes modules to monitor the power supply for faults. The internal power rails that are monitored are AVDD, DVDD, VBRG, and EEPROM charge pump. Please refer to the electrical specifications for the thresholds.

When a fault is detected, an appropriate bit in the PSMON1 and PSMON2 registers is set. If the faulty condition is removed, the fault bits will remain latched. To remove the fault the 8051W software should read the fault bit and write a logic zero back to the bit. In addition a system reset will clear the fault.

### 6.25.2 Resistive Bridge Sensor Connectivity Diagnostics

The device includes modules to monitor for sensor faults. Specifically, the device monitors the sensor pins for opens (including loss of connection from the sensor), short-to-ground, and short to sensor supply.

When a fault is detected, an appropriate bit in the AFEDIAG register is set. All three types of sensor faults will result in the setting of the same bit, meaning it is not possible to distinguish the type of fault that has occured. Even after the faulty condition is removed, the fault bits remains latched. To remove the fault the 8051W software should read the fault bit and write a logic zero back to the bit. In addition a system reset will clear the fault.

Open Sensor Faults are detected through the use of an internal pull-down resistor. The value of the resistor can be configured using DIS_R1M and DIS_R2M bits in Decimator and Low Power Control Register (DECCTRL) in the ESFR memory space. This configurability allows the detection of open sensor faults for various Stage 1 Gain settings.

### 6.25.3 AFE Diagnostics

The device includes modules that verify that the input signal of each stage is within a certain range. This ensures that every stage of the signal chain is working normally. Overvoltage and undervoltage range flags are implemented in four locations along the signal chain (Sensor Input, Stage 1 Gain output, Stage 2 Gain output, and ADC Buffer output). When a fault is detected, the corresponding bit is set in the AFEDIAG registers. It is noted both overvoltage and undervoltage conditions set a common bit; i.e., it is not possible to distinguish between overvoltage and undervoltage.

The AFE Diagnostics also includes the monitoring of the frequency of the Self-Oscillating Demodulator circuit used for capacitive sensor interface. If the frequency is less than 40KHz (typical) or more than 1MHz (typical), a fault flag is set in the AFEDIAG register. The monitoring of this frequency can be enabled or disabled using the CTOV_CLK_MON_EN bit in the ENABLE CONTROL register. Both over-frequency and under-frequency conditions set same bit which means it is not possible to distinguish which type of fault occured that resulting in the flag.

The typical threshold values for these faults are in boxes in Figure 6-14.

When a fault is detected, an appropriate bit in the AFEDIAG register is set. All sensor faults will result in the setting of the same bit, meaning there is no way to distinguish the type of fault. Even after the faulty condition is removed, the fault bits will remain latched. To remove the fault the 8051W software should read the fault bit and write a logic zero back to the bit. In addition a system reset will clear the fault.


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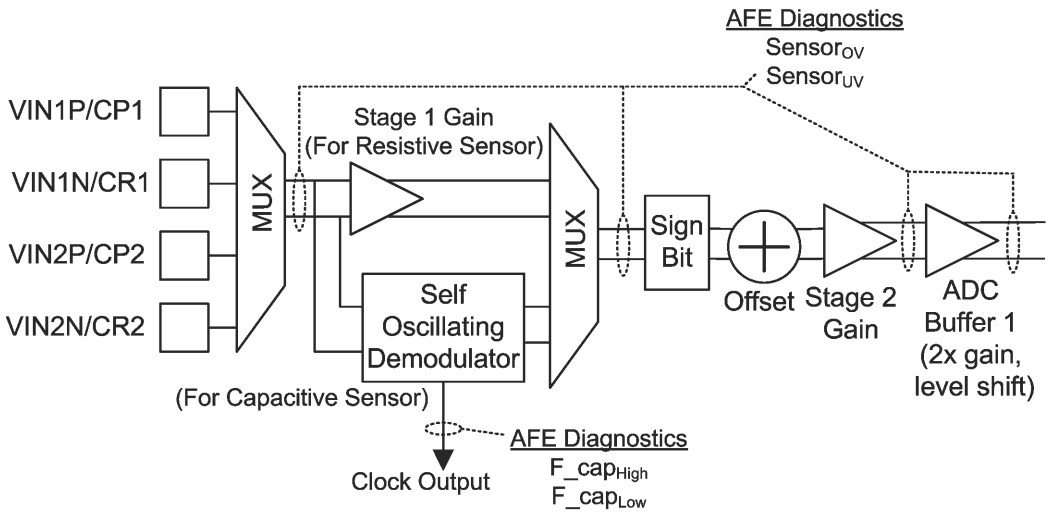


**Figure 6-14. Block Diagram of AFE Diagnostics**

### 6.25.4 Internal Capacitors for Capacitive Sensor Diagnostics

The device includes Cp and Cr Test capacitors that can be connected to the capacitive AFE via software control. This allows the software to check the integrity of the capacitive signal chain in the IC.

Figure Figure 6-15 shows the block diagram with the Cp and Cr Test capacitors. The Cp Test capacitor is 10pF and Cr Test capacitor is 8pF.

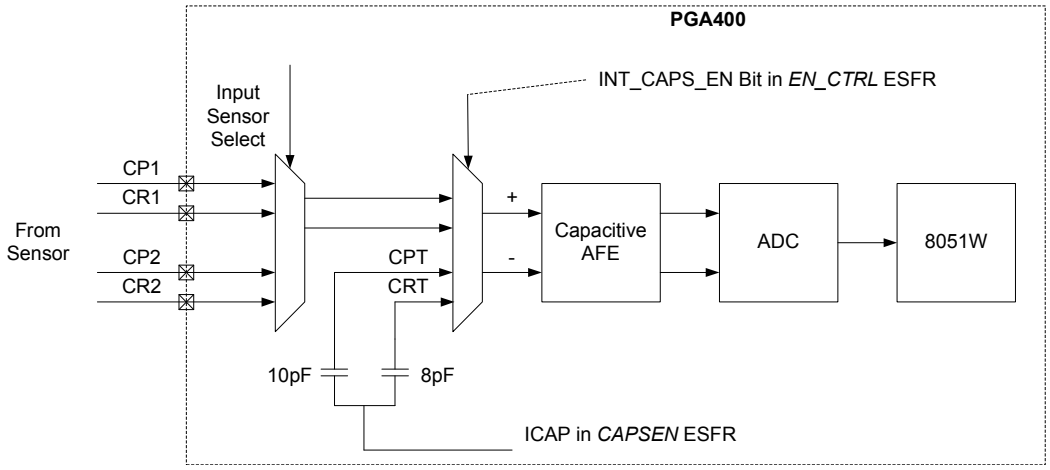


**Figure 6-15. Internal Capacitors for Capacitive Sensor Diagnostics.**

### 6.25.5 DAC Diagnostics

The device implements a “Loop Back” feature to check the integrity of the two DAC outputs. Figure Figure 6-16 shows the block diagram representation of the Loop Back feature. This figure shows that DAC1 output is connected to positive side of the differential input while DAC2 is connected to negative side of the differential input.

The DAC outputs are voltage divided by a nominal factor of 6/11 before being connected to the AFE inputs.

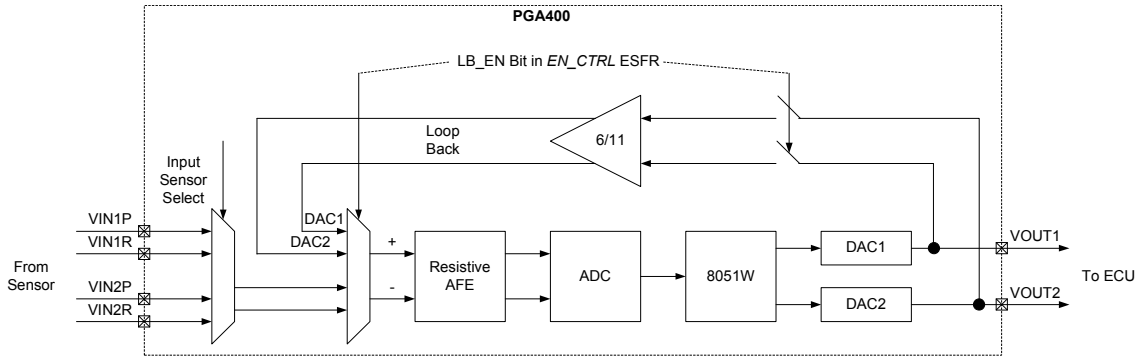


**Figure 6-16. DAC Loop Back.**

DAC loop back is enabled by setting LB_EN bit in EN_CTRL to 1. In this mode, Sensor 1 Channel gain and offset settings are used. Note that ADC output represents the voltage difference between DAC1 and DAC2 outputs scaled by the voltage divider and the AFE gains/offsets.

Note that when LB_EN is set to 1, the AFE is switched to resistive mode, even if SEN_TYP bit is set to Capacitive mode.

The DAC outputs continue to be available on VOUT1 and VOUT2 pins in the Loop Back mode.

### *6.25.6 EEPROM CRC and TRIM Error*

The 9th Byte in Bank 5 of the EEPROM stores the CRC for all the data in EEPROM Banks 1 through 5.

The user can verify the EEPROM CRC at any time by loading Banks 1 through 5 in sequence into the EEPROM Cache. When Bank 5 is loaded into the Cache, the device automatically calculates the CRC and updates the CRC_ERR bit in EE_STATUS ESFR.

The device also has analog trim values. The validity of the analog trim values is checked on power up and before the 8051W reset is de-asserted. The validity of the trim values can be inferred using the TRIM_ERR bit in EE_STATUS ESFR.

Note that Banks 0 can be updated by software in the field, but the user has to maintain CRC (or checksum) for this bank using software.

### *6.25.7 RAM MBIST*

The device implements RAM MBIST (Memory Built-In Self-Test). This diagnostic checks the integrity of the internal RAM on an on-demand basis.

The procedure to start this diagnostic and check for status is as below:

- 1. Set EN_IRAM_MBIST to 1 in EN_CTRL2 register. This starts the RAM MBIST.
- 2. Wait for IRAM_MBIST_DONE in RAM_MBIST_ST to be set to 1 by the RAM MBIST algorithm
- 3. Check IRAM_MBIST_FAIL bit in RAM_MBIST_ST register after IRAM_MBIST_DONE flag is set to 1. If IRAM_MIBIST_FAIL is 1, then RAM MBIST failed, indicating faulty RAM. If IRAM_MBIST_FAIL is 0, then RAM has no faults.

The RAM MBIST can be run only once every power cycle.

**NOTE**

While the RAM MBIST is running, the 8051W should not access the RAM.


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### 6.25.8 Main Oscillator Watchdog

There is watch dog monitor for the main oscillator clock whether using the internal 40MHz oscillator or the external crystal input. When the frequency is outside the range of 35-45MHz the entire device is reset. The main oscillator watchdog can be disabled using MAIN_OSC_WD_EN bit in the ENABLE CONTROL register.

### 6.25.9 Software Watchdog

The device also implements a software watchdog. This watchdog has to be serviced by software every 500ms. If the software does not service the watchdog within 500ms of the last service, then the 8051W core is reset. The software services the watchdog by toggling the state of an internal pin between the two blocks. The state of this pin cannot be read back to the 8051W. If this function is not desired the software watchdog can be disabled using CPU_WD_EN bit in the ENABLE CONTROL register.

When the software watchdog times out and resets the 8051W, DAC1 and DAC2 registers are reset to 0, which causes VOUT1 and VOUT2 to be driven to 0V. The remaining ESFRs retains the settings from prior to the reset events. This implies that CPU_WD_EN also remains set.

## 6.26 Low Power Mode

The device has multiple low power modes. In each mode, certain functional blocks can be turned on or off through the use of different ESFRs. Table 6-6 lists which bits in each ESFR that disables certain blocks of the device.

**Table 6-6. Low Power Control**

| CONTROL BIT | ESFR | CONTROL ACTION |
|---|---|---|
| VBRG_EN | SENCTRL | Enables/Disables VBRG supply |
| DAC2_EN | DECCTRL | Enables/Disables DAC2 |
| AFE_EN | DECCTRL | Enables/Disable AFE |
| EN_DI_IF_CLK | EN_CTRL2 | Enable/Disable Digital Interface |
| EN_EEPROM_CTRL_CLK | EN_CTRL2 | Enable/Disable EEPROM clock |

The following blocks does not enter low power mode at any time:

- Microprocessor – the microprocessor continues to operate at the same frequency
- OTP/EEPROM – The memory is kept alive and runs at the same speed VOUT1/OWI

# 7 PROGRAMMER MODEL

## 7.1 8051W Memory Map

The Memory block consists of SRAM, OTP, and EEPROM. The SRAM is used as storage for volatile software variables during program execution. The OTP consists of the program code and the EEPROM consists of calibrations.

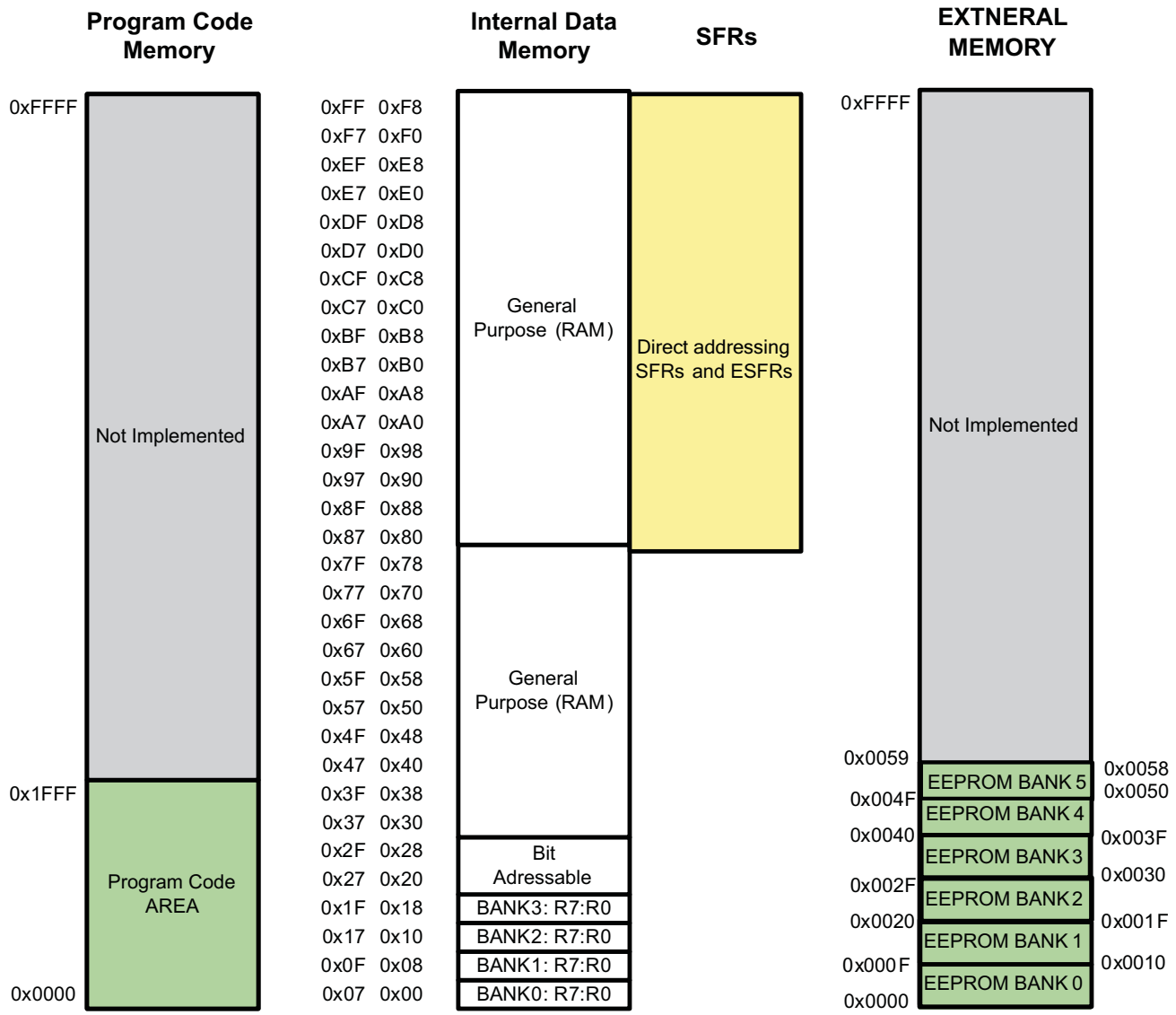


**Figure 7-1. Memory Map**


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## 7.2 SFR

| ADDRESS (hex) | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | R/W | POWER UP | DESCRIPTION (PROGRAMMABLE REGS) |
|---|---|---|---|---|---|---|---|---|---|---|---|
| 80 | P0<7> | P0<6> | P0<5> | P0<4> | P0<3> | P0<2> | P0<1> | P0<0> | R/W | 0xFF | P0 |
| 81 | SP<7> | SP<6> | SP<5> | SP<4> | SP<3> | SP<2> | SP<1> | SP<0> | R/W | 0 | SP |
| 82 | DPTR<7> | DPTR<6> | DPTR<5> | DPTR<4> | DPTR<3> | DPTR<2> | DPTR<1> | DPTR<0> | R/W | 0 | DPL |
| 83 | DPTR<15> | DPTR<14> | DPTR<13> | DPTR<12> | DPTR<11> | DPTR<10> | DPTR<9> | DPTR<8> | R/W | 0 | DPH |
| 87 | SMOD | - | - | - | GF1 | GF0 | PD | IDL | R/W | 0 | PCON |
| 88 | TF1 | TR1 | TF0 | TR0 | IE1 | IT1 | IE0 | IT0 | R/W | 0 | TCON |
| 89 | GATE1 | CNT1 | M1 (1) | M0 (1) | GATE0 | CNT0 | M1 (0) | M0 (0) | R/W | 0 | TMOD |
| 8A | TL0<7> | TL0<6> | TL0<5> | TL0<4> | TL0<3> | TL0<2> | TL0<1> | TL0<0> | R/W | 0 | TL0 |
| 8B | TL1<7> | TL1<6> | TL1<5> | TL1<4> | TL1<3> | TL1<2> | TL1<1> | TL1<0> | R/W | 0 | TL1 |
| 8C | TH0<7> | TH0<6> | TH0<5> | TH0<4> | TH0<3> | TH0<2> | TH0<1> | TH0<0> | R/W | 0 | TH0 |
| 8D | TH1<7> | TH1<6> | TH1<5> | TH1<4> | TH1<3> | TH1<2> | TH1<1> | TH1<0> | R/W | 0 | TH1 |
| 90 | P1<7> | P1<6> | P1<5> | P1<4> | P1<3> | P1<2> | P1<1> | P1<0> | R/W | 0xFF | P1 |
| 98 | SM0 | SM1 | SM2 | REN | TB8 | RB8 | TI | RI | R/W | 0 | SCON |
| 99 | SBUF<7> | SBUF<6> | SBUF<5> | SBUF<4> | SBUF<3> | SBUF<2> | SBUF<1> | SBUF<0> | R/W | 0 | SBUF |
| A0 | P2<7> | P2<6> | P2<5> | P2<4> | P2<3> | P2<2> | P2<1> | P2<0> | R/W | 0xFF | P2 |
| A8 | EA | - | EI5 | ES | ET1 | EX1 | ET0 | EX0 | R/W | 0 | IE0 |
| B0 | P3<7> | P3<6> | P3<5> | P3<4> | P3<3> | P3<2> | P3<1> | P3<0> | R/W | 0 | P3 |
| B8 | - | - | PI5 | PS | PT1 | PX1 | PT0 | PX0 | R/W | 0xFF | IP0 |
| D0 | CY | AC | F0 | RS1 | RS0 | OV | F1 | P | R/W | 0 | PSW |
| E0 | ACC<7> | ACC<6> | ACC<5> | ACC<4> | ACC<3> | ACC<2> | ACC<1> | ACC<0> | R/W | 0 | ACC |
| E8 | EI13 | EI12 | EI11 | EI10 | EI9 | EI8 | EI7 | EI6 | R/W | 0 | IE1 |
| F0 | B<7> | B<6> | B<5> | B<4> | B<3> | B<2> | B<1> | B<0> | R/W | 0 | B |
| F8 | PI13 | PI12 | PI11 | PI10 | PI9 | PI8 | PI7 | PI6 | R/W | 0 | IP1 |

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### 7.2.1 I/O PORTS(P0,P1,P2,P3)

P0, P1, P2 and P3 are latches used to drive the 32 quasi-bi-directional I/O lines. On reset they are all set to the value FF hex, which is input mode.

| I/O PORTS(P0,P1,P2,P3) | | | | Bit Addressable | | | | |
|---|---|---|---|---|---|---|---|---|
| SFR: | 0xB0 | P3 | | | | | | |
| | BIT 7 | BIT 6 | BIT 5 | BIT 4 | BIT 3 | BIT 2 | BIT 1 | BIT 0 |
| | P3<7> | P3<6> | P3<5> | P3<4> | P3<3> | P3<2> | P3<1> | P3<0> |
| Access | r/w | r/w | r/w | r/w | r/w | r/w | w | R |
| At Reset | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |

| Some of the Port 3 have alternate function as shown below. | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | BIT 7 | BIT 6 | BIT 5 | BIT 4 | BIT 3 | BIT 2 | BIT 1 | BIT 0 |
| | - | - | T1 | T0 | NINT1 | NINT0 | TXD | RXD |
| | - | - | input | input | input | input | output | Input |
| BIT1: TXD | output | Serial Transmit Data from UART and transmit clock in UART mode 0. | | | | | | |
| BIT0: RXD | input | Serial Receive Data to UART | | | | | | |
| SFR: | 0xA0 | P2 | | | | | | |
| | BIT 7 | BIT 6 | BIT 5 | BIT 4 | BIT 3 | BIT 2 | BIT 1 | BIT 0 |
| | P2<7> | P2<6> | P2<5> | P2<4> | P2<3> | P2<2> | P2<1> | P2<0> |
| Access | r/w | r/w | r/w | r/w | r/w | r/w | r/w | r/w |
| At Reset | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| SFR: | 0x90 | P1 | | | | | | |
| | BIT 7 | BIT 6 | BIT 5 | BIT 4 | BIT 3 | BIT 2 | BIT 1 | BIT 0 |
| | P1<7> | P1<6> | P1<5> | P1<4> | P1<3> | P1<2> | P1<1> | P1<0> |
| Access | r/w | r/w | r/w | r/w | r/w | r/w | r/w | r/w |
| At Reset | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| SFR: | 0x80 | P0 | | | | | | |
| | BIT 7 | BIT 6 | BIT 5 | BIT 4 | BIT 3 | BIT 2 | BIT 1 | BIT 0 |
| | P0<7> | P0<6> | P0<5> | P0<4> | P0<3> | P0<2> | P0<1> | P0<0> |
| Access | r/w | r/w | r/w | r/w | r/w | r/w | r/w | r/w |
| At Reset | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |

### 7.2.2 Stack Pointer (SP)

The SP register contains the Stack Pointer. The Stack Pointer is used to load the program counter into Internal Data Memory during LCALL and ACALL instructions and is used to retrieve the program counter from memory during RET and RETI instructions. Data may also be saved on or retrieved from the stack using PUSH and POP instructions. Instructions that use the stack automatically pre-increment or post-decrement the stack pointer so that the stack pointer always points to the last byte written to the stack, i.e. the top of the stack. On reset the Stack Pointer is set to 07 hex. It falls to the programmer to ensure that the location of the stack in Internal Data Memory does not interfere with other data stored therein.


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Another use of the Scratchpad area is for the programmer's stack. This area is selected using the Stack Pointer (SP, SFR 81h). Whenever a call or interrupt is invoked, the return address is placed on the Stack. It also is available to the programmer for variables, etc., since the Stack can be moved and there is no fixed location within the RAM designated as Stack. The Stack Pointer defaults to 07h on reset and the user can then move it as needed. The SP will point to the last used value. Therefore, the next value placed on the Stack is put at SP + 1. Each PUSH or CALL increments the SP by the appropriate value and each POP or RET decrements it.

| Stack Pointer (SP) | | | | Not Bit Addressable | | | | |
|---|---|---|---|---|---|---|---|---|
| SFR: | 0x81 | SP | | | | | | |
| | BIT 7 | BIT 6 | BIT 5 | BIT 4 | BIT 3 | BIT 2 | BIT 1 | BIT 0 |
| | SP<7> | SP<6> | SP<5> | SP<4> | SP<3> | SP<2> | SP<1> | SP<0> |
| Access | r/w | r/w | r/w | r/w | r/w | r/w | r/w | r/w |
| At Reset | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 |

### 7.2.3 Data Pointer (DPTR)

The Data Pointer (DPTR) is a 16-bit register that may be accessed via the two SFR locations, Data Pointer High byte (DPH) and Data Pointer Low byte (DPL). Two true 16-bit operations are allowed on the Data Pointer - load immediate and increment. The Data Pointer is used to form 16-bit addresses for External Data Memory accesses (MOVX), for program byte moves (MOVC) and for indirect program jumps (JMP @A+DPTR). On reset the Data Pointer is set to 0000 hex.

| Data Pointer (DPTR) | | | | Not Bit Addressable | | | | |
|---|---|---|---|---|---|---|---|---|
| SFR: | 0x82 | DPL | | | | | | |
| | BIT 7 | BIT 6 | BIT 5 | BIT 4 | BIT 3 | BIT 2 | BIT 1 | BIT 0 |
| | DPTR<7> | DPTR<6> | DPTR<5> | DPTR<4> | DPTR<3> | DPTR<2> | DPTR<1> | DPTR<0> |
| Access | r/w | r/w | r/w | r/w | r/w | r/w | r/w | r/w |
| At Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | | | | | | | | |
| SFR: | 0x83 | DPH | | | | | | |
| | BIT 7 | BIT 6 | BIT 5 | BIT 4 | BIT 3 | BIT 2 | BIT 1 | BIT 0 |
| | DPTR<15> | DPTR<14> | DPTR<13> | DPTR<12> | DPTR<11> | DPTR<10> | DPTR<9> | DPTR<8> |
| Access | r/w | r/w | r/w | r/w | r/w | r/w | r/w | r/w |
| At Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

### 7.2.4 Power Control Register (PCON)

| Power Control Register (PCON) | | | | Not Bit Addressable | | | | |
|---|---|---|---|---|---|---|---|---|
| SFR: | 0x87 | PCON | | | | | | |
| | BIT 7 | BIT 6 | BIT 5 | BIT 4 | BIT 3 | BIT 2 | BIT 1 | BIT 0 |
| | SMOD | - | - | - | GF1 | GF0 | PD | IDL |
| Access | r/w | r | r | r | r/w | r/w | r/w | r/w |
| At Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| The bit definitions for this register are as follows. | |
|---|---|
| BIT7: SMOD | Double baud rate bit. For use, see the Serial Interface section below. |
| BIT3: GF1 | General purpose flag bit. |
| BIT2: GF0 | General purpose flag bit. |
| BIT1: PD | Power-Down bit. If 1, Power-Down mode is entered. |
| BIT0: IDL | Idle bit. If "1", Idle mode is entered. |

### 7.2.5 Timer/Counter Control (TCON)

Two 16-bit timer/counters are provided. TCON and TMOD are used to set the mode of operation and to control the running and interrupt generation of the timer/counters. The timer/counter values are stored in two pairs of 8-bit registers (TL0, TH0, and TL1, TH1).

| Timer/Counter Register (TCON) | | | | Bit Addressable | | | | |
|---|---|---|---|---|---|---|---|---|
| SFR: | 0x88 | TCON | | | | | | |
| | BIT 7 | BIT 6 | BIT 5 | BIT 4 | BIT 3 | BIT 2 | BIT 1 | BIT 0 |
| | TF1 | TR1 | TF0 | TR0 | IE1 | IT1 | IE0 | IT0 |
| Access | r/w | r/w | r/w | r/w | r/w | r/w | r/w | r/w |
| At Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

The bit definitions for this register are as follows.

| | | |
|---|---|---|
| Timer1 | BIT7: TF1 | Timer 1 overflow flag. Set by hardware when Timer/Counter 1 overflows. Cleared by hardware when the processor calls the interrupt service routine. |
| Timer1 | BIT6: TR1 | Timer 1 run control. If “1”, timer runs; if “0”, timer is halted. |
| Timer0 | BIT5: TF0 | Timer 0 overflow flag. Set by hardware when Timer/Counter 0 overflows. Cleared by hardware when the processor calls the interrupt service routine. |
| Timer0 | BIT4: TR0 | Timer 0 run control. If “1”, timer runs; if “0”, timer is halted. |
| External Interrupt1 | BIT3: IE1 | External Interrupt 1 edge flag. Set by hardware when an External Interrupt 1 edge is detected. |
| External Interrupt1 | BIT2: IT1 | External Interrupt 1 control bit. If “1”, External Interrupt 1 is “edge-triggered”; if “0”, External Interrupt 1 is “level triggered” |
| External Interrupt0 | BIT1: IE0 | External Interrupt 0 edge flag. Set by hardware when an External Interrupt 0 edge is detected. |
| External Interrupt0 | BIT0: IT0 | External Interrupt 1 control bit. If “1”, External Interrupt 1 is “edge-triggered”; if “0”, External Interrupt 1 is “level triggered” |

### 7.2.6 Timer/Counter Mode (TMOD)

| Timer/Counter Mode (TMOD) | | | | Not Bit Addressable | | | | |
|---|---|---|---|---|---|---|---|---|
| SFR: | 0x89 | TCON | | | | | | |
| | BIT 7 | BIT 6 | BIT 5 | BIT 4 | BIT 3 | BIT 2 | BIT 1 | BIT 0 |
| | GATE1 | CNT1 | M1 (1) | M0 (1) | GATE0 | CNT0 | M1 (0) | M0 (0) |
| Access | r/w | r/w | r/w | r/w | r/w | r/w | r/w | r/w |
| At Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

The bit definitions for this register are as follows.

| | | |
|---|---|---|
| Timer1 | BIT7: GATE1 | Timer 1 gate flag. When TCON.6 is set and GATE1= 1, Timer/Counter 1 will only run if NINT1 pin is 1 (hardware control). When GATE1= 0, Timer/Counter 1 will only run if TCON.6 = 1 (software control). |
| Timer1 | BIT6: CNT1 | Timer/Counter 1 selector. If 0, input is from internal system clock; if “1”, input is from T1 pin. |
| Timer1 | BIT5: M1(1) | Timer 1 Mode control bit M1. |
| Timer1 | BIT4: M0(1) | Timer 1 Mode control bit M0. |
| Timer0 | BIT3: GATE0 | Timer 0 gate flag. When TCON.4 is set and GATE0= 1, Timer/Counter 0 will only run if NINT0 pin is 1 (hardware control). When GATE0 = 0, Timer/Counter 0 will only run if TCON.4 = 1 (software control). |
| Timer0 | BIT2: CNT0 | Timer/Counter 0 selector. If 0, input is from internal system clock; if “1”, input is from T0 pin. |
| Timer0 | BIT1: M1(0) | Timer 0 Mode control bit M1. |
| Timer0 | BIT0: M0(0) | Timer 0 Mode control bit M0. |

For both timer/counters, the mode bits M0 and M1 apply as follows:

| M1 | M0 | Operating Mode |
|---|---|---|
| 0 | 0 | 13-bit timer/counter (M8048 compatible mode). |
| 0 | 1 | 16-bit timer/counter. |
| 1 | 0 | 8-bit auto-reload timer/counter. |


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| | | |
|---|---|---|
| 1 | 1 | Timer 0 is split into two halves. TL0 is an 8-bit timer/counter controlled by the standard Timer 0control bits. TH0 is an 8-bit timer/counter controlled by the standard Timer 1 control bits. TH1 and TL1 are held (Timer 1 is stopped). |

### 7.2.7 Timer/Counter Data (TL0 TL1 TH0 TH1)

TL0 and TH0 are the low and high bytes of Timer/Counter 0 respectively. TL1 and TH1 are the low and high bytes of Timer/Counter 1 respectively. In Mode 2, the TL register is an 8-bit counter and TH stores the reload value. On reset all timer/counter registers are 00 hex.

| Timer/Counter Data (TL0 TL1 TH0 TH1) | | | | Not Bit Addressable | | | | |
|---|---|---|---|---|---|---|---|---|
| SFR: | 0x8A | TL0 | | | | | | |
| | BIT 7 | BIT 6 | BIT 5 | BIT 4 | BIT 3 | BIT 2 | BIT 1 | BIT 0 |
| | TL0<7> | TL0<6> | TL0<5> | TL0<4> | TL0<3> | TL0<2> | TL0<1> | TL0<0> |
| Access | r/w | r/w | r/w | r/w | r/w | r/w | r/w | r/w |
| At Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| SFR: | 0x8B | TL1 | | | | | | |
| | BIT 7 | BIT 6 | BIT 5 | BIT 4 | BIT 3 | BIT 2 | BIT 1 | BIT 0 |
| | TL1<7> | TL1<6> | TL1<5> | TL1<4> | TL1<3> | TL1<2> | TL1<1> | TL1<0> |
| Access | r/w | r/w | r/w | r/w | r/w | r/w | r/w | r/w |
| At Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| SFR: | 0x8C | TH0 | | | | | | |
| | BIT 7 | BIT 6 | BIT 5 | BIT 4 | BIT 3 | BIT 2 | BIT 1 | BIT 0 |
| | TH0<7> | TH0<6> | TH0<5> | TH0<4> | TH0<3> | TH0<2> | TH0<1> | TH0<0> |
| Access | r/w | r/w | r/w | r/w | r/w | r/w | r/w | r/w |
| At Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| SFR: | 0x8D | TH1 | | | | | | |
| | BIT 7 | BIT 6 | BIT 5 | BIT 4 | BIT 3 | BIT 2 | BIT 1 | BIT 0 |
| | TH1<7> | TH1<6> | TH1<5> | TH1<4> | TH1<3> | TH1<2> | TH1<1> | TH1<0> |
| Access | r/w | r/w | r/w | r/w | r/w | r/w | r/w | r/w |
| At Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

The timer clock resolution is 5MHz.

### 7.2.8 UART Control (SCON)

The UART uses two SFRs, SCON and SBUF. SCON is the control register, SBUF the data register. Data is written to SBUF for transmission and SBUF is read to obtain received data. The received data and transmitted data registers are independent.

| UART Control (SCON) | | | | Bit Addressable | | | | |
|---|---|---|---|---|---|---|---|---|
| SFR: | 0x98 | SCON | | | | | | |
| | BIT 7 | BIT 6 | BIT 5 | BIT 4 | BIT 3 | BIT 2 | BIT 1 | BIT 0 |
| | SM0 | SM1 | SM2 | REN | TB8 | RB8 | TI | RI |
| Access | r/w | r/w | r/w | r/w | r/w | r/w | r/w | r/w |
| At Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| The bit definitions for this register are as follows. | |
|---|---|
| BIT7: SM0 | UART mode specifier. |
| BIT6: SM1 | UART mode specifier. |
| BIT5: SM2 | UART mode specifier. |
| BIT4: REN | If “1”, enables reception; if “0”, disables reception. |
| BIT3: TB8 | In Modes 2 and 3, this is the 9th data bit sent. |
| BIT2: RB8 | In Modes 2 and 3, this is the 9th data bit received. In Mode 1, if SM2 = 0, this is the stop bit received. In Mode 0, this bit is not used. |

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| | |
|---|---|
| BIT1: TI | Transmit interrupt flag. This is set by hardware at the end of the 8th bit in Mode 0, or at the beginning of the stop bit in other modes. Must be cleared by software. beginning of the stop bit in other modes. Must be cleared by software. beginning of the stop bit in other modes. Must be cleared by software. |
| BIT0: RI | Receive interrupt flag. This is set by hardware at the end of the 8th bit in Mode 0, or at the half point of the stop bit in other modes. Must be cleared by software. |

The mode control bits operate as follows.

| Mode | SM0 | SM1 | Operating Mode | Baud Rate |
|---|---|---|---|---|
| Mode 0 | 0 | 0 | Mode 0: 8 bit shift register. ftimer_clk /2 | Baud Rate = ftimer_clk / 2 |
| Mode 1 | 0 | 1 | Mode 1: 8 bit UART. | Baud Rate = ( SMOD+1) * ftimer_clk / (32 * (256 - TH1)) |
| Mode 2 | 1 | 0 | Mode 2: 9 bit UART. | Baud Rate = ( SMOD+1) * ftimer_clk / 64 |
| Mode 3 | 1 | 1 | Mode 3: 9 bit UART. | Baud Rate = ( SMOD+1) * ftimer_clk / (32 * (256 - TH1)) |

where ftimer_clk is the frequency of the TIMER_CLK input (5MHz).

SM2 enables multi-processor communication over a single serial line and modifies the above as follows. In Modes 2 & 3, if SM2 is set then the receive interrupt will not be generated if the received 9th data bit is 0. In Mode 1, the receive interrupt will not be generated unless a valid stop bit is received. In Mode 0, SM2 should be 0.

### 7.2.9 UART Data (SBUF)

This register is used for both transmit and receive data. Transmit data is written to this location and receive data is read from this location, but the two paths are independent.

| UART Data (SBUF) | | | | Not Bit Addressable | | | | |
|---|---|---|---|---|---|---|---|---|
| SFR: | 0x99 | SBUF | | | | | | |
| | BIT 7 | BIT 6 | BIT 5 | BIT 4 | BIT 3 | BIT 2 | BIT 1 | BIT 0 |
| | SBUF<7> | SBUF<6> | SBUF<5> | SBUF<4> | SBUF<3> | SBUF<2> | SBUF<1> | SBUF<0> |
| Access | r/w | r/w | r/w | r/w | r/w | r/w | r/w | r/w |
| At Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

### 7.2.10 Interrupt Enable Register 0 (IE)

| Interrupt Enable Register 0 (IE) | | | | Bit Addressable | | | | |
|---|---|---|---|---|---|---|---|---|
| SFR: | 0xA8 | IE | | | | | | |
| | BIT 7 | BIT 6 | BIT 5 | BIT 4 | BIT 3 | BIT 2 | BIT 1 | BIT 0 |
| | EA | - | EI5 | ES | ET1 | EX1 | ET0 | EX0 |
| Access | r/w | r | r/w | r/w | r/w | r/w | r/w | r/w |
| At Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |


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| | | |
|---|---|---|
| For each bit in this register, a 1 enables the corresponding interrupt and a 0 disables it. | | |
| | BIT7: EA | Enable or disable all interrupt bits. |
| | BIT5: EI5 | Enable External Interrupt 5. |
| | BIT4: ES | Enable Serial Port interrupt. |
| | BIT3: ET1 | Enable Timer 1 overflow interrupt. |
| | BIT2: EX1 | Enable External Interrupt 1. |
| | BIT1: ET0 | Enable Timer 0 overflow interrupt. |
| | BIT0: EX0 | Enable External Interrupt 0. |

### 7.2.11 Interrupt Enable Register 1 (IE1)

| Interrupt Enable Register 1 (IE1) | | | | Bit Addressable | | | | |
|---|---|---|---|---|---|---|---|---|
| SFR: | 0xE8 | IE1 | | | | | | |
| | BIT 7 | BIT 6 | BIT 5 | BIT 4 | BIT 3 | BIT 2 | BIT 1 | BIT 0 |
| | EI13 | EI12 | EI11 | EI10 | EI9 | EI8 | EI7 | EI6 |
| Access | r/w | r/w | r/w | r/w | r/w | r/w | r/w | r/w |
| At Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| | | |
|---|---|---|
| For each bit in this register, a 1 enables the corresponding interrupt and a 0 disables it. | | |
| | BIT7: EI13 | Enable External Interrupt 13. |
| | BIT6: EI12 | Enable External Interrupt 12. |
| | BIT5: EI11 | Enable External Interrupt 11. |
| | BIT4: EI10 | Enable External Interrupt 10. |
| | BIT3: EI9 | Enable External Interrupt 9. |
| | BIT2: EI8 | Enable External Interrupt 8. |
| | BIT1: EI7 | Enable External Interrupt 7. |
| | BIT0: EI6 | Enable External Interrupt 6. |

### 7.2.12 Interrupt Priority Register 0 (IP)

| Interrupt Priority Register 0 (IP0) | | | | Bit Addressable | | | | |
|---|---|---|---|---|---|---|---|---|
| SFR: | 0xB8 | IP | | | | | | |
| | BIT 7 | BIT 6 | BIT 5 | BIT 4 | BIT 3 | BIT 2 | BIT 1 | BIT 0 |
| | - | - | PI5 | PS | PT1 | PX1 | PT0 | PX0 |
| Access | r | r | r/w | r/w | r/w | r/w | r/w | r/w |
| At Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| | | |
|---|---|---|
| For each bit in this register, a 1 selects high priority for the corresponding interrupt and a 0 selects low priority. The allocation of interrupts to bits is as follows. | | |
| | BIT5: PI5 | Select priority for External Interrupt 5. |
| | BIT4: PS | Select priority for Serial Port interrupt. |
| | BIT3: PT1 | Select priority for Timer 1 overflow interrupt. |
| | BIT2: PX1 | Select priority for External Interrupt 1. |
| | BIT1: PT0 | Select priority for Timer 0 overflow interrupt. |
| | BIT0: PX0 | Select priority for External Interrupt 0. |
| While an interrupt is being serviced, it may only be interrupted by a higher priority interrupt. | | |

### 7.2.13 Interrupt Priority Register 1 (IP1)

| Interrupt Priority Register 1 (IP1) | | | | Bit Addressable | | | | |
|---|---|---|---|---|---|---|---|---|
| SFR: | 0xF8 | IP1 | | | | | | |
| | BIT 7 | BIT 6 | BIT 5 | BIT 4 | BIT 3 | BIT 2 | BIT 1 | BIT 0 |
| | PI13 | PI12 | PI11 | PI10 | PI9 | PI8 | PI7 | PI6 |
| Access | r/w | r/w | r/w | r/w | r/w | r/w | r/w | r/w |
| At Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

For each bit in this register, a 1 selects high priority for the corresponding interrupt and a 0 selects low priority. The allocation of interrupts to bits is as follows.For each bit in this register, a 1 enables the corresponding interrupt and a 0 disables it.

| | |
|---|---|
| BIT7: PI13 | Select priority for External Interrupt 13. |
| BIT6: PI12 | Select priority for External Interrupt 12. |
| BIT5: PI11 | Select priority for External Interrupt 11. |
| BIT4: PI10 | Select priority for External Interrupt 10. |
| BIT3: PI9 | Select priority for External Interrupt 9. |
| BIT2: PI8 | Select priority for External Interrupt 8. |
| BIT1: PI7 | Select priority for External Interrupt 7. |
| BIT0: PI6 | Select priority for External Interrupt 6. |

While an interrupt is being serviced, it may only be interrupted by a higher priority interrupt.

### 7.2.14 Program Status Word (PSW)

| Program Status Word (PSW) | | | | Bit Addressable | | | | |
|---|---|---|---|---|---|---|---|---|
| SFR: | 0xD0 | PSW | | | | | | |
| | BIT 7 | BIT 6 | BIT 5 | BIT 4 | BIT 3 | BIT 2 | BIT 1 | BIT 0 |
| | CY | AC | F0 | RS1 | RS0 | OV | F1 | P |
| Access | r/w | r/w | r/w | r/w | r/w | r/w | r/w | r/w |
| At Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

This register contains status information resulting from CPU and ALU operation. The bit definitions are given below:

| | |
|---|---|
| BIT7: CY | ALU carry flag. |
| BIT6: AC | ALU auxiliary carry flag. |
| BIT5: F0 | General purpose user-definable flag. |
| BIT4: RS1 | Register Bank Select bit 1. |
| BIT3: RS0 | Register Bank Select bit 0. |
| BIT2: OV | ALU overflow flag. |
| BIT1: F1 | User-definable flag. |
| BIT0: P | Parity flag. Set each instruction cycle to indicate odd/even parity in the accumulator. |

The Register Bank Select bits operate as follows.

| RS1 | RS0 | Register Bank Select |
|---|---|---|
| 0 | 0 | RB0: Registers from 00 - 07 hex. |
| 0 | 1 | RB1: Registers from 08 - 0F hex. |
| 1 | 0 | RB2: Registers from 10 - 17 hex. |
| 1 | 1 | RB3: Registers from 18 - 1F hex. |


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### 7.2.15 Accumulator (ACC)

This register provides one of the operands for most ALU operations. It is denoted as "A" in the instruction table.

| Accumulator (ACC) | | | | Bit Addressable | | | | |
|---|---|---|---|---|---|---|---|---|
| SFR: | 0xE0 | ACC | | | | | | |
| | BIT 7 | BIT 6 | BIT 5 | BIT 4 | BIT 3 | BIT 2 | BIT 1 | BIT 0 |
| | ACC<7> | ACC<6> | ACC<5> | ACC<4> | ACC<3> | ACC<2> | ACC<1> | ACC<0> |
| Access | r/w | r/w | r/w | r/w | r/w | r/w | r/w | r/w |
| At Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

### 7.2.16 Register (B)

This register provides the second operand for multiply or divide instructions. Otherwise, it may be used as a scratch pad register.

| B Register (B) | | | | Bit Addressable | | | | |
|---|---|---|---|---|---|---|---|---|
| SFR: | 0xF0 | B | | | | | | |
| | BIT 7 | BIT 6 | BIT 5 | BIT 4 | BIT 3 | BIT 2 | BIT 1 | BIT 0 |
| | B<7> | B<6> | B<5> | B<4> | B<3> | B<2> | B<1> | B<0> |
| Access | r/w | r/w | r/w | r/w | r/w | r/w | r/w | r/w |
| At Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

## 7.3 ESFR

The ESFRs are External Special Function Registers that are external to the 8051W core and are specific to PGA400-Q1.

| ADDRESS (hex) | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | R/W | POWER UP | DESCRIPTION (PROGRAMMABLE REGS) |
|---|---|---|---|---|---|---|---|---|---|---|---|
| 91 | PSMON[7] | PSMON[6] | PSMON[5] | PSMON[4] | PSMON[3] | PSMON[2] | PSMON[1] | PSMON[0] | R/W | 0x00 | PSMON1 |
| 92 | PSMON[15] | PSMON[14] | PSMON[13] | PSMON[12] | PSMON[11] | PSMON[10] | PSMON[9] | PSMON[8] | R/W | 0x00 | PSMON2 |
| 93 | AFEDIAG[7] | AFEDIAG[6] | AFEDIAG[5] | AFEDIAG[4] | AFEDIAG[3] | AFEDIAG[2] | AFEDIAG[1] | AFEDIAG[0] | R/W | 0x00 | AFEDIAG |
| 94 | - | - | - | - | - | - | - | CPU_WD_RESET | R/W | 0xx0 | CLKDIAG |
| A1 | S1_G1[2] | S1_G1[1] | S1_G1[0] | S1_G2[4] | S1_G2[3] | S1_G2[2] | S1_G2[1] | S1_G2[0] | R/W | 0xx0 | SEN1GAIN |
| A2 | S2_G1[2] | S2_G1[1] | S2_G1[0] | S2_G1[4] | S2_G1[3] | S2_G1[2] | S2_G1[1] | S2_G1[0] | R/W | 0x00 | SEN2GAIN |
| A3 | S1_OS [7] | S1_OS [6] | S1_OS [5] | S1_OS [4] | S1_OS [3] | S1_OS [2] | S1_OS [1] | S1_OS [0] | R/W | 0x00 | SEN1OFF1 |
| A4 | S1_OS[9] | S1_OS[8] | S1_OS[5] | S1_OS[4] | S1_OS[3] | S1_OS[2] | S1_OS[1] | S1_OS[0] | R/W | 0x00 | SEN1OFF2 |
| A5 | S2_OS [7] | S2_OS [6] | S2_OS [5] | S2_OS [4] | S2_OS [3] | S2_OS [2] | S2_OS [1] | S2_OS [0] | R/W | 0x00 | SEN2OFF1 |
| A6 | S2_OS[9] | S2_OS[8] | S2_OS[5] | S2_OS[4] | S2_OS[3] | S2_OS[2] | S2_OS[1] | S2_OS[0] | R/W | 0x00 | SEN2OFF2 |
| A7 | SEN_TYP | CI[2] | CI[1] | CI[0] | CV[1] | CV[0] | CR[1] | CR[0] | R/W | 0x00 | CAPSEN |
| A9 | SEN_CHNL | S1_INV | S2_INV | ADC_BUF | TEMP_SEN | XTAL_EN | VBRG_EN | – | R/W | 0x00 | SENCTRL |
| AA | ST_TX | - | ST_GPO5 | ST_GPO4 | ST_GPO3 | ST_GPO2 | ST_GPO1 | – | R/W | 0x00 | GPIO_STRG |
| AB | CLKCNT[7] | CLKCNT[6] | CLKCNT[5] | CLKCNT[4] | CLKCNT[3] | CLKCNT[2] | CLKCNT[1] | CLKCNT[0] | R/W | 0x00 | CTOV_VLK_CNT |
| B1 | ADC[15] | ADC[14] | ADC[13] | ADC[12] | ADC[11] | ADC[10] | ADC[9] | ADC[8] | R/W | 0x00 | ADCMSB |
| B2 | ADC[7] | ADC[6] | ADC[5] | ADC[4] | ADC[3] | ADC[2] | ADC[1] | ADC[0] | R/W | 0x00 | SDCLSB |
| B3 | – | – | – | – | – | LD_SADC1 | LD_SADC2 | LD_TADC | R/W | 0x00 | LD_DEC |
| B7 | – | – | – | DAC1[11] | DAC1[10] | DAC1[9] | DAC1[8] | PX0 | R/W | 0x00 | DAC1MSB |
| B9 | DAC1[7] | DAC1[6] | DAC1[5] | DAC1[4] | DAC1[3] | DAC1[2] | DAC1[1] | DAC1[0] | R/W | 0x00 | DAC1LSB |
| BA | – | – | – | – | DAC2[11] | DAC2[10] | DAC2[9] | DAC2[8] | R/W | 0x00 | DAC2MSB |
| BB | DAC2[7] | DAC2[6] | DAC2[5] | DAC2[4] | DAC2[3] | DAC2[2] | DAC2[1] | DAC2[0] | R/W | 0x00 | DAC2LSB |
| BC | – | – | DAC2_EN | AFE_EN | – | – | OSR[1] | OSR[0] | R/W | 0x00 | DECCTRL |
| C0 | – | – | IC_OC_TIM_LAT | OC2_LVL | OC1_LVL | IC2_EDGE | IC1_EDGE | 10_20_MHZ | R/W | 0x00 | IC_OC_CTRL |
| C1 | IC1[15] | IC1[14] | IC1[13] | IC1[12] | IC1[11] | IC1[10] | IC1[9] | IC1[8] | R/W | 0x00 | IC1MSB |
| C2 | IC1[7] | IC1[6] | IC1[5] | IC1[4] | IC1[3] | IC1[2] | IC1[1] | IC1[0] | R/W | 0x00 | IC1LSB |
| C3 | IC2[15] | IC2[14] | IC2[13] | IC2[12] | IC2[11] | IC2[10] | IC2[9] | IC2[8] | R/W | 0x00 | IC2MSB |
| C4 | IC2[7] | IC2[6] | IC2[5] | IC2[4] | IC2[3] | IC2[2] | IC2[1] | IC2[0] | R/W | 0x00 | IC2lSB |
| C5 | OC1[15] | OC1[14] | OC1[13] | OC1[12] | OC1[11] | OC1[10] | OC1[9] | OC1[8] | R/W | 0x00 | OC1MSB |
| C6 | OC1[7] | OC1[6] | OC1[5] | OC1[4] | OC1[3] | OC1[2] | OC1[1] | OC1[0] | R/W | 0x00 | OC1LSB |
| C7 | – | – | – | – | OC2_ACT | OC1_ACT | IC2_ACT | IC1_ACT | R/W | 0x00 | IC_OC_GPIO |
| C9 | OC2[15] | OC2[14] | OC2[13] | OC2[12] | OC2[11] | OC2[10] | OC2[9] | OC2[8] | R/W | 0x00 | OC2MSB |
| CA | OC2[7] | OC2[6] | OC2[5] | OC2[4] | OC2[3] | OC2[2] | OC2[1] | OC2[0] | R/W | 0x00 | OC2LSB |


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| ADDRESS (hex) | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | R/W | POWER UP | DESCRIPTION (PROGRAMMABLE REGS) |
|---|---|---|---|---|---|---|---|---|---|---|---|
| CB | FRT[15] | FRT[14] | FRT[13] | FRT[12] | FRT[11] | FRT[10] | FRT[9] | FRT[8] | R/W | 0x00 | FRTMSB |
| CC | FRT[7] | FRT[6] | FRT[5] | FRT[4] | FRT[3] | FRT[2] | FRT[1] | FRT[0] | R/W | 0x00 | FRTLSB |
| D3 | COMBUF[7] | COMBUF[6] | COMBUF[5] | COMBUF[4] | COMBUF[3] | COMBUF[2] | COMBUF[1] | COMBUF[0] | R/W | 0x00 | COMBUF |
| D4 | – | – | – | – | OWI_DEGLITCH_SEL | OWI_XCR_EN | DI_CTRL[1] | DI_CTRL[0] | R/W | 0x00 | DI_CTRL |
| D5 | – | – | – | INT_CAPS_EN | LB_EN | CTOV_CLK_MON_EN | MAIN_OSC_WD_EN | CPU_WD_EN | R/W | 0x00 | EN_CTRL |
| D6 | | | | | | EN_IRAM_MBIST | EN_DI_IF_CLK | EN_EEPROM_CTRL_CLK | R/W | 0x00 | EN_CTRL2 |
| D7 | - | - | - | - | - | - | IRAM_MBIST_FAIL | IRAM_MBIST_DONE | R/W | 0x00 | RAM_MBIST_ST |
| E1 | TRIM_ERR | CRC_ERR | EEPROG_GOOD | EE_READ_IN_PROG | EE_PROG_IN_PROG | EE_BNK[2] | EE_BNK[1] | EE_BNK[0] | R/W | 0x00 | EE_STATUS |
| E2 | – | – | – | – | – | – | - | MICRO_EEPROG | R/W | 0x00 | EE_CTRL |

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### 7.3.1 PSMON Diagnostics Status (PSMON1, PSMON2)

| PSMON STATUS (PSMON1, PSMON2) | | | | Not Bit Addressable | | | | |
|---|---|---|---|---|---|---|---|---|
| ESFR: | 0x91 | PSMON1 | | | | | | |
| | BIT 7 | BIT 6 | BIT 5 | BIT 4 | BIT 3 | BIT 2 | BIT 1 | BIT 0 |
| | PSMON[7] | PSMON[6] | PSMON[5] | PSMON[4] | PSMON[3] | PSMON[2] | PSMON[1] | PSMON[0] |
| Access | r | r | r | r | r | r | r | r |
| At Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| ESFR: | 0x92 | PSMON2 | | | | | | |
| | BIT 7 | BIT 6 | BIT 5 | BIT 4 | BIT 3 | BIT 2 | BIT 1 | BIT 0 |
| | PSMON[15] | PSMON[14] | PSMON[13] | PSMON[12] | PSMON[11] | PSMON[10] | PSMON[9] | PSMON[8] |
| Access | r | r | r | r | r | r | r | r |
| At Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| Bit Definitions | | |
|---|---|---|
| PSMON2 | BIT 0:PSMON[0] | 1: AVDD Overvoltage |
| | BIT 1:PSMON[1] | 1: AVDD Undervoltage |
| | BIT 2:PSMON[2] | - |
| | BIT 3:PSMON[3] | - |
| | BIT 4:PSMON[4] | 1: VBRG Overvoltage |
| | BIT 5:PSMON[5] | 1: VBRG Undervoltage |
| | BIT 6:PSMON[6] | - |
| | BIT 7:PSMON[7] | - |
| PSMON1 | BIT 0:PSMON[8] | 1: EEPROG Overvotlage |
| | BIT 1:PSMON[9] | 1: EEPROG Undervoltage |
| | BIT 2:PSMON[10] | - |
| | BIT 3:PSMON[11] | - |
| | BIT 4:PSMON[12] | - |
| | BIT 5:PSMON[13] | - |
| | BIT 6:PSMON[14] | - |
| | BIT 7:PSMON[15] | - |


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### 7.3.2 AFE Diagnostics Status (AFEDIAG)

| AFE STATUS (AFEDIAG) | | | | Not Bit Addressable | | | | |
|---|---|---|---|---|---|---|---|---|
| ESFR: | 0x93 | AFEDIAG | | | | | | |
| | BIT 7 | BIT 6 | BIT 5 | BIT 4 | BIT 3 | BIT 2 | BIT 1 | BIT 0 |
| | AFEDIAG[7] | AFEDIAG[6] | AFEDIAG[5] | AFEDIAG[4] | AFEDIAG[3] | AFEDIAG[2] | AFEDIAG[1] | AFEDIAG[0] |
| Access | | r | r | r | r | r | r | r |
| At | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| Bit Definitions | | |
|---|---|---|
| PSMON2 | BIT 0:AFEDIAG[0] | 1: Res Sensor Open / Short to Supply/ Short to Gnd<br>0: Normal |
| | BIT 1:AFEDIAG[1] | 1: AFE Stage1 Output / C2V Output Over Range Flag<br>0: Normal |
| | BIT 2:AFEDIAG[2] | 1: AFE Stage2 Output Over Range Flag<br>0: Normal |
| | BIT 3:AFEDIAG[3] | 1: Normal<br>0: ADC Input Over Range Flag |
| | BIT 4:AFEDIAG[4] | - |
| | BIT 5:AFEDIAG[5] | - |
| | BIT 6:AFEDIAG[6] | - |
| | BIT 7:AFEDIAG[7] | 1: Capacitive Sensor Clock High/Low flag (Sensor fault Detection)<br>0: Normal |

### 7.3.3 CPU Watchdog (CLKDIAG)

| MICRO RESET (MICRORESET) | | | | Not Bit Addressable | | | | |
|---|---|---|---|---|---|---|---|---|
| ESFR: | 0x94 | MICRORESET | | | | | | |
| | BIT 7 | BIT 6 | BIT 5 | BIT 4 | BIT 3 | BIT 2 | BIT 1 | BIT 0 |
| | - | - | - | - | - | - | - | CPU_WD_RESET |
| Access | | R | r | r | r | r | r | r |
| At | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Reset | | | | | | | | |

| Bit Definitions | | |
|---|---|---|
| CLKDIAG | BIT 0:CPU_WD_RESET | 1: Microprocessor is in reset<br>0: Microprocessor is not reset |
| | BIT 1: | - |
| | BIT 2: | - |
| | BIT 3: | - |
| | BIT 4: | - |
| | BIT 5: | - |
| | BIT 6: | - |
| | BIT 7: | |

### 7.3.4 Sensor 1 Gain Register (SEN1GAIN)

| SEN1GAIN | | | | Not Bit Addressable | | | | |
|---|---|---|---|---|---|---|---|---|
| ESFR: | 0xA1 | SEN1GAIN | | | | | | |
| | BIT 7 | BIT 6 | BIT 5 | BIT 4 | BIT 3 | BIT 2 | BIT 1 | BIT 0 |
| | S1_G1[2] | S1_G1[1] | S1_G1[0] | S1_G2[4] | S1_G2[3] | S1_G2[2] | S1_G2[1] | S1_G2[0] |
| Access | r/w | r/w | r/w | r/w | r/w | r/w | r/w | r/w |
| At Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| Bit Definitions | | | |
|---|---|---|---|
| SENS1GAIN | BIT 0: S1_G2[0] | **S1_G2[4:0}** | **Sensor 1 Stage 2 Gain (V/V)** |
| | BIT 1: S1_G2[1] | 00000 | 1.00 |
| | BIT 2: S1_G2[2] | 00001 | 1.10 |
| | BIT 3: S1_G2[3]] | 00010 | 1.22 |
| | BIT 4: S1_G2[4]] | 00011 | 1.35 |
| | | 00100 | 1.50 |
| | | 00101 | 1.67 |
| | | 00110 | 1.85 |
| | | 00111 | 2.05 |
| | | 01000 | 2.28 |
| | | 01001 | 2.53 |
| | | 01010 | 2.81 |
| | | 01011 | 3.11 |
| | | 01100 | 3.46 |
| | | 01101 | 3.86 |
| | | 01110 | 4.26 |
| | | 01111 | 4.76 |
| | | 10000 | 5.26 |
| | | 10001 | 5.86 |
| | | 10010 | 6.46 |
| | | 10011 | 7.16 |
| | | 10100 | 7.96 |
| | | 10101 | 8.86 |
| | | 10110 | 9.86 |
| | | 10111 | 10.96 |
| | | 11000 | 12.16 |
| | | 11001 | 13.46 |
| | | 11010 | 14.96 |
| | | 11011 | 16.56 |
| | | 11100 | 18.36 |
| | | 11101 | 20.46 |
| | | 11110 | 22.56 |
| | | 11111 | 25.06 |
| | BIT 5: S1_G1[0]] | **S1_G1[2:0}** | **Sensor 1 Stage 1 Gain (V/V)** |
| | BIT 6: S1_G1[1] | 000 | 3.00 |
| | BIT 7: S1_G1[2] | 001 | 4.43 |
| | | 010 | 6.80 |
| | | 011 | 10.20 |
| | | 100 | 14.57 |
| | | 101 | 25.50 |


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### 7.3.5 Sensor 2 Gain Register (SEN2GAIN)

| SENS1GAIN | | | | Not Bit Addressable | | | | |
|---|---|---|---|---|---|---|---|---|
| ESFR: | 0xA2 | SEN2GAIN | | | | | | |
| | BIT 7 | BIT 6 | BIT 5 | BIT 4 | BIT 3 | BIT 2 | BIT 1 | BIT 0 |
| | S2_G1[2] | S2_G1[1] | S2_G1[0] | S2_G1[4] | S2_G1[3] | S2_G1[2] | S2_G1[1] | S2_G1[0] |
| Access | r/w | r/w | r/w | r/w | r/w | r/w | r/w | r/w |
| At | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Reset | | | | | | | | |

| Bit Definitions | | | |
|---|---|---|---|
| SENS1GAIN | BIT 0: S2_G2[0] | **S2_G2[4:0}** | **Sensor 2 Stage 2 Gain (V/V)** |
| | BIT 1: S2_G2[1] | 00000 | 1.00 |
| | BIT 2: S2_G2[2] | 00001 | 1.10 |
| | BIT 3: S2_G2[3]] | 00010 | 1.22 |
| | BIT 4: S2_G2[4]] | 00011 | 1.35 |
| | | 00100 | 1.50 |
| | | 00101 | 1.67 |
| | | 00110 | 1.85 |
| | | 00111 | 2.05 |
| | | 01000 | 2.28 |
| | | 01001 | 2.53 |
| | | 01010 | 2.81 |
| | | 01011 | 3.11 |
| | | 01100 | 3.46 |
| | | 01101 | 3.86 |
| | | 01110 | 4.26 |
| | | 01111 | 4.76 |
| | | 10000 | 5.26 |
| | | 10001 | 5.86 |
| | | 10010 | 6.46 |
| | | 10011 | 7.16 |
| | | 10100 | 7.96 |
| | | 10101 | 8.86 |
| | | 10110 | 9.86 |
| | | 10111 | 10.96 |
| | | 11000 | 12.16 |
| | | 11001 | 13.46 |
| | | 11010 | 14.96 |
| | | 11011 | 16.56 |
| | | 11100 | 18.36 |
| | | 11101 | 20.46 |
| | | 11110 | 22.56 |
| | | 11111 | 25.06 |
| | BIT 5: S2_G1[0]] | **S2_G1[2:0}** | **Sensor 2 Stage 1 Gain (V/V)** |
| | BIT 6: S2_G1[1] | 000 | 3.00 |
| | BIT 7: S2_G1[2] | 001 | 4.43 |
| | | 010 | 6.80 |
| | | 011 | 10.20 |
| | | 100 | 14.57 |
| | | 101 | 25.50 |

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### 7.3.6 Sensor 1 Offset Register (SEN1OFF1, SEN1OFF2)

| SENSOR 1 OFFSET (SEN1OFF1, SEN1OFF2) | | | | Not Bit Addressable | | | | |
|---|---|---|---|---|---|---|---|---|
| ESFR: | 0xA3 | SEN1OFF1 | | | | | | |
| | BIT 7 | BIT 6 | BIT 5 | BIT 4 | BIT 3 | BIT 2 | BIT 1 | BIT 0 |
| | S1_OS [7] | S1_OS [6] | S1_OS [5] | S1_OS [4] | S1_OS [3] | S1_OS [2] | S1_OS [1] | S1_OS [0] |
| Access | r/w | r/w | r/w | r/w | r/w | r/w | r/w | r/w |
| At Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| ESFR: | 0xA4 | SEN1OFF2 | | | | | | |
| | BIT 7 | BIT 6 | BIT 5 | BIT 4 | BIT 3 | BIT 2 | BIT 1 | BIT 0 |
| | S1_OS[9] | S1_OS[8] | S1_OS[5] | S1_OS[4] | S1_OS[3] | S1_OS[2] | S1_OS[1] | S1_OS[0] |
| Access | r/w | r/w | r/w | r/w | r/w | r/w | r/w | r/w |
| At Reset | 1 | 0 | 1 | 0 | 0 | 0 | 0 | 0 |


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| Bit Definitions | | |
|---|---|---|
| SEN1OFF1 | BIT 0:S1_OS[0] | S1_OS: Sensor 1 Offset Compensation Setting |
| | BIT 1:S1_OS[1] | |
| | BIT 2:S1_OS[2] | |
| | BIT 3:S1_OS[3] | |
| | BIT 4:S1_OS[4] | |
| | BIT 5:S1_OS[5] | |
| | BIT 6:S1_OS[6] | |
| | BIT 7:S1_OS[7] | |
| SEN1OFF2 | BIT 0:S1_TC[0] | S1_TC: Sensor 1 Offset TC Compensation Setting |
| | BIT 1:S1_TC[1] | |
| | BIT 2:S1_TC[2] | |
| | BIT 3:S1_TC[3] | |
| | BIT 4:S1_TC[4] | |
| | BIT 5:S1_TC[5] | |
| | BIT 6:S1_OS[8] | |
| | BIT 7:S1_OS[9] | |

### 7.3.7 Sensor 2 Offset Register(SEN2OFF1, SEN2OFF2)

| SENSOR 1 OFFSET (SEN1OFF1, SEN1OFF2) | | | | Not Bit Addressable | | | | |
|---|---|---|---|---|---|---|---|---|
| ESFR: | 0xA5 | SEN1OFF1 | | | | | | |
| | BIT 7 | BIT 6 | BIT 5 | BIT 4 | BIT 3 | BIT 2 | BIT 1 | BIT 0 |
| | S2_OS [7] | S2_OS [6] | S2_OS [5] | S2_OS [4] | S2_OS [3] | S2_OS [2] | S2_OS [1] | S2_OS [0] |
| Access | r/w | r/w | r/w | r/w | r/w | r/w | r/w | r/w |
| At Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| ESFR: | 0xA6 | SEN1OFF2 | | | | | | |
| | BIT 7 | BIT 6 | BIT 5 | BIT 4 | BIT 3 | BIT 2 | BIT 1 | BIT 0 |
| | S2_OS[9] | S2_OS[8] | S2_OS[5] | S2_OS[4] | S2_OS[3] | S2_OS[2] | S2_OS[1] | S2_OS[0] |
| Access | r/w | r/w | r/w | r/w | r/w | r/w | r/w | r/w |
| At Reset | 1 | 0 | 1 | 0 | 0 | 0 | 0 | 0 |

| Bit Definitions | | |
|---|---|---|
| SEN1OFF1 | BIT 0:S2_OS[0] | S1_OS: Sensor 2 Offset Compensation Setting |
| | BIT 1:S2_OS[1] | |
| | BIT 2:S2_OS[2] | |
| | BIT 3:S2_OS[3] | |
| | BIT 4:S2_OS[4] | |
| | BIT 5:S2_OS[5] | |
| | BIT 6:S2_OS[6] | |
| | BIT 7:S2_OS[7] | |
| SEN1OFF2 | BIT 0:S2_TC[0] | S1_TC: Sensor 2 Offset TC Compensation Setting |
| | BIT 1:S2_TC[1] | |
| | BIT 2:S2_TC[2] | |
| | BIT 3:S2_TC[3] | |
| | BIT 4:S2_TC[4] | |
| | BIT 5:S2_TC[5] | |
| | BIT 6:S2_OS[8] | |
| | BIT 7:S2_OS[9] | |


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### 7.3.8 Capacitive Sensor Settings Register (CAPSEN)

| CAPACITIVE SENSOR REGISTER (CAPSEN) | | | | | Not Bit Addressable | | | | |
|---|---|---|---|---|---|---|---|---|---|
| ESFR: | 0xA7 | | CAPSEN | | | | | | |
| | | BIT 7 | BIT 6 | BIT 5 | BIT 4 | BIT 3 | BIT 2 | BIT 1 | BIT 0 |
| | | SEN_TYP | CI[2] | CI[1] | CI[0] | CV[1] | CV[0] | CR[1] | CR[0] |
| Access | | r/w | r/w | r/w | r/w | r/w | r/w | r/w | r/w |
| At Reset | | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| Bit Definitions | | | | | |
|---|---|---|---|---|---|
| CAPSEN | BIT 0:CR[0] | **CR[1]** | | **CR[0]** | **Capacitive Sensor Transimpedance (KΩ)** |
| | BIT 1:CR[1] | 0 | | 0 | 78 |
| | | 0 | | 1 | 156 |
| | | 1 | | 0 | 312 |
| | | 1 | | 1 | 625 |
| | BIT 2:CV[0] | **CV[1]** | | **CV[0]** | **Capacitive Sensor Drive Threshold Voltage (mV)** |
| | BIT 3:CV[1] | 0 | | 0 | 100 |
| | | 0 | | 1 | 300 |
| | | 1 | | 0 | 500 |
| | | 1 | | 1 | 700 |
| | BIT 4:CI[0] | **CI[2]** | **CI[1]** | **CI[0]** | **Capacitive Sensor Drive Current (µA)** |
| | BIT 5:CI[1] | 0 | 0 | 0 | 5 |
| | BIT 6:CI[2] | 0 | 0 | 1 | 7.5 |
| | | 0 | 1 | 0 | 10 |
| | | 0 | 1 | 1 | 12.5 |
| | | 1 | 0 | 0 | 15 |
| | | 1 | 0 | 1 | 17.5 |
| | | 1 | 1 | 0 | 20 |
| | | 1 | 1 | 1 | 22 |
| | BIT 7:SEN_TYP | 0: Capacitive Front End<br>1: Resistive Bridge Front End | | | |

### 7.3.9 Sensor Control (SENCTRL)

| SENSOR CONTROL (SENCTRL) | | | | | Not Bit Addressable | | | | |
|---|---|---|---|---|---|---|---|---|---|
| ESFR: | 0xA9 | | SENCTRL | | | | | | |
| | | BIT 7 | BIT 6 | BIT 5 | BIT 4 | BIT 3 | BIT 2 | BIT 1 | BIT 0 |
| | | SEN_CHNL | S1_INV | S2_INV | ADC_BUF | TEMP_SEN | XTAL_EN | VBRG_EN | – |
| Access | | | r/w | r/w | r/w | r/w | r/w | r/w | r/w |
| At | | 0 | 0 | 0 | 1 | 0 | 0 | 1 | 0 |

| | | |
|---|---|---|
| Bit Definitions | | |
| SENCTRL | BIT 0: | |
| | BIT 1: VBRG_EN | VBRG Enable<br>0: Disabled<br>1: Enabled |
| | BIT 2: XTAL_EN | 0: Internal Oscillator<br>1: External Crystal |
| | BIT 3: TEMP_SEN | 0: Internal Temperature Sensor<br>1: External Temperature Sensor |
| | BIT 4: ADC_BUF | 0: ADC Buffer Output is not level-shifted<br>1: ADC Buffer Output is level-shifted |
| | BIT 5: S2_INV | S2 Sign Bit<br>1: S2 signal chain is inverted<br>0: S2 signal chain is not inverted |
| | BIT 6: S1_INV | S1 Sign Bit<br>1: S1 signal chain is inverted<br>0: S1 signal chain is not inverted |
| | BIT 7: SEN_CHNL | 0: S1 Channel<br>1: S2 Channel |

### 7.3.10 GPIO Strong Output Drive Mode (GPIO_STRG)

| GPIO Strong Output Drive Mode (GPIO_STRG) | | | | Not Bit Addressable | | | | |
|---|---|---|---|---|---|---|---|---|
| ESFR: | 0xAA | GPIO_STRG | | | | | | |
| | BIT 7 | BIT 6 | BIT 5 | BIT 4 | BIT 3 | BIT 2 | BIT 1 | BIT 0 |
| | ST_TX | - | ST_GPO5 | ST_GPO4 | ST_GPO3 | ST_GPO2 | ST_GPO1 | – |
| Access | r/w | r/w | r/w | r/w | r/w | r/w | r/w | r/w |
| At Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| | | |
|---|---|---|
| Bit Definitions | | |
| SENCTRL | BIT 0: | - |
| | BIT 1: ST_GPO1 | 0: Normal 8051W Mode<br>1: Strong Output Mode |
| | BIT 2: ST_GPO2 | 0: Normal 8051W Mode<br>1: Strong Output Mode |
| | BIT 3: ST_GPO3 | 0: Normal 8051W Mode<br>1: Strong Output Mode |
| | BIT 4: ST_GPO4 | 0: Normal 8051W Mode<br>1: Strong Output Mode |
| | BIT 5: ST_GPO5 | 0: Normal 8051W Mode<br>1: Strong Output Mode |
| | BIT 6: - | - |
| | BIT 6: ST_TX | 0: Normal 8051W Mode |
| | | 1: Strong Output Mode |


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### 7.3.11 CTOV clock Count Register (CTOV_CLK_CNT)

| CLOCK COUNT REGISTER (CTOV_CLK_CNT) | | | | Not Bit Addressable | | | | |
|---|---|---|---|---|---|---|---|---|
| ESFR: | 0xAB | CTOV_CLK_CNT | | | | | | |
| | BIT 7 | BIT 6 | BIT 5 | BIT 4 | BIT 3 | BIT 2 | BIT 1 | BIT 0 |
| | CLKCNT[7] | CLKCNT[6] | CLKCNT[5] | CLKCNT[4] | CLKCNT[3] | CLKCNT[2] | CLKCNT[1] | CLKCNT[0] |
| Access | r/w | r/w | r/w | r/w | r/w | r/w | r/w | r/w |
| At Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

The clock count register has a resolution of 10MHz.

### 7.3.12 ADC Decimator Output (ADCMSB, ADCLSB)

| ADC Decimator Output | | | | Not Bit Addressable | | | | |
|---|---|---|---|---|---|---|---|---|
| ESFR: | 0xB1 | ADCMSB | | | | | | |
| | BIT 7 | BIT 6 | BIT 5 | BIT 4 | BIT 3 | BIT 2 | BIT 1 | BIT 0 |
| | ADC[15] | ADC[14] | ADC[13] | ADC[12] | ADC[11] | ADC[10] | ADC[9] | ADC[8] |
| Access | r | r | r | r | r | r | r | r |
| At Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| ESFR: | 0xB2 | ADCLSB | | | | | | |
| | BIT 7 | BIT 6 | BIT 5 | BIT 4 | BIT 3 | BIT 2 | BIT 1 | BIT 0 |
| | ADC[7] | ADC[6] | ADC[5] | ADC[4] | ADC[3] | ADC[2] | ADC[1] | ADC[0] |
| Access | r/w | r/w | r/w | r/w | r/w | r/w | r/w | r/w |
| At Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

### 7.3.13 Load ADC Decimator Shadow Register (LD_DEC)

| LOAD DECIMATOR SHADOW REGISTER (LD_DEC) | | | | Not Bit Addressable | | | | |
|---|---|---|---|---|---|---|---|---|
| ESFR: | 0xB3 | LD_DEC | | | | | | |
| | BIT 7 | BIT 6 | BIT 5 | BIT 4 | BIT 3 | BIT 2 | BIT 1 | BIT 0 |
| | – | – | – | – | – | LD_SADC1 | LD_SADC2 | LD_TADC |
| Access | – | – | – | – | – | w | w | w |
| At Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| Bit Definitions | | |
|---|---|---|
| SENCTRL | BIT 0: LD_TADC | 0: No Action<br>1: Load the output of the Temperature Decimator to ADC Decimator Output Register |
| | BIT 1: LD_SADC2 | 0: No Action<br>1: Load the output of the Stage 2 Decimator to ADC Decimator Output Register |
| | BIT 2: LD_SADC1 | 0: No Action<br>1: Load the output of the Stage 1 Decimator to ADC Decimator Output Register |
| | BIT 3: – | – |
| | BIT 4: – | – |
| | BIT 5: – | – |
| | BIT 6: – | – |
| | BIT 7: – | – |

### 7.3.14 DAC 1 Register (DAC1MSB, DAC1LSB)

| DAC1 Register (DAC1MSB, DAC1LSB) | | | | Not Bit Addressable | | | | |
|---|---|---|---|---|---|---|---|---|
| ESFR: | 0xB7 | DAC1MSB | | | | | | |
| | BIT 7 | BIT 6 | BIT 5 | BIT 4 | BIT 3 | BIT 2 | BIT 1 | BIT 0 |
| | – | – | – | – | DAC1[11] | DAC1[10] | DAC1[9] | DAC1[8] |
| Access | r/w | r/w | r/w | r/w | r/w | r/w | w | R |
| At Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| ESFR: | 0xB9 | DAC1LSB | | | | | | |
| | BIT 7 | BIT 6 | BIT 5 | BIT 4 | BIT 3 | BIT 2 | BIT 1 | BIT 0 |
| | DAC1[7] | DAC1[6] | DAC1[5] | DAC1[4] | DAC1[3] | DAC1[2] | DAC1[1] | DAC1[0] |
| Access | r/w | r/w | r/w | r/w | r/w | r/w | w | R |
| At Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

### 7.3.15 DAC 2 Register (DAC2MSB, DAC2LSB)

| DAC2 (DAC2MSB, DAC2LSB) | | | | Not Bit Addressable | | | | |
|---|---|---|---|---|---|---|---|---|
| ESFR: | 0xBA | DAC2MSB | | | | | | |
| | BIT 7 | BIT 6 | BIT 5 | BIT 4 | BIT 3 | BIT 2 | BIT 1 | BIT 0 |
| | – | – | – | – | DAC2[11] | DAC2[10] | DAC2[9] | DAC2[8] |
| Access | r/w | r/w | r/w | r/w | r/w | r/w | w | r/w |
| At Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| ESFR: | 0xBB | DAC2LSB | | | | | | |
| | BIT 7 | BIT 6 | BIT 5 | BIT 4 | BIT 3 | BIT 2 | BIT 1 | BIT 0 |
| | DAC2[7] | DAC2[6] | DAC2[5] | DAC2[4] | DAC2[3] | DAC2[2] | DAC2[1] | DAC2[0] |
| Access | r/w | r/w | r/w | r/w | r/w | r/w | r/w | r/w |
| At Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

### 7.3.16 Decimator and Low Power Control Register (DECCTRL)

| DECIMATOR CONTROL (DECCTRL) | | | | Not Bit Addressable | | | | |
|---|---|---|---|---|---|---|---|---|
| ESFR: | 0xBC | DECCTRL | | | | | | |
| | BIT 7 | BIT 6 | BIT 5 | BIT 4 | BIT 3 | BIT 2 | BIT 1 | BIT 0 |
| | DIS_R1M | DIS_R2M | DAC2_EN | AFE_EN | – | – | OSR[1] | OSR[0] |
| Access | r | r | r/w | r/w | r | r | r/w | r/w |
| At | 0 | 0 | 1 | 1 | 0 | 0 | 0 | 0 |


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| Bit Definitions | | |
|---|---|---|
| DECCTRL | BIT 0:OSR[0] | 2nd Stage Decimator OSR Control |
| | BIT 1:OSR[1] | 00: 2<br>01: 4<br>10: 8<br>11:: N/A |
| | BIT 2: - | – |
| | BIT 3: - | – |
| | BIT 4:AFE_EN | 0: AFE is disabled<br>1: AFE is enabled |
| | BIT 5:-DAC2_EN | 0: DAC2 is disabled<br>1: DAC2 is enabled |
| | BIT 6:- | – |
| | BIT 7:- | – |

### 7.3.17 Input Capture/Output Compare Control Register (IC_OC_CTRL)

| IC_OC_CTRL | | | | Not Bit Addressable | | | | |
|---|---|---|---|---|---|---|---|---|
| ESFR: | 0xC0 | IC_OC_CTRL | | | | | | |
| | BIT 7 | BIT 6 | BIT 5 | BIT 4 | BIT 3 | BIT 2 | BIT 1 | BIT 0 |
| | – | – | IC_OC_TIM_LAT | OC2_LVL | OC1_LVL | IC2_EDGE | IC1_EDGE | 10_20_MHZ |
| Access | r/w | r/w | r/w | r/w | r/w | r/w | r/w | r/w |
| At | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| Bit Definitions | | | | |
|---|---|---|---|---|
| | BIT 0:10_20_MHz | 0: Free Running Timer Resolution is 20MHz<br>1: Free Running Timer Resolution is 10MHz | | |
| | BIT 1:IC1_EDGE | 0: Capture Falling Edge on Input Capture 1<br>1: Capture Rising Edge on Input Capture 1 | | |
| | BIT 2:IC2_EDGE | 0: Capture Falling Edge on Input Capture 2<br>1: Capture Rising Edge on Input Capture 2 | | |
| | BIT 3:OC1_LVL | 0: OC_1 is set to 0 upon match<br>1: OC_1 is set to 1 upon match | | |
| | BIT 4:OC2_LVL | 0: OC_2 is set to 0 upon match<br>1: OC_2 is set to 1 upon match | | |
| | BIT 5: IC_OC_TIM_LAT | 0: No Action<br>1: Latches the free-running timer values into the free running timer shadow register | | |
| | BIT 6: DIS_R2M | AFE Pull-Down Resistor Value | | |
| | BIT 7: DIS_R1M | DIS_R1M | DIS_R2M | Pull-down Resistor Value (MΩ) |
| | | 0 | 0 | 4 |
| | | 0 | 1 | 2 |
| | | 1 | 0 | 3 |
| | | 1 | 1 | 1 |

### 7.3.18 Input Capture 1 Register (IC1MSB, IC1LSB)

| INPUT CAPTURE 1 (IC1MSB, IC1LSB) | | | | Not Bit Addressable | | | | |
|---|---|---|---|---|---|---|---|---|
| ESFR: | 0xC1 | IC1MSB | | | | | | |
| | BIT 7 | BIT 6 | BIT 5 | BIT 4 | BIT 3 | BIT 2 | BIT 1 | BIT 0 |
| | IC1[15] | IC1[14] | IC1[13] | IC1[12] | IC1[11] | IC1[10] | IC1[9] | IC1[8] |
| Access | r | r | r | r | r | r | r | r |
| At Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| ESFR: | 0xC2 | IC1LSB | | | | | | |
| | BIT 7 | BIT 6 | BIT 5 | BIT 4 | BIT 3 | BIT 2 | BIT 1 | BIT 0 |
| | IC1[7] | IC1[6] | IC1[5] | IC1[4] | IC1[3] | IC1[2] | IC1[1] | IC1[0] |
| Access | r | r | r | r | r | r | r | r |
| At Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

### 7.3.19 Input Capture 2 Register (IC2MSB, IC2LSB)

| INPUT CAPTURE 1 (IC2MSB, IC2LSB) | | | | Not Bit Addressable | | | | |
|---|---|---|---|---|---|---|---|---|
| ESFR: | 0xC3 | IC2MSB | | | | | | |
| | BIT 7 | BIT 6 | BIT 5 | BIT 4 | BIT 3 | BIT 2 | BIT 1 | BIT 0 |
| | IC2[15] | IC2[14] | IC2[13] | IC2[12] | IC2[11] | IC2[10] | IC2[9] | IC2[8] |
| Access | r | r | r | r | r | r | r | r |
| At Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| ESFR: | 0xC4 | IC2LSB | | | | | | |
| | BIT 7 | BIT 6 | BIT 5 | BIT 4 | BIT 3 | BIT 2 | BIT 1 | BIT 0 |
| | IC2[7] | IC2[6] | IC2[5] | IC2[4] | IC2[3] | IC2[2] | IC2[1] | IC2[0] |
| Access | r | r | r | r | r | r | r | r |
| At Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

### 7.3.20 Output Compare 1 Register (OC1MSB, OC1LSB)

| OUTPUT COMPARE 1 (OC1MSB, OC1LSB) | | | | Not Bit Addressable | | | | |
|---|---|---|---|---|---|---|---|---|
| ESFR: | 0xC5 | OC1MSB | | | | | | |
| | BIT 7 | BIT 6 | BIT 5 | BIT 4 | BIT 3 | BIT 2 | BIT 1 | BIT 0 |
| | OC1[15] | OC1[14] | OC1[13] | OC1[12] | OC1[11] | OC1[10] | OC1[9] | OC1[8] |
| Access | r/w | r/w | r/w | r/w | r/w | r/w | r/w | r/w |
| At Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| ESFR: | 0xC6 | OC1LSB | | | | | | |
| | BIT 7 | BIT 6 | BIT 5 | BIT 4 | BIT 3 | BIT 2 | BIT 1 | BIT 0 |
| | OC1[7] | OC1[6] | OC1[5] | OC1[4] | OC1[3] | OC1[2] | OC1[1] | OC1[0] |
| Access | r/w | r/w | r/w | r/w | r/w | r/w | r/w | r/w |
| At Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |


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### 7.3.21 Input Capture/Output Compare GPIO Register (IC_OC_GPIO)

| IC_OC_GPIO | | | | Not Bit Addressable | | | | |
|---|---|---|---|---|---|---|---|---|
| ESFR: | 0xC7 | IC_OC_GPIO | | | | | | |
| | BIT 7 | BIT 6 | BIT 5 | BIT 4 | BIT 3 | BIT 2 | BIT 1 | BIT 0 |
| | – | – | – | – | OC2_ACT | OC1_ACT | IC2_ACT | IC1_ACT |
| Access | r/w | r/w | r/w | r/w | r/w | r/w | r/w | r/w |
| At | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| Bit Definitions | | |
|---|---|---|
| | BIT 0:IC1_ACT | 0: GPIO_1 is not configured for IC_1<br>1: GPIO_1 is configured for IC_1 |
| | BIT 1:IC2_ACT | 0: GPIO_2 is not configured for IC_2<br>1: GPIO_2 is configured for IC_2 |
| | BIT 2:OC1_ACT | 0: GPIO_3 is not configured for OC_1<br>1: GPIO_3 is configured for OC_1 |
| | BIT 3:OC2_ACT | 0: GPIO_4 is not configured for OC_2<br>1: GPIO_4 is configured for OC_2 |
| | BIT 4:- | – |
| | BIT 5: - | – |
| | BIT 6: - | – |
| | BIT 7:- | – |

### 7.3.22 Output Compare 2 Register (OC2MSB, OC2LSB)

| OUTPUT COMPARE 1 (OC2MSB, OC2LSB) | | | | Not Bit Addressable | | | | |
|---|---|---|---|---|---|---|---|---|
| ESFR: | 0xC9 | OC2MSB | | | | | | |
| | BIT 7 | BIT 6 | BIT 5 | BIT 4 | BIT 3 | BIT 2 | BIT 1 | BIT 0 |
| | OC2[15] | OC2[14] | OC2[13] | OC2[12] | OC2[11] | OC2[10] | OC2[9] | OC2[8] |
| Access | r/w | r/w | r/w | r/w | r/w | r/w | r/w | r/w |
| At Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| ESFR: | 0xCA | OC2LSB | | | | | | |
| | BIT 7 | BIT 6 | BIT 5 | BIT 4 | BIT 3 | BIT 2 | BIT 1 | BIT 0 |
| | OC2[7] | OC2[6] | OC2[5] | OC2[4] | OC2[3] | OC2[2] | OC2[1] | OC2[0] |
| Access | r/w | r/w | r/w | r/w | r/w | r/w | r/w | r/w |
| At Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

### 7.3.23 Free Running Timer Shadow Register (FRTMSB, FRTLSB)

| FREE RUNNING TIMER 1 (FRTMSB, FRTLSB) | | | | Not Bit Addressable | | | | |
|---|---|---|---|---|---|---|---|---|
| ESFR: | 0xCB | FRTMSB | | | | | | |
| | BIT 7 | BIT 6 | BIT 5 | BIT 4 | BIT 3 | BIT 2 | BIT 1 | BIT 0 |
| | FRT[15] | FRT[14] | FRT[13] | FRT[12] | FRT[11] | FRT[10] | FRT[9] | FRT[8] |
| Access | r | r | r | r | r | r | r | r |
| At Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| ESFR: | 0xCC | FRTLSB | | | | | | |
| | BIT 7 | BIT 6 | BIT 5 | BIT 4 | BIT 3 | BIT 2 | BIT 1 | BIT 0 |
| | FRT[7] | FRT[6] | FRT[5] | FRT[4] | FRT[3] | FRT[2] | FRT[1] | FRT[0] |
| Access | r | r | r | r | r | r | r | r |
| At Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

### 7.3.24 Communication Data Buffer (COMBUF)

| COMM DATA BUFFER (COMBUF) | | | | Not Bit Addressable | | | | |
|---|---|---|---|---|---|---|---|---|
| ESFR: | 0xD3 | COMBUF | | | | | | |
| | BIT 7 | BIT 6 | BIT 5 | BIT 4 | BIT 3 | BIT 2 | BIT 1 | BIT 0 |
| | COMBUF[7] | COMBUF[6] | COMBUF[5] | COMBUF[4] | COMBUF[3] | COMBUF[2] | COMBUF[1] | COMBUF[0] |
| Access | r/w | r/w | r/w | r/w | r/w | r/w | r/w | r/w |
| At | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |


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### 7.3.25 Digital Interface Control Register (DI_CTRL)

| DI CONTROL REGISTER (DI_CTRL) | | | | Not Bit Addressable | | | | |
|---|---|---|---|---|---|---|---|---|
| ESFR: | 0xD4 | DI_CTRL | | | | | | |
| | BIT 7 | BIT 6 | BIT 5 | BIT 4 | BIT 3 | BIT 2 | BIT 1 | BIT 0 |
| | – | – | – | – | OWI_DEGLITCH_SEL | OWI_XCR_EN | DI_CTRL[1] | DI_CTRL[0] |
| Access | | R | r | r | r/w | r/w | r/w | r/w |
| At | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| Bit Definitions | | |
|---|---|---|
| | BIT 0:DI_CTRL[0] | 00: SPI/DAC1 are active<br>01: I2C/DAC1 are active |
| | BIT 1: DI_CTRL[1] | 10: OWI is active<br>11: SPI/DAC1 is active |
| | BIT 2:OWI_XCR_EN | 0: Disable OWI Transceiver – DAC1 is connected to VOUT1/OWI<br>1: Enable OWI Transceiver – OWI Transceiver is connected to VOUT1/OWI |
| | BIT 3: OWI_DEGLITCH_SEL | 0: OWI activation deglitch filters are set to 1ms<br>1: OWI activation deglitch filters are set to 10ms |
| | BIT 4: - | – |
| | BIT 5: - | – |
| | BIT 6: - | – |
| | BIT 7:- | – |

### 7.3.26 Enable Control Register (EN_CTRL)

| ENABLE REGISTER (EN_CTRL) | | | | Not Bit Addressable | | | | |
|---|---|---|---|---|---|---|---|---|
| ESFR: | 0xD5 | EN_CTRL | | | | | | |
| | BIT 7 | BIT 6 | BIT 5 | BIT 4 | BIT 3 | BIT 2 | BIT 1 | BIT 0 |
| | - | - | - | INT_CAPS_EN | LB_EN | CTOV_CLK_MON_EN | MAIN_OSC_WD_EN | CPU_WD_EN |
| Access | | r/w | r/w | r/w | r/w | r/w | r/w | r/w |
| At | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| Bit Definitions | | |
|---|---|---|
| | BIT 0:CPU_WD_EN | 0: Software watchdog is disabled<br>1: Software watchdog is enabled |
| | BIT 1: MAIN_OSC_WD_EN | 0: Internal Oscillator watchdog is disabled<br>1: Internal Oscillator watchdog is enabled |
| | BIT 2:CTOV_CLK_MON_EN | 0: Disable Cap Sensor Clock High/Low flag operation<br>1: Enable Cap Sensor Clock High/Low flag operation |
| | BIT 3: LB_EN | 0: DAC loopback is disabled<br>1: DAC Loopback is enabled in both resistive and capacitive modes. The AFE is switched to resistive bridge mode |
| | BIT 4: INT_CAPS_EN | 0: External Sensor Caps are connected to Capacitive AFE<br>1: Internal Test Caps are connected to Capacitive AFE |
| | BIT 5: - | – |
| | BIT 6: - | – |
| | BIT 7:- | – |

### 7.3.27 Enable Control Register (EN_CTRL2)

| ENABLE REGISTER (EN_CTRL2) | | | | Not Bit Addressable | | | | |
|---|---|---|---|---|---|---|---|---|
| ESFR: | 0xD6 | EN_CTRL2 | | | | | | |
| | BIT 7 | BIT 6 | BIT 5 | BIT 4 | BIT 3 | BIT 2 | BIT 1 | BIT 0 |

| | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | - | - | - | - | - | EN_IRAM_MBIST | EN_DI_IF_CLK | EN_EEPROM_CTRL_CLK |
| Access | | r/w | r/w | r/w | r/w | r/w | r/w | r/w |
| At | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| Bit Definitions | | |
|---|---|---|
| | BIT 0: EN_EEPROM_CTRL_CLK | 0: Disable clock to the EEPROM controller. All EEPROM access is disabled<br>1: Enable clock to the EEPROM Controller |
| | BIT 1: EN_DI_IF_CLK | 0: Disable clock to the Digital Interface controller. No digital interface can be used<br>1: Enable clock to the Digital Interface Controller<br>Special note: This bit will automatically be set to '1' if an OWI activation interrupt occurs or if NCS (SPI chip select = '0' for at least 5 10MHz clock cycles. Noise on the NCS pin can cause the unintentional activation of the Digital Interface clock |
| | BIT 2: EN_IRAM_MBIST | 0: Disable IRAM MBIST<br>1: Enable IRAM MBIST. 8051W will not have access to RAM |
| | BIT 3: - | – |
| | BIT 4: - | – |
| | BIT 5: - | – |
| | BIT 6: - | – |
| | BIT 7:- | – |

### 7.3.28 RAM MBIST Status Register (RAM_MBIST_ST)

| ENABLE REGISTER (EN_CTRL2) | | | | Not Bit Addressable | | | | |
|---|---|---|---|---|---|---|---|---|
| ESFR: | 0xD5 | EN_CTRL2 | | | | | | |
| | BIT 7 | BIT 6 | BIT 5 | BIT 4 | BIT 3 | BIT 2 | BIT 1 | BIT 0 |
| | - | - | - | - | - | - | IRAM_MBIST_FAIL | IRAM_MBIST_DONE |
| Access | | r/w | r/w | r/w | r/w | r/w | r | r |
| At | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| Bit Definitions | | |
|---|---|---|
| | BIT 0: IRAM_MBIST_DONE | 0: RAM MBIST is not complete<br>1: RAM MBIST complete<br>Note: This bit is valid only after IRAM_MBIST_EN has been set to 1 |
| | BIT 1: IRAM_MBIST_FAIL | 0: RAM MBIST had no failures after completion<br>1: RAM MBIST experienced a failure<br>Note: This bit is valid only after IRAM_MBIST_DONE flag is set 1 |
| | BIT 2: - | – |
| | BIT 3: - | – |
| | BIT 4: - | – |
| | BIT 5: - | – |
| | BIT 6: - | – |
| | BIT 7:- | – |


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### 7.3.29 EEPROM Status Register (EE_STATUS)

| EEPROM STATUS (EE_STATUS) | | | | Not Bit Addressable | | | | |
|---|---|---|---|---|---|---|---|---|
| ESFR: | 0xE1 | EE_STATUS | | | | | | |
| | BIT 7 | BIT 6 | BIT 5 | BIT 4 | BIT 3 | BIT 2 | BIT 1 | BIT 0 |
| | TRIM_ERR | CRC_ERR | EEPROG_GOOD | EE_READ_IN_PROG | EE_PROG_IN_PROG | EE_BNK[2] | EE_BNK[1] | EE_BNK[0] |
| Access | | r | r | r | r | r | r | r |
| At | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| Bit Definitions | | |
|---|---|---|
| | BIT 0:EE_BNK[0] | 000: Bank 0 has been selected<br>001: Bank 1 has been selected |
| | BIT 1:EE_BNK[1] | 010: Bank 2 has been selected<br>011: Bank 3 has been selected |
| | BIT 2:EE_BNK[2] | 100: Bank 4 has been selected<br>101: Bank 5 has been selected<br>110: D/C<br>111 D/C |
| | BIT 3: EE_PROG_IN_PROG | 0: Idle<br>1: EEPROM programming in progress |
| | BIT 4: EE_READ_IN_PROG | 0: Idle<br>1: EEPROM data transfer to cache in progress |
| | BIT 5: EEPROG_GOOD | 0: EEPROM programming not good<br>1: EEPROM programming good |
| | BIT 6:CRC_ERR | 0: EEPROM CRC is good<br>1: EEPROM CRC is in error |
| | BIT 7:TRIM_ERR | 0: Internal TRIM Value is good<br>1: Internal TRIM Value is corrupted |

### 7.3.30 EEPROM Control Register (EE_CTRL)

| EEPROM CONTROL REGISTER (EE_CTRL) | | | | Not Bit Addressable | | | | |
|---|---|---|---|---|---|---|---|---|
| ESFR: | 0xE2 | EE_CTRL | | | | | | |
| | BIT 7 | BIT 6 | BIT 5 | BIT 4 | BIT 3 | BIT 2 | BIT 1 | BIT 0 |
| | – | – | – | – | – | – | - | MICRO_EEPROG |
| Access | | r/w | r/w | r/w | r/w | r/w | r/w | r/w |
| At | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| Bit Definitions | | |
|---|---|---|
| | BIT 0:MICRO_EEPROG | 0: No Action<br>1: Program Bank 0 of EEPROM |
| | BIT 1: - | – |
| | BIT 2: - | – |
| | BIT 3: - | – |
| | BIT 4: - | – |
| | BIT 5:- | – |
| | BIT 6: - | – |
| | BIT 7: - | – |

## 7.4 Test Registers

The Test Registers are special registers that are accessible only via Digital Interface (SPI, OWI, I2C). Note that these registers are not mapped into the 8051W address space and hence are not accessible to the 8051W microprocessor.

**Upon Power-up the Digital interface will only have access to the test register space.** For the Digital interface (SPI, I2C, OWI) to gain access to the other Memory spaces, it is necessary to set the IF_SEL bit in the Micro/Interface Control register (address 0xD0). After setting this bit to '1' the digital interface will have access to all of the memory space while the 8051W will be denied access to all memory spaces. Since the 8051W will be denied access to any memory including the program memory space, it is recommended for the user to put the 8051W in reset state by writing a '1' to MICRO_RESET bit sin the Micro/Interface Control register before IF_SEL bit is set to '1'.

| ADDRESS (hex) | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | R/W | POWER UP | DESCRIPTION (PROGRAMMABLE REGS) |
|---|---|---|---|---|---|---|---|---|---|---|---|
| 03 | – | – | – | – | CLR_OWI_START | TOP_ACT | TON_ACT | TIP_ACT | R/W | 0x00 | TESTMUX_ACT |
| 04 | COMBUF[7] | COMBUF[6] | COMBUF[5] | COMBUF[4] | COMBUF[3] | COMBUF[2] | COMBUF[1] | COMBUF[0] | R/W | 0x00 | COMBUF_T |
| 05 | – | – | – | – | – | – | – | COMM_DATA_RDY | R/W | 0x00 | COMBUF_R |
| 06 | – | – | AMUX_0[5] | AMUX_0[4] | AMUX_0[3] | AMUX_0[2] | AMUX_0[1] | AMUX_0[0] | R/W | 0xx0 | AMUX_O |
| 07 | – | – | – | DMUX_O[4] | DMUX_O[3] | DMUX_O[2] | DMUX_O[1] | DMUX_O[0] | R/W | 0xx0 | DMUX_O |
| 08 | – | – | AMUX_I[5] | AMUX_I[4] | AMUX_I[3] | AMUX_I[2] | AMUX_I[1] | AMUX_I[0] | R/W | 0x00 | AMUX_I |
| 09 | – | – | – | – | DMUX_I[3] | DMUX_I[2] | DMUX_I[1] | DMUX_I[0] | R/W | 0x00 | DMUX_I |
| 0D | – | – | EE_BANK_RELOAD | IGN_PROG_TIMER | DI_EEPROG | EE_BANK _SEL[2] | EE_BANK _SEL[1] | EE_BANK _SEL[0] | R/W | 0x00 | EEPROM_A |
| 0E | – | – | – | – | – | – | MICRO_RESET | IF_SEL | R/W | 0x00 | MICRO_IF_SEL_T |
| 14 | OWI_ERR_1[7] | OWI_ERR_1[6] | OWI_ERR_1[5] | OWI_ERR_1[4] | OWI_ERR_1[3] | OWI_ERR_1[2] | OWI_ERR_1[1] | OWI_ERR_1[0] | R/W | 0x00 | OWI_ERR_1 |
| 15 | - | - | - | - | - | - | OWI_ERR_2[1] | OWI_ERR_2[0] | R/W | 0x00 | OWI_ERR_2 |


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### 7.4.1 Test MUX Activation Register (TESTMUX_ACT)

| Test MUX Activation Register (TESTMUX_ACT) | | | | Not Bit Addressable | | | | |
|---|---|---|---|---|---|---|---|---|
| TEST: | 0x03 | | | | | | | |
| | BIT 7 | BIT 6 | BIT 5 | BIT 4 | BIT 3 | BIT 2 | BIT 1 | BIT 0 |
| | – | – | – | – | CLR_OWI_STAT | TOP_ACT | TON_ACT | TIP_ACT |
| Access | r/w | r/w | r/w | r/w | r/w | r/w | r/w | r/w |
| At Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| Bit Definitions | | |
|---|---|---|
| | BIT 0:TIP_ACT | 0: No Action<br>1: Activates GPIO_2 for Test Digital Input P |
| | BIT 1: TON_ACT | 0: No Action<br>1: Activates GPIO_4 for Test Digital Output N |
| | BIT 2: TOP_ACT | 0: No Action<br>1: Activates GPIO_3 for Test Digital Output P |
| | BIT 3: CLR_OWI_STAT | 0: OWI Error bits not cleared<br>1: OWI Error bits are cleared |
| | BIT 4: - | – |
| | BIT 5:- | – |
| | BIT 6: - | – |
| | BIT 7: - | – |

**NOTE**

The TEST MUX register is only meant to be used for debugging purposes. The performance of this test mux registers is not characterized.

### 7.4.2 Communication Data Buffer (COMBUF_T)

| Communication Data Buffer Test (COMBUF_T) | | | | Not Bit Addressable | | | | |
|---|---|---|---|---|---|---|---|---|
| TEST: | 0x04 | | | | | | | |
| | BIT 7 | BIT 6 | BIT 5 | BIT 4 | BIT 3 | BIT 2 | BIT 1 | BIT 0 |
| | COMBUF[7] | COMBUF[6] | COMBUF[5] | COMBUF[4] | COMBUF[3] | COMBUF[2] | COMBUF[1] | COMBUF[0] |
| Access | r/w | r/w | r/w | r/w | r/w | r/w | r/w | r/w |
| At Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

### 7.4.3 Communication Data Buffer Ready (COMBUF_R)

| Communication Data Buffer Ready (COMBUF_R) | | | | Not Bit Addressable | | | | |
|---|---|---|---|---|---|---|---|---|
| TEST: | 0x05 | | | | | | | |
| | BIT 7 | BIT 6 | BIT 5 | BIT 4 | BIT 3 | BIT 2 | BIT 1 | BIT 0 |
| | – | – | – | – | – | – | – | COMM_DATA_RDY |
| Access | r/w | r/w | r/w | r/w | r/w | r/w | r/w | r/w |
| At Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| Bit Definitions | | |
|---|---|---|
| | BIT 0: COMM_DATA_RDY | 0: Communication Data Not available<br>1: Microprocessor had loaded data into the COMBUF ESFR |
| | BIT 1: TON_ACT | – |
| | BIT 2: TOP_ACT | – |
| | BIT 3: - | – |
| | BIT 4: - | – |
| | BIT 5:- | – |

| | | |
|---|---|---|
| | BIT 6: - | – |
| | BIT 7: - | – |


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### 7.4.4 Analog Test MUX Out Register (AMUX_O)

| Analog Test MUX Out Register (AMUX_O) | | | | Not Bit Addressable | | | | |
|---|---|---|---|---|---|---|---|---|
| TEST: | 0x06 | | | | | | | |
| | BIT 7 | BIT 6 | BIT 5 | BIT 4 | BIT 3 | BIT 2 | BIT 1 | BIT 0 |
| | – | – | AMUX_0[5] | AMUX_0[4] | AMUX_0[3] | AMUX_0[2] | AMUX_0[1] | AMUX_0[0] |
| Access | r/w | r/w | r/w | r/w | r/w | r/w | r/w | r/w |
| At Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| AMUX_O[5:0] (Hex) | TOP Output | TON Output | Voltage Divider | Description |
|---|---|---|---|---|
| 00 | GND | GND | - | 30K Resistor to Ground |
| 01 | TOUT_STAGE1p | TOUT_STAGE1n | | Stage 1 Output |
| 02 | TOUT_STAGE2p | TOUT_STAGE2n | | Stage 2 Output |
| 03 | TOUT_ADC_BUFp | TADC_BUFn | | ADC Buffer Output |
| 04 | TOUT_CTOV_OUTp | TOUT_CTOV_OUTn | | CtoV Output Prior to Buffer |
| 05 | TOUT_CTOV_BUFp | TOUT_CTOV_BUFn | | CtoV Output After Buffer |
| 06 | TOUT_OSCMP_OUTp | TOUT_OSCMP_OUTn | | Offset Compensation DAC before (A1)/E Amp |
| 07 | TOUT_OSCMP_AMPp | TOUT_OSCMP_AMPn | | Offset Compensation Outptu delivered to Stage 2 Input |
| 08 | TOUT_V2P475 | TOUT_V0P825 | | Internal 2.475V and 0.825V references |
| 09 | TOUT_VBG3V | TOUT_VPTAT | | Internal BG ZTC voltage (buffered) and PTAT signal used by temp sensor and offset compensation (un-buffered) |
| 0A | TOUT_VBG5V | GND (Spare) | | 5V ZTC reference voltage (buffered) used as a ref by AVDD & DVDD |
| 0B | TOUT_V1P65V | GND (Spare) | | Output the internal common mode reference voltage |
| 0C | TOUT_TEMP_ADC_IN | GND (Spare) | | Output of the buffer driving the temp ADC |
| 0D | TOUT_VCCINT | GND (Spare) | 0.2*VCC_INT | Internal protected 5V supply |
| 0E | TOUT_OTP_REG2V | GND (Spare) | | OTP 2V regulator voltage |
| 0F | TOUT_EEPROM_VPROG | GND (Spare) | 0.2*VEEPROM_P | EEPROM program voltage |
| 10 | TOUT_EEPROM_VSHIFT | GND (Spare) | | EEPROM Vshift voltage |
| 11 | TOUT_EEPROM_VT | GND (Spare) | | EEPROM VT voltage |

**NOTE**

The TEST MUX register is only meant to be used for debugging purposes. The performance of this test mux registers is not characterized.

### 7.4.5 Digital Test MUX Out Register (DMUX_O)

| Digital Test MUX Out Register (DMUX_O) | | | | Not Bit Addressable | | | | |
|---|---|---|---|---|---|---|---|---|
| TEST: | 0x07 | | | | | | | |
| | BIT 7 | BIT 6 | BIT 5 | BIT 4 | BIT 3 | BIT 2 | BIT 1 | BIT 0 |
| | – | – | – | DMUX_O[4] | DMUX_O[3] | DMUX_O[2] | DMUX_O[1] | DMUX_O[0] |
| Access | r/w | r/w | r/w | r/w | r/w | r/w | r/w | r/w |
| At Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| DMUX_O[4:0] (Hex) | TOP_D (GPIO3) | TON_D (GPIO4) | Remark |
|---|---|---|---|
| 00 | ZERO | ZERO | Ground |
| 01 | PSMON[0] | PSMON[1] | PSMON Flags |
| 02 | PSMON[2] | PSMON[3] | PSMON Flags |
| 03 | PSMON[4] | PSMON[5] | PSMON Flags |
| 04 | PSMON[6] | PSMON[7] | PSMON Flags |
| 05 | PSMON[8] | PSMON[9] | PSMON Flags |
| 06 | PSMON[10] | PSMON[11] | PSMON Flags |
| 07 | AFEDIAG[0] | AFEDIAG[1] | AFEDIAG Flags |
| 08 | AFEDIAG[2] | AFEDIAG[3] | AFEDIAG Flags |
| 09 | OWI_5P4_COMP_IN | OWI_6P8_COMP_IN | Low and High comparator outputs used by OWI Activation circuit |
| 0A | OSC_5M | OSC_200K | 5MHz Internal oscillator and 200KHz Watchdog Oscillator |
| 0B | OSC_XTAL | CLK_EE_2M | Crystal Oscillator and EEPROM Charge Pump Clk |
| 0C | CLK_ADC_1M | CLK_TADC_128K | PRessure ADC Clock and Temperature ADC Clock |
| 0D | CHOP_CLK_700K | CTOV_CLK | First Stage Chopper Clock, Capacitive AFE Clock |
| 0E | SDM_PWM | SDM_ERR | PWM and ERR output from Pressure SDM |
| 0F | SDM_TEMP | CIRAM_MBIST_RETENTION | PWM from Temperature SDM, CIRAM MBIST Retention Stop |
| 10 | LOAD_DS1 | LOAD_DS2 | Sensor decimator downsample pulses |
| 11 | LOAD_DS_TEMP | XINTR_SRC[5] | Temperature decimator downsample pulse, External Interrupt |
| 12 | XINTR_SRC[7] | XINTR_SRC[8] | External Interrupt |
| 13 | XINTR_SRC[9] | XINTR_SRC[10] | External Interrupt |
| 14 | XINTR_SRC[11] | XINTR_SRC[12] | External Interrupt |


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### 7.4.6 Analog Test MUX In Register (AMUX_I)

| Analog Test MUX In Register (AMUX_I) | | | | Not Bit Addressable | | | | |
|---|---|---|---|---|---|---|---|---|
| TEST: | 0x08 | | | | | | | |
| | BIT 7 | BIT 6 | BIT 5 | BIT 4 | BIT 3 | BIT 2 | BIT 1 | BIT 0 |
| | – | – | - | AMUX_I[4] | AMUX_I[3] | AMUX_I[2] | AMUX_I[1] | AMUX_I[0] |
| Access | r/w | r/w | r/w | r/w | r/w | r/w | r/w | r/w |
| At Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| AMUX_I[4:0] (Hex) | TIP | TIN | Remark |
|---|---|---|---|
| 00 | GND | GND | 30K Resistor to Ground |
| 01 | TIN_STAGE2p | TIN_STAGE2N | Input to Stage 2 Amp |
| 02 | TIN_ADC_BUFp | TIN_ADC_BUFn | Input to ADC Buffer |
| 03 | TIN_ADCp | TIN_ADCn | Input to Pressure SDM |
| 04 | TIN_CTOV_AMPp | TIN_CTOV_AMPn | Input to CTOV Trans-Z configured as voltage amplifier in test mode |
| 05 | TIN_CTOV_OUTp | TIN_CTOV_OUTn | Input to output buffer in the CTOV AFE |
| 06 | TIN_OSCMP_AMPp | TIN_OSCMP_AMPn | Input to the voltage amplifier in the offset compensation circuit |
| 07 | TIN_V2P475 | TIN_V0P825 | Set the internal 2.475V and 0.825V references |
| 08 | TIN_DAC_BUFF1 | TIN_DAC_BUFF2 | Input to the DAC Buffers |
| 09 | TIN_OSCMP_VBG | TIN_OSCMP_VPTAT | Set the ZTC and PTAT signals used by the offset compensation circuit |
| 0A | TIN_COMPREF | GND | Reference input to the comparator in the Capacitive AFE circuit |
| 0B | TIN_CTOV_CLK | GND | Set the clock used by Capacitive AFE |
| 0C | TIN_V1P65 | GND | Set the internal 1.65V reference |
| 0D | TIN_BG5 | GND | Set the internal 5V bandgap reference signal |
| 0E | TIN_TEMP_ADC | GND | Input to Temperature ADC |
| 0F | TIN_SNSR_SUPPLY_REF | GND | Set the reference used by VBRG |
| 10 | TIN_IBIST_OTP | GND | Input current for OTP test |
| 11 | TOUT_IB10U_5V | TOUT_IB10U_3V | Bias current from 5V and 3V bandgaps |

**NOTE**

The TEST MUX register is only meant to be used for debugging purposes. The performance of this test mux registers is not characterized.

### 7.4.7 Digital Test MUX In Register (DMUX_I)

| Digital Test MUX In Register (DMUX_I) | | | | Not Bit Addressable | | | | |
|---|---|---|---|---|---|---|---|---|
| TEST: | 0x09 | | | | | | | |
| | BIT 7 | BIT 6 | BIT 5 | BIT 4 | BIT 3 | BIT 2 | BIT 1 | BIT 0 |
| | – | – | – | – | DMUX_I[3] | DMUX_I[2] | DMUX_I[1] | DMUX_I[0] |
| Access | r/w | r/w | r/w | r/w | r/w | r/w | r/w | r/w |
| At Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| DMUX_I[3:0] (Hex) | TIP_D Connected to | Remark |
|---|---|---|
| 00 | GND | Reference |
| 01 | OTP_CLK | OTP Clock |
| 02 | SADC_PWM | Pressure ADC PWM Bit |
| 03 | TADC_PWM | Temperature ADC PWM Bit |
| 04 | CLK_ADC_1M | Pressure SDM Clock |
| 05 | CLK_TADC_128K | Temperature SDM Clock |
| 06 | CHOP_CLK_700K | Clock for first stage chopper amplifier |
| 07 | CLK_EE_CP | Clock for EEPROM charge pump |
| 08 | XINTR_ACK[5] | Interrupt Acknowledge |
| 09 | XINTR_ACK[7] | Interrupt Acknowledge |
| 0A | XINTR_ACK[8] | Interrupt Acknowledge |
| 0B | XINTR_ACK[9] | Interrupt Acknowledge |
| 0C | XINTR_ACK[10] | Interrupt Acknowledge |

**NOTE**

The TEST MUX register is only meant to be used for debugging purposes. The performance of this test mux registers is not characterized.


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### 7.4.8 EEPROM Access Control Register (EEPROM_A)

| EEPROM Access Control Register (EEPROM_A) | | | | Not Bit Addressable | | | | |
|---|---|---|---|---|---|---|---|---|
| TEST: | 0x0D | | | | | | | |
| | BIT 7 | BIT 6 | BIT 5 | BIT 4 | BIT 3 | BIT 2 | BIT 1 | BIT 0 |
| | – | – | EE_BANK_ RELOAD | IGN_PROG _ TIMER | DI_EEPRO G | EE_BANK _ SEL[2] | EE_BANK _ SEL[1] | EE_BANK _ SEL[0] |
| Access | r/w | r/w | r/w | r/w | r/w | r/w | r/w | r/w |
| At Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| | | |
|---|---|---|
| Bit Definitions | | |
| | BIT 0: EE_BANK_SEL[0] | EE_BANK_SEL[0:2]<br>0b000: Bank 0 |
| | BIT 1: EE_BANK_SEL[1] | 0b001: Bank 1<br>0b010: Bank 2 |
| | BIT 2: EE_BANK_SEL[2] | 0b011: Bank 3<br>0b100: Bank 4<br>0b101: Bank 5 |
| | BIT 3: DI_EEPROG | 0: No Action<br>1: Program EEPROM via Digital Interface (SPI, I2C, OWI) |
| | BIT 4: IGN_PROG_TIMER | 0: DI_EEPROG is reset to 0 15ms after being set to 1 by Digital Interface<br>1: Program timer timeout is ignored |
| | BIT 5: EE_BANK_RELOAD | 0: No Action<br>1: Force Reload current EEPROM bank contents into EEPROM Cache |
| | BIT 6: - | |
| | BIT 7: - | |

### 7.4.9 Micro/Interface Control Register (MICRO_IF_SEL_T)

| Micro/Interface Control Register (MICRO_IF_SEL_T) | | | | Not Bit Addressable | | | | |
|---|---|---|---|---|---|---|---|---|
| TEST: | 0x0E | | | | | | | |
| | BIT 7 | BIT 6 | BIT 5 | BIT 4 | BIT 3 | BIT 2 | BIT 1 | BIT 0 |
| | – | – | – | – | – | – | MICRO_RESET | IF_SEL |
| Access | r/w | r/w | r/w | r/w | r/w | r/w | r/w | r/w |
| At Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| | | |
|---|---|---|
| Bit Definitions | | |
| | BIT 0: IF_SEL | 0: 8051W microprocessor will access Memory (EEPROM, OTP, ESFR, RAM)<br>1: Digital Interface will access Memory |
| | BIT 1: MICRO_RESET | 0: No Action<br>1: 8051W is in reset |
| | BIT 2: – | |
| | BIT 3: – | |
| | BIT 4: – | |
| | BIT 5: – | |
| | BIT 6: – | |
| | BIT 7: – | |

### 7.4.10 OWI Error Status 1 (OWI_ERR_1)

| OWI Error Status 1 (OWI_ERR_1) | | | | Not Bit Addressable | | | | |
|---|---|---|---|---|---|---|---|---|
| TEST: | 0x14 | | | | | | | |
| | BIT 7 | BIT 6 | BIT 5 | BIT 4 | BIT 3 | BIT 2 | BIT 1 | BIT 0 |
| | OWI_ERR_1[7] | OWI_ERR_1[6] | OWI_ERR_1[5] | OWI_ERR_1[4] | OWI_ERR_1[3] | OWI_ERR_1[2] | OWI_ERR_1[1] | OWI_ERR_1[0] |
| Access | r/w | r/w | r/w | r/w | r/w | r/w | r/w | r/w |
| At Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| | | |
|---|---|---|
| Bit Definitions | | |
| | BIT 0: OWI_ERR_1[0] | 0: No Error<br>1: SYNC Field bit rate is < 2000bps |
| | BIT 1: OWI_ERR_1[1] | 0: No Error<br>1: SYNC Field bit rate is < `25Kbps |
| | BIT 2: OWI_ERR_1[2] | 0: No Error |


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| | | |
|---|---|---|
| | | 1: SYNC Field stop bit too short |
| | BIT 3: OWI_ERR_1[3] | 0: No Error<br>1: CMD Field: incorrect stop bit value |
| | BIT 4: OWI_ERR_1[4] | 0: No Error<br>1: CMD Field: stop bit too short |
| | BIT 5: OWI_ERR_1[5] | 0: No Error<br>1: DATA Field: incorrect stop bit value |
| | BIT 6: OWI_ERR_1[6] | 0: No Error<br>1: DATA Field; stop bit too short |
| | BIT 7: OWI_ERR_1[7] | 0: No Error<br>1: DATA Field: slave transmit value overdriven to dominant value during stop bit transmit |

### 7.4.11 OWI Error Status 2 (OWI_ERR_2)

| OWI Error Status 2 (OWI_ERR_2) | | | | Not Bit Addressable | | | | |
|---|---|---|---|---|---|---|---|---|
| TEST: | 0x15 | | | | | | | |
| | BIT 7 | BIT 6 | BIT 5 | BIT 4 | BIT 3 | BIT 2 | BIT 1 | BIT 0 |
| | - | - | - | - | - | - | OWI_ERR_2[1] | OWI_ERR_2[0] |
| Access | r/w | r/w | r/w | r/w | r/w | r/w | r/w | r/w |
| At Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| Bit Definitions | | |
|---|---|---|
| | BIT 0: OWI_ERR_2[0] | 0: No Error<br>1: Consecutive bits in the sync field are different by more than +/-25% tolerance |
| | BIT 1: OWI_ERR_2[1] | 0: No Error<br>1: INVALID command sent through OWI protocol |
| | BIT 2: - | - |
| | BIT 3: - | - |
| | BIT 4: - | - |
| | BIT 5: - | - |
| | BIT 6: - | - |
| | BIT 7: - | - |

## 7.5 8051W Interrupts

MCU8051 provides the five standard 8051-compatible 'Legacy' interrupts, plus expansion capability for a further nine 'Extended' interrupts sourced from external user logic. The standard and extended interrupts each have separate enable register bits associated with them, allowing software control. They can also have two levels of priority assigned to them.

### *7.5.1 Standard Interrupts*

The five standard interrupts comprise two timer overflow interrupts, an interrupt associated with the core's built-in serial interface, and two external interrupts (referred to as 'Legacy' external interrupts).

**The two Timer overflow interrupts**, TF0 and TF1, are set whenever timer 0 or timer 1 respectively roll-over to zero. The states of these interrupts are also stored in the TCON register. TF0 and TF1 are automatically cleared by hardware on entry to the corresponding interrupt service routine.

**The Serial interrupt** source comprises the logical OR of the two serial interface status bits RI and TI in register SCON. These are set automatically upon receipt or transmission of a data frame. These two bits are not cleared by hardware.

**The Legacy external interrupts**, NINT0 and NINT1, are driven from inputs PORT3(2) and PORT3(3) respectively. These interrupts may be either edge- or level-sensitive, depending on settings within the TCON register. Two further TCON register bits, IE0 and IE1, act as interrupt flags. If the external interrupt is set to edge-triggered, the corresponding register bit IE0/1 is set by a falling edge on NINT0/1 and cleared by hardware on entry to the corresponding interrupt service routine. If the interrupt is set to be level-sensitive, IE0/1 reflects the logic level on NINT0/1. (The TCON register is described in Section 5.2.5.1).

**NOTE**

All events on NINT0 and NINT1, whether level-triggered or edge-triggered, are detected by sampling the relevant interrupt line on the rising edge of SCLK at the end of Phase 1 of every machine cycle. Where NINT0/NINT1 is level-triggered, a response is made to the signal being sampled low and, to ensure detection, the external source needs to hold the line low until the resulting interrupt is generated. (It also needs to ensure that the request is de-activated before the end of the associated service routine.) Where NINT0/NINT1 is edge-triggered, the response is made to a transition on the signal from high to low between successive samples. This means that, to ensure detection, NINT0/NINT1 needs to have been high for at least two clocks before it goes low and then needs to be held low for at least two clocks after this transition.

(Further information about these five standard interrupts can be found, for example, in the Intel 8-Bit Embedded Controller Handbook in the 'Hardware Description of the 8051, 8052 & 80C51'.)

### *7.5.2 Extended Interrupts*

Source and acknowledge signals are provided for a further nine interrupts. These interrupts are driven from external user logic, typically a user ESFR. The extended interrupts are input to the core on bits 5 to 13 of input bus XINTR_SRC, while acknowledge signals are output from the core on bits 5 to 13 of bus XINTR_ACK. Note: If the timers or the UART are omitted from the design, their corresponding interrupt inputs (plus those of the Legacy external interrupts where the timers are omitted) are made available at the core periphery as XINTR_SRC[4:0], along with corresponding XINTR_ACK acknowledge signals, for use as additional Extended interrupts.)

The extended interrupt lines are sampled on the rising edge of PCLK at the beginning of Phase 2 of the last cycle of the current instruction. To ensure detection, the external source needs to hold the XINTR_SRC line high until the resulting interrupt is generated. (It also needs to ensure that the request is deactivated before the end of the associated service routine.). Note: Any edge-triggering that is required will need to be taken care of by individual peripherals.


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#### 7.5.2.1 Interrupt Flag Clear

If the Legacy external interrupts NINT0 and NINT1 are edge triggered, the interrupt flag is cleared on vectoring to the service routine. If they are level triggered, the flag is controlled by the external signal. Timer/counter flags are cleared on vectoring to the interrupt service routine but the serial interrupt flag is not affected by hardware. The serial interrupt flag should be cleared by software. Acknowledge signals are provided for clearing any registers used to source the nine additional interrupts.

#### 7.5.2.2 Priority Levels / Interrupt Vectors

One of two priority levels may be selected for each interrupt. An interrupt of a high priority may interrupt the service routine of a low priority interrupt and, if two interrupts of different priority occur at the same time, the higher level interrupt will be serviced first. An interrupt cannot be interrupted by another interrupt of the same priority level. If two interrupts of the same priority level occur simultaneously, a polling sequence is observed. The polling sequence is described in Table 21.

When an interrupt is serviced, a long call instruction is executed to an address location, according to the interrupt's source: The interrupt vector addresses for each interrupt is listed in Table 21.

**Table 7-1. Interrupt Summary.**
**The entries that are greyed out in the above table are not available for use in the PGA400-Q1.**

| 8051W Source | PGA400 | Vector Address | Polling Sequence | Flag | Enable | Priority Control |
|---|---|---|---|---|---|---|
| External Interrupt 0 (GPI0_5) | GPIO_5 | 0x0003 | 1 (Highest) | IE0 (TCON.1) | EX0 (IE.0) | PX0 (IP.0) |
| Timer/Counter Interrupt 0 | ← | 0x000B | 2 | TF0 (TCON.5) | ET0 (IE.1) | PT0 (IP.1) |
| External Interrupt 1 | | 0x0013 | 3 | IE1 (TCON.3) | EX1 (IE.2) | PX1 (IP.2) |
| Timer/Counter Interrupt 1 | ← | 0x001B | 4 | TF1 (TCON.7) | ET1 (IE.3) | PT1 (IP.3) |
| Serial Port 0 | ← | 0x0023 | 5 | RI_0 (SCON0.0) TI_0 (SCON0.1) | ES0 (IE.4) | PS0 (IP.4) |
| External Interrupt 5 | OWI ACTIVATION | 0x002B | 6 | - | EI5 (IE.5) | PI5 (IP.5) |
| External Interrupt 6 | COMM DATA BUFFER | 0x0033 | 7 | - | EI6 (IE1.0) | PI6 (IP1.0) |
| External Interrupt 7 | IC_1 | 0x003B | 8 | - | EI7 (IE1.1) | PI7 (IP1.1) |
| External Interrupt 8 | IC_2 | 0x0043 | 9 | - | EI8 (IE1.2) | PI8 (IP1.2) |
| External Interrupt 9 | OC_1 | 0x004B | 10 | - | EI9 (IE1.3) | PI9 (IP1.3) |
| External Interrupt 10 | OC_2 | 0x0053 | 11 | - | EI10 (IE14) | P10 (IP1.4) |
| External Interrupt 11 | Signal Channel 1st Stage Decimator | 0x005B | 12 | - | EI11 (IE1.5) | P11 (IP1.5) |
| External Interrupt 12 | Signal Channel 2nd Stage Decimator | 0x0063 | 13 | - | EI12 (IE1.6) | P12 (IP16) |
| External Interrupt 13 | | 0x006B | 14 (Lowest) | - | EI13 (IE1.7) | P13 (IP.7) |

#### 7.5.2.3 Interrupt Latency

The response time in a single interrupt system is between 3 and 9 machine cycles.

## 7.6 8051 Instructions

The M8051 Warp instruction set is shown as a table in a following section. Some of the features supported are outlined below.

### *7.6.1 Addressing Modes*

The M8051 Warp provides a variety of addressing modes, which are outlined below.

#### 7.6.1.1 Direct Addressing

In Direct Addressing, the operand is specified by an 8-bit address field. Only internal data and SFRs may be accessed using this mode.

#### 7.6.1.2 Indirect Addressing

In Indirect Addressing, the operand is specified by an address contained in a register. Two registers (R0 and R1) from the current bank or the Data Pointer may be used for addressing in this mode. Both internal and external Data Memory may be indirectly addressed.

#### 7.6.1.3 Register Addressing

In Register Addressing, the operand is specified by the top 3 bits of the opcode, which selects one of the current bank of registers. Four banks of registers are available. The current bank is selected by bits 3 and 4 of the PSW.

#### 7.6.1.4 Register Specific Addressing

Some instructions only operate on specific registers. This is defined by the opcode. In particular many accumulator operations and some stack pointer operations are defined in this manner.

#### 7.6.1.5 Immediate Data

Instructions which use Immediate Data are 2 or 3 bytes long and the Immediate operand is stored in Program Memory as part of the instruction.

#### 7.6.1.6 Indexed Addressing

Only Program Memory may be addressed using Indexed Addressing. It is intended for simple implementation of look-up tables. A 16-bit base register (either the PC or the DPTR) is combined with an offset stored in the accumulator to access data in Program Memory.

### *7.6.2 Arithmetic Instructions*

The M8051 Warp implements ADD, ADDC (Add with Carry), SUBB (Subtract with Borrow), INC (Increment) and DEC (Decrement) functions, which may be used in most addressing modes. There are three accumulator-specific instructions, DA A (Decimal Adjust A), MUL AB (Multiply A by B) and DIV AB (Divide A by B).

### *7.6.3 Logical Instructions*

The M8051 Warp implements ANL (AND Logical), ORL (OR Logical), and XRL (Exclusive-OR Logical) functions, which again may be used in most addressing modes. There are seven accumulator-specific instructions, CLR A (Clear A), CPL A (Complement A), RL A (Rotate Left A), RLC A (Rotate Left through Carry A), RR A (Rotate Right A), RRC A (Rotate Right through Carry A), and SWAP A (Swap Nibbles of A).


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### 7.6.4 Data Transfers

#### 7.6.4.1 Internal Data Memory

Data may be moved from the accumulator to any Internal Data Memory location, from any Internal Data Memory location to the accumulator, and from any Internal Data Memory location to any SFR or other Internal Data Memory location.

#### 7.6.4.2 External Data Memory

Data may be moved from the accumulator to or from an external memory location in one of two addressing modes. In 8-bit addressing mode, the external location is addressed by either R0 or R1; in 16-bit addressing mode, the location is addressed by the DPTR.

### 7.6.5 Jump Instructions

#### 7.6.5.1 Unconditional Jumps

Four sorts of unconditional jump instructions are available. Short jumps (SJMP) are relative jumps (limited to -128 to +127 bytes), Long jumps (LJMP) are absolute 16-bit jumps and Absolute jumps (AJMP) are absolute 11-bit jumps (ie. within a 2K byte memory page). The last type is an Indexed jump, JMP @A+DPTR, which jumps to a location contained in the DPTR register, offset by a value stored in the accumulator.

#### 7.6.5.2 Subroutine Calls and Returns

There are only two sorts of subroutine call, ACALL and LCALL, which are Absolute and Long as above. Two return instructions are provided, RET and RETI. The latter is for interrupt service routines.

#### 7.6.5.3 Conditional Jumps

Conditional jump instructions all use relative addressing, so are limited to the same -128 to +127 byte range as above.

#### 7.6.5.4 Boolean Instructions

The bit-addressable registers in both direct and SFR space may be manipulated using Boolean instructions. Logical functions are available which use the carry flag and an addressable bit as the operands and each addressable bit may be set, cleared or tested in a jump instruction.

### 7.6.6 Flags

The following instructions affect flags generated by the ALU:

| Instruction | Flag | | | Instruction | Flag | | |
|---|---|---|---|---|---|---|---|
| | C | OV | AC | | C | OV | AC |
| ADD | ? | ? | ? | CLRC | 0 | | |
| ADDC | ? | ? | ? | CPLC | ? | | |
| SUBB | ? | ? | ? | ANL C, bit | ? | | |
| MUL | 0 | ? | | ANL C, /bit | ? | | |
| DIV | 0 | ? | | ORL C, bit | ? | | |
| DA | ? | | | ORL C, /bit | ? | | |
| RRC | ? | | | MOV C, bit | ? | | |
| RLC | ? | | | CJNE | ? | | |
| SETB C | 1 | | | | | | |

In the above table, a 0 means the flag is always cleared, a 1 means the flag is always set and an "?" means that the state of the flag depends on the result of the operation. The Flag specified as Blank means that the state is unknown.


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### 7.6.7 Instruction Table

Instructions are either 1, 2 or 3 bytes long as listed in the 'Bytes' column below. Each instruction takes either 1, 2 or 4 machine cycles to execute as listed in the following table. 1 machine cycle comprises 2 CCLK clock cycles.

| **ARITHMETIC** | | | | |
|---|---|---|---|---|
| **Mnemonic** | **Description** | **Bytes** | **Cycles** | **Hex code** |
| ADD A,Rn | Add register to A | 1 | 1 | 28–2F |
| ADD A,dir | Add direct byte to A | 2 | 1 | 25 |
| ADD A,@Ri | Add indirect memory to A | 1 | 1 | 26–27 |
| ADD A,#data | Add immediate to A | 2 | 1 | 24 |
| ADDC A,Rn | Add register to A with carry | 1 | 1 | 38–3F |
| ADDC A,dir | Add direct byte to A with carry | 2 | 1 | 35 |
| ADDC A,@Ri | Add indirect memory to A with carry | 1 | 1 | 36–37 |
| ADDC A,#data | Add immediate to A with carry | 2 | 1 | 34 |
| SUBB A,Rn | Subtract register from A with borrow | 1 | 1 | 98–9F |
| SUBB A,dir | Subtract direct byte from A with borrow | 2 | 1 | 95 |
| SUBB A,@RI | Subtract indirect memory from A with borrow | 1 | 1 | 96–97 |
| SUBB A,#data | Subtract immediate from A with borrow | 2 | 1 | 94 |
| INC A | Increment A | 1 | 1 | 04 |
| INC Rn | Increment register | 1 | 1 | 08–0F |
| INC dir | Increment direct byte | 2 | 1 | 05 |
| INC @Ri | Increment indirect memory | 1 | 1 | 06–07 |
| DEC A | Decrement A | 1 | 1 | 14 |
| DEC Rn | Decrement register | 1 | 1 | 18–1F |
| DEC dir | Decrement direct byte | 2 | 1 | 15 |
| DEC @Ri | Decrement indirect memory | 1 | 1 | 16–17 |
| INC DPTR | Increment data pointer | 1 | 2 | A3 |
| MUL AB | Multiply A by B | 1 | 4 | A4 |
| DIV AB | Divide A by B | 1 | 4 | 84 |
| DA A | Decimal Adjust A | 1 | 1 | D4 |
| **LOGICAL** | | | | |
| ANL A,Rn | AND register to A | 1 | 1 | 58–5F |
| ANL A,diR | AND direct byte to A | 2 | 1 | 55 |
| ANL A,@Ri | AND indirect memory to A | 1 | 1 | 56–57 |
| ANL A,#data | AND immediate to A | 2 | 1 | 54 |
| ANL dir,A | AND A to direct byte | 2 | 1 | 52 |
| ANL dir,#data | AND immediate to direct byte | 3 | 2 | 53 |
| ORL A,Rn | OR register to A | 1 | 1 | 48–4F |
| ORL A,dir | OR direct byte to A | 2 | 1 | 45 |
| ORL A,@Ri | OR indirect memory to A | 1 | 1 | 46–47 |
| ORL A,#data | OR immediate to A | 2 | 1 | 44 |
| ORL dir,A | OR A to direct byte | 2 | 1 | 42 |
| ORL dir,#data | OR immediate to direct byte | 3 | 2 | 43 |
| XRL A,Rn | Exclusive-OR register to A | 1 | 1 | 68–6F |
| XRL A,dir | Exclusive-OR direct byte to A | 2 | 1 | 65 |
| XRL A, @Ri | Exclusive-OR indirect memory to A | 1 | 1 | 66–67 |
| XRL A,#data | Exclusive-OR immediate to A | 2 | 1 | 64 |
| XRL dir,A | Exclusive-OR A to direct byte | 2 | 1 | 62 |
| XRL dir,#data | Exclusive-OR immediate to direct byte | 3 | 2 | 63 |

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| ARITHMETIC | | | | |
|---|---|---|---|---|
| **Mnemonic** | **Description** | **Bytes** | **Cycles** | **Hex code** |
| CLR A | Clear A | 1 | 1 | E4 |
| CPL A | Complement A | 1 | 1 | F4 |
| SWAP A | Swap Nibbles of A | 1 | 1 | C4 |
| RL A | Rotate A left | 1 | 1 | 23 |
| RLC A | Rotate A left through carry | 1 | 1 | 33 |
| RR A | Rotate A right | 1 | 1 | 03 |
| RRC A | Rotate A right through carry | 1 | 1 | 13 |
| **DATA TRANSFER** | | | | |
| MOV A,Rn | Move register to A | 1 | 1 | E8–EF |
| MOV A,dir | Move direct byte to A | 2 | 1 | E5 |
| MOV A,@Ri | Move indirect memory to A | 1 | 1 | E6–E7 |
| MOV A,#data | Move immediate to A | 2 | 1 | 74 |
| MOV Rn,A | Move A to register | 1 | 1 | F8–FF |
| MOV Rn,dir | Move direct byte to register | 2 | 2 | A8–AF |
| MOV Rn,#data | Move immediate to register | 2 | 1 | 78–7F |
| MOV dir,A | Move A to direct byte | 2 | 1 | F5 |
| MOV dir,Rn | Move register to direct byte | 2 | 2 | 88–8F |
| MOV dir,dir | Move direct byte to direct byte | 3 | 2 | 85 |
| MOV dir,@Ri | Move indirect memory to direct byte | 2 | 2 | 86–87 |
| MOV dir,#data | Move immediate to direct byte | 3 | 2 | 75 |
| MOV @Ri,A | Move A to indirect memory | 1 | 1 | F6–F7 |
| MOV @Ri,dir | Move direct byte to indirect memory | 2 | 2 | A6–A7 |
| MOV @Ri,#data | Move immediate to indirect memory | 2 | 1 | 76–77 |
| MOV DPTR,#data | Move immediate to data pointer | 3 | 2 | 90 |
| MOVC A,@A+DPTR | Move code byte relative DPTR to A | 1 | 2 | 93 |
| MOVC A,@A+PC | Move code byte relative PC to A | 1 | 2 | 83 |
| MOVX A,@Ri | Move external data(A8) to A | 1 | 2 | E2–E3 |
| MOVX A,@DPTR | Move external data(A16) to A | 1 | 2 | E0 |
| MOVX @Ri,A | Move A to external data(A8) | 1 | 2 | F2–F3 |
| MOVX @DPTR,A | Move A to external data(A16) | 1 | 2 | F0 |
| PUSH dir | Push direct byte onto stack | | | C0 |
| POP dir | Pop direct byte from stack | | | D0 |
| XCH A,Rn | Exchange A and register | | | C8–CF |
| XCH A,dir | Exchange A and direct byte | | | C5 |
| XCH A,@Ri | Exchange A and indirect memory | | | C6–C7 |
| XCHD A,@Ri | Exchange A and indirect memory nibble | | | D6–D7 |
| **BOOLEAN** | | | | |
| CLR C | Clear carry | 1 | 1 | C3 |
| CLR bit | Clear direct bit | 2 | 1 | C2 |
| SETB C | Set carry | 1 | 1 | D3 |
| SETB bit | Set direct bit | 2 | 1 | D2 |
| CPL C | Complement carry | 1 | 1 | B3 |
| CPL bit | Complement direct bit | 2 | 1 | B2 |
| ANL C,bit | AND direct bit to carry | 2 | 2 | 82 |
| ANL C,/bit | AND direct bit inverse to carry | 2 | 2 | B0 |
| ORL C,bit | OR direct bit to carry | 2 | 2 | 72 |
| ORL C,/bit | OR direct bit inverse to carry | 2 | 2 | A0 |
| MOV C,bit | Move direct bit to carry | 2 | 1 | A2 |


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| ARITHMETIC | | | | |
|---|---|---|---|---|
| **Mnemonic** | **Description** | **Bytes** | **Cycles** | **Hex code** |
| MOV bit,C | Move carry to direct bit | 2 | 2 | 92 |
| **BRANCHING** | | | | |
| ACALL addr 11 | Absolute jump to subroutine | 2 | 2 | 11→F1 |
| LCALL addr 16 | Long jump to subroutine | 3 | 2 | 12 |
| RET | Return from subroutine | 1 | 2 | 22 |
| RETI | Return from interrupt | 1 | 2 | 32 |
| AJMP addr 11 | Absolute jump unconditional | 2 | 2 | 01→E1 |
| LJMP addr 16 | Long jump unconditional | 3 | 2 | 02 |
| SJMP rel | Short jump (relative address) | 2 | 2 | 80 |
| JC rel | Jump on carry = 1 | 2 | 2 | 40 |
| JNC rel | Jump on carry = 0 | 2 | 2 | 50 |
| JB bit,rel | Jump on direct bit = 1 | 3 | 2 | 20 |
| JNB bit,rel | Jump on direct bit = 0 | 3 | 2 | 30 |
| JBC bit,rel | Jump on direct bit = 1 and clear | 3 | 2 | 10 |
| JMP @A+DPTR | Jump indirect relative DPTR | 1 | 2 | 73 |
| JZ rel | Jump on accumulator = 0 | 2 | 2 | 60 |
| JNZ rel | Jump on accumulator ≠ 0 | 2 | 2 | 70 |
| CJNE A,dir,rel | Compare A,direct jne relative | 3 | 2 | B5 |
| CJNE A,#d,rel | Compare A,immediate jne relative | 3 | 2 | B4 |
| CJNE Rn,#d,rel | Compare register, immediate jne relative | 3 | 2 | B8–BF |
| CJNE @Ri,#d,rel | Compare indirect, immediate jne relative | 3 | 2 | B6–B7 |
| DJNZ Rn,rel | Decrement register, jnz relative | 2 | 2 | D8–DF |
| DJNZ dir,rel | Decrement direct byte, jnz relative | 3 | 2 | D5 |
| **MISCELLANEOUS** | | | | |
| NOP | No operation | 1 | 1 | 00 |

In the above table, an entry such as E8-EF indicates a continuous block of hex opcodes used for 8 different registers, the register numbers of which are defined by the lowest three bits of the corresponding code. Non-continuous blocks of codes, shown as 11→F1 (for example), are used for absolute jumps and calls, with the top 3 bits of the code being used to store the top three bits of the destination address. The CJNE instructions use the abbreviation #d for immediate data; other instructions use #data.

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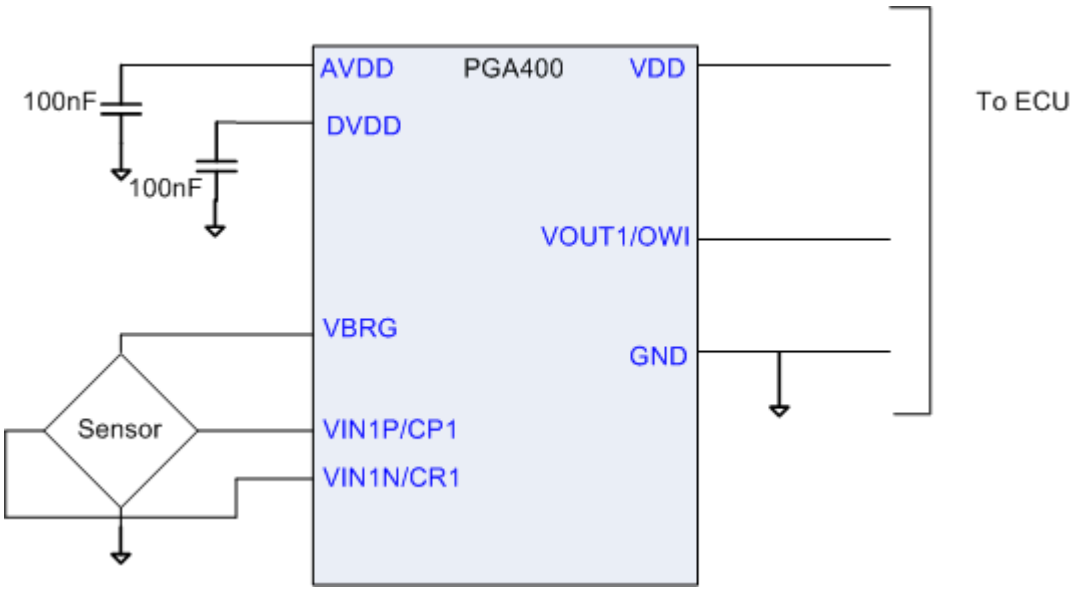
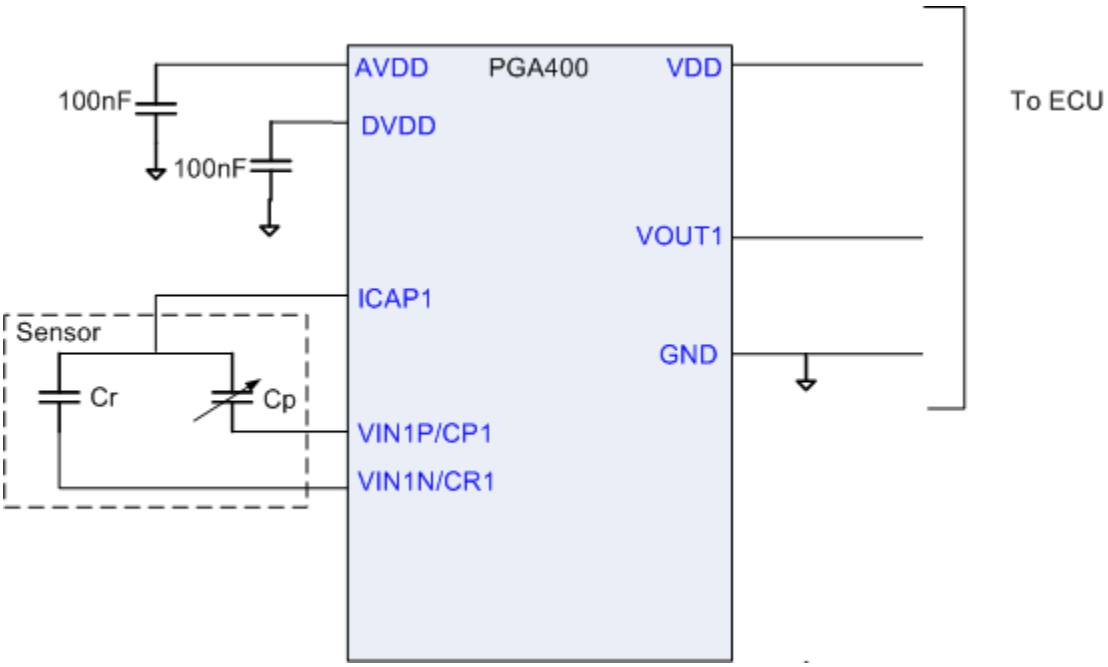
# 8 APPLICATION SCHEMATIC

## 8.1 Resistive Bridge Interface




## 8.2 Capacitive Sensor Interface





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# 9 REVISION HISTORY

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

| Changes from Revision A (June 2013) to Revision B | Page |
|---|---|
| • Changed pins 25 - 30 | 3 |

## PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/Ball Finish (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|---|---|---|---|---|---|---|---|---|---|---|---|
| PGA400QRHHTEP | ACTIVE | VQFN | RHH | 36 | 250 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-3-260C-168 HR | -40 to 125 | PGA400Q RHH -EP | Samples |
| V62/13619-01XE | ACTIVE | VQFN | RHH | 36 | 250 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-3-260C-168 HR | -40 to 125 | PGA400Q RHH -EP | Samples |

(1) The marketing status values are defined as follows:
**ACTIVE:** Product device recommended for new designs.
**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.
**OBSOLETE:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
**TBD:** The Pb-Free/Green conversion plan has not been defined.
**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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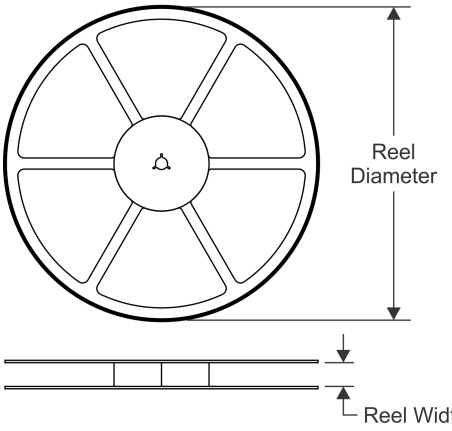
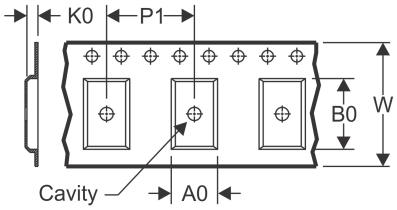
## TAPE AND REEL INFORMATION

**REEL DIMENSIONS**

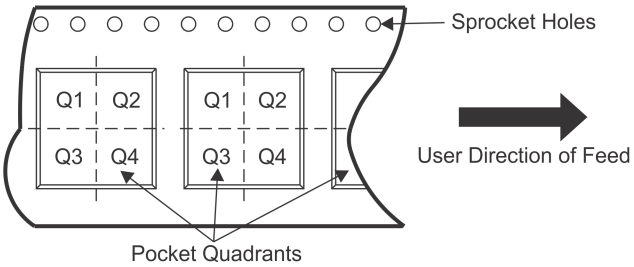



**TAPE DIMENSIONS**




| | |
|---|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

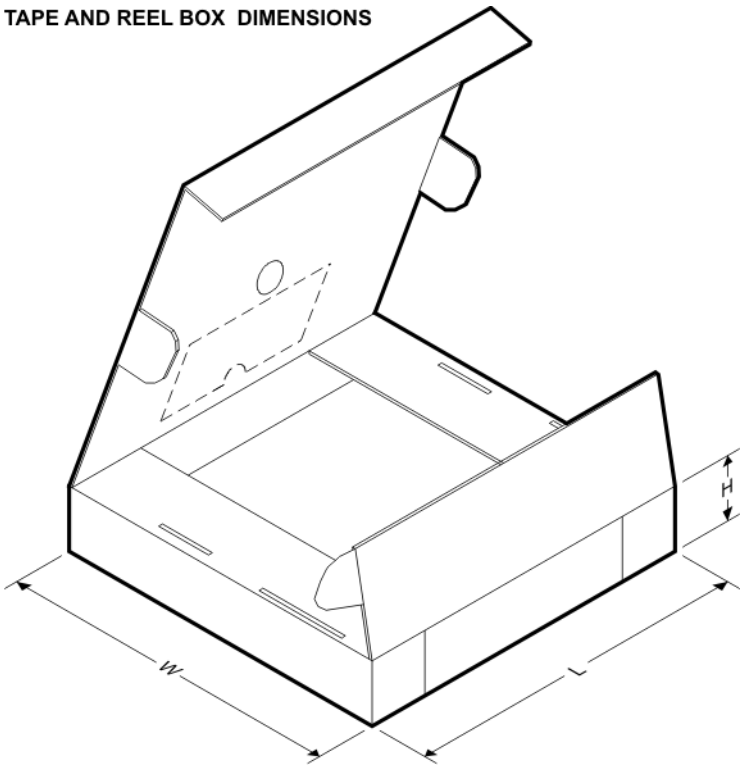
**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| PGA400QRHHTEP | VQFN | RHH | 36 | 250 | 180.0 | 16.4 | 6.3 | 6.3 | 1.1 | 12.0 | 16.0 | Q2 |

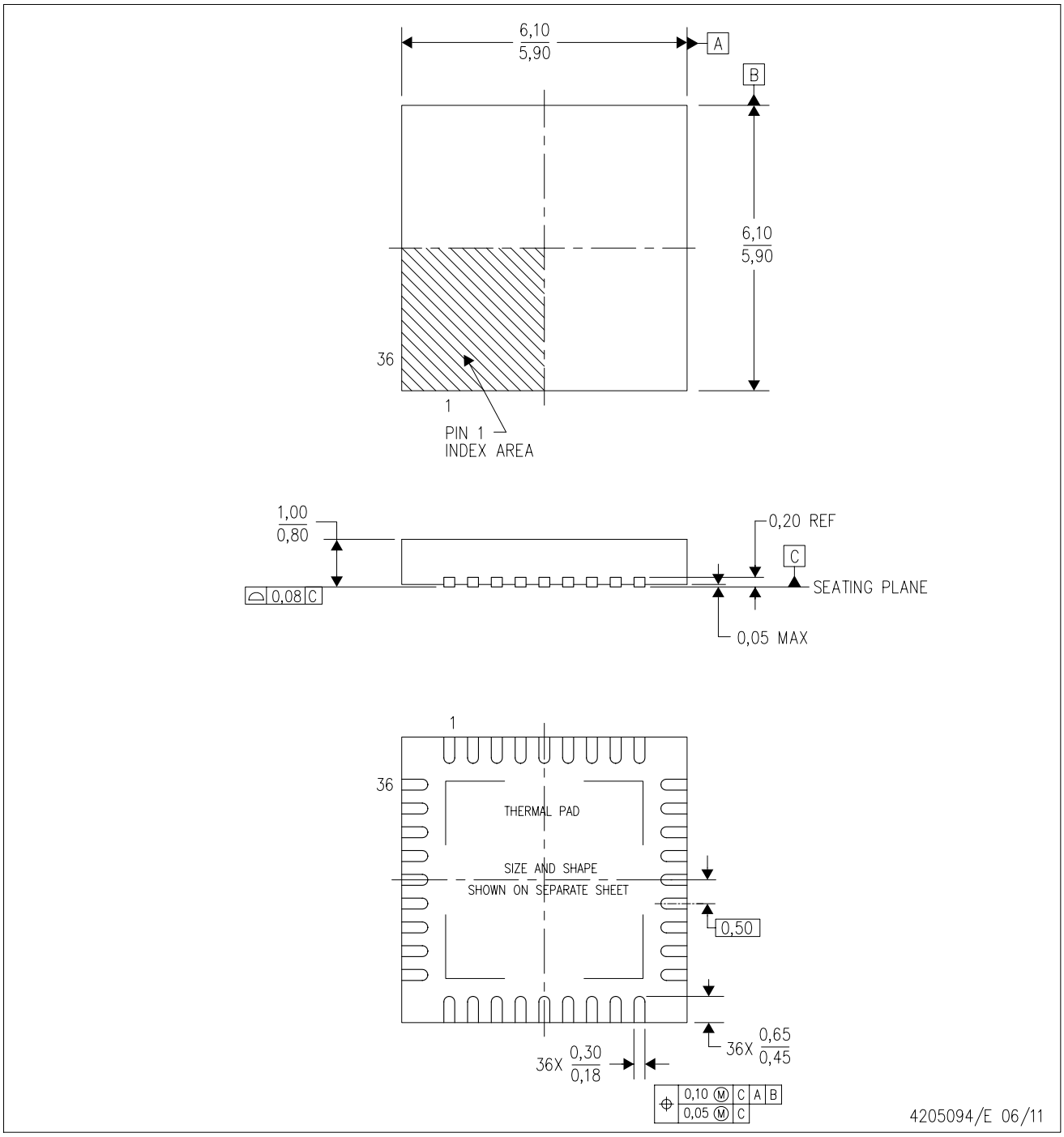
**TAPE AND REEL BOX DIMENSIONS**




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| PGA400QRHHTEP | VQFN | RHH | 36 | 250 | 210.0 | 185.0 | 35.0 |

RHH (S–PVQFN–N36) PLASTIC QUAD FLATPACK NO–LEAD




NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. QFN (Quad Flatpack No–Lead) Package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
F. Falls within JEDEC MO–220.

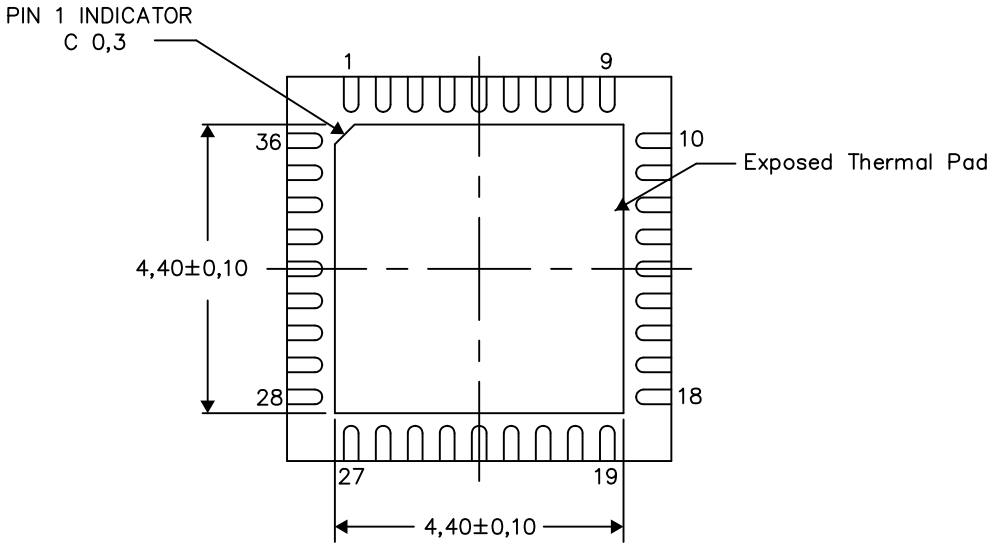
RHH (S–PVQFN–N36) PLASTIC QUAD FLATPACK NO–LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



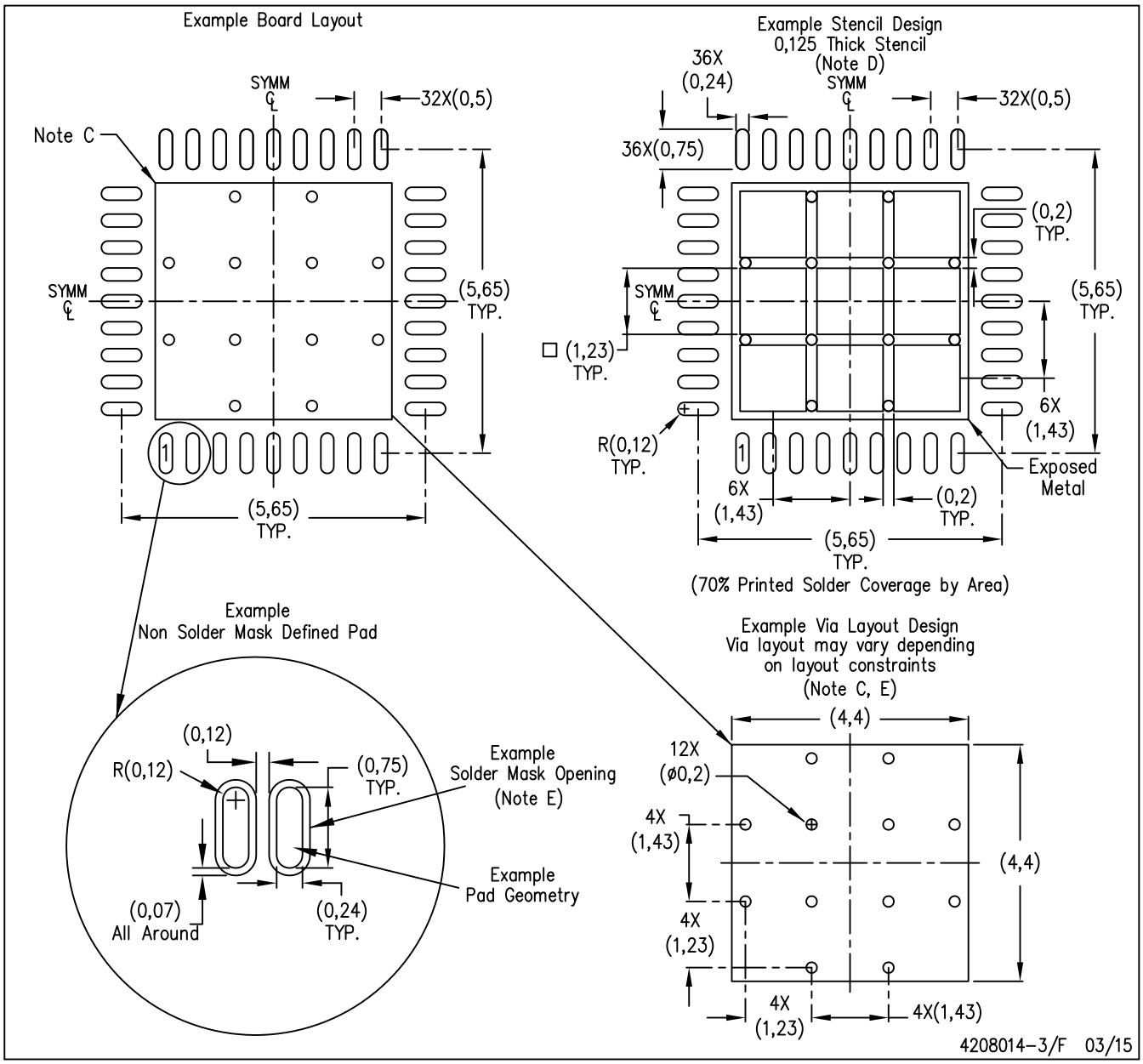

Bottom View

Exposed Thermal Pad Dimensions

4206362–5/M 11/13

NOTE: All linear dimensions are in millimeters

RHH (S-PVQFN-N36) PLASTIC QUAD FLATPACK NO-LEAD




NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat-Pack Packages, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
E. Customers should contact their board fabrication site for recommended solder mask tolerances and via tenting recommendations for any larger diameter vias placed in the thermal pad.

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