Triple, Wideband, Voltage-Feedback OPERATIONAL AMPLIFIER with Disable

Check for Samples: OPA3690

FEATURES

- **FLEXIBLE SUPPLY RANGE:**
  +5V to +12V Single Supply
  ±2.5V to ±6V Dual Supply
- **WIDEBAND +5V OPERATION: 220MHz (G = 2)**
- **HIGH OUTPUT CURRENT: 190mA**
- **OUTPUT VOLTAGE SWING: ±4.0V**
- **HIGH SLEW RATE: 1800V/μs**
- **LOW SUPPLY CURRENT: 5.5mA/ch**
- **LOW DISABLE CURRENT: 100μA/ch**

APPLICATIONS

- **VIDEO LINE DRIVING**
- **HIGH-SPEED IMAGING CHANNELS**
- **ADC BUFFERS**
- **PORTABLE INSTRUMENTS**
- **TRANSIMPEDANCE AMPLIFIERS**
- **ACTIVE FILTERS**

DESCRIPTION

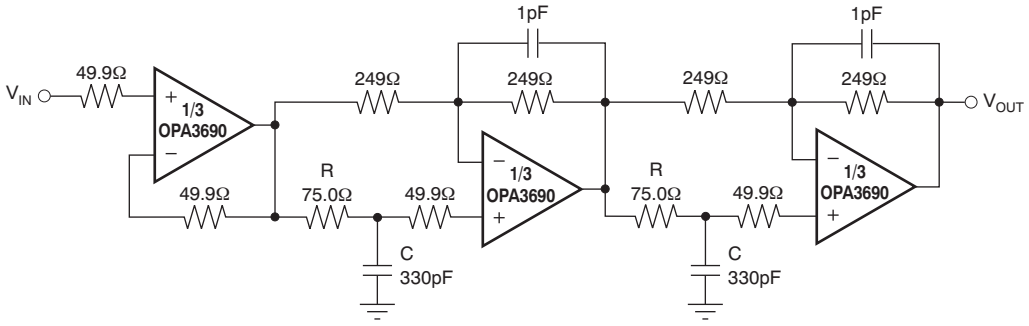
The OPA3690 represents a major step forward in unity-gain stable, voltage-feedback op amps. A new internal architecture provides slew rate and full-power bandwidth previously found only in wideband, current-feedback op amps. A new output stage architecture delivers high currents with a minimal headroom requirement. These give exceptional single-supply operation. Using a single +5V supply, the OPA3690 can deliver a 1V to 4V output swing with over 120mA drive current and 150MHz bandwidth. This combination of features makes the OPA3690 an ideal RGB line driver or single-supply Analog-to-Digital Converter (ADC) input driver.

The low 5.5mA/ch supply current of the OPA3690 is precisely trimmed at +25°C. This trim, along with low temperature drift, provides lower maximum supply current than competing products. System power may be reduced further using the optional disable control pin. Leaving this disable pin open, or holding it HIGH, will operate the OPA3690 normally. If pulled LOW, the OPA3690 supply current drops to less than 200μA/ch while the output goes to a high-impedance state. This feature may be used for power savings.

OPA3690 RELATED PRODUCTS

	SINGLES	DUALS	TRIPLES
Voltage-Feedback	OPA690	OPA2690	—
Current-Feedback	OPA691	OPA2691	OPA3691
Fixed Gain	OPA692	—	OPA3692

Buffered Analog Delay Line



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

ORDERING INFORMATION(1)

PRODUCT	PACKAGE-LEAD	PACKAGE DESIGNATOR	SPECIFIED TEMPERATURE RANGE	PACKAGE MARKING	ORDERING NUMBER	TRANSPORT MEDIA, QUANTITY
OPA3690	SO-16	D	–40°C to +85°C	OPA3690	OPA3690ID	Rails, 48
					OPA3690IDR	Tape and Reel, 2500
OPA3690	SSOP-16	DBQ	–40°C to +85°C	OPA3690	OPA3690IDBQT	Tape and Reel, 250
					OPA3690IDBQR	Tape and Reel, 2500

(1) For the most current package and ordering information, see the Package Option Addendum located at the end of this data sheet, or see the TI web site at www.ti.com.

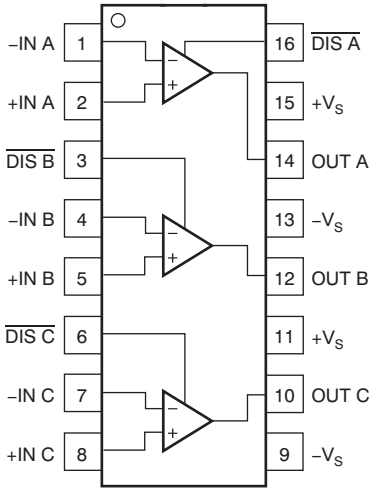
ABSOLUTE MAXIMUM RATINGS(1)

Over operating free-air temperature range, unless otherwise noted.

		OPA3690	UNIT
Power Supply		±6.5	V_{DC}
Internal Power Dissipation		See *Thermal Analysis* section	
Differential Input Voltage		±1.2	V
Input Voltage Range		$\pm V_S$	V
Storage Temperature Range: D, DBQ		–65 to +125	°C
Junction Temperature (T_J)		+150	°C
ESD Ratings	Human Body Model (HBM)	2000	V
	Charge Device Model (CDM)	1500	V
	Machine Model (MM)	200	V

(1) Stresses above these ratings may cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those specified is not supported.

D AND DBQ PACKAGES
SO-16 AND SSOP-16
(TOP VIEW)



ELECTRICAL CHARACTERISTICS: V_S = ±5V

Boldface limits are tested at **+25°C**.

At R_F = 402Ω for G = +2, (see Figure 36 for ac performance only), R_F = 25Ω for G = +1, and R_L = 100Ω, unless otherwise noted.

PARAMETER	TEST CONDITIONS	OPA3690ID, IDBQ						TEST LEVELS[1]
		TYP	MIN/MAX OVER TEMPERATURE			UNIT	MIN/ MAX	
		+25°C	+25°C[2]	0°C to +70°C[3]	-40°C to +85°C[3]			
AC PERFORMANCE (see Figure 36)								
Small-Signal Bandwidth	G = +1, V_O = 0.5V_{PP}, R_F = 25Ω	500				MHz	typ	C
	G = +2, V_O = 0.5V_{PP}	220	165	160	150	MHz	min	C
	G = +10, V_O = 0.5V_{PP}	30	20	19	18	MHz	min	C
Gain Bandwidth Product	G ≥ 10	300	200	190	180	MHz	min	C
Bandwidth for 0.1dB Gain Flatness	G = +2, V_O < 0.5V_{PP}	30				MHz	typ	C
Peaking at a Gain of +1	V_O < 0.5V_{PP}	4				dB	typ	C
Large-Signal Bandwidth	G = +2, V_O < 5V_{PP}	200				MHz	typ	C
Slew Rate	G = +2, 4V Step	1800	1400	1200	500	V/µs	min	C
Rise-and-Fall Time	G = +2, V_O = 0.5V Step	1.4				ns	max	C
	G = +2, V_O = 4V Step	2.8				ns	max	C
Settling Time to 0.02%	G = +2, V_O = 2V Step	12				ns	typ	C
Settling Time to 0.1%	G = +2, V_O = 2V Step	8				ns	typ	C
Harmonic Distortion	G = +2, f = 5MHz, V_O = 2V_{PP}							
2nd-Harmonic	R_L = 100Ω	–68	–64	–62	–60	dBc	typ	C
	R_L ≥ 500Ω	–77	–70	–68	–66	dBc	typ	C
3rd-Harmonic	R_L = 100Ω	–70	–68	–66	–64	dBc	typ	C
	R_L ≥ 500Ω	–81	–78	–76	–75	dBc	typ	C
Crosstalk	Input-Referred, f = 5MHz, All Hostile	–64				dBc	typ	C
Input Voltage Noise	f > 1MHz	5.5				nV/√Hz	typ	C
Input Current Noise	f > 1MHz	3.1				pA/√Hz	typ	C
Differential Gain	G = +2, NTSC, V_O = 1.4V_P, R_L = 150Ω	0.06				%	typ	C
Differential Phase	G = +2, NTSC, V_O = 1.4V_P, R_L = 150Ω	0.01				deg	typ	C
DC PERFORMANCE[4]								
Open-Loop Voltage Gain (A_{OL})	V_{OL} = 0V, R_L = 100Ω	69	**58**	56	54	dB	min	A
Input Offset Voltage	V_{CM} = 0V	±1.0	**±4.5**	±5.0	±5.2	mV	max	A
Average Offset Voltage Drift	V_{CM} = 0V			±12	±12	µV/°C	max	B
Input Bias Current	V_{CM} = 0V	+5	**±11**	±12	±13	µA	max	A
Average Bias Current Drift (magnitude)	V_{CM} = 0V			±20	±40	nA/°C	max	B
Input Offset Current	V_{CM} = 0V	±0.1	**±1.0**	±1.4	±1.6	µA	max	A
Average Offset Current Drift	V_{CM} = 0V			±7	±9	nA/°C	max	B
INPUT								
Common-Mode Input Range (CMIR)[5]		±3.5	**±3.4**	±3.3	±3.2	V	min	A
Common-Mode Rejection Ratio (CMRR)	V_{CM} = ±1V	65	**60**	57	56	dB	min	A
Input Impedance								
Differential Mode		190 || 0.6				kΩ || pF	typ	C
Common-Mode		3.2 || 0.9				MΩ || pF	typ	C

(1) Test levels: **(A)** 100% tested at +25°C. Over temperature limits by characterization and simulation. **(B)** Limits set by characterization and simulation. **(C)** Typical value only for information.
(2) Junction temperature = ambient for +25°C specifications.
(3) Junction temperature = ambient at low temperature limits; junction temperature = ambient +20°C at high temperature limit for over temperature specifications.
(4) Current is considered positive out-of-node. V_{CM} is the input common-mode voltage.
(5) Tested < 3dB below minimum specified CMRR at ±CMIR limits.

ELECTRICAL CHARACTERISTICS: V_S = ±5V (continued)

Boldface limits are tested at **+25°C**.

At R_F = 402Ω for G = +2, (see Figure 36 for ac performance only), R_F = 25Ω for G = +1, and R_L = 100Ω, unless otherwise noted.

PARAMETER	TEST CONDITIONS	OPA3690ID, IDBQ						TEST LEVELS[1]
		TYP	MIN/MAX OVER TEMPERATURE			UNIT	MIN/ MAX	
		+25°C	+25°C[2]	0°C to +70°C[3]	-40°C to +85°C[3]			
OUTPUT								
Voltage Output Swing	No Load	±4.0	**±3.8**	±3.7	±3.6	V	min	A
	100Ω Load	±3.9	**±3.7**	±3.6	±3.3	V	min	A
Current Output, Sourcing	V_O = 0V	+190	**+160**	+140	+100	mA	min	A
Current Output, Sinking	V_O = 0V	–190	**–160**	–140	–100	mA	min	A
Short-Circuit Current	V_O = 0V	±250				mA	typ	C
Closed-Loop Output Impedance	G = +2, f = 100kHz	0.04				Ω	typ	C
DISABLE	Disabled LOW							
Power-Down Supply Current (+V_S)	$V_{\overline{DIS}}$ = 0V, All Channels	–300	**–600**	–720	–780	µA	max	A
Disable Time	V_{IN} = 1V_{DC}	200				ns	typ	C
Enable Time	V_{IN} = 1V_{DC}	25				ns	typ	C
Off Isolation	G = +2, 5MHz	70				dB	typ	C
Output Capacitance in Disable		4				pF	typ	C
Turn-On Glitch	G = +2, R_L = 150Ω, V_{IN} = 0V	±50				mV	typ	C
Turn-Off Glitch	G = +2, R_L = 150Ω, V_{IN} = 0V	±20				mV	typ	C
Enable Voltage		3.3	**3.5**	3.6	3.7	V	min	A
Disable Voltage		1.8	**1.7**	1.6	1.5	V	max	A
Control Pin Input BIas Current	$V_{\overline{DIS}}$ = 0V, Each Channel	75	**130**	150	160	µA	max	A
POWER SUPPLY								
Specified Operating Voltage		±5				V	typ	C
Maximum Operating Voltage Range			**±6.0**	±6.0	±6.0	V	max	A
Maximum Quiescent Current (3 Channels)	V_S = ±5V	16.5	**17.4**	18.6	19.8	mA	max	A
Minimum Quiescent Current (3 Channels)	V_S = ±5V	16.5	**15.9**	13.8	12.9	mA	min	A
Power-Supply Rejection Ratio (+PSRR)	Input-Referred	75	**68**	66	64	dB	min	A
THERMAL CHARACTERISTICS								
Specified Operating Range: D, DBQ		–40 to +85				°C	typ	C
Thermal Resistance, θ_{JA}								
D SO-16		100				°C/W	typ	C
DBQ SSOP-16		100				°C/W	typ	C

ELECTRICAL CHARACTERISTICS: V_S = +5V

Boldface limits are tested at **+25°C**.

At R_F = 402Ω for G = +2 (see Figure 37 for ac performance only), R_F = 25Ω for G = +1, and R_L = 100Ω to V_S/2, unless otherwise noted.

PARAMETER	TEST CONDITIONS	OPA3690ID, IDBQ						TEST LEVELS(1)
		TYP	MIN/MAX OVER TEMPERATURE			UNIT	MIN/ MAX	
		+25°C	+25°C(2)	0°C to +70°C(3)	-40°C to +85°C(3)			
AC PERFORMANCE (see Figure 37)								
Small-Signal Bandwidth	G = +1, V_O < 0.5V_{PP}	400				MHz	typ	C
	G = +2, V_O < 0.5V_{PP}	190	150	145	140	MHz	min	C
	G = +10, V_O < 0.5V_{PP}	25	18	17	16	MHz	min	C
Gain Bandwidth Product	G ≥ 10	250	180	170	160	MHz	min	C
Bandwidth for 0.1dB Gain Flatness	G = +2, V_O < 0.5V_{PP}	20				MHz	typ	C
Peaking at a Gain of +1	V_O < 0.5V_{PP}	5				dB	typ	C
Large-Signal Bandwidth	G = +2, V_O = 2V_{PP}	220				MHz	typ	C
Slew Rate	G = +2, 2V Step	1000	700	670	550	V/µs	min	C
Rise Time	G = +2, V_O = 0.5V Step	1.6				ns	typ	C
Fall Time	G = +2, V_O = 2V Step	2.0				ns	typ	C
Settling Time to 0.02%	G = +2, V_O = 2V Step	12				ns	typ	C
Settling Time to 0.1%	G = +2, V_O = 2V Step	8				ns	typ	C
Harmonic Distortion	G = +2, f = 5MHz, V_O = 2V_{PP}							
2nd-Harmonic	R_L = 100Ω	–65	–60	–59	–56	dBc	typ	C
	R_L ≥ 500Ω	–75	–70	–68	–66	dBc	typ	C
3rd-Harmonic	R_L = 100Ω	–68	–64	–62	–60	dBc	typ	C
	R_L ≥ 500Ω	–77	–73	–71	–70	dBc	typ	C
Input Voltage Noise	f > 1MHz	5.6				nV/√Hz	typ	C
Input Current Noise	f > 1MHz	3.2				pA/√Hz	typ	C
Differential Gain	G = +2, NTSC, V_O = 1.4V_P, R_L = 150Ω to V_S/2	0.06				%	typ	C
Differential Phase	G = +2, NTSC, V_O = 1.4V_P, R_L = 150Ω to V_S/2	0.02				deg	typ	C
DC PERFORMANCE(4)								
Open-Loop Voltage Gain (A_{OL})	V_O = 0V, R_L = 100Ω	63	**56**	54	52	dB	min	A
Input Offset Voltage	V_{CM} = 2.5V	±1.0	**±4.5**	±4.8	±5.2	mV	max	A
Average Offset Voltage Drift	V_{CM} = 2.5V			±10	±10	µV/°C	max	B
Input Bias Current	V_{CM} = 2.5V	+5	**±11**	±12	±13	µA	max	A
Average Bias Current Drift (magnitude)	V_{CM} = 2.5V			±20	±40	nA/°C	max	B
Input Offset Current	V_{CM} = 2.5V	±0.3	**±1.0**	±1.4	±1.6	µA	max	A
Average Offset Current Drift	V_{CM} = 2.5V			±7	±9	nA/°C	max	B
INPUT								
Least Positive Input Voltage(5)		1.5	**1.6**	1.7	1.8	V	min	A
Most Positive Input Voltage(5)		3.5	**3.4**	3.3	3.2	V	max	A
Common-Mode Rejection Ratio (CMRR)	V_{CM} = 2.5V	63	**58**	56	54	dB	min	A
Input Impedance								
Differential Mode		92 || 1.4				kΩ || pF	typ	C
Common-Mode		2.2 || 1.5				MΩ || pF	typ	C

(1) Test levels: **(A)** 100% tested at +25°C. Over temperature limits by characterization and simulation. **(B)** Limits set by characterization and simulation. **(C)** Typical value only for information.
(2) Junction temperature = ambient for +25°C specifications.
(3) Junction temperature = ambient at low temperature limits; junction temperature = ambient +20°C at high temperature limit for over temperature specifications.
(4) Current is considered positive out of node. V_{CM} is the input common-mode voltage.
(5) Tested < 3dB below minimum specified CMRR at ±CMIR limits.

ELECTRICAL CHARACTERISTICS: V_S = +5V (continued)

Boldface limits are tested at **+25°C**.

At R_F = 402Ω for G = +2 (see Figure 37 for ac performance only), R_F = 25Ω for G = +1, and R_L = 100Ω to V_S/2, unless otherwise noted.

PARAMETER	TEST CONDITIONS	OPA3690ID, IDBQ						TEST LEVELS[1]
		TYP	MIN/MAX OVER TEMPERATURE			UNIT	MIN/ MAX	
		+25°C	+25°C[2]	0°C to +70°C[3]	-40°C to +85°C[3]			
OUTPUT								
Most Positive Output Voltage	No Load	4	**3.8**	3.6	3.5	V	min	A
	R_L = 100Ω to 2.5V	3.9	**3.7**	3.5	3.4	V	min	A
Least Positive Output Voltage	No Load	1	**1.2**	1.4	1.5	V	min	A
	R_L = 100Ω to 2.5V	1.1	**1.3**	1.5	1.7	V	min	A
Current Output, Sourcing		+160	**+120**	+100	+80	mA	min	A
Current Output, Sinking		–160	**–120**	–100	–80	mA	min	A
Short-Circuit Current	$V_O = V_S/2$	±250				mA	typ	C
Closed-Loop Output Impedance	G = +2, f = 100kHz	0.04				Ω	typ	C
DISABLE	Disabled LOW							
Power-Down Supply Current (+V_S)	$V_{\overline{DIS}}$ = 0V, All Channels	–300	**–600**	–720	–780	µA	max	A
Off Isolation	G = +2, 5MHz	65				dB	typ	C
Output Capacitance in Disable		4				pF	typ	C
Turn-On Glitch	G = +2, R_L = 150Ω, $V_{IN} = V_S/2$	±50				mV	typ	C
Turn-Off Glitch	G = +2, R_L = 150Ω, $V_{IN} = V_S/2$	±20				mV	typ	C
Enable Voltage		3.3	**3.5**	3.6	3.7	V	min	A
Disable Voltage		1.8	**1.7**	1.6	1.5	V	max	A
Control Pin Input BIas Current	$V_{\overline{DIS}}$ = 0V, Each Channel	75	130	150	160	µA	typ	C
POWER SUPPLY								
Specified Single-Supply Operating Voltage		5				V	typ	C
Maximum Single-Supply Operating Voltage			**12**	12	12	V	max	A
Maximum Quiescent Current (3 Channels)	V_S = +5V	14.7	**16.32**	17.16	18.06	mA	max	A
Minimum Quiescent Current (3 Channels)	V_S = +5V	14.7	**13.44**	12.00	11.58	mA	min	A
Power-Supply Rejection Ratio (+PSRR)	Input-Referred	72				dB	typ	C
THERMAL CHARACTERISTICS								
Specification: D, DBQ		–40 to +85				°C	typ	C
Thermal Resistance, θ_{JA}								
D SO-16		100				°C/W	typ	C
DBQ SSOP-16		100				°C/W	typ	C

TYPICAL CHARACTERISTICS: V_S = ±5V

At T_A = +25°C, G = +2, R_F = 402Ω, and R_L = 100Ω (see Figure 36 for ac performance only), unless otherwise noted.

SMALL−SIGNAL FREQUENCY RESPONSE

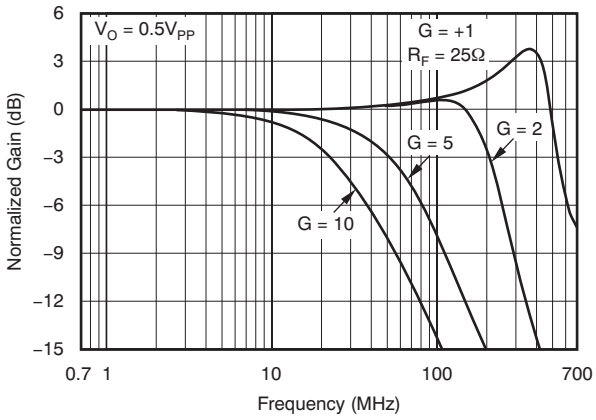


Figure 1.

LARGE−SIGNAL FREQUENCY RESPONSE

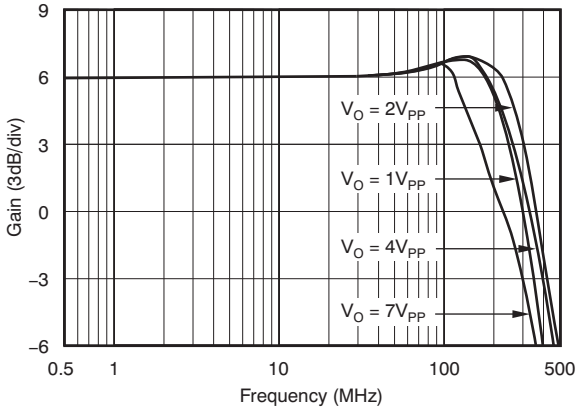


Figure 2.

SMALL-SIGNAL PULSE RESPONSE

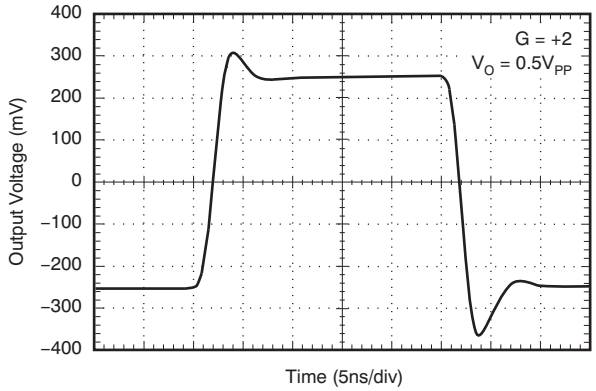


Figure 3.

LARGE-SIGNAL PULSE RESPONSE

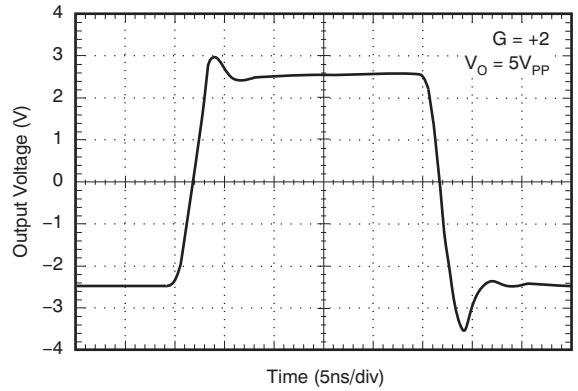


Figure 4.

COMPOSITE VIDEO dG/dP

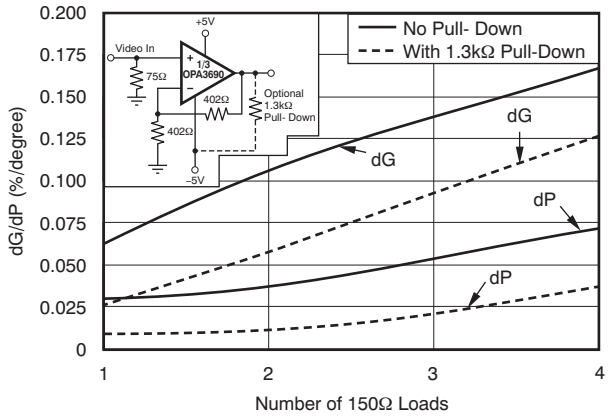


Figure 5.

ALL HOSTILE CROSSTALK

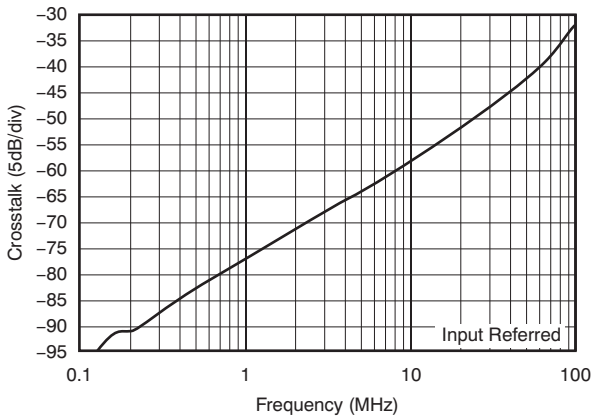


Figure 6.

TYPICAL CHARACTERISTICS: V_S = ±5V (continued)

At T_A = +25°C, G = +2, R_F = 402Ω, and R_L = 100Ω (see Figure 36 for ac performance only), unless otherwise noted.

HARMONIC DISTORTION vs LOAD RESISTANCE

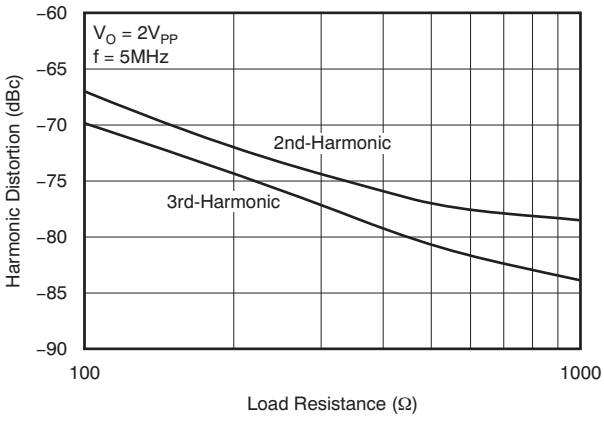


Figure 7.

5MHz HARMONIC DISTORTION vs SUPPLY VOLTAGE

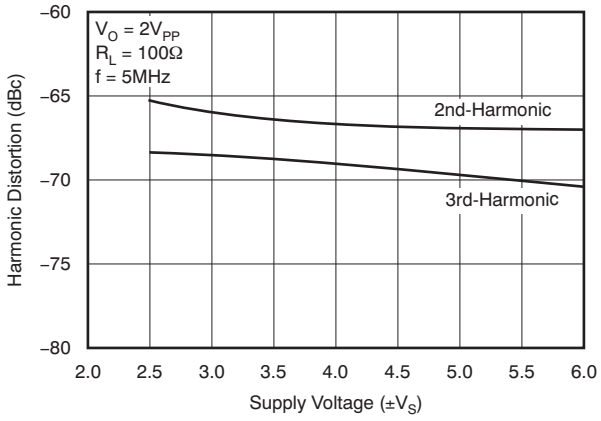


Figure 8.

HARMONIC DISTORTION vs FREQUENCY

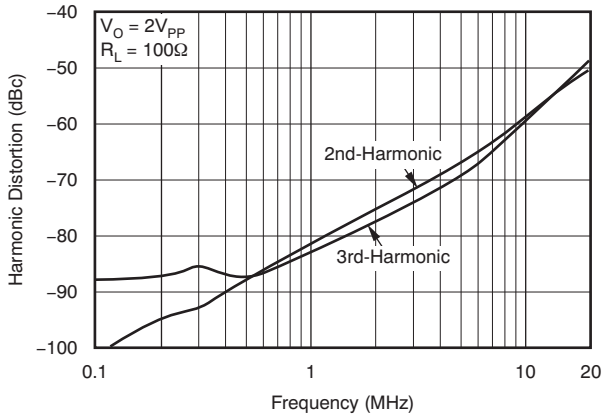


Figure 9.

HARMONIC DISTORTION vs OUTPUT VOLTAGE

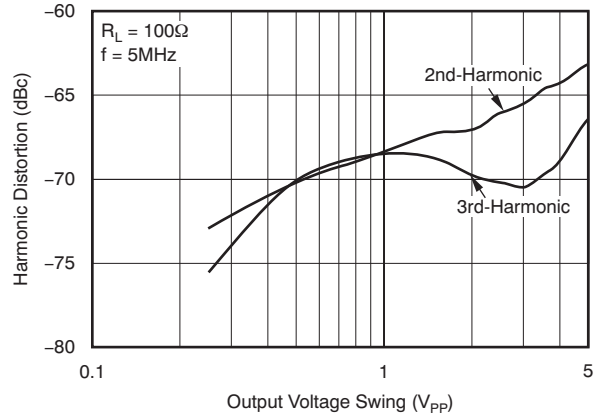


Figure 10.

HARMONIC DISTORTION vs NONINVERTING GAIN

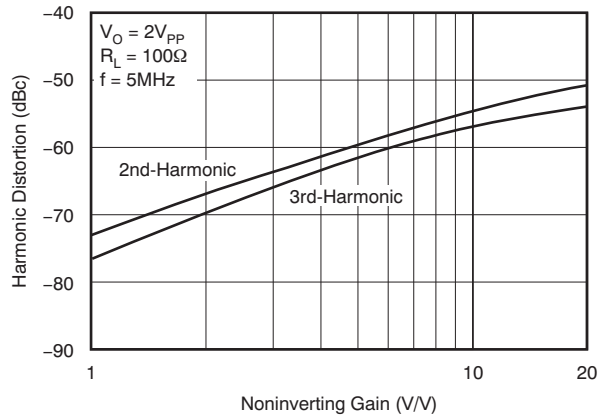


Figure 11.

HARMONIC DISTORTION vs INVERTING GAIN

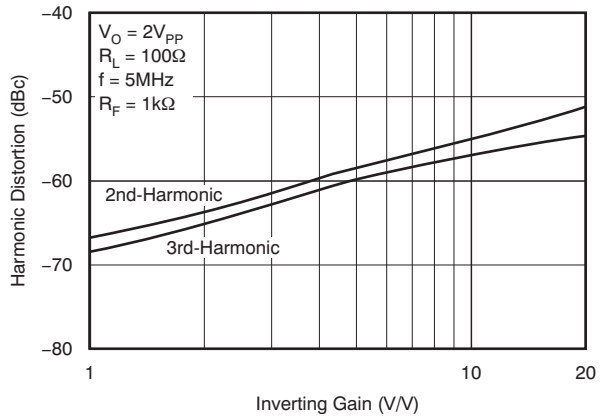


Figure 12.

TYPICAL CHARACTERISTICS: V_S = ±5V (continued)

At T_A = +25°C, G = +2, R_F = 402Ω, and R_L = 100Ω (see Figure 36 for ac performance only), unless otherwise noted.

INPUT VOLTAGE AND CURRENT NOISE DENSITY

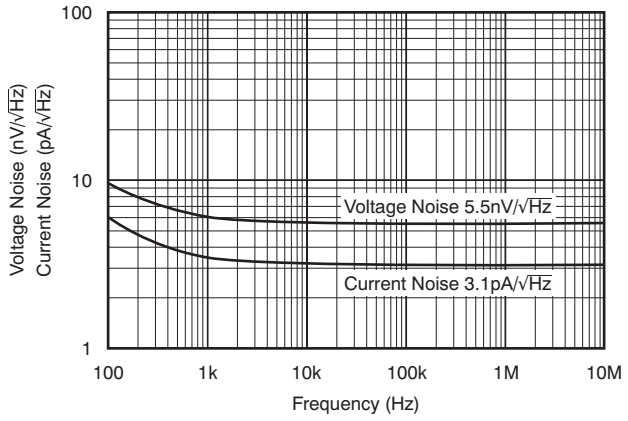


Figure 13.

TWO-TONE, 3RD-ORDER INTERMODULATION SPURIOUS

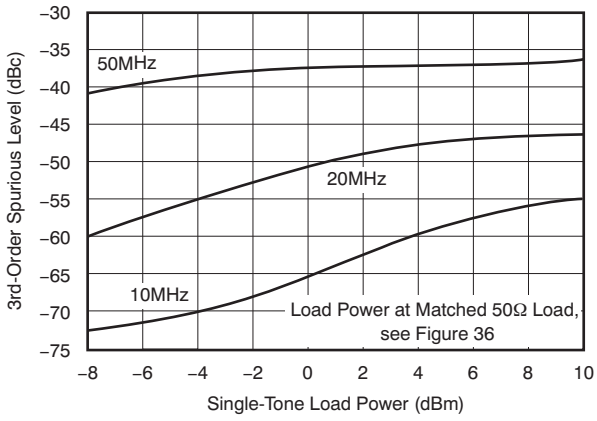


Figure 14.

RECOMMENDED R_S vs CAPACITIVE LOAD

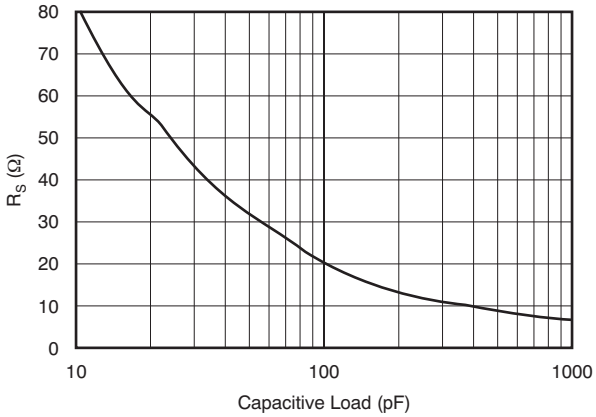


Figure 15.

FREQUENCY RESPONSE vs CAPACITIVE LOAD

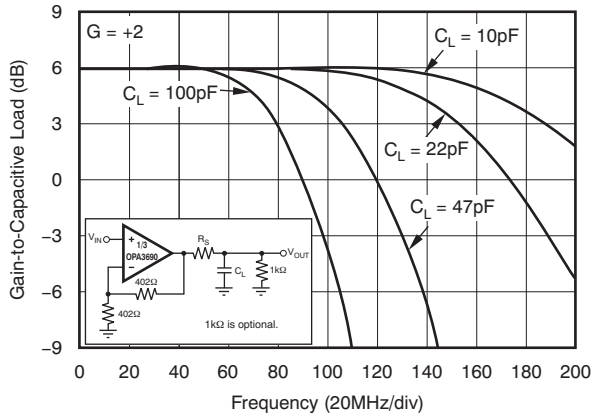


Figure 16.

LARGE-SIGNAL ENABLE/DISABLE RESPONSE

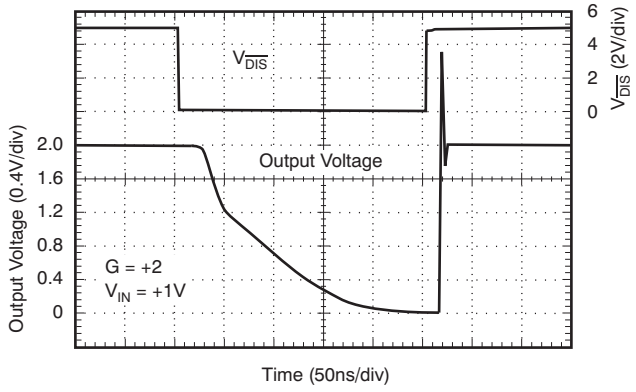


Figure 17.

DISABLE FEEDTHROUGH vs FREQUENCY

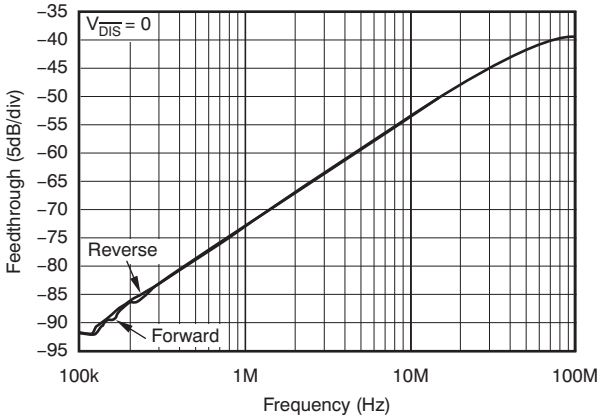


Figure 18.

TYPICAL CHARACTERISTICS: V_S = ±5V (continued)

At T_A = +25°C, G = +2, R_F = 402Ω, and R_L = 100Ω (see Figure 36 for ac performance only), unless otherwise noted.

OUTPUT VOLTAGE AND CURRENT LIMITATIONS

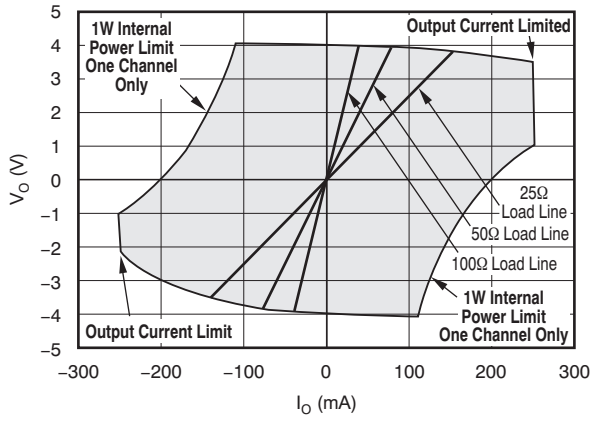


Figure 19.

TYPICAL DC DRIFT OVER TEMPERATURE

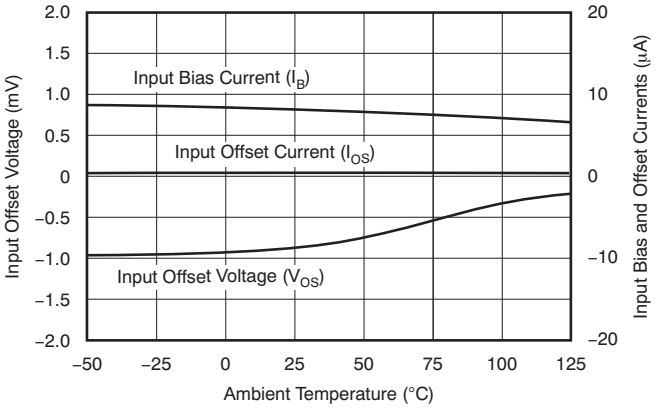


Figure 20.

COMMON−MODE REJECTION RATIO AND POWER−SUPPLY REJECTION RATIO vs FREQUENCY

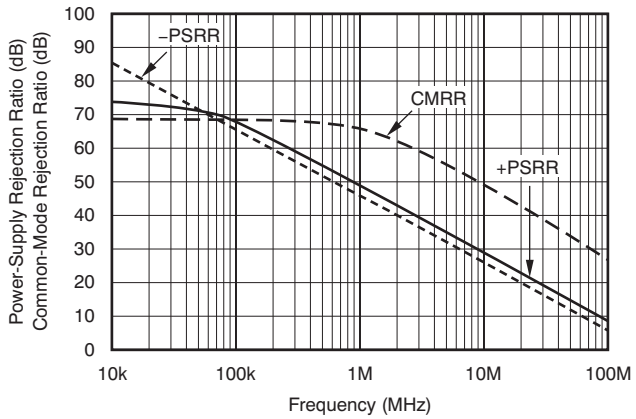


Figure 21.

SUPPLY AND OUTPUT CURRENTS vs TEMPERATURE

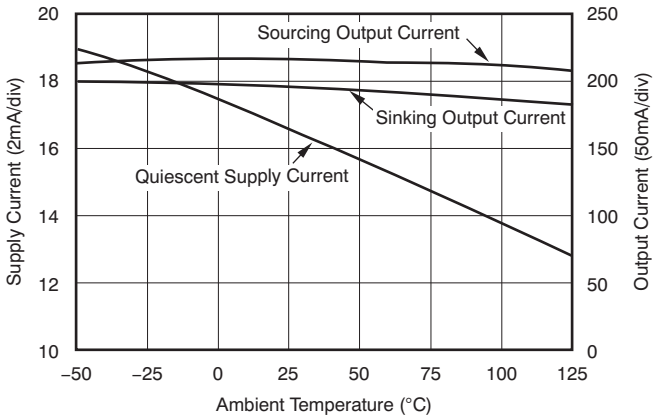


Figure 22.

CLOSED-LOOP OUTPUT IMPEDANCE vs FREQUENCY

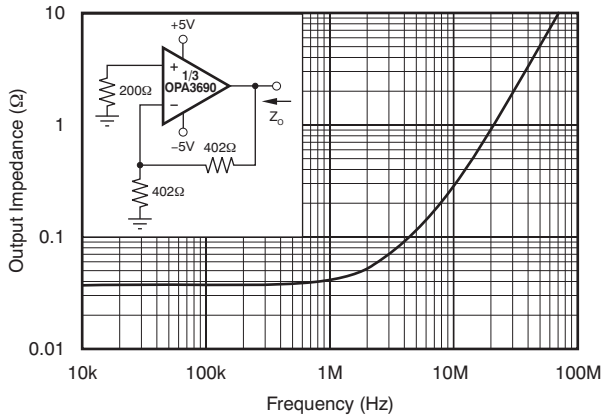


Figure 23.

OPEN-LOOP GAIN AND PHASE

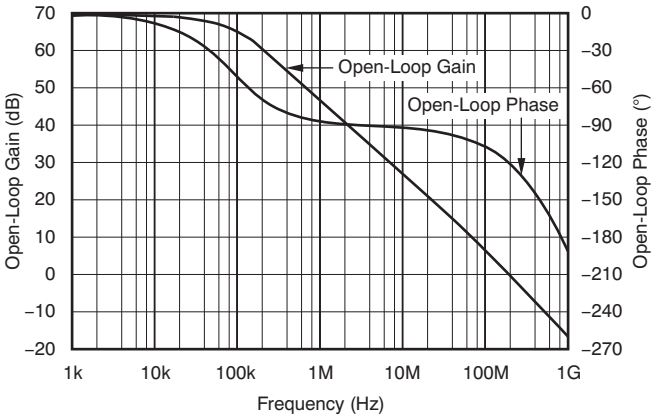


Figure 24.

TYPICAL CHARACTERISTICS: V_S = ±5V (continued)

At T_A = +25°C, G = +2, R_F = 402Ω, and R_L = 100Ω (see Figure 36 for ac performance only), unless otherwise noted.

NONINVERTING OVERDRIVE RECOVERY

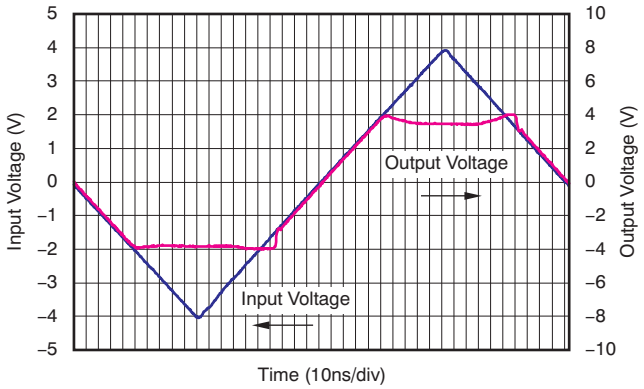


Figure 25.

TYPICAL CHARACTERISTICS: +5V

At T_A = +25°C, G = +2, R_F = 402Ω, and R_L = 100Ω (see Figure 37 for ac performance only), unless otherwise noted.

SMALL−SIGNAL FREQUENCY RESPONSE

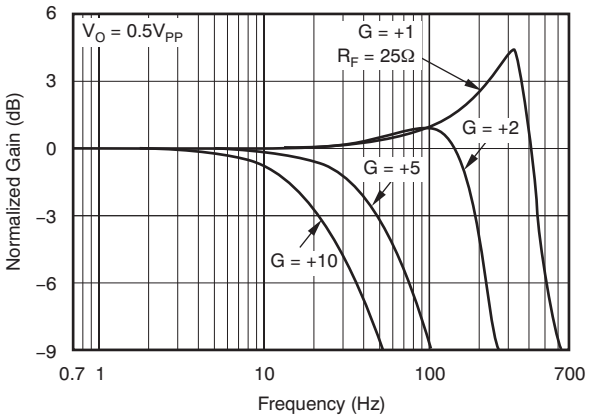


Figure 26.

LARGE−SIGNAL FREQUENCY RESPONSE

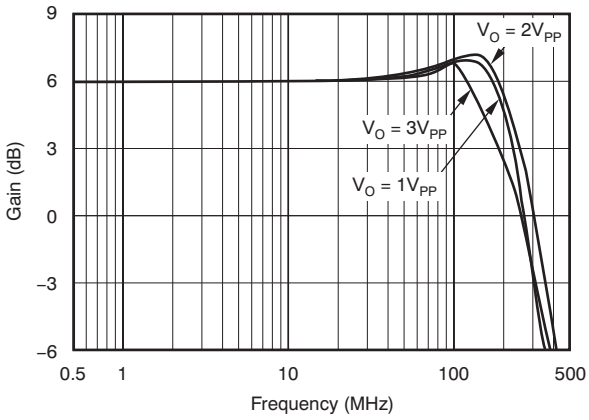


Figure 27.

SMALL-SIGNAL PULSE RESPONSE

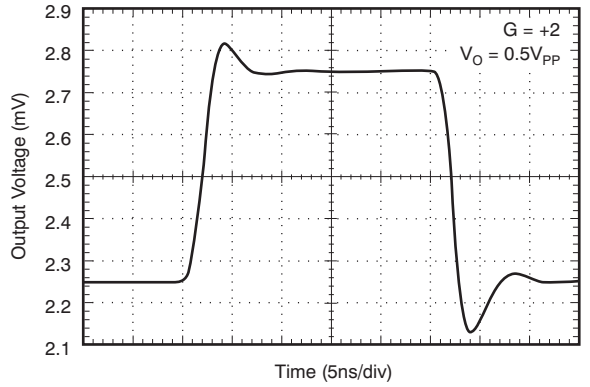


Figure 28.

LARGE-SIGNAL PULSE RESPONSE

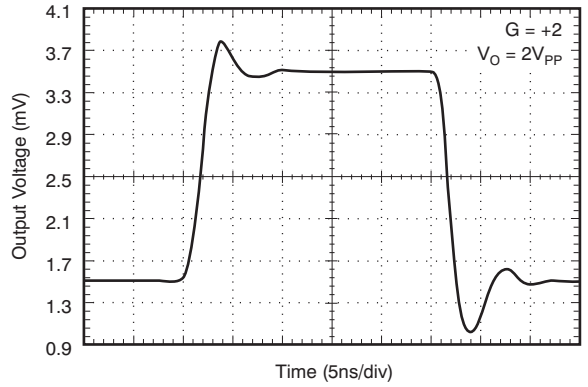


Figure 29.

RECOMMENDED R_S vs CAPACITIVE LOAD

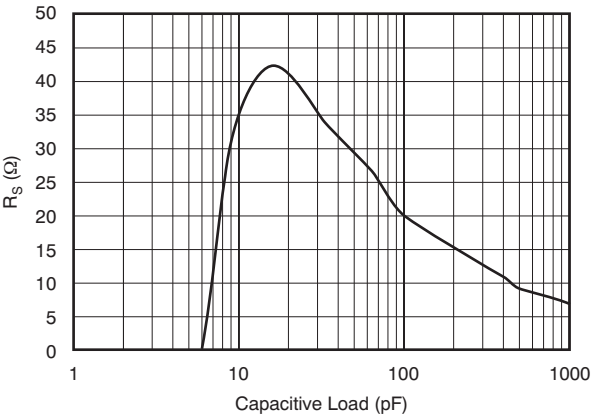


Figure 30.

FREQUENCY RESPONSE vs CAPACITIVE LOAD

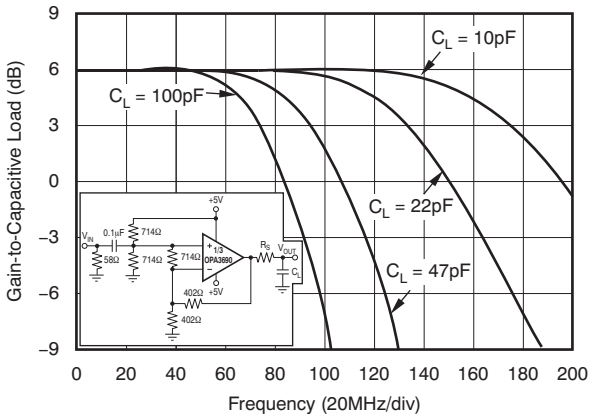


Figure 31.

TYPICAL CHARACTERISTICS: +5V (continued)

At T_A = +25°C, G = +2, R_F = 402Ω, and R_L = 100Ω (see Figure 37 for ac performance only), unless otherwise noted.

HARMONIC DISTORTION vs LOAD RESISTANCE

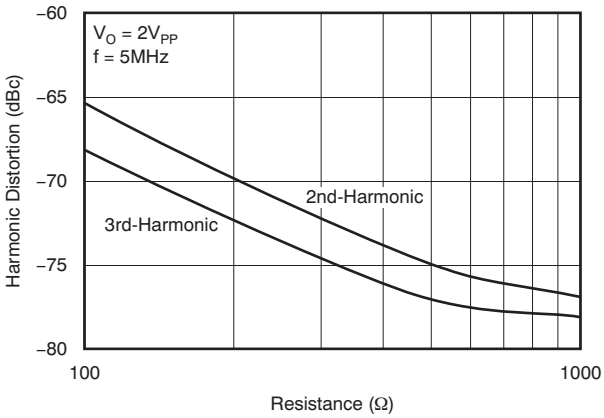


Figure 32.

HARMONIC DISTORTION vs FREQUENCY

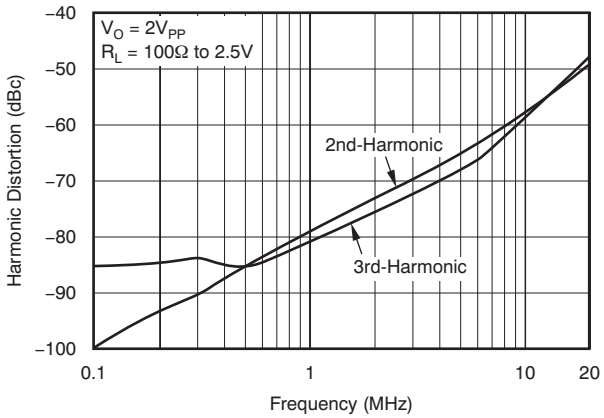


Figure 33.

HARMONIC DISTORTION vs OUTPUT VOLTAGE

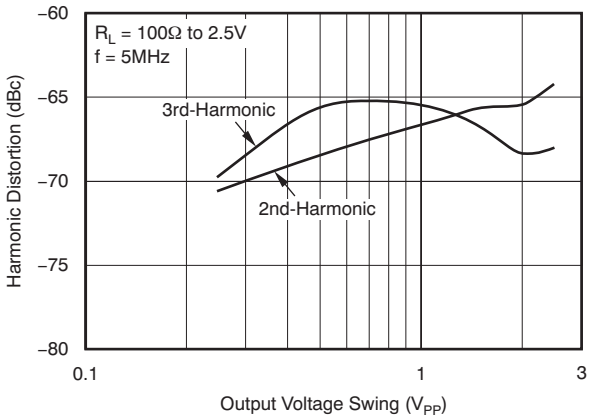


Figure 34.

TWO-TONE, 3RD-ORDER INTERMODULATION SPURIOUS

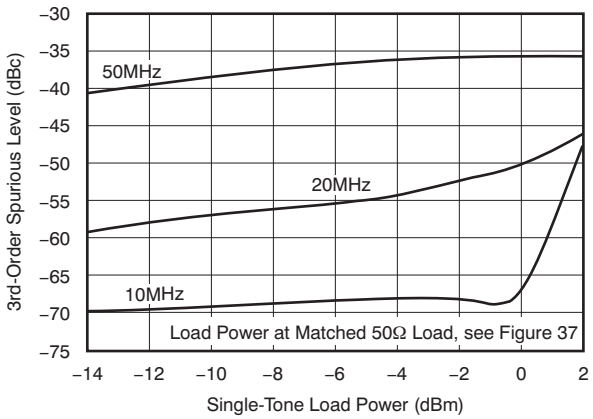


Figure 35.

APPLICATION INFORMATION

WIDEBAND VOLTAGE-FEEDBACK OPERATION

The OPA3690 provides an exceptional combination of high output power capability in a wideband, unity-gain stable voltage-feedback op amp using a new high slew rate input stage. Typical differential input stages used for voltage feedback op amps are designed to steer a fixed-bias current to the compensation capacitor, setting a limit to the achievable slew rate. The OPA3690 uses a new input stage that places the transconductance element between two input buffers, using their output currents as the forward signal. As the error voltage increases across the two inputs, an increasing current is delivered to the compensation capacitor. This provides very high slew rate (1800V/μs) while consuming relatively low quiescent current (5.5mA). This exceptional, full-power performance comes at the price of a slightly higher input noise voltage than alternative architectures. The 5.5nV/√Hz input voltage noise for the OPA3690 is exceptionally low for this type of input stage.

Figure 36 shows the dc-coupled, gain of +2, dual power supply circuit configuration used as the basis of the ±5V *Electrical Characteristics* and *Typical Characteristics*. For test purposes, the input impedance is set to 50Ω with a resistor to ground and the output impedance is set to 50Ω with a series output resistor. Voltage swings reported in the Electrical Characteristics are taken directly at the input and output pins, while output powers (dBm) are at the matched 50Ω load. For the circuit of Figure 36, the total effective load will be 100Ω || 804Ω. The disable control line is typically left open for normal amplifier operation. Two optional components are included in Figure 36. An additional resistor (100Ω) is included in series with the noninverting input. Combined with the 25Ω dc source resistance looking back towards the signal generator, this gives an input bias current cancelling resistance that matches the 125Ω source resistance seen at the inverting input (see the *DC Accuracy and Offset Control* section). In addition to the usual power-supply decoupling capacitors to ground, a 0.1μF capacitor is included between the two power-supply pins. In practical printed circuit board (PCB) layouts, this optional-added capacitor will typically improve the 2nd-harmonic distortion performance by 3dB to 6dB.

Figure 37 shows the ac-coupled, gain of +2, single-supply circuit configuration used as the basis of the +5V *Electrical Characteristics* and *Typical Characteristics*. Though not a rail-to-rail design, the OPA3690 requires minimal input and output voltage headroom compared to other very wideband voltage-feedback op amps. It will deliver a $3V_{PP}$ output swing on a single +5V supply with > 150MHz bandwidth. The key requirement of broadband single-supply operation is to maintain input and output signal swings within the usable voltage ranges at both the input and the output. The circuit of Figure 37 establishes an input midpoint bias using a simple resistive divider from the +5V supply (two 698Ω resistors). The input signal is then ac-coupled into the midpoint voltage bias. The input voltage can swing to within 1.5V of either supply pin, giving a $2V_{PP}$ input signal range centered between the supply pins. The input impedance matching resistor (59Ω) used for testing is adjusted to give a 50Ω input load when the parallel combination of the biasing divider network is included.

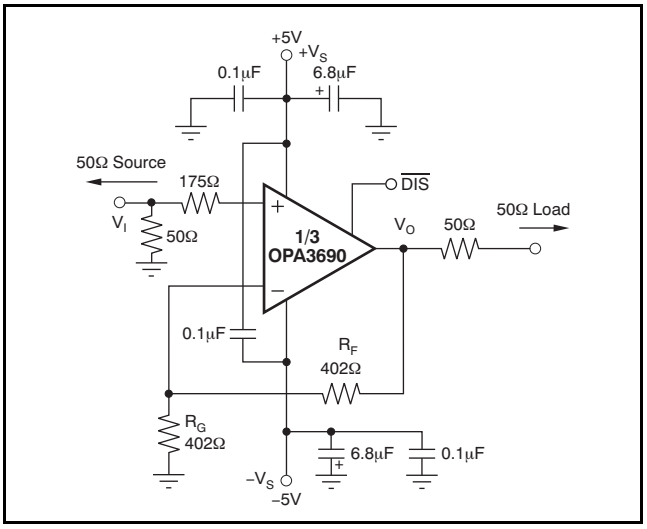


Figure 36. DC-Coupled, G = +2, Bipolar-Supply Specification and Test Circuit

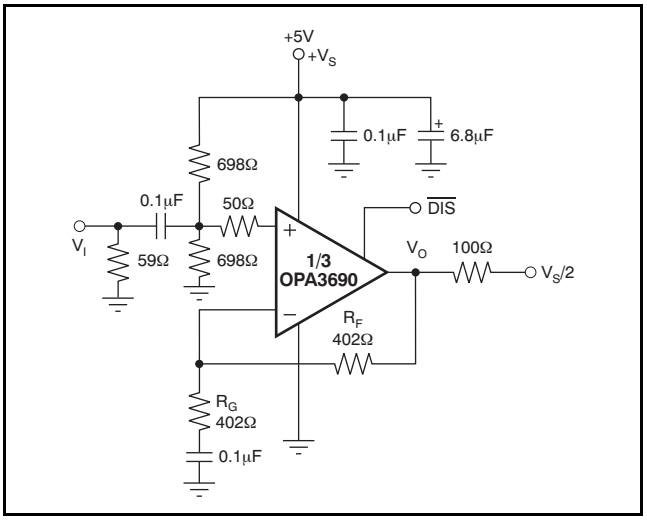


Figure 37. AC-Coupled, G = +2, Single-Supply Specification and Test Circuit

Again, an additional resistor (50Ω in this case) is included directly in series with the noninverting input. This minimum recommended value provides part of the dc source resistance matching for the noninverting input bias current. It is also used to form a simple parasitic pole to roll off the frequency response at very high frequencies (> 500MHz) using the input parasitic capacitance to form a bandlimiting pole. The gain resistor (R_G) is ac-coupled, giving the circuit a dc gain of +1, which puts the input dc bias voltage (2.5V) on the output as well. The output voltage can swing to within 1V of either supply pin while delivering > 100mA output current. A demanding 100Ω load to a midpoint bias is used in this characterization circuit. The new output stage circuit used in the OPA3690 can deliver large bipolar output currents into this midpoint load with minimal crossover distortion, as shown in the ±5V supply harmonic distortion plots.

SINGLE-SUPPLY ADC INTERFACE

Most modern, high-performance ADCs (such as the TI ADS8xx and ADS9xx series from Texas Instruments) operate on a single +5V (or lower) power supply. It has been a considerable challenge for single-supply op amps to deliver a low distortion input signal at the ADC input for signal frequencies exceeding 5MHz. The high slew rate, exceptional output swing, and high linearity of the OPA3690 make it an ideal single-supply ADC driver. The circuit on the front page shows one possible interface particularly suited to differential I/O, ac-coupled requirements. Figure 39 shows the test circuit of Figure 37 modified for a capacitive (ADC) load and with an optional output pull-down resistor (R_B). This circuit would be suitable to dual-channel ADC driving with a single-ended I/O.

The OPA3690 in the circuit of Figure 39 provides > 200MHz bandwidth for a $2V_{PP}$ output swing. Minimal 3rd-harmonic distortion or two-tone, 3rd-order intermodulation distortion will be observed due to the very low crossover distortion in the OPA3690 output stage. The limit of output Spurious-Free Dynamic Range (SFDR) will be set by the 2nd-harmonic distortion. Without R_B, the circuit of Figure 39 measured at 10MHz shows an SFDR of 57dBc. This may be improved by pulling additional dc bias current (I_B) out of the output stage through the optional R_B resistor to ground (the output midpoint is at 2.5V for Figure 39). Adjusting I_B gives the improvement in SFDR shown in Figure 38. SFDR improvement is achieved for I_B values up to 5mA, with worse performance for higher values. Using the dual OPA3690 in an I/Q receiver channel will give matched ac performance through high frequencies.

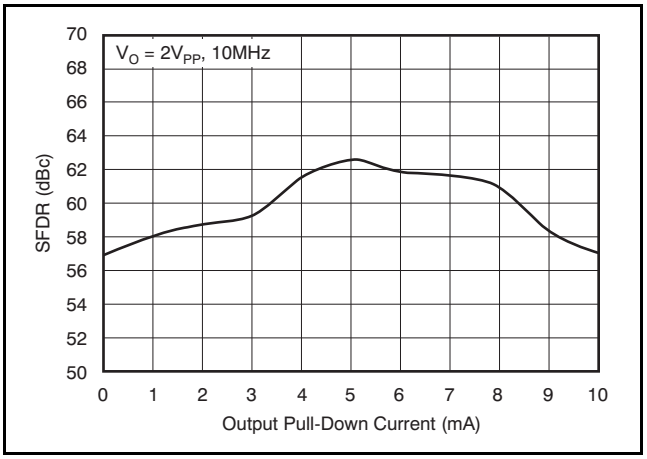


Figure 38. SFDR vs I_B

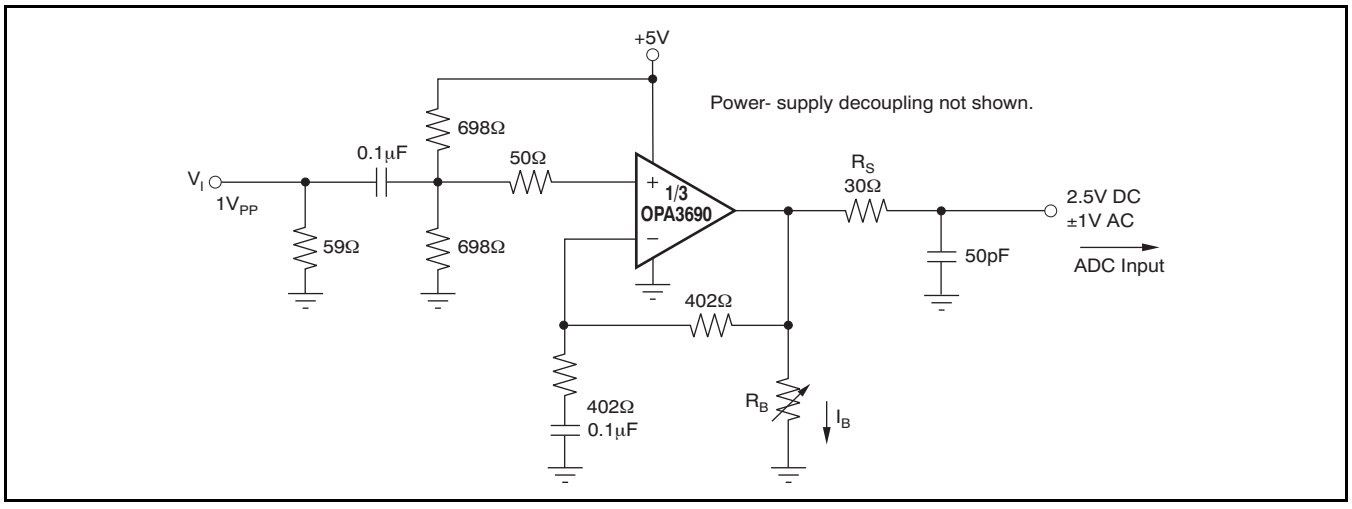


Figure 39. Single-Supply ADC Input Driver (one of three channels)

ANALOG DELAY LINE

The circuit on the front page of this data sheet shows an analog delay line using the OPA3690. The first op amp buffers the delay line from the source, and can be used to establish the dc operating point if single +5V supply operation is desired. The last two sections provide an analog delay function given by Equation 1:

$$\text{Delay} = \frac{2\tau}{1 + (2\pi f\tau)^2}, \text{ for each section.} \quad (1)$$

Where:

τ = RC.

f represents the frequency components of interest in the input signal.

For input frequencies below $0.39/2\pi\tau$ = 2.5MHz, the delay will be within 15% of the desired value (2τ). The circuit on the front page gives a delay of 50ns per stage for a total delay of 100ns. Excellent pulse fidelity will be retained as long as the first five harmonics are delayed equally. For the circuit on the front page, the 5th-harmonic should be = 2.5MHz/5, which will support a square wave up to 500kHz, with good pulse response. The input rise-and-fall times also need to be = 0.30/2.5MHz = 120ns in order to keep the spectral energy within this 2.5MHz limit. Quicker rise or fall times will cause propagation delay errors and excessive pre-shoot.

Shorter delays may be implemented at higher frequencies by adjusting R and C. To maintain bias current cancellation, it is best to simply reduce C without changing R. The analog delay line pulse response is shown in Figure 40.

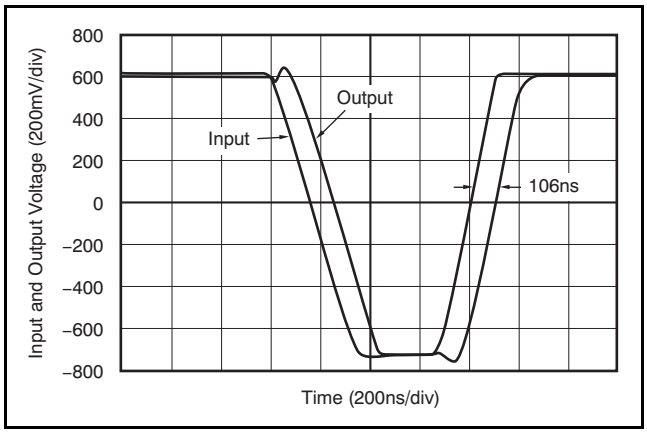


Figure 40. Analog Delay Line Pulse Response

The 1pF capacitors limit the noise, while maintaining good pulse response. If desired, these two capacitors may be removed for circuits that produce less delay.

INSTRUMENTATION DIFFERENTIAL AMPLIFIER

Figure 41 shows an instrumentation differential amplifier based on the OPA3690. This application benefits from the OPA3690 dc precision, common-mode rejection, high impedance input, and low-current noise. The resistors on the last (difference) amplifier were selected to keep the loads equal on the input stage op amps. The matched loads and a careful PCB layout can improve 2nd-harmonic distortion at higher frequencies. Figure 42 shows the frequency response of the instrumentation differential amplifier.

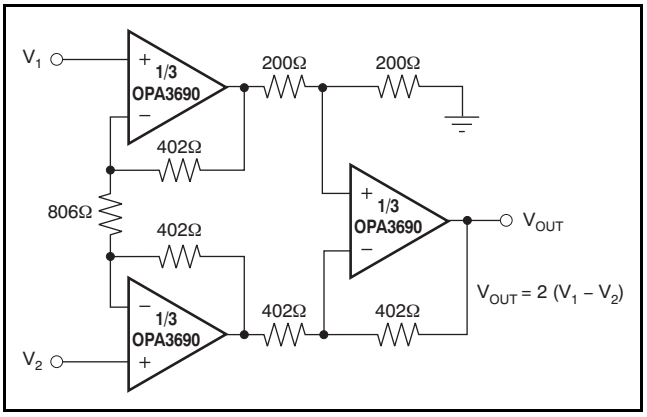


Figure 41. Instrumentation Amplifier

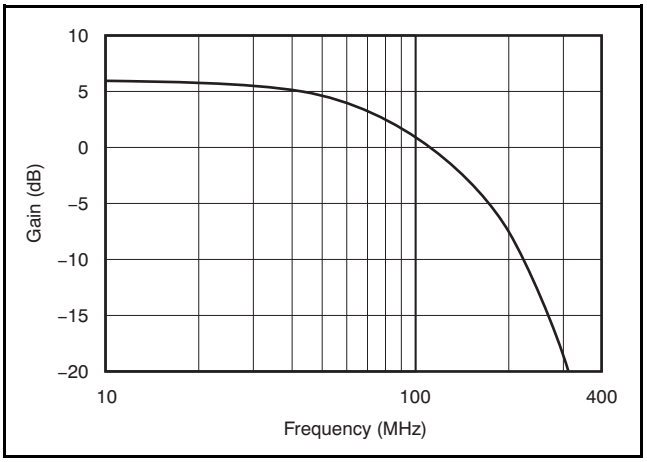


Figure 42. Frequency Response for the OPA3690 as an Instrumentation Amplifier

In applications where current-feedback amplifiers or fixed-gain amplifiers can be used, the OPA3691 or OPA3692 will provide wider bandwidth instrumentation amplifiers.

BUFFERED 2 x 1 MULTIPLEXER

Using two of the three channels in an OPA3690 to select one of two possible input signals, then using the 3rd to isolate the summing point and drive the load, will give a very flexible, wideband, multiplexing capability. See Figure 44 for one example of this where the two input stages have been set up for a gain of +2.

Summing the two output signals together at the output stage buffer noninverting input through 400Ω resistors allows excellent isolation between the two channels to be maintained. When one channel is operating, the other will see an attenuated version of the active channel signal on its inverting node. In this circuit, that signal is attenuated by 20dB at this inactive inverting input—this will keep the swing low enough on the off channel to avoid parasitic turn-on at that input stage. The desired signal is attenuated by 0.6V/V due to this resistor divider, then recovered by the gain set in the output stage.

One modification to this circuit would give a high-speed switched gain. The same signal would be fed into both inputs and each amplifier would be set to a different gain.

TRIPLE ADC DRIVER

Figure 43 shows the OPA3690 driving a triple ADC. Most ADCs are defined for single +5V operation. The OPA3690 can be adapted to single +5V as well, using the techniques described for Figure 37. The signal flowthrough pinout for the OPA3690 allows a higher signal fidelity through higher frequencies due to the simplified PCB layout requirements.

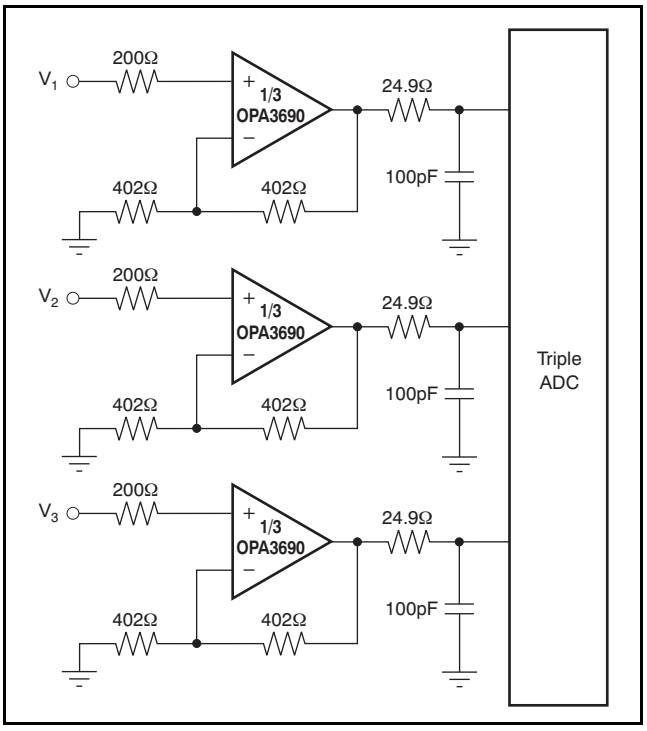


Figure 43. Triple ADC Driver

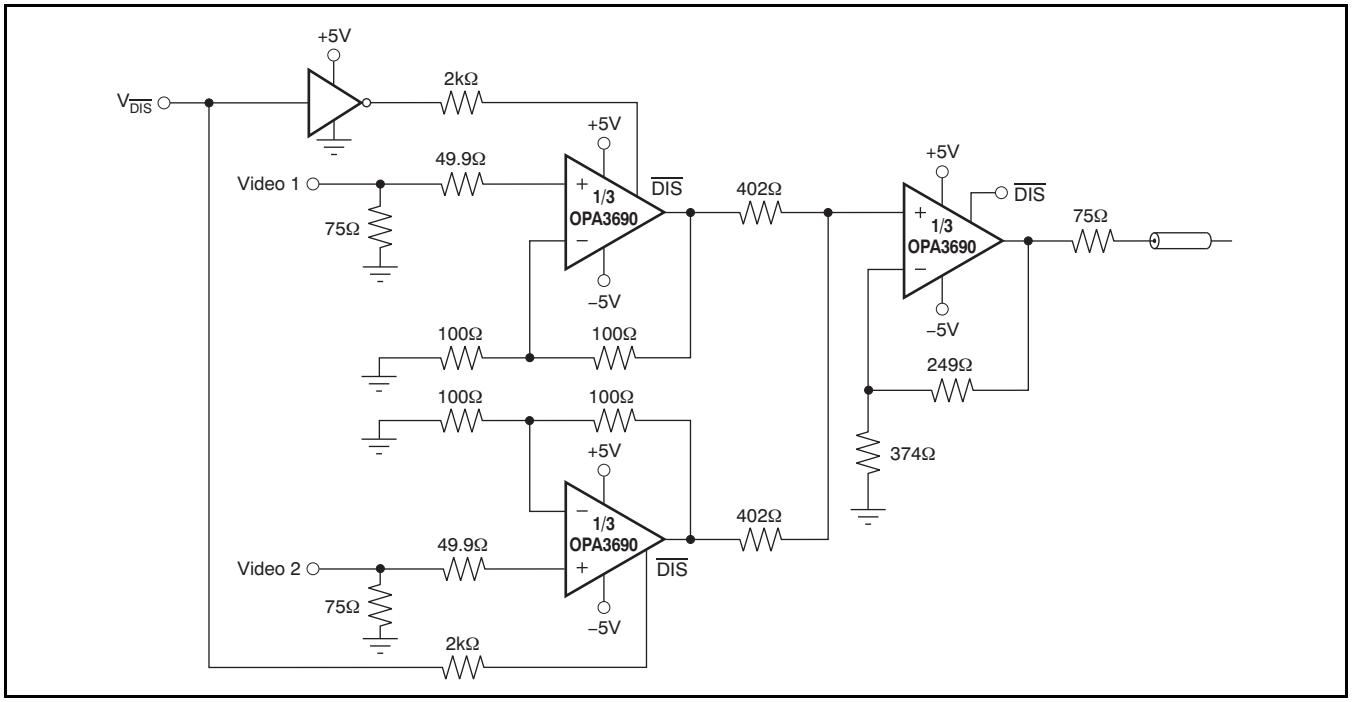


Figure 44. Buffered 2 x 1 Multiplexer

WIDEBAND INTEGRATOR

The three unity-gain stable, voltage-feedback amplifiers in the OPA3690 may be used to develop an exceptional integrator function, as shown in Figure 45. This circuit effectively multiplies the open-loop gain using two of the amplifiers and uses the third to provide an input impedance buffering and low output impedance over broad frequencies required for proper operation. The interstage attenuator (resistive divider into the last stage noninverting input) is critical to maintaining stability; see Figure 43. This circuit can deliver a 90° phase shift over a five-decade frequency span.

STATE VARIABLE FILTER

Figure 46 shows a state variable filter using the OPA3690. This active filter is quite useful for high Q filter responses, and will produce low-pass, high-pass, bandpass, notch, and all-pass functions. The filter response is:

$$\frac{V_{OUT}}{V_{IN}} = -\frac{S^2(\alpha) + \frac{S\omega_P}{Q_P}(\beta - \chi) + \omega_P{}^2(\delta)}{S^2 + \frac{S\omega_P}{Q_P} + \omega_P{}^2}$$

$$\text{where } \omega_P = \frac{1}{RC} \tag{2}$$

The desired filter frequency response is achieved by the correct selection of the feed-forward components at the input.

The resistor R_{ISO} isolates the last op amp and the input driver from capacitive loading problems when $\alpha > 0$. To ensure good performance, make sure that:

$$\frac{\omega_P}{2\pi} \le \begin{cases} \frac{f_{GBP}}{20Q_P}, & Q_P > 1 \\ \frac{f_{GBP}}{20}, & Q_P \le 1 \end{cases} \tag{3}$$

where f_{GBP} is the OPA3690 gain bandwidth product (300MHz).

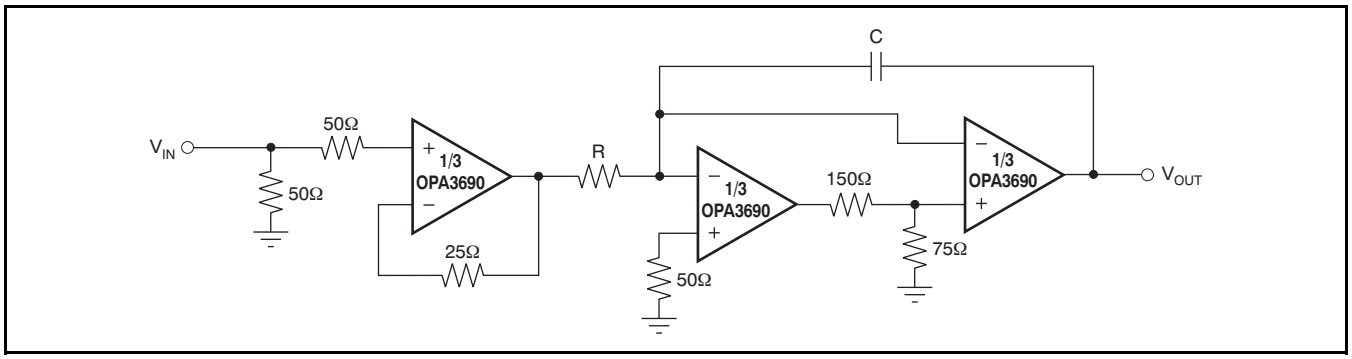


Figure 45. Wideband Integrator

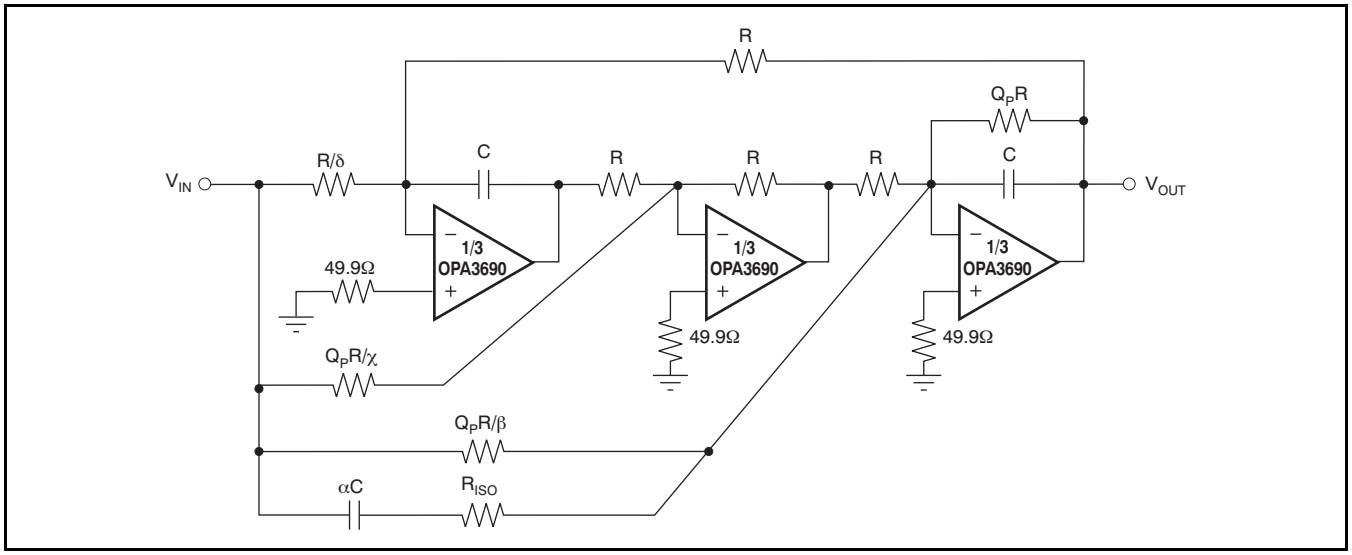


Figure 46. State Variable Filter

DESIGN-IN TOOLS

DEMONSTRATION FIXTURES

Two printed circuit boards (PCBs) are available to assist in the initial evaluation of circuit performance using the OPA3690 in its two package options. Both of these are offered free of charge as unpopulated PCBs, delivered with a user's guide. The summary information for these fixtures is shown in Table 1.

Table 1. Demonstration Fixtures by Package

PRODUCT	PACKAGE	ORDERING NUMBER	LITERATURE NUMBER
OPA3690IDBQ	SSOP-16	DEM-OPA-SSOP-3A	SBOU006
OPA3690ID	SO-16	DEM-OPA-SO-3A	SBOU007

The demonstration fixtures can be requested at the Texas Instruments web site (www.ti.com) through the OPA3690 product folder.

MACROMODELS

Computer simulation of circuit performance using SPICE is often useful when analyzing the performance of analog circuits and systems. This is particularly true for video and RF amplifier circuits where parasitic capacitance and inductance can have a major effect on circuit performance. A SPICE model for the OPA3690 (use three OPA690 SPICE models) is available through the OPA3690 product folder under *Simulation Models*. These models do a good job of predicting small-signal ac and transient performance under a wide variety of operating conditions. They do not do as well in predicting the harmonic distortion, temperature performance, or dG/dP characteristics. These models do not attempt to distinguish between the package types in their small-signal ac performance.

OPERATING SUGGESTIONS

OPTIMIZING RESISTOR VALUES

Since the the OPA3690 is a unity-gain stable, voltage-feedback op amp, a wide range of resistor values may be used for the feedback and gain setting resistors. The primary limits on these values are set by dynamic range (noise and distortion) and parasitic capacitance considerations. For a noninverting unity-gain follower application, the feedback connection should be made with a 25Ω resistor, not a direct short. This will isolate the inverting input capacitance from the output pin and improve the frequency response flatness. Usually, for G > 1 applications, the feedback resistor value should be between 100Ω and 1.5kΩ. Below 100Ω, the feedback network will present additional output loading which can degrade the harmonic distortion performance of the OPA3690. Above 1.5kΩ, the typical parasitic capacitance (approximately 0.2pF) across the feedback resistor can cause unintentional band-limiting in the amplifier response.

A good rule of thumb is to target the parallel combination of R_F and R_G (see Figure 36) to be less than approximately 125Ω. The combined impedance $R_F \parallel R_G$ interacts with the inverting input capacitance, placing an additional pole in the feedback network and thus, a zero in the forward response. Assuming a 3pF total parasitic on the inverting node, holding $R_F \parallel R_G < 125\Omega$ will keep this pole above 400MHz. By itself, this constraint implies that feedback resistor R_F can increase to several kΩ at high gains. This is acceptable as long as the pole formed by R_F and any parasitic capacitance appearing in parallel is kept out of the frequency range of interest.

BANDWIDTH vs GAIN: NONINVERTING OPERATION

Voltage-feedback op amps exhibit decreasing closed-loop bandwidth as the signal gain is increased. In theory, this relationship is described by the Gain Bandwidth Product (GBP) shown in the Electrical Characteristics. Ideally, dividing GBP by the noninverting signal gain (also called the Noise Gain, or NG) will predict the closed-loop bandwidth. In practice, this only holds true when the phase margin approaches 90°, as it does in high gain configurations. At low gains (increased feedback factors), most amplifiers will exhibit a more complex response with lower phase margin. The OPA3690 is compensated to give a slightly peaked response in a noninverting gain of 2 (see Figure 36). This results in a typical gain of +2 bandwidth of 220MHz, far exceeding that predicted by dividing the 300MHz GBP by 2. Increasing the gain will cause the phase margin to approach 90° and the bandwidth to more closely approach the predicted value of (GBP/NG). At a gain of +10, the 30MHz bandwidth shown in the Electrical Characteristics agrees with that predicted using the simple formula and the typical GBP of 300MHz.

The frequency response in a gain of +2 may be modified to achieve exceptional flatness simply by increasing the noise gain to 2.5. One way to do this, without affecting the +2 signal gain, is to add an 453Ω resistor across the two inputs in the circuit of Figure 36. A similar technique may be used to reduce peaking in unity-gain (voltage follower) applications. For example, by using a 402Ω feedback resistor along with a 402Ω resistor across the two op amp inputs, the voltage follower response will be similar to the gain of +2 response of Figure 37. Reducing the value of the resistor across the op amp inputs will further limit the frequency response due to increased noise gain.

The OPA3690 exhibits minimal bandwidth reduction going to single-supply (+5V) operation as compared with ±5V. This is because the internal bias control circuitry retains nearly constant quiescent current as the total supply voltage between the supply pins is changed.

INVERTING AMPLIFIER OPERATION

Since the OPA3690 is a general-purpose, wideband voltage-feedback op amp, all of the familiar op amp application circuits are available to the designer. Inverting operation is one of the more common requirements and offers several performance benefits. Figure 47 shows a typical inverting configuration where the I/O impedances and signal gain from Figure 36 are retained in an inverting circuit configuration.

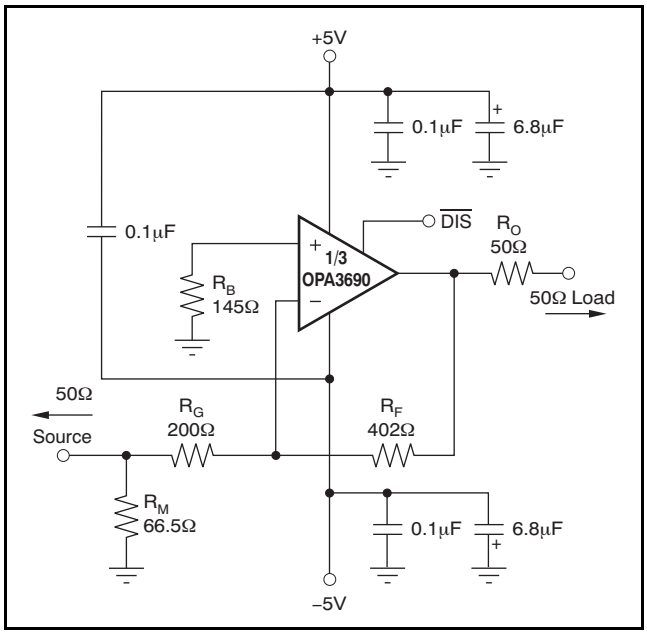


Figure 47. Gain of –2 Example Circuit

In the inverting configuration, three key design considerations must be noted. The first is that the gain resistor (R_G) becomes part of the signal channel input impedance. If input impedance matching is desired (which is beneficial whenever the signal is coupled through a cable, twisted-pair, long PCB trace, or other transmission line conductor), R_G may be set equal to the required termination value and R_F adjusted to give the desired gain. This is the simplest approach and results in optimum bandwidth and noise performance. However, at low inverting gains, the resultant feedback resistor value can present a significant load to the amplifier output. For an inverting gain of –2, setting R_G to 54Ω for input matching eliminates the need for R_M but requires a 100Ω feedback resistor. This has the interesting advantage that the noise gain becomes equal to 2 for a 50Ω source impedance—the same as the noninverting circuits considered in the previous section. The amplifier output, however, will now see the 100Ω feedback resistor in parallel with the external load. In general, the feedback resistor should be limited to the 100Ω to 1.5kΩ range. In this case, it is preferable to increase both the R_F and R_G values, as shown in Figure 47, and then achieve the input matching impedance with a third resistor (R_M) to ground. The total input impedance becomes the parallel combination of R_G and R_M.

The second major consideration, touched on in the previous paragraph, is that the signal source impedance becomes part of the noise gain equation and influences the bandwidth. For the example in Figure 47, the R_M value combines in parallel with the external 50Ω source impedance, yielding an effective driving impedance of 50Ω || 66.5Ω = 28.5Ω. This impedance is added in series with R_G for calculating the noise gain (NG). The resultant NG is 2.76 for Figure 47, as opposed to only 2 if R_M could be eliminated as discussed above. The bandwidth will therefore be slightly lower for the gain of –2 circuit of Figure 47 than for the gain of +2 circuit of Figure 36.

The third important consideration in inverting amplifier design is setting the bias current cancellation resistor on the noninverting input (R_B). If this resistor is set equal to the total dc resistance looking out of the inverting node, the output dc error, due to the input bias currents, will be reduced to (Input Offset Current) × R_F. If the 50Ω source impedance is dc-coupled in Figure 47, the total resistance to ground on the inverting input will be 228Ω. Combining this in parallel with the feedback resistor gives the R_B = 145Ω used in this example. To reduce the additional high-frequency noise introduced by this resistor, it is sometimes bypassed with a capacitor. As long as R_B < 350Ω, the capacitor is not required because the total noise contribution of all other terms will be less than that of the op amp input noise voltage. As a minimum, the OPA3690 requires an R_B value of 50Ω to damp out parasitic-induced peaking—a direct short to ground on the noninverting input runs the risk of a very high-frequency instability in the input stage.

OUTPUT CURRENT AND VOLTAGE

The OPA3690 provides output voltage and current capabilities that are unsurpassed in a low-cost monolithic op amp. Under no-load conditions at +25°C, the output voltage typically swings closer than 1V to either supply rail; the specified swing limit is within 1.2V of either rail. Into a 15Ω load (the minimum tested load), it will deliver more than ±160mA.

The specifications described previously, though familiar in the industry, consider voltage and current limits separately. In many applications, it is the voltage × current, or V-I product, that is more relevant to circuit operation. Refer to Figure 19, the *Output Voltage and Current Limitations* plot in the Typical Characteristics. The X- and Y-axes of this graph show the zero-voltage output current limit and the zero-current output voltage limit, respectively. The four quadrants give a more detailed view of the OPA3690 output drive capabilities, noting that the graph is bounded by a *Safe Operating Area* of 1W maximum internal power dissipation for a single channel. Superimposing resistor load lines onto the plot shows that the OPA3690 can drive ±2.5V into 25Ω or ±3.5V into 50Ω without exceeding the output capabilities or the 1W dissipation limit. A 100Ω load line (the standard test circuit load) shows the full ±3.9V output swing capability (see the Electrical Characteristics).

The minimum specified output voltage and current specifications over temperature are set by worst-case simulations at the cold temperature extreme. Only at cold startup will the output current and voltage decrease to the numbers shown in the Electrical Characteristic tables. As the output transistors deliver power, their junction temperatures increase, decreasing their V_{BE}s (increasing the available output voltage swing) and increasing their current gains (increasing the available output current). In steady-state operation, the available output voltage and current is always greater than that shown in the over-temperature specifications because the output stage junction temperatures will be higher than the minimum specified operating ambient.

To protect the output stage from accidental shorts to ground and the power supplies, output short-circuit protection is included in the OPA3690. The circuit acts to limit the maximum source or sink current to approximately 250mA.

DRIVING CAPACITIVE LOADS

One of the most demanding and yet very common load conditions for an op amp is capacitive loading. Often, the capacitive load is the input of an ADC—including additional external capacitance which may be recommended to improve ADC linearity. A high-speed, high open-loop gain amplifier like the OPA3690 can be very susceptible to decreased stability and closed-loop response peaking when a capacitive load is placed directly on the output pin. When the amplifier's open-loop output resistance is considered, this capacitive load introduces an additional pole in the signal path that can decrease the phase margin. Several external solutions to this problem have been suggested. When the primary considerations are frequency response flatness, pulse response fidelity, and/or distortion, the simplest and most effective solution is to isolate the capacitive load from the feedback loop by inserting a series-isolation resistor between the amplifier output and the capacitive load. This does not eliminate the pole from the loop response, but rather shifts it and adds a zero at a higher frequency. The additional zero acts to cancel the phase lag from the capacitive load pole, thus increasing the phase margin and improving stability.

The Typical Characteristics show the recommended R_S versus capacitive load (Figure 15 for ±5V and Figure 30 for +5V) and the resulting frequency response at the load. Parasitic capacitive loads greater than 2pF can begin to degrade the performance of the OPA3690. Long PCB traces, unmatched cables, and connections to multiple devices can easily exceed this value. Always consider this effect carefully, and add the recommended series resistor as close as possible to the OPA3690 output pin (see the *Board Layout Guidelines* section).

The criterion for setting this R_S resistor is a maximum bandwidth, flat frequency response at the load. For the OPA3690 operating in a gain of +2, the frequency response at the output pin is already slightly peaked without the capacitive load requiring relatively high values of R_S to flatten the response at the load. Increasing the noise gain will reduce the peaking as described previously. The circuit of Figure 48 demonstrates this technique, allowing lower values of R_S to be used for a given capacitive load. This was used to generate the Recommended R_S vs Capacitive Load plots (Figure 15 for ±5V and Figure 30 for +5V).

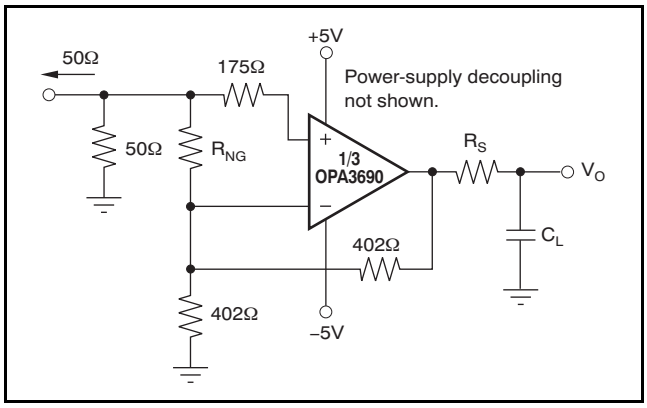


Figure 48. Capacitive Load Driving with Noise Gain Tuning

This gain of +2 circuit includes a noise gain tuning resistor across the two inputs to increase the noise gain, increasing the unloaded phase margin for the op amp. Although this technique will reduce the required R_S resistor for a given capacitive load, it does increase the noise at the output. It also will decrease the loop gain, slightly decreasing the distortion performance. If, however, the dominant distortion mechanism arises from a high R_S value, significant dynamic range improvement can be achieved using this technique. Figure 49 shows the required R_S versus C_{LOAD} parametric on noise gain using this technique. This is the circuit of Figure 48 with R_{NG} adjusted to increase the noise gain (increasing the phase margin) then sweeping C_{LOAD} and finding the required R_S to get a flat frequency response. This plot also gives the required R_S versus C_{LOAD} for the OPA3690 operated at higher signal gains without R_{NG}.

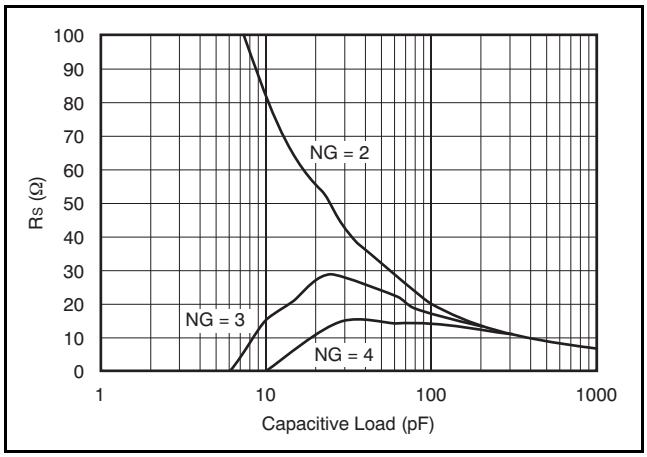


Figure 49. Required R_S vs Noise Gain

DISTORTION PERFORMANCE

The OPA3690 provides good distortion performance into a 100Ω load on ±5V supplies. Relative to alternative solutions, it provides exceptional performance into lighter loads and/or operating on a single +5V supply. The distortion plots show which changes in operation will improve distortion. Increasing the load impedance improves distortion directly. Remember that the total load includes the feedback network; in the noninverting configuration (see Figure 36), this is sum of $R_F + R_G$, while in the inverting configuration (see Figure 46) it is just R_F. Also, providing an additional supply-decoupling capacitor (0.1μF) between the supply pins (for bipolar operation) improves the 2nd-order distortion slightly (3dB to 6dB).

In most op amps, increasing the output voltage swing increases intermodulation distortion directly. The new output stage used in the OPA3690 actually holds the difference between fundamental power and the 3rd-order intermodulation powers relatively constant with increasing output power until very large output swings are required (> $4V_{PP}$). The 3rd-order spurious levels are extremely low at low output power levels. The output stage continues to hold them low even as the fundamental power reaches very high levels. As the Typical Characteristics show, the spurious intermodulation powers do not increase as predicted by a traditional intercept model. As the fundamental power level increases, the dynamic range does not decrease significantly. For two tones centered at 20MHz, with 10dBm/tone into a matched 50Ω load (that is, $2V_{PP}$ for each tone at the load, which requires $8V_{PP}$ for the overall two-tone envelope at the output pin), the Typical Characteristics show 46dBc difference between the test-tone powers and the 3rd-order intermodulation spurious powers. This exceptional performance improves further when operating at lower frequencies.

NOISE PERFORMANCE

High slew rate, unity-gain stable, voltage-feedback op amps usually achieve their slew rate at the expense of a higher input noise voltage. The 5.5nV/√Hz input voltage noise for the OPA3690 is, however, much lower than comparable amplifiers. The input-referred voltage noise, and the two input-referred current noise terms, combine to give low output noise under a wide variety of operating conditions. Figure 50 shows the op amp noise analysis model with all the noise terms included. In this model, all noise terms are taken to be noise voltage or current density terms in either nV/√Hz or pA/√Hz.

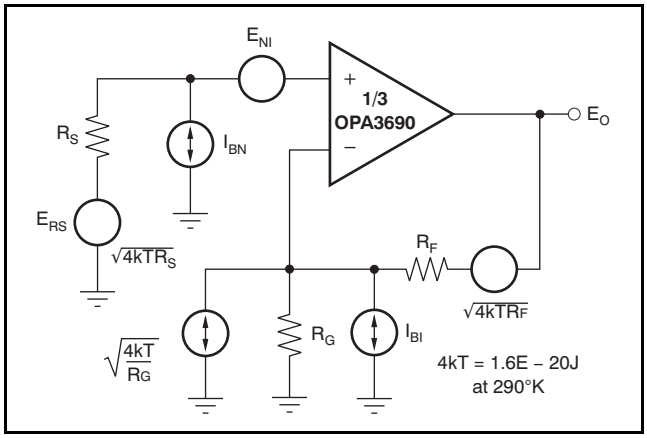


Figure 50. Op Amp Noise Analysis Model

The total output spot noise voltage can be computed as the square root of the sum of all squared output noise voltage contributors. Equation 4 shows the general form for the output noise voltage using the terms shown in Figure 50.

$$E_O = \sqrt{\left(E_{NI}^2 + (I_{BN}R_S)^2 + 4kTR_S\right)NG^2 + (I_{BI}R_F)^2 + 4kTR_FNG} \quad (4)$$

Dividing this expression by the noise gain [NG = (1 + R_F/R_G)] will give the equivalent input-referred spot noise voltage at the noninverting input, as shown in Equation 5.

$$E_N = \sqrt{E_{NI}^2 + (I_{BN}R_S)^2 + 4kTR_S + \left(\frac{I_{BI}R_F}{NG}\right)^2 + \frac{4kTR_F}{NG}} \quad (5)$$

Evaluating these two equations for the OPA3690 circuit and component values (see Figure 36) gives a total output spot noise voltage of 12.3nV/√Hz and a total equivalent input spot noise voltage of 6.1nV/√Hz. This is including the noise added by the bias current cancellation resistor (100Ω) on the noninverting input. This total input-referred spot noise voltage is only slightly higher than the 5.5nV/√Hz specification for the op amp voltage noise alone. This will be the case as long as the impedances appearing at each op amp input are limited to the previously recommend maximum value of 300Ω. Keeping both (R_F || R_G) and the noninverting input source impedance less than 300Ω will satisfy both noise and frequency response flatness considerations. As the resistor-induced noise is relatively negligible, additional capacitive decoupling across the bias current cancellation resistor (R_B) for the inverting op amp configuration of Figure 47 is not required.

DC ACCURACY AND OFFSET CONTROL

The balanced input stage of a wideband voltage-feedback op amp allows good output dc accuracy in a wide variety of applications. The power-supply current trim for the OPA3690 gives even tighter control than comparable amplifiers. Although the high-speed input stage does require relatively high input bias current (typically 5μA out of each input terminal), the close matching between them may be used to reduce the output dc error caused by this current. The total output offset voltage may be considerably reduced by matching the dc source resistances appearing at the two inputs. This reduces the output dc error due to the input bias currents to the offset current times the feedback resistor. Evaluating the configuration of Figure 36, and using worst-case +25°C input offset voltage and current specifications, gives a worst-case output offset voltage equal to:

– (NG = noninverting signal gain)

$\pm(NG \times V_{OS(MAX)}) \pm (R_F \times I_{OS(MAX)})$

$= \pm(2 \times 4.5mV) \pm (250\Omega \times 1\mu A)$

$= \pm 9.25mV$

A fine-scale output offset null, or dc operating point adjustment, is often required. Numerous techniques are available for introducing dc offset control into an op amp circuit. Most of these techniques eventually reduce to adding a dc current through the feedback resistor. In selecting an offset trim method, one key consideration is the impact on the desired signal path frequency response. If the signal path is intended to be noninverting, the offset control is best applied as an inverting summing signal to avoid interaction with the signal source. If the signal path is intended to be inverting, applying the offset control to the noninverting input may be considered. However, the dc offset voltage on the summing junction will set up a dc current back into the source that must be considered. Applying an offset adjustment to the inverting op amp input can change the noise gain and frequency response flatness. For a dc-coupled inverting amplifier, Figure 51 shows one example of an offset adjustment technique that has minimal impact on the signal frequency response. In this case, the dc offsetting current is brought into the inverting input node through resistor values that are much larger than the signal path resistors. This ensures that the adjustment circuit has minimal effect on the loop gain and hence, the frequency response.

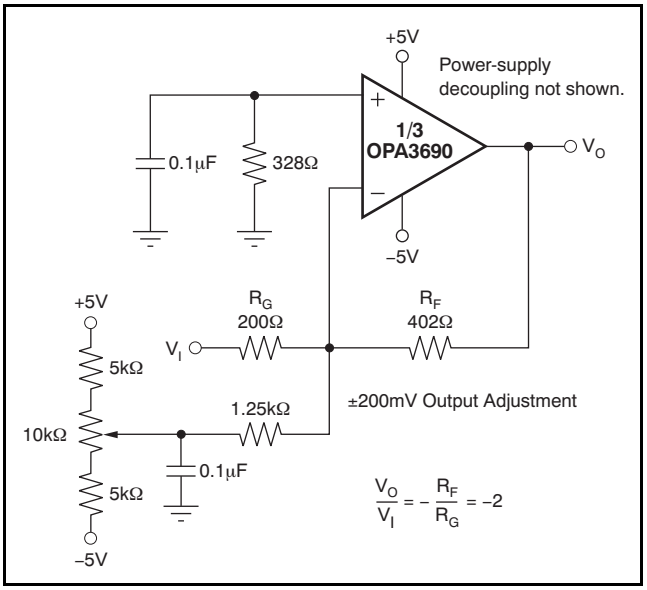


Figure 51. DC-Coupled, Inverting Gain of –2, with Offset Adjustment

DISABLE OPERATION

The OPA3690 provides an optional disable feature on each channel that may be used either to reduce system power or to implement a simple channel multiplexing operation. If the $\overline{DIS}$ control pin is left unconnected, the OPA3690 will operate normally. To disable, the control pin must be asserted LOW. Figure 52 shows a simplified internal circuit for the disable control feature available on each channel.

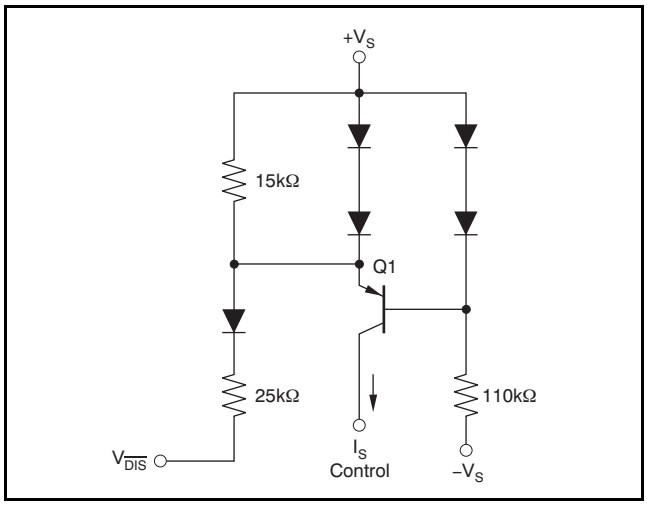


Figure 52. Simplified Disable Control Circuit

In normal operation, base current to Q1 is provided through the 110kΩ resistor, while the emitter current through the 15kΩ resistor sets up a voltage drop that is inadequate to turn on the two diodes in Q1's emitter. As $V_{\overline{DIS}}$ is pulled LOW, additional current is pulled through the 15kΩ resistor, eventually turning on those two diodes (≈75μA). At this point, any further current pulled out of $V_{\overline{DIS}}$ goes through those diodes holding the emitter-base voltage of Q1 at approximately 0V. This shuts off the collector current out of Q1, turning the amplifier off. The supply current in the disable mode are only those required to operate the circuit of Figure 52. Additional circuitry ensures that turn-on time occurs faster than turn-off time (make-before-break).

When disabled, the output and input nodes go to a high-impedance state. If the OPA3690 is operating at a gain of +1, this will show a very high impedance at the output and exceptional signal isolation. If operating at a gain greater than +1, the total feedback network resistance ($R_F + R_G$) will appear as the impedance looking back into the output, but the circuit will still show very high forward and reverse isolation. If configured as an inverting amplifier, the input and output will be connected through the feedback network resistance ($R_F + R_G$) and the isolation will be very poor as a result.

One key parameter in disable operation is the output glitch when switching in and out of the disabled mode. Figure 53 shows these glitches for the circuit of Figure 36 with the input signal at 0V. The glitch waveform at the output pin is plotted along with the $\overline{DIS}$ pin voltage.

The transition edge rate (dV/dt) of the $\overline{DIS}$ control line will influence this glitch. For the plot of Figure 53, the edge rate was reduced until no further reduction in glitch amplitude was observed. This approximately 1V/ns maximum slew rate may be achieved by adding a simple RC filter into the $\overline{DIS}$ pin from a higher speed logic line. If extremely fast transition logic is used, a 1kΩ series resistor between the logic gate and the $\overline{DIS}$ input pin provides adequate bandlimiting using just the parasitic input capacitance on the $\overline{DIS}$ pin while still ensuring adequate logic level swing.

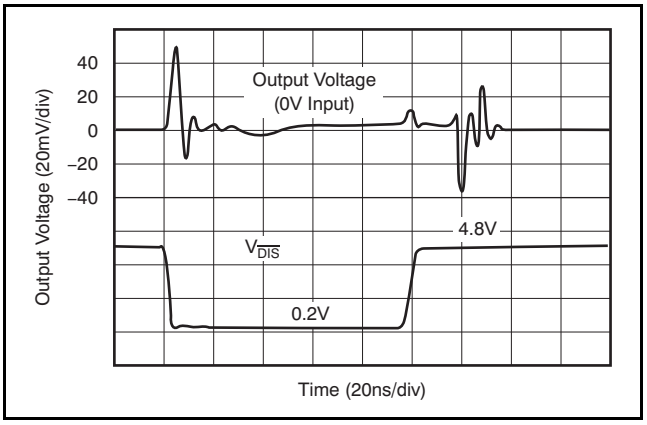


Figure 53. Disable/Enable Glitch

THERMAL ANALYSIS

Due to the high output power capability of the OPA3690, heatsinking or forced airflow may be required under extreme operating conditions. Maximum desired junction temperature will set the maximum allowed internal power dissipation as described below. In no case should the maximum junction temperature be allowed to exceed 175°C.

Operating junction temperature (T_J) is given by:

$$T_A + P_D \times \theta_{JA}$$

The total internal power dissipation (P_D) is the sum of quiescent power (P_{DQ}) and additional power dissipated in the output stage (P_{DL}) to deliver load power. Quiescent power is simply the specified no-load supply current times the total supply voltage across the part. P_{DL} depends on the required output signal and load but, for a grounded resistive load, is at a maximum when the output is fixed at a voltage equal to 1/2 of either supply voltage (for equal bipolar supplies). Under this condition, $P_{DL} = V_{S2}/(4 \times R_L)$ where R_L includes feedback network loading.

Note that it is the power in the output stage and not into the load that determines internal power dissipation.

As a worst-case example, compute the maximum T_J using an OPA3690IDBQ in the circuit of Figure 36 operating at the maximum specified ambient temperature of +85°C and driving a grounded 100Ω.

$$P_D = 10V \times 18.6mA + 3\ [5^2/(4 \times (100\Omega \parallel 804\Omega))$$

$$= 397mW$$

$$\text{Maximum } T_J = +85°C + (0.40W \times 100°C/W)$$

$$= 125°C$$

This worst-case condition is still well within rated maximum T_J for this 100Ω load. Heavier loads may, however, exceed the 150°C maximum junction temperature rating. Careful attention to internal power dissipation is required and perhaps airflow considered under extreme conditions.

BOARD LAYOUT GUIDELINES

Achieving optimum performance with a high-frequency amplifier like the OPA3690 requires careful attention to board layout parasitics and external component types. Recommendations that will optimize performance include:

a. **Minimize parasitic capacitance** to any ac ground for all of the signal I/O pins. Parasitic capacitance on the output and inverting input pins can cause instability: on the noninverting input, it can react with the source impedance to cause unintentional bandlimiting. To reduce unwanted capacitance, a window around the signal I/O pins should be opened in all of the ground and power planes around those pins. Otherwise, ground and power planes should be unbroken elsewhere on the board.

b. **Minimize the distance** (< 0.25") from the power-supply pins to high-frequency 0.1μF decoupling capacitors. At the device pins, the ground and power-plane layout should not be in close proximity to the signal I/O pins. Avoid narrow power and ground traces to minimize inductance between the pins and the decoupling capacitors. The power-supply connections should always be decoupled with these capacitors. An optional supply decoupling capacitor (0.1μF) across the two power supplies (for bipolar operation) will improve 2nd-harmonic distortion performance. Larger (2.2μF to 6.8μF) decoupling capacitors, effective at lower frequencies, should also be used on the main supply pins. These may be placed somewhat farther from the device and may be shared among several devices in the same area of the PCB.

c. **Careful selection and placement of external components will preserve the high-frequency performance of the OPA3690.** Resistors should be a very low reactance type. Surface-mount resistors work best and allow a tighter overall layout. Metal film or carbon composition axially-leaded resistors can also provide good high-frequency performance. Again, keep their leads and PCB traces as short as possible. Never use wirewound type resistors in a high-frequency application. Since the output pin and inverting input pin are the most sensitive to parasitic capacitance, always position the feedback and series output resistor, if any, as close as possible to the output pin. Other network components, such as noninverting input termination resistors, should also be placed close to the package. Where double-side component mounting is allowed, place the feedback resistor directly under the package on the other side of the board between the output and inverting input pins. Even with a low parasitic capacitance shunting the external resistors, excessively high resistor values can create significant time constants that can degrade performance. Good axial metal film or surface-mount resistors have approximately 0.2pF in shunt with the resistor. For resistor values > 1.5kΩ, this parasitic capacitance can add a pole and/or zero below 500MHz that can affect circuit operation. Keep resistor values as low as possible consistent with load driving considerations. The 402Ω feedback used in the Electrical Characteristics is a good starting point for design. Note that a 25Ω feedback resistor, rather than a direct short, is suggested for the unity-gain follower application. This effectively isolates the inverting input capacitance from the output pin that would otherwise cause an additional peaking in the gain of +1 frequency response.

d. **Connections to other wideband devices** on the board may be made with short, direct traces or through onboard transmission lines. For short connections, consider the trace and the input to the next device as a lumped capacitive load. Relatively wide traces (50mils or 1,27mm to 100mils or 2,54mm) should be used, preferably with ground and power planes opened up around them. Estimate the total capacitive load and set R_S from the plot of Recommended R_S vs Capacitive Load (Figure 15 for ±5V and Figure 30 for +5V). Low parasitic capacitive loads (< 5pF) may not need an R_S because the OPA3690 is nominally compensated to operate with a 2pF parasitic load. Higher parasitic capacitive loads without an R_S are allowed as the signal gain increases (increasing the unloaded phase margin). If a long trace is required, and the 6dB signal loss intrinsic to a doubly-terminated transmission line is acceptable, implement a matched impedance transmission line using microstrip or stripline techniques (consult an ECL design handbook for microstrip and stripline layout techniques). A 50Ω environment is normally not necessary on board, and in fact, a higher impedance environment will improve distortion as shown in the distortion versus load plots (Figure 7 for the ±5v and Figure 32 for the +5V). With a characteristic board trace impedance defined (based on board material and trace dimensions), a matching series resistor into the trace from the output of the OPA3690 is used as well as a terminating shunt resistor at the input of the destination device. Remember also that the terminating impedance will be the parallel combination of the shunt resistor and the input impedance of the destination device; this total effective impedance should be set to match the trace impedance. The high output voltage and

current capability of the OPA3690 allows multiple destination devices to be handled as separate transmission lines, each with their own series and shunt terminations. If the 6dB attenuation of a doubly-terminated transmission line is unacceptable, a long trace can be series-terminated at the source end only. Treat the trace as a capacitive load in this case and set the series resistor value as shown in the plots of Recommended R_S vs Capacitive Load (Figure 15 for ±5V and Figure 30 for +5V). This will not preserve signal integrity as well as a doubly-terminated line. If the input impedance of the destination device is low, there will be some signal attenuation due to the voltage divider formed by the series output into the terminating impedance.

INPUT AND ESD PROTECTION

The OPA3690 is built using a very high-speed complementary bipolar process. The internal junction breakdown voltages are relatively low for these very small geometry devices. These breakdowns are reflected in the Absolute Maximum Ratings table. All device pins are protected with internal ESD protection diodes to the power supplies, as shown in Figure 54.

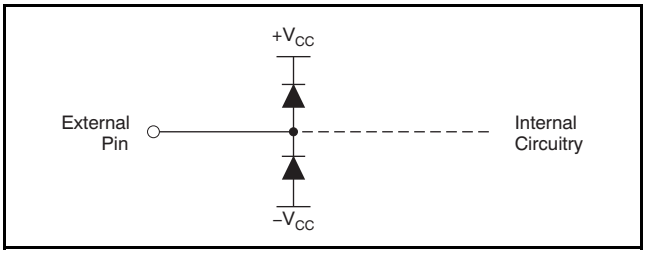


Figure 54. Internal ESD Protection

These diodes provide moderate protection to input overdrive voltages above the supplies as well. The protection diodes can typically support 30mA continuous current. Where higher currents are possible (for example, in systems with ±15V supply parts driving into the OPA3690), current-limiting series resistors should be added into the two inputs. Keep these resistor values as low as possible since high values degrade both noise performance and frequency response.

REVISION HISTORY

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision F (August 2008) to Revision G **Page**

- Changed data sheet format to current standards 1
- Deleted *Lead Temperature* specification from Absolute Maximum Ratings table 2
- Added condition to Figure 12 8
- Added Figure 25, Noninverting Overdrive Recovery graph 11
- Changed typo in Equation 2 18
- Changed *dG/df* to *dG/dP* (typo) in *Macromodels* section 19
- Changed typo in Equation 5 24
- Changed unit in equation from 250W to 250Ω in *DC Accuracy and Offset Control* section 25

Changes from Revision E (June 2006) to Revision F **Page**

- Changed Storage Temperature minimum value from −40°C to −65°C 2

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
OPA3690ID	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR		OPA3690	Samples
OPA3690IDBQT	ACTIVE	SSOP	DBQ	16	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR		OPA 3690	Samples
OPA3690IDG4	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR		OPA3690	Samples
OPA3690IDR	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	OPA3690	Samples
OPA3690IDRG4	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	OPA3690	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

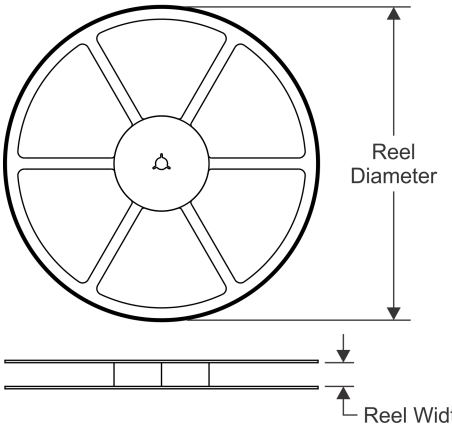
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

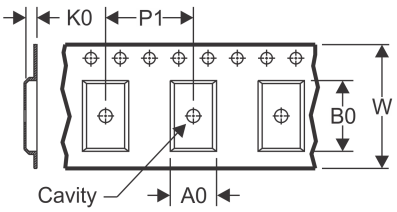
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

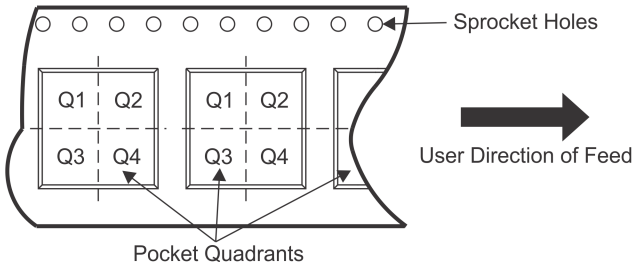


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

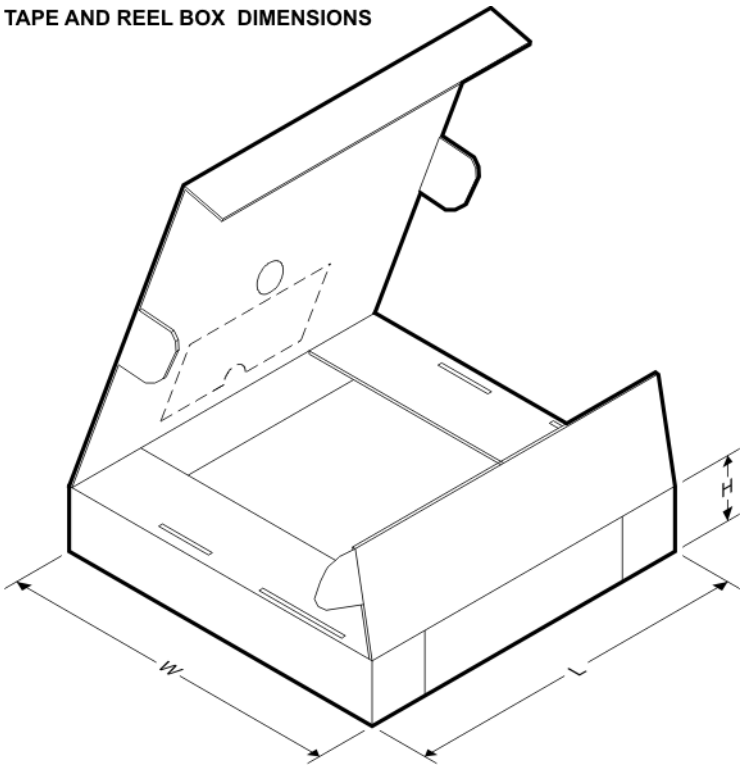
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
OPA3690IDBQT	SSOP	DBQ	16	250	180.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
OPA3690IDR	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1

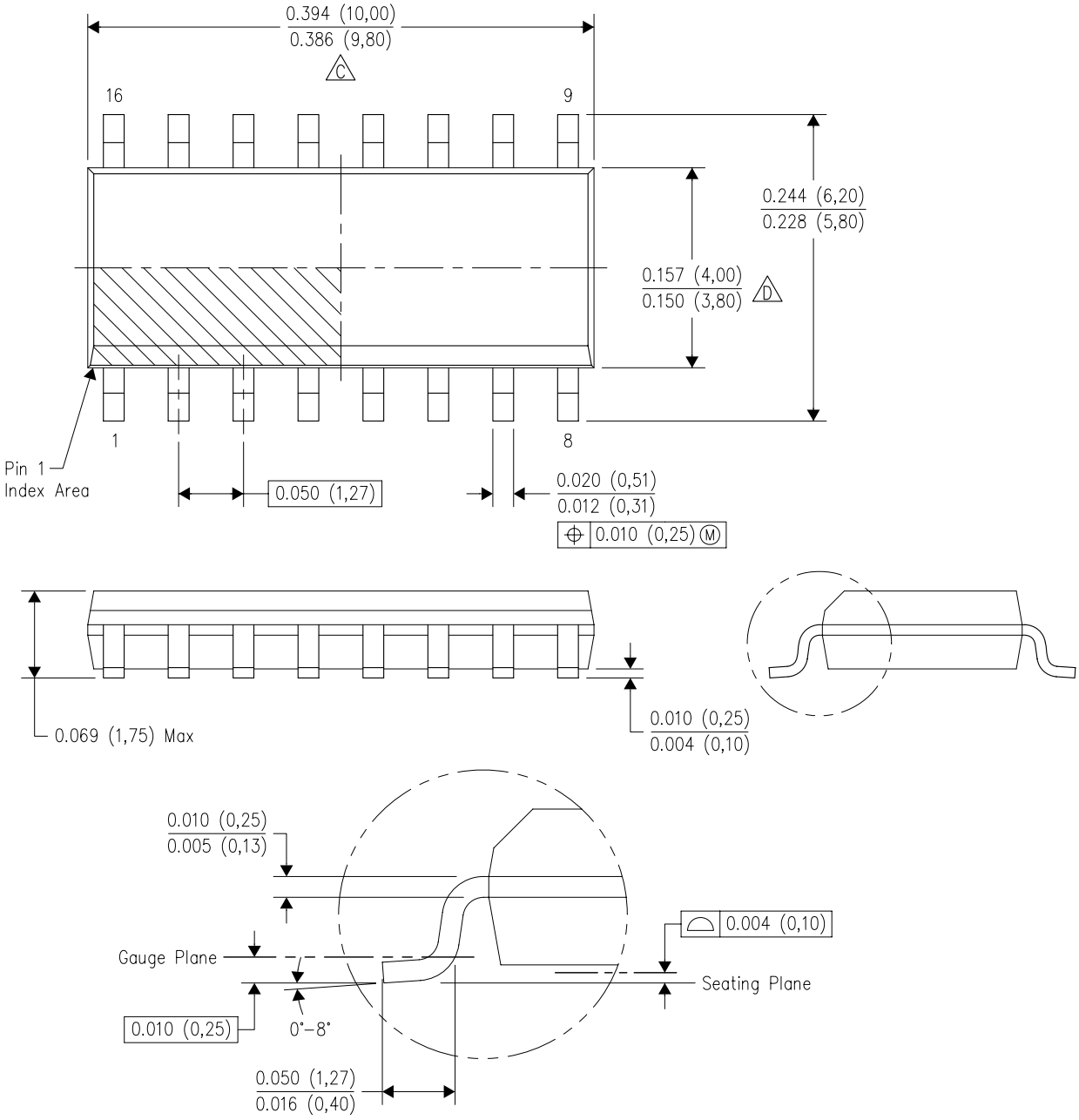
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

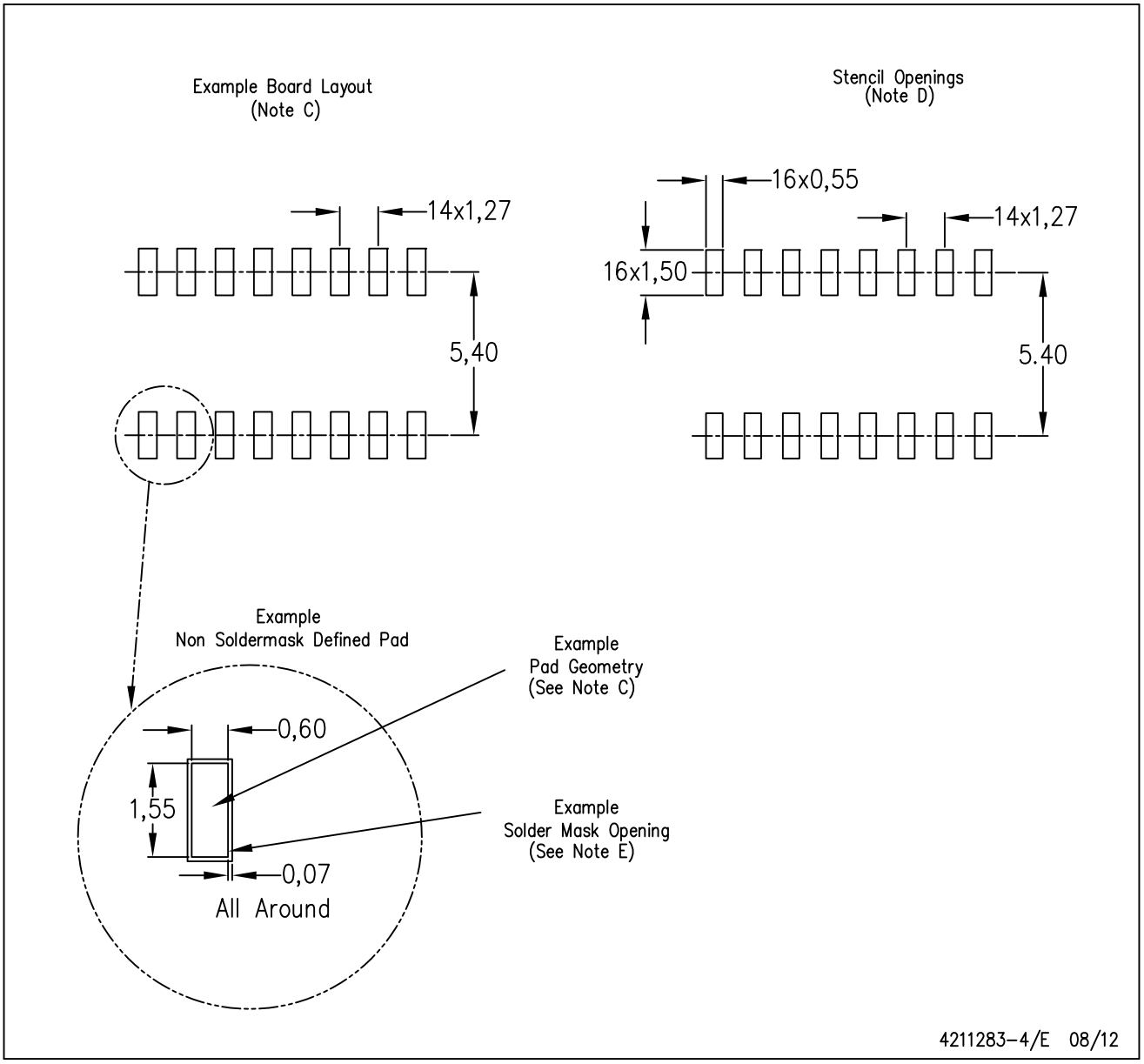
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
OPA3690IDBQT	SSOP	DBQ	16	250	210.0	185.0	35.0
OPA3690IDR	SOIC	D	16	2500	367.0	367.0	38.0

D (R–PDSO–G16) PLASTIC SMALL OUTLINE



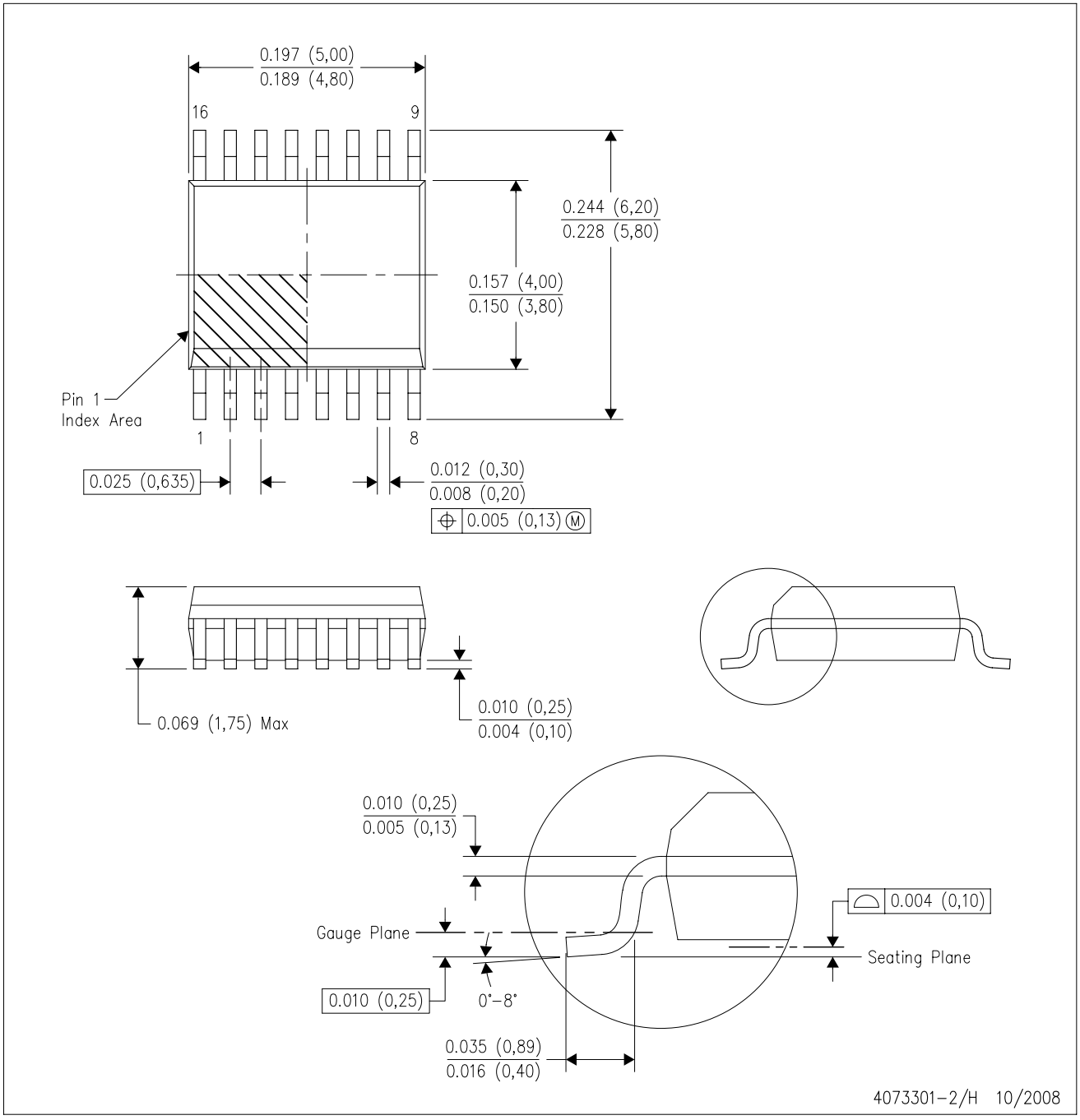
NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AC.

D (R–PDSO–G16) PLASTIC SMALL OUTLINE



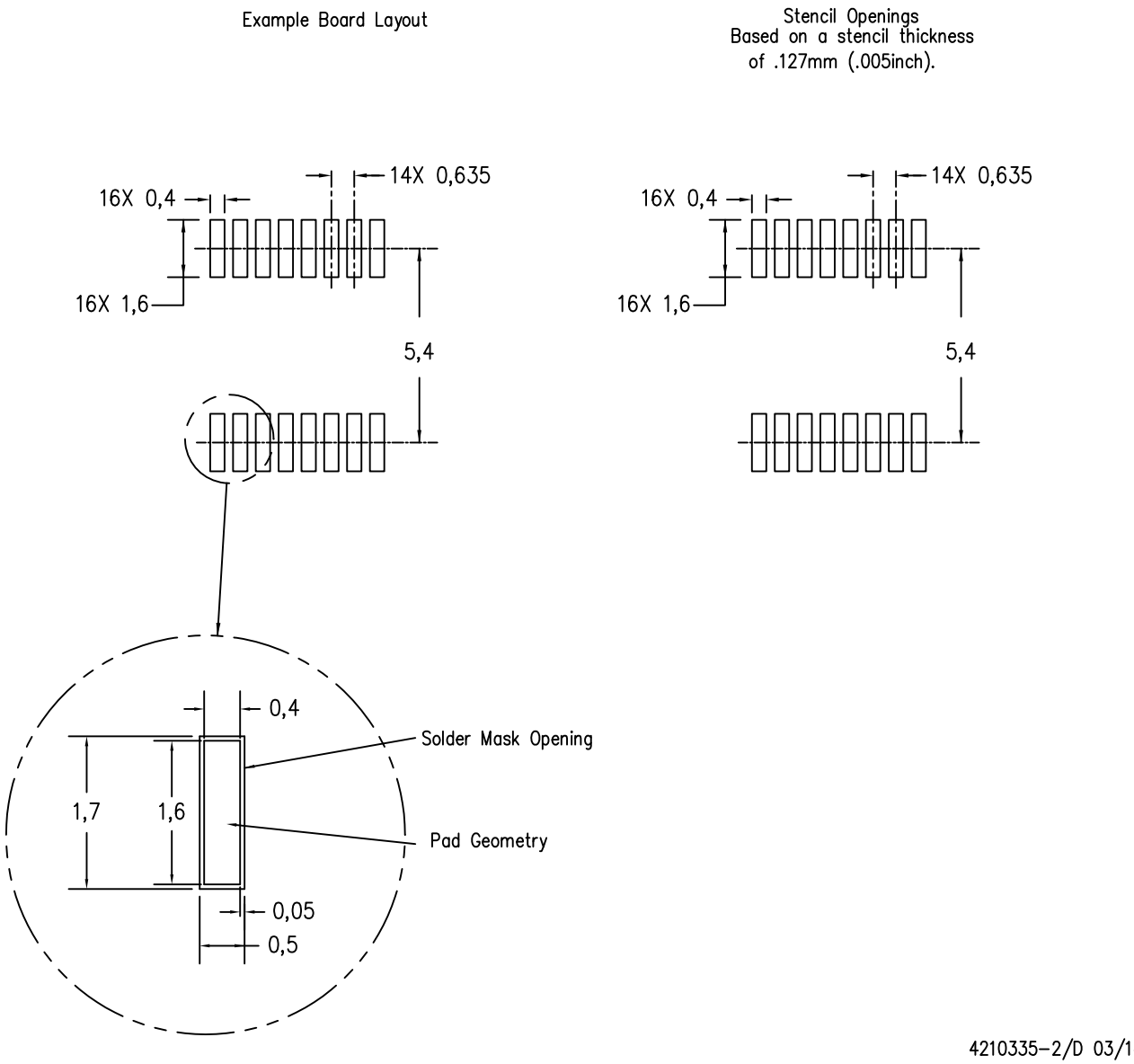
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

DBQ (R–PDSO–G16) PLASTIC SMALL–OUTLINE PACKAGE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15) per side.
D. Falls within JEDEC MO–137 variation AB.

DBQ (R–PDSO–G16) PLASTIC SMALL OUTLINE PACKAGE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC–7525 for other stencil recommendations.

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