OCTAL BUFFERS/DRIVERS WITH 3-STATE OUTPUTS

Check for Samples: SN54AHCT541, SN74AHCT541

FEATURES

- **Inputs Are TTL-Voltage Compatible**
- **Latch-Up Performance Exceeds 250 mA Per JESD 17**
- **ESD Protection Exceeds JESD 22**
  - **2000-V Human-Body Model (A114-A)**
  - **200-V Machine Model (A115-A)**
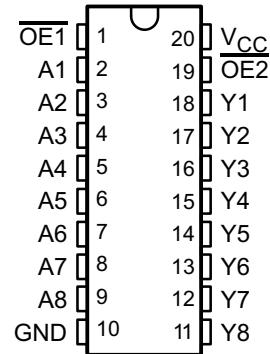 - **1000-V Charged-Device Model (C101)**

DESCRIPTION

The 'AHCT541 octal buffers/drivers are ideal for driving bus lines or buffer memory address registers. These devices feature inputs and outputs on opposite sides of the package to facilitate printed circuit board layout.
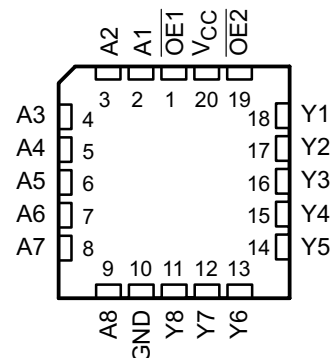
The 3-state control gate is a 2-input AND gate with active-low inputs so that if either output-enable ($\overline{OE1}$ or $\overline{OE2}$) input is high, all corresponding outputs are in the high-impedance state. The outputs provide non-inverted data when they are not in the high-impedance state.

To ensure the high-impedance state during power up or power down, $\overline{OE}$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

SN54AHCT541 . . . J or W PACKAGE
SN74AHCT541 . . . DB, DGV, DW, N, NS, OR PW PACKAGE
(TOP VIEW)

$\overline{OE1}$	1	20	V_{CC}
A1	2	19	$\overline{OE2}$
A2	3	18	Y1
A3	4	17	Y2
A4	5	16	Y3
A5	6	15	Y4
A6	7	14	Y5
A7	8	13	Y6
A8	9	12	Y7
GND	10	11	Y8

SN54AHCT541 . . . FK PACKAGE
(TOP VIEW)

Top pins: A2 (3), A1 (2), $\overline{OE1}$ (1), V_{CC} (20), $\overline{OE2}$ (19)

Left pins: A3 (4), A4 (5), A5 (6), A6 (7), A7 (8)

Right pins: Y1 (18), Y2 (17), Y3 (16), Y4 (15), Y5 (14)

Bottom pins: A8 (9), GND (10), Y8 (11), Y7 (12), Y6 (13)

FUNCTION TABLE
(EACH FLIP-FLOP)

INPUTS			OUTPUT Y
$\overline{OE1}$	$\overline{OE2}$	A	
L	L	L	L
L	L	H	H
H	X	X	Z
X	H	X	Z

LOGIC DIAGRAM, EACH FLIP-FLOP (POSITIVE LOGIC)

To Seven Other Channels
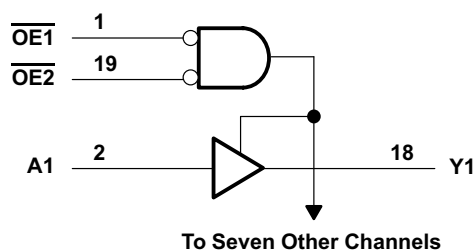
ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted)[1]

		VALUE	UNIT
Supply voltage range, V_{CC}		−0.5 to 7	V
Input voltage range, V_I[2]		−0.5 to 7	V
Output voltage range, V_O[2]		−0.5 to V_{CC} + 0.5	V
Input clamp current, I_{IK} (V_I < 0)		−20	mA
Output clamp current, I_{OK} (V_O < 0 or V_O > V_{CC})		±20	mA
Continuous output current, I_O (V_O = 0 to V_{CC})		±25	mA
Continuous current through V_{CC} or GND		±75	mA
Package thermal impedance, θ_{JA} [3]	DB package	70	°C/W
	DGV package	92	
	DW package	58	
	N package	69	
	NS package	60	
	PW package	83	
Storage temperature range, T_{stg}		−65 to 150	°C

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
(3) The package thermal impedance is calculated in accordance with JESD 51-7.

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Product Folder Links: *SN54AHCT541 SN74AHCT541*

RECOMMENDED OPERATING CONDITIONS[(1)]

		SN54AHCT541		SN74AHCT541		UNIT
		MIN	**MAX**	**MIN**	**MAX**	
V_{CC}	Supply voltage	4.5	5.5	4.5	5.5	V
V_{IH}	High-level input voltage	2		2		V
V_{IL}	Low-level Input voltage		0.8		0.8	V
V_I	Input voltage	0	5.5	0	5.5	V
V_O	Output voltage	0	V_{CC}	0	V_{CC}	V
I_{OH}	High-level output current		−8		−8	mA
I_{OL}	Low-level output current		8		8	mA
Δt/Δv	Input Transition rise or fall rate		20		20	ns/V
T_A	Operating free-air temperature	−55	125	−40	125	°C

(1) All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

ELECTRICAL CHARACTERISTICS

over operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}	T_A = 25°C			T_A = −55°C TO 125°C SN54AHCT541		T_A = −40°C TO 85°C SN74AHCT541		T_A = −40°C TO 125°C Recommended SN74AHCT541		UNIT
			MIN	**TYP**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	
V_{OH}	I_{OH} = −50 µA	4.5 V	4.4	4.5		4.4		4.4		4.4		V
	I_{OH} = −8 mA		3.94			3.8		3.8		3.8		
V_{OL}	I_{OL} = 50 µA	4.5 V			0.1		0.1		0.1		0.1	V
	I_{OH} = 8 mA				0.36		0.44		0.44		0.44	
I_I	V_I = 5.5 V or GND	0 V to 5.5 V			±0.1		±1 [(1)]		±1		±1	µA
I_{OZ}	V_O = V_{CC} or GND	5.5 V			±0.25		±2.5		±2.5		±2.5	
I_{CC}	V_I = V_{CC} or GND, I_O = 0	5.5 V			4		40		20		40	µA
ΔI_{CC}[(2)]	One input at 3.4 V, Other inputs at V_{CC} or GND	5.5 V			1.35		1.5		1.5		1.5	mA
C_i	V_I = V_{CC} or GND	5 V		2	10			10				pF
C_O	V_O = V_{CC} or GND	5V		4								

(1) On products compliant to MIL-PRF-38535, this parameter is not production tested at VCC = 0 V.
(2) This is the increase in supply current for each input at one of the specified TTL voltage levels, rather than 0 V or VCC.

SWITCHING CHARACTERISTICS

over recommended operating free-air temperature range, V_{CC} = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	T_A = 25°C		T_A = −55°C TO 125°C SN54AHCT541		T_A = −40°C TO 85°C SN54AHCT541		T_A = −40°C TO 125°C Recommended SN54AHCT541		UNIT
				TYP	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	A	Y	C_L = 15 pF	4.1[1]	6.0[1]	1[1]	6.5[1]	1	6.5	1	6.5	ns
t_{PHL}				4.1[1]	6.0[1]	1[1]	6.5[1]	1	6.5	1	6.5	
t_{PZH}	$\overline{OE}$	Y	C_L = 15 pF	5.0[1]	7.0[1]	1[1]	8.0[1]	1	8.0	1	8.0	ns
t_{PZL}				5.0[1]	7.0[1]	1[1]	8.0[1]	1	8.0	1	8.0	
t_{PHZ}	$\overline{OE}$	Y	C_L = 15 pF	4.5[1]	7.0[1]	1[1]	8.0[1]	1	8.0	1	8.0	ns
t_{PLZ}				4.5[1]	7.0[1]	1[1]	8.0[1]	1	8.0	1	8.0	
t_{PLH}	A	Y	C_L = 50 pF	6.2	8.5	1	9.5	1	9.5	1	9.5	ns
t_{PHL}				6.2	8.5	1	9.5	1	9.5	1	9.5	
t_{PZH}	$\overline{OE}$	Y	C_L = 50 pF	7.5	10.0	1	12	1	12	1	12	ns
t_{PZL}				7.5	10.0	1	12	1	12	1	12	
t_{PHZ}	$\overline{OE}$	Y	C_L = 50 pF	7.0	10.0	1	12	1	12	1	12	ns
t_{PLZ}				7.0	10.0	1	12	1	12	1	12	
$t_{sk(o)}$			C_L = 50 pF		1[2]				1	1		

(1) On products compliant to MIL-PRF-38535, this parameter is not production tested.
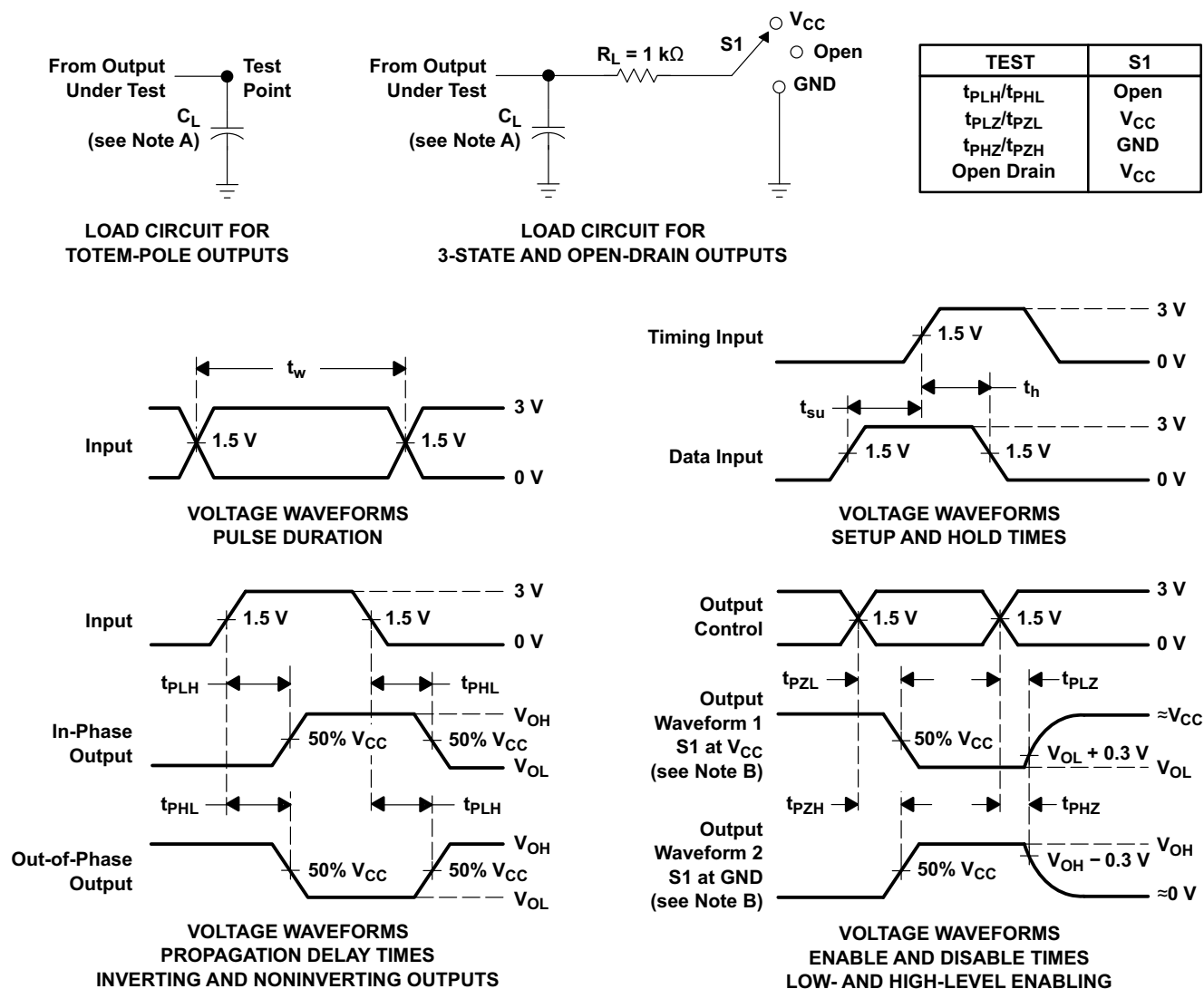(2) On products compliant to MIL-PRF-38535, this parameter does not apply

OPERATING CHARACTERISTICS

V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS		TYP	UNIT
C_{pd}	Power dissipation capacitance	No load,	f = 1 MHz	12	pF

Product Folder Links: *SN54AHCT541 SN74AHCT541*

PARAMETER MEASUREMENT INFORMATION

TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	V_{CC}
t_{PHZ}/t_{PZH}	GND
Open Drain	V_{CC}

**LOAD CIRCUIT FOR
TOTEM-POLE OUTPUTS**

**LOAD CIRCUIT FOR
3-STATE AND OPEN-DRAIN OUTPUTS**

**VOLTAGE WAVEFORMS
PULSE DURATION**

**VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES**

**VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS**

**VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING**

A. C_L includes probe and jig capacitance.

B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control.
   Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.

C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, Z_O = 50 Ω, t_r ≤ 3 ns, t_f ≤ 3 ns.

D. The outputs are measured one at a time with one input transition per measurement.

E. All parameters and waveforms are not applicable to all devices.

Figure 1. Load Circuit and Voltage Waveforms

REVISION HISTORY

Changes from Revision O (July 2003) to Revision P   **Page**

Product Folder Links: *SN54AHCT541 SN74AHCT541*

![Texas Instruments logo]

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
5962-9685801Q2A	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	-55 to 125	5962-9685801Q2A SNJ54AHCT541FK	Samples
5962-9685801QRA	ACTIVE	CDIP	J	20	1	TBD	A42	N / A for Pkg Type	-55 to 125	5962-9685801QRA SNJ54AHCT541J	Samples
5962-9685801QSA	ACTIVE	CFP	W	20	1	TBD	A42	N / A for Pkg Type	-55 to 125	5962-9685801QSA SNJ54AHCT541W	Samples
SN74AHCT541DBLE	OBSOLETE	SSOP	DB	20		TBD	Call TI	Call TI	-40 to 125		
SN74AHCT541DBR	ACTIVE	SSOP	DB	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	HB541	Samples
SN74AHCT541DBRE4	ACTIVE	SSOP	DB	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	HB541	Samples
SN74AHCT541DW	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	AHCT541	Samples
SN74AHCT541DWG4	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	AHCT541	Samples
SN74AHCT541DWR	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	AHCT541	Samples
SN74AHCT541DWRE4	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	AHCT541	Samples
SN74AHCT541N	ACTIVE	PDIP	N	20	20	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	-40 to 125	SN74AHCT541N	Samples
SN74AHCT541NSR	ACTIVE	SO	NS	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	AHCT541	Samples
SN74AHCT541PW	ACTIVE	TSSOP	PW	20	70	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	HB541	Samples
SN74AHCT541PWE4	ACTIVE	TSSOP	PW	20	70	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	HB541	Samples
SN74AHCT541PWG4	ACTIVE	TSSOP	PW	20	70	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	HB541	Samples
SN74AHCT541PWLE	OBSOLETE	TSSOP	PW	20		TBD	Call TI	Call TI	-40 to 125		

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN74AHCT541PWR	ACTIVE	TSSOP	PW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU | CU SN	Level-1-260C-UNLIM	-40 to 125	HB541	Samples
SN74AHCT541PWRE4	ACTIVE	TSSOP	PW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	HB541	Samples
SN74AHCT541PWRG3	ACTIVE	TSSOP	PW	20	2000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	HB541	Samples
SN74AHCT541PWRG4	ACTIVE	TSSOP	PW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	HB541	Samples
SNJ54AHCT541FK	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	-55 to 125	5962-9685801Q2A SNJ54AHCT 541FK	Samples
SNJ54AHCT541J	ACTIVE	CDIP	J	20	1	TBD	A42	N / A for Pkg Type	-55 to 125	5962-9685801QRA SNJ54AHCT541J	Samples
SNJ54AHCT541W	ACTIVE	CFP	W	20	1	TBD	A42	N / A for Pkg Type	-55 to 125	5962-9685801QSA SNJ54AHCT541W	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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OTHER QUALIFIED VERSIONS OF SN54AHCT541, SN74AHCT541 :

● Catalog: SN74AHCT541

● Enhanced Product: SN74AHCT541-EP, SN74AHCT541-EP

● Military: SN54AHCT541

NOTE: Qualified Version Definitions:

　　● Catalog - TI's standard catalog product

　　● Enhanced Product - Supports Defense, Aerospace and Medical Applications

　　● Military - QML certified for Military and Defense Applications

PACKAGE MATERIALS INFORMATION

TAPE AND REEL INFORMATION

REEL DIMENSIONS

TAPE DIMENSIONS

A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74AHCT541DBR	SSOP	DB	20	2000	330.0	16.4	8.2	7.5	2.5	12.0	16.0	Q1
SN74AHCT541DWR	SOIC	DW	20	2000	330.0	24.4	10.8	13.3	2.7	12.0	24.0	Q1
SN74AHCT541NSR	SO	NS	20	2000	330.0	24.4	9.0	13.0	2.4	12.0	24.0	Q1
SN74AHCT541PWR	TSSOP	PW	20	2000	330.0	16.4	6.95	7.1	1.6	8.0	16.0	Q1
SN74AHCT541PWR	TSSOP	PW	20	2000	330.0	16.4	6.95	7.1	1.6	8.0	16.0	Q1
SN74AHCT541PWRG3	TSSOP	PW	20	2000	330.0	16.4	6.95	7.1	1.6	8.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74AHCT541DBR	SSOP	DB	20	2000	367.0	367.0	38.0
SN74AHCT541DWR	SOIC	DW	20	2000	367.0	367.0	45.0
SN74AHCT541NSR	SO	NS	20	2000	367.0	367.0	45.0
SN74AHCT541PWR	TSSOP	PW	20	2000	364.0	364.0	27.0
SN74AHCT541PWR	TSSOP	PW	20	2000	367.0	367.0	38.0
SN74AHCT541PWRG3	TSSOP	PW	20	2000	364.0	364.0	27.0

W (R−GDFP−F20)   CERAMIC DUAL FLATPACK
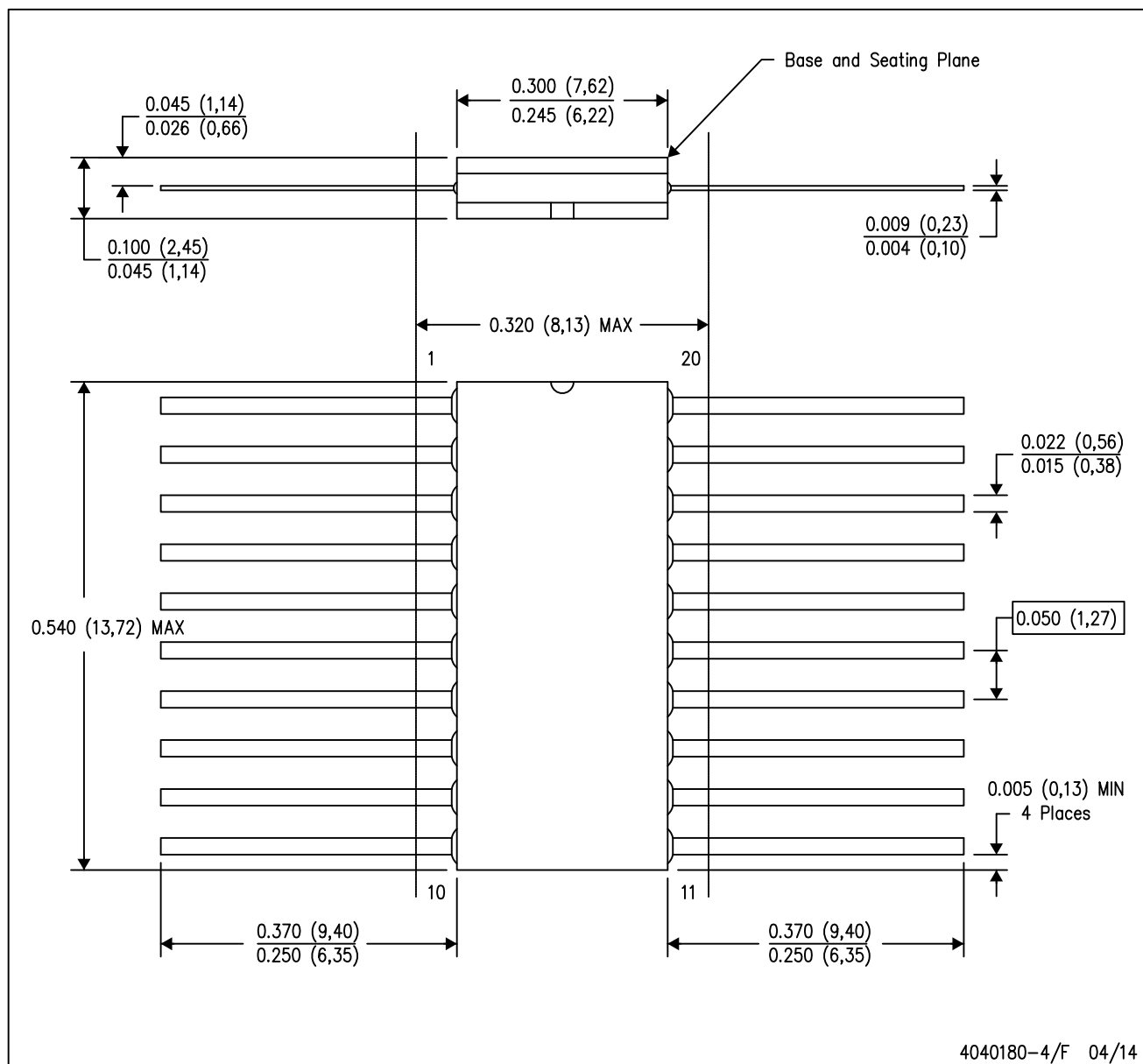
Base and Seating Plane

$\dfrac{0.045\ (1,14)}{0.026\ (0,66)}$

$\dfrac{0.300\ (7,62)}{0.245\ (6,22)}$

$\dfrac{0.100\ (2,45)}{0.045\ (1,14)}$

$\dfrac{0.009\ (0,23)}{0.004\ (0,10)}$

0.320 (8,13) MAX

1   20

$\dfrac{0.022\ (0,56)}{0.015\ (0,38)}$

0.540 (13,72) MAX

0.050 (1,27)

0.005 (0,13) MIN
4 Places

10   11

$\dfrac{0.370\ (9,40)}{0.250\ (6,35)}$ $\dfrac{0.370\ (9,40)}{0.250\ (6,35)}$

4040180−4/F   04/14

NOTES: A.   All linear dimensions are in inches (millimeters).
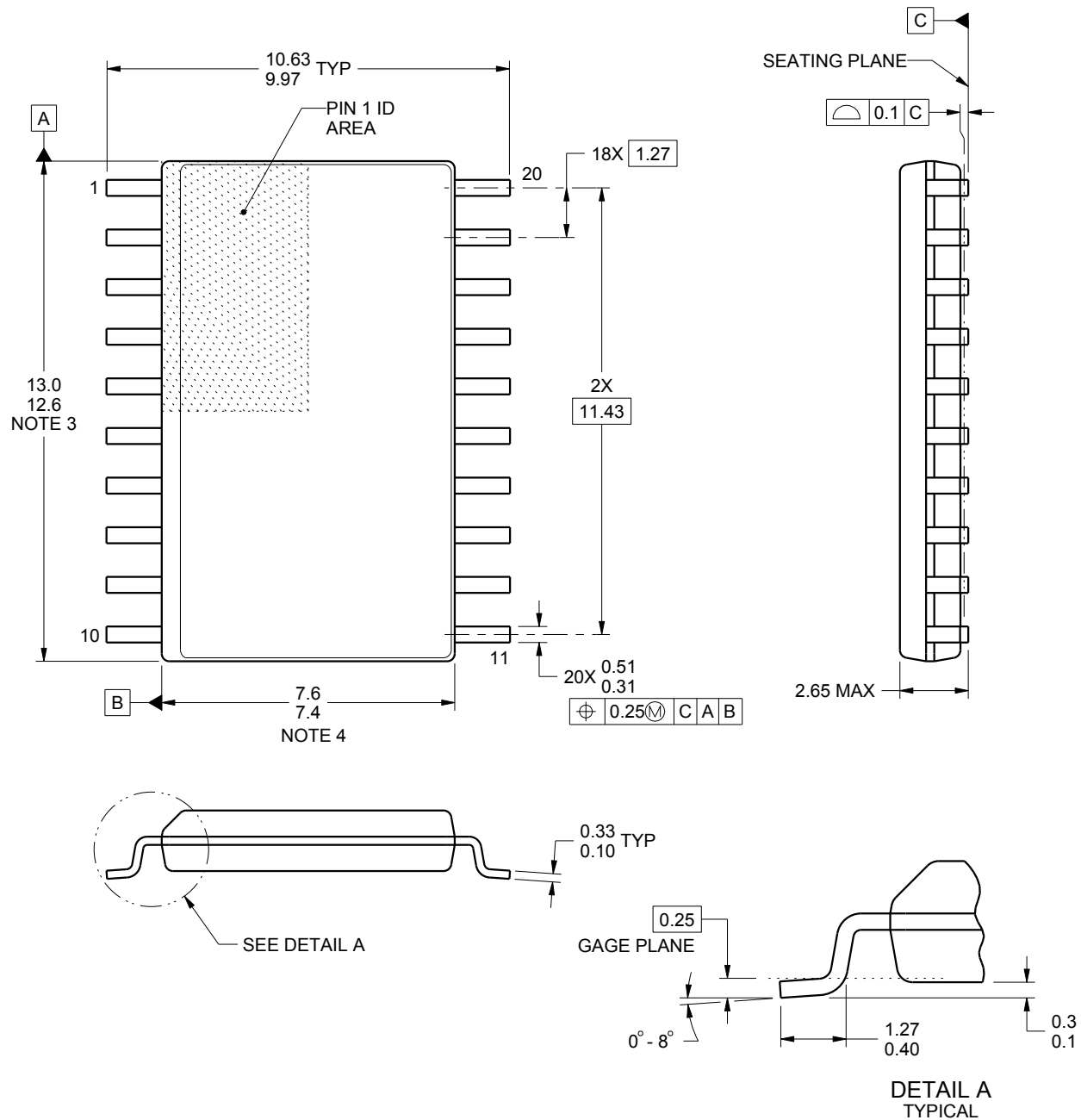   B.   This drawing is subject to change without notice.
         C.   This package can be hermetically sealed with a ceramic lid using glass frit.
         D.   Index point is provided on cap for terminal identification only.
         E.   Falls within Mil−Std 1835 GDFP2−F20

FK (S−CQCC−N**)
28 TERMINAL SHOWN

LEADLESS CERAMIC CHIP CARRIER
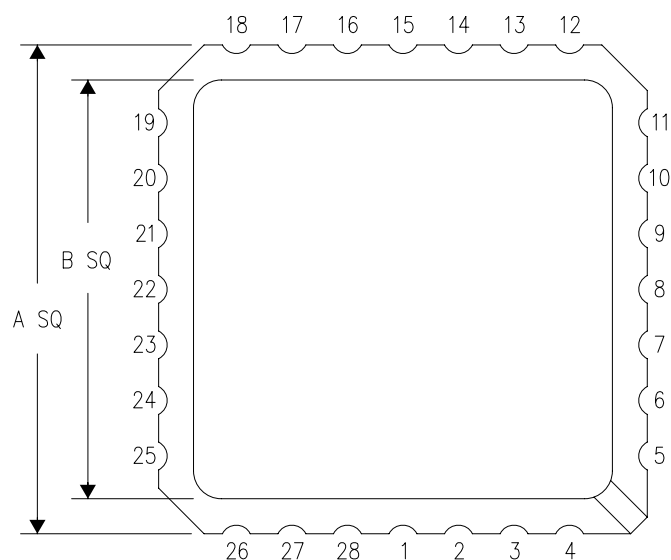
NO. OF TERMINALS **	A		B	
	MIN	MAX	MIN	MAX
20	0.342 (8,69)	0.358 (9,09)	0.307 (7,80)	0.358 (9,09)
28	0.442 (11,23)	0.458 (11,63)	0.406 (10,31)	0.458 (11,63)
44	0.640 (16,26)	0.660 (16,76)	0.495 (12,58)	0.560 (14,22)
52	0.740 (18,78)	0.761 (19,32)	0.495 (12,58)	0.560 (14,22)
68	0.938 (23,83)	0.962 (24,43)	0.850 (21,6)	0.858 (21,8)
84	1.141 (28,99)	1.165 (29,59)	1.047 (26,6)	1.063 (27,0)

$\frac{0.020 \ (0,51)}{0.010 \ (0,25)}$

$\frac{0.020 \ (0,51)}{0.010 \ (0,25)}$

$\frac{0.080 \ (2,03)}{0.064 \ (1,63)}$

$\frac{0.055 \ (1,40)}{0.045 \ (1,14)}$

$\frac{0.045 \ (1,14)}{0.035 \ (0,89)}$

$\frac{0.028 \ (0,71)}{0.022 \ (0,54)}$

0.050 (1,27)

$\frac{0.045 \ (1,14)}{0.035 \ (0,89)}$
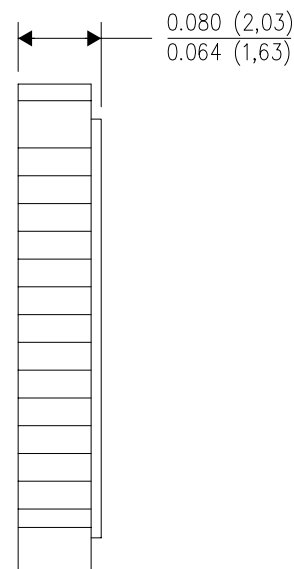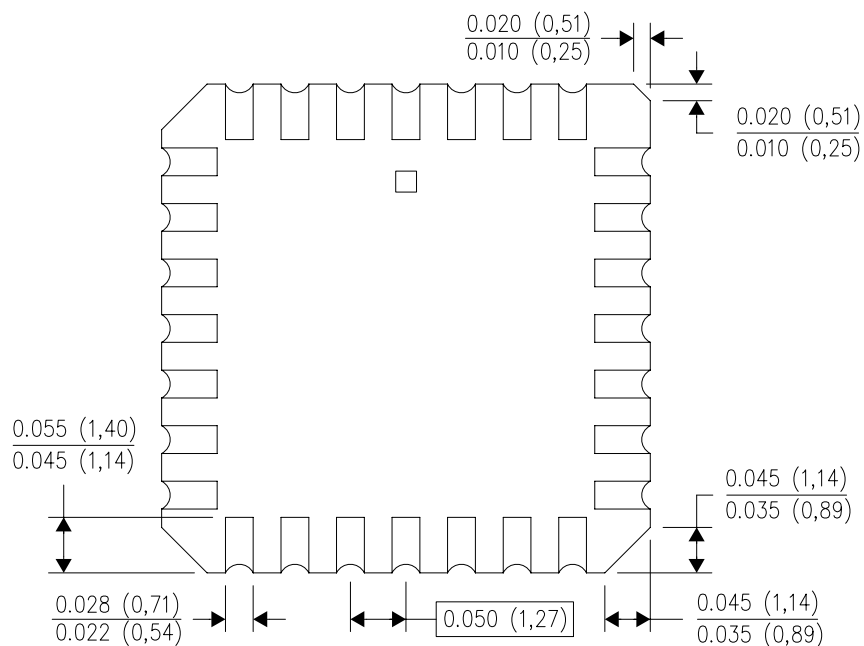
4040140/D 01/11

NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package can be hermetically sealed with a metal lid.
D. Falls within JEDEC MS−004

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NS (R-PDSO-G)** PLASTIC SMALL-OUTLINE PACKAGE

14-PINS SHOWN
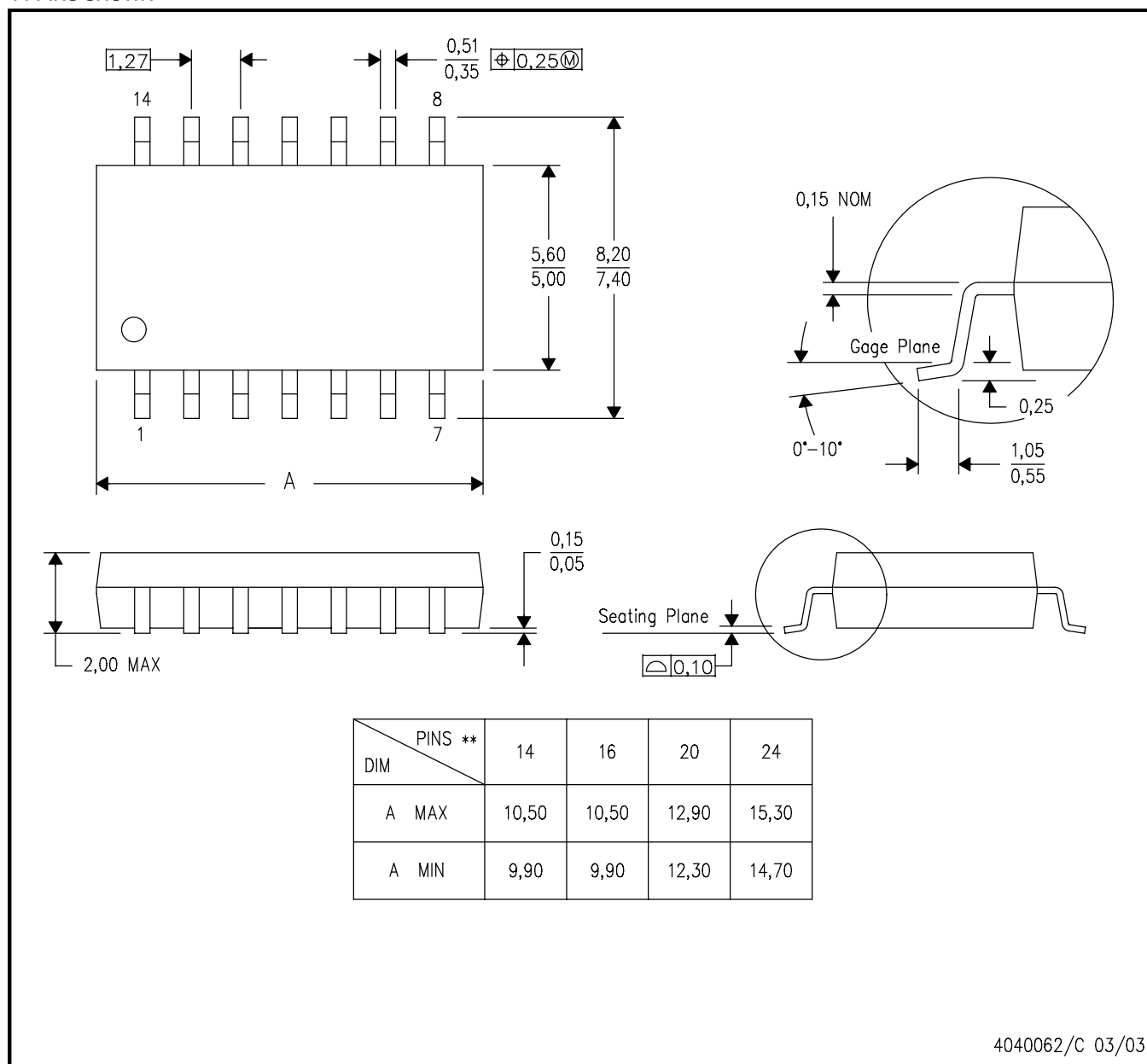
DIM	PINS **	14	16	20	24
A MAX		10,50	10,50	12,90	15,30
A MIN		9,90	9,90	12,30	14,70

4040062/C 03/03

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.
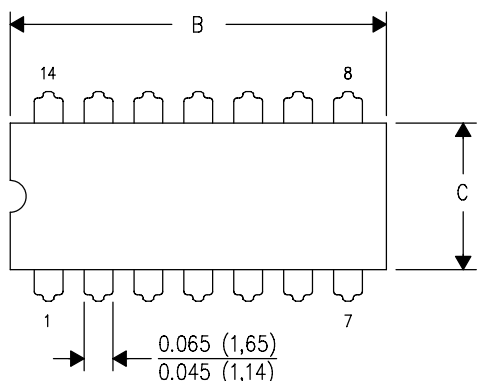
PINS ** DIM	14	16	18	20
[A]	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	——	——	——	——
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)

B

14   8

C

1   7

0.065 (1,65)
0.045 (1,14)

0.005 (0,13) MIN

0.060 (1,52)
0.015 (0,38)

0.200 (5,08) MAX

Seating Plane

0.130 (3,30) MIN

0.026 (0,66)
0.014 (0,36)

0.100 (2,54)

[A]

0°−15°

0.014 (0,36)
0.008 (0,20)
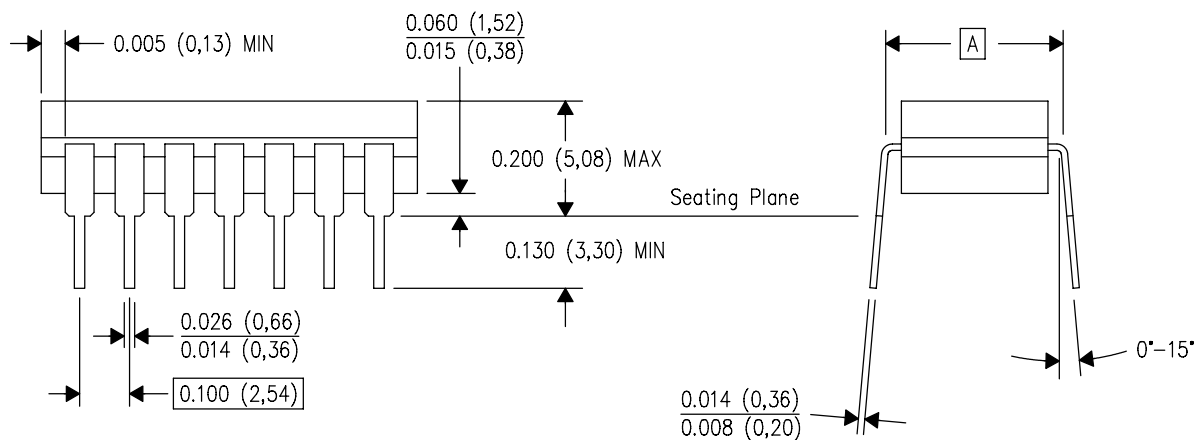
4040083/F 03/03

NOTES: A.   All linear dimensions are in inches (millimeters).
         B.   This drawing is subject to change without notice.
         C.   This package is hermetically sealed with a ceramic lid using glass frit.
         D.   Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
         E.   Falls within MIL STD 1835 GDIP1−T14, GDIP1−T16, GDIP1−T18 and GDIP1−T20.

PW (R−PDSO−G20)   PLASTIC SMALL OUTLINE

0,65   0,30   ⊕ | 0,10 Ⓜ
           0,19

20   11

⧊D 4,50   6,60
    4,30   6,20

1   10

6,60
6,40
△C

0,15 NOM

Gage Plane

0°−8°   0,25

0,75
0,50

1,20 MAX   0,15
               0,05

Seating Plane

⬠ | 0,10
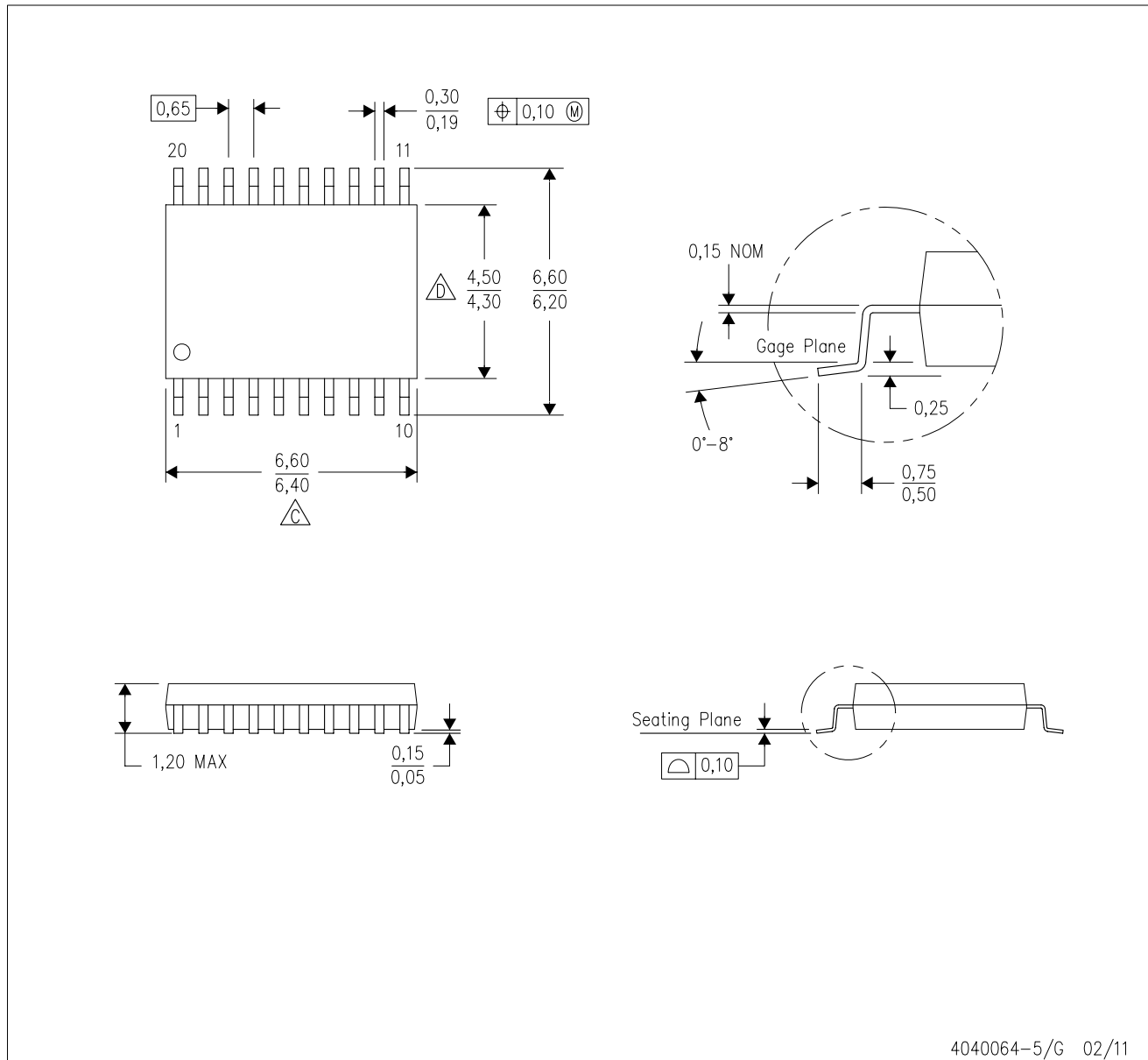
4040064−5/G 02/11

NOTES: A.   All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M−1994.
         B.   This drawing is subject to change without notice.
        △C   Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall
              not exceed 0,15 each side.
        △D   Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
         E.   Falls within JEDEC MO−153
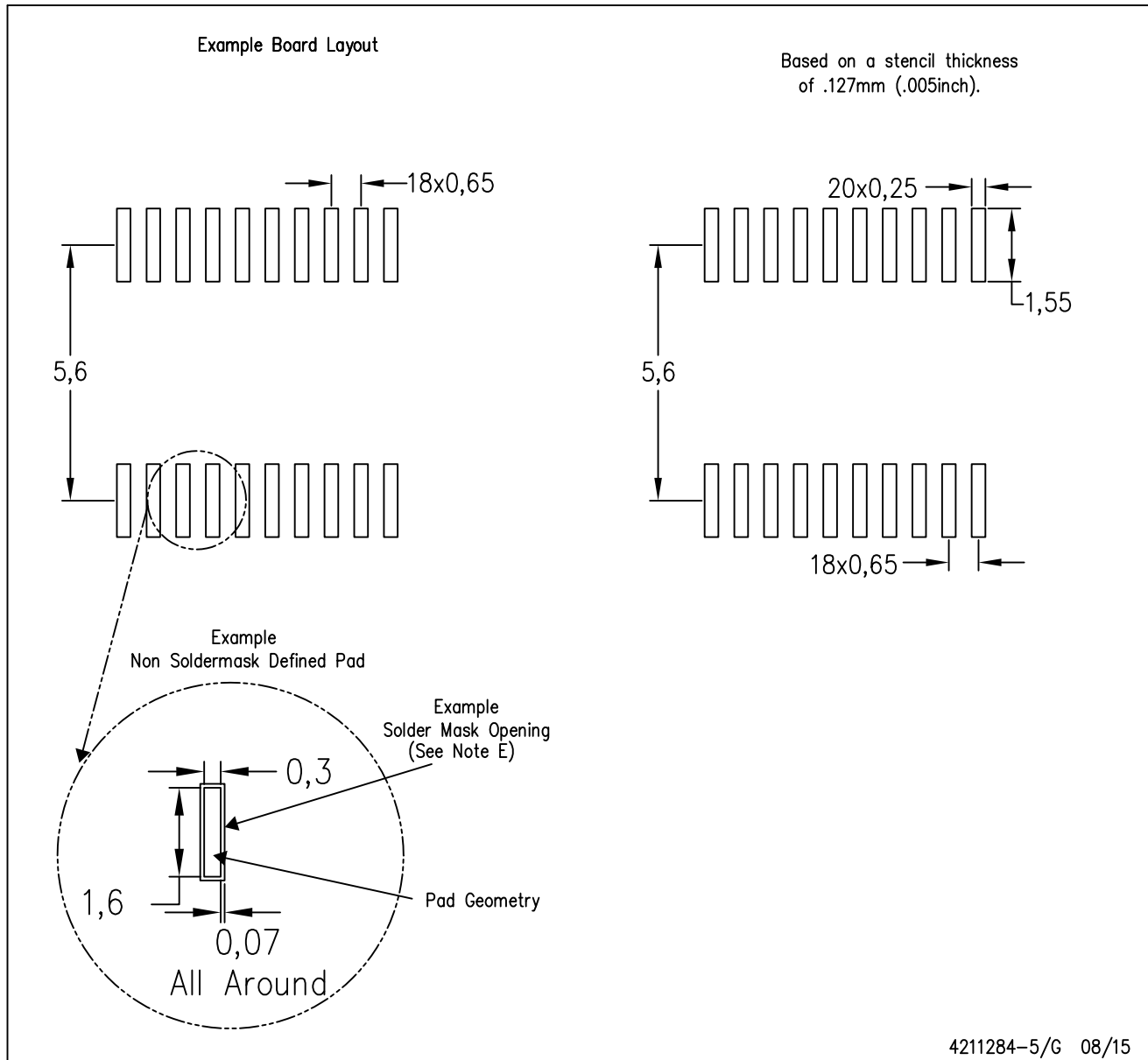
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PW (R–PDSO–G20)   PLASTIC SMALL OUTLINE

Example Board Layout

Based on a stencil thickness
of .127mm (.005inch).

18x0,65

20x0,25

1,55

5,6

5,6

18x0,65

Example
Non Soldermask Defined Pad

Example
Solder Mask Opening
(See Note E)

0,3

1,6

Pad Geometry

0,07
All Around

4211284–5/G   08/15

NOTES: A.   All linear dimensions are in millimeters.
         B.   This drawing is subject to change without notice.
         C.   Publication IPC–7351 is recommended for alternate design.
         D.   Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should
              contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
         E.   Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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DB (R-PDSO-G**)   **PLASTIC SMALL-OUTLINE**

28 PINS SHOWN

PINS ** / DIM	14	16	20	24	28	30	38
A MAX	6,50	6,50	7,50	8,50	10,50	10,50	12,90
A MIN	5,90	5,90	6,90	7,90	9,90	9,90	12,30

4040065 /E 12/01

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
D. Falls within JEDEC MO-150

N (R−PDIP−T**) PLASTIC DUAL−IN−LINE PACKAGE

16 PINS SHOWN
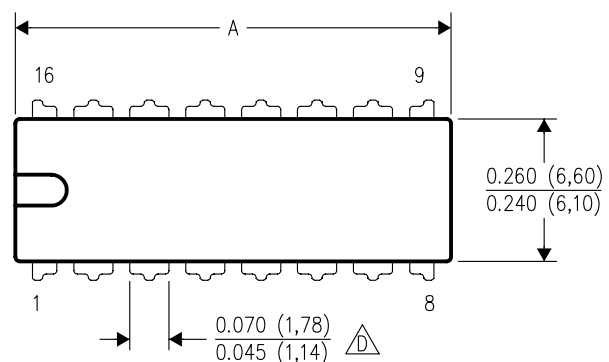
DIM \ PINS **	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
△C△ MS−001 VARIATION	AA	BB	AC	AD

0.260 (6,60) / 0.240 (6,10)

0.070 (1,78) / 0.045 (1,14) △D△

0.045 (1,14) / 0.030 (0,76) △D△

0.020 (0,51) MIN

0.200 (5,08) MAX

Seating Plane

0.125 (3,18) MIN

0.100 (2,54)

0.021 (0,53) / 0.015 (0,38)

⊕ 0.010 (0,25) Ⓜ

0.325 (8,26) / 0.300 (7,62)

0.015 (0,38)

Gauge Plane

0.010 (0,25) NOM

0.430 (10,92) MAX

14/18 Pin Only
20 Pin vendor option △D△
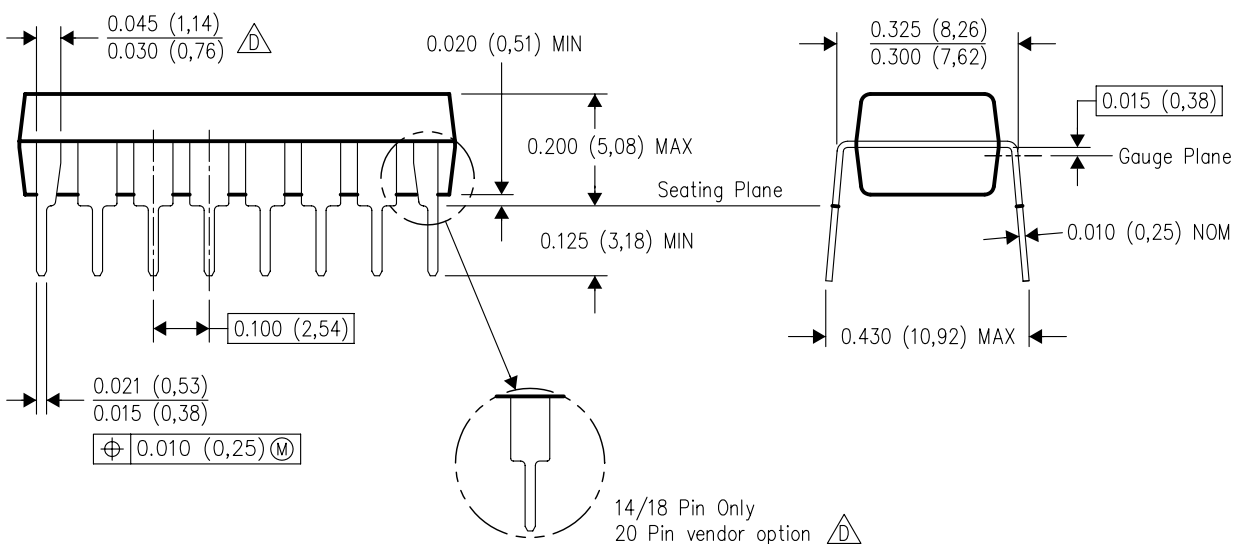
4040049/E   12/2002

NOTES: A. All linear dimensions are in inches (millimeters).
        B. This drawing is subject to change without notice.
        △C△ Falls within JEDEC MS−001, except 18 and 20 pin minimum body length (Dim A).
        △D△ The 20 pin end lead shoulder width is a vendor option, either half or full width.

10.63 / 9.97 TYP

A

PIN 1 ID
AREA

1

18X 1.27

20

2X
11.43

13.0
12.6
NOTE 3

10

11

B

7.6
7.4
NOTE 4

20X 0.51 / 0.31

⊕ 0.25ⓂC A B

C ◄

SEATING PLANE

⌒ 0.1 C

2.65 MAX

SEE DETAIL A

0.33 / 0.10 TYP

0.25
GAGE PLANE

0° - 8°

1.27
0.40

0.3
0.1

DETAIL A
TYPICAL

4220724/A 05/2016

NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing
   per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not
   exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm per side.
5. Reference JEDEC registration MS-013.

20X (2)

1

20X (0.6)

18X (1.27)

SYMM

20

SYMM

(R0.05)
TYP

10

11

(9.3)
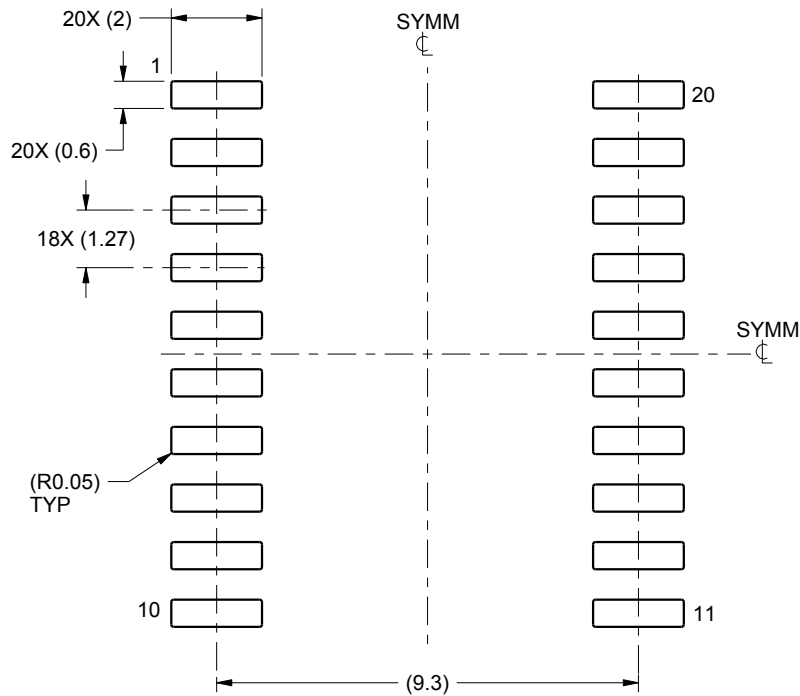
LAND PATTERN EXAMPLE
SCALE:6X

SOLDER MASK
OPENING

METAL

0.07 MAX
ALL AROUND

**NON SOLDER MASK
DEFINED**

METAL UNDER
SOLDER MASK

SOLDER MASK
OPENING

0.07 MIN
ALL AROUND

**SOLDER MASK
DEFINED**
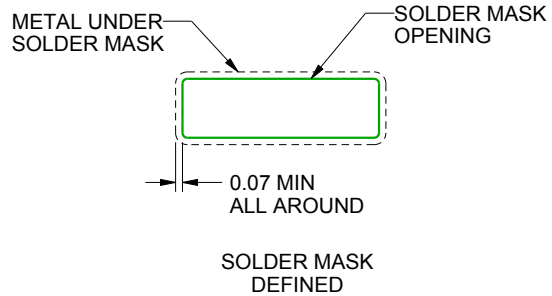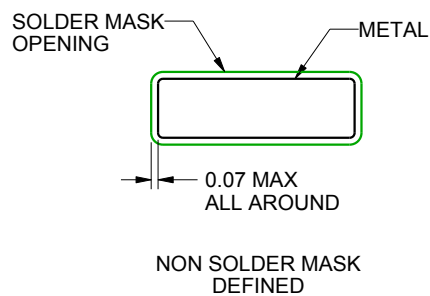
SOLDER MASK DETAILS

4220724/A   05/2016

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

20X (2)

1

20X (0.6)

18X (1.27)

SYMM

SYMM

20

10

11

(9.3)
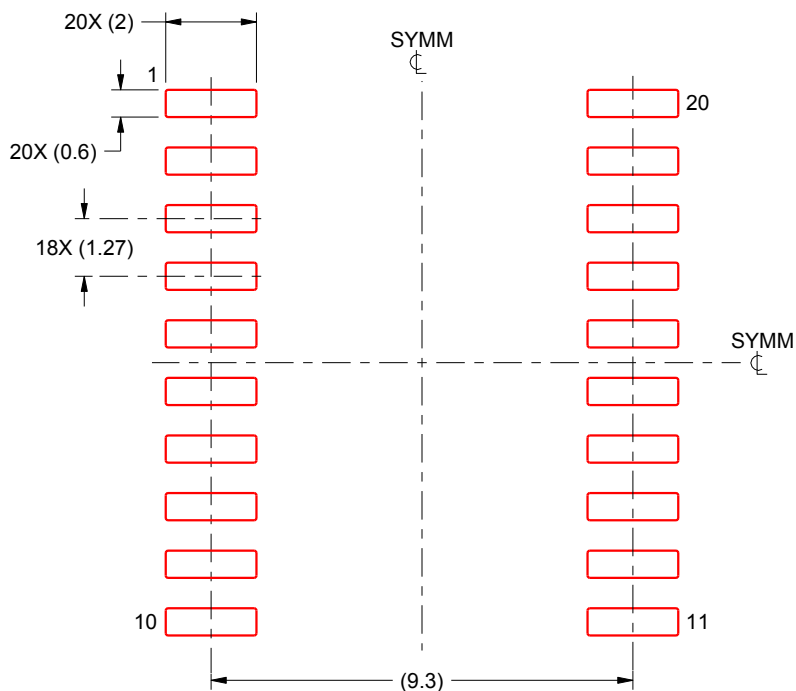
SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:6X

4220724/A   05/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate
   design recommendations.
9. Board assembly site may have different recommendations for stencil design.

IMPORTANT NOTICE