

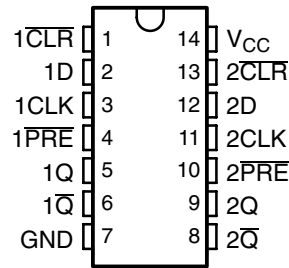
# SN74LV74A-Q1

## DUAL POSITIVE-EDGE-TRIGGERED D-TYPE FLIP-FLOP

SCLS556B – DECEMBER 2003 – REVISED APRIL 2008

- Qualified for Automotive Applications
- 2-V to 5.5-V  $V_{CC}$  Operation
- Max  $t_{pd}$  of 13 ns at 5 V
- Typical  $V_{OLP}$  (Output Ground Bounce)  
<0.8 V at  $V_{CC} = 3.3$  V,  $T_A = 25^\circ\text{C}$
- Typical  $V_{OHV}$  (Output  $V_{OH}$  Undershoot)  
>2.3 V at  $V_{CC} = 3.3$  V,  $T_A = 25^\circ\text{C}$
- Support Mixed-Mode Voltage Operation on All Ports
- $I_{off}$  Supports Partial-Power-Down Mode Operation
- Latch-Up Performance Exceeds 250 mA Per JESD 17
- ESD Protection Exceeds JESD 22
  - 2000-V Human-Body Model (A114-A)
  - 200-V Machine Model (A115-A)
  - 1000-V Charged-Device Model (C101)

D OR PW PACKAGE  
(TOP VIEW)



### description/ordering informationS

This dual positive-edge-triggered D-type flip-flop is designed for 2-V to 5.5-V  $V_{CC}$  operation.

A low level at the preset ( $\overline{PRE}$ ) or clear ( $\overline{CLR}$ ) inputs sets or resets the outputs, regardless of the levels of the other inputs. When  $\overline{PRE}$  and  $\overline{CLR}$  are inactive (high), data at the data (D) inputs meeting the setup-time requirements is transferred to the outputs on the positive-going edge of the clock pulse. Clock triggering occurs at a voltage level and is not directly related to the rise time of the clock pulse. Following the hold-time interval, data at the D input can be changed without affecting the levels at the outputs.

This device is fully specified for partial-power-down applications using  $I_{off}$ . The  $I_{off}$  circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.

### ORDERING INFORMATION†

| $T_A$          | PACKAGE‡   |               | ORDERABLE PART NUMBER | TOP-SIDE MARKING |
|----------------|------------|---------------|-----------------------|------------------|
| -40°C to 125°C | SOIC – D   | Tape and reel | SN74LV74AQDRQ1        | LV74A            |
|                | TSSOP – PW | Tape and reel | SN74LV74AQPWRQ1       | LV74A            |

† For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at <http://www.ti.com>.

‡ Package drawings, thermal data, and symbolization are available at <http://www.ti.com/packaging>.



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PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

**TEXAS  
INSTRUMENTS**

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# SN74LV74A-Q1

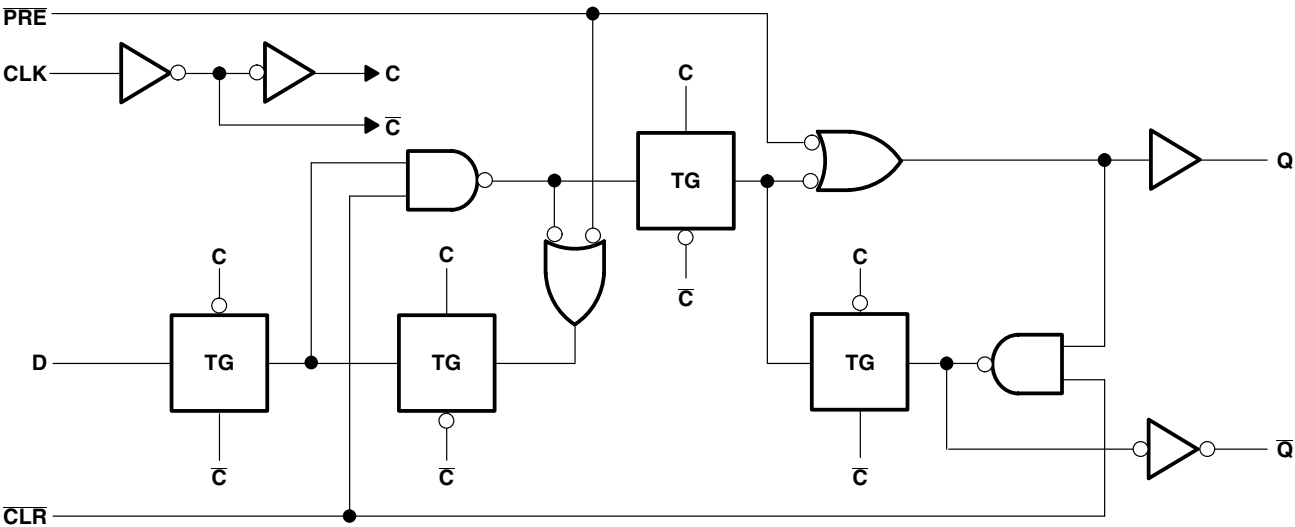
## DUAL POSITIVE-EDGE-TRIGGERED D-TYPE FLIP-FLOP

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| FUNCTION TABLE |     |     |   |                |                  |
|----------------|-----|-----|---|----------------|------------------|
| INPUTS         |     |     |   | OUTPUTS        |                  |
| PRE            | CLR | CLK | D | Q              | $\overline{Q}$   |
| L              | H   | X   | X | H              | L                |
| H              | L   | X   | X | L              | H                |
| L              | L   | X   | X | H <sup>†</sup> | H <sup>†</sup>   |
| H              | H   | ↑   | H | H              | L                |
| H              | H   | ↑   | L | L              | H                |
| H              | H   | L   | X | Q <sub>0</sub> | $\overline{Q}_0$ |

<sup>†</sup> This configuration is nonstable; that is, it does not persist when PRE or CLR returns to its inactive (high) level.

### logic diagram, each flip-flop (positive logic)



### absolute maximum ratings over operating free-air temperature range (unless otherwise noted)<sup>‡</sup>

|                                                                                                  |                            |
|--------------------------------------------------------------------------------------------------|----------------------------|
| Supply voltage range, $V_{CC}$                                                                   | −0.5 V to 7 V              |
| Input voltage range, $V_I$ (see Note 1)                                                          | −0.5 V to 7 V              |
| Voltage range applied to any output in the high-impedance or power-off state, $V_O$ (see Note 1) | −0.5 V to 7 V              |
| Output voltage range, $V_O$ (see Notes 1 and 2)                                                  | −0.5 V to $V_{CC} + 0.5$ V |
| Input clamp current, $I_{IK}$ ( $V_I < 0$ )                                                      | −20 mA                     |
| Output clamp current, $I_{OK}$ ( $V_O < 0$ )                                                     | −50 mA                     |
| Continuous output current, $I_O$ ( $V_O = 0$ to $V_{CC}$ )                                       | ±25 mA                     |
| Continuous current through $V_{CC}$ or GND                                                       | ±50 mA                     |
| Package thermal impedance, $\theta_{JA}$ (see Note 3): D package                                 | 86°C/W                     |
| PW package                                                                                       | 113°C/W                    |
| Storage temperature range, $T_{stg}$                                                             | −65°C to 150°C             |

<sup>‡</sup> Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output current ratings are observed.  
2. This value is limited to 5.5 V maximum.  
3. The package thermal impedance is calculated in accordance with JESD 51-7.

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## DUAL POSITIVE-EDGE-TRIGGERED D-TYPE FLIP-FLOP

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### recommended operating conditions (see Note 4)

|                     |                                    | MIN                                     | MAX                 | UNIT               |
|---------------------|------------------------------------|-----------------------------------------|---------------------|--------------------|
| $V_{CC}$            | Supply voltage                     | 2                                       | 5.5                 | V                  |
| $V_{IH}$            | High-level input voltage           | $V_{CC} = 2\text{ V}$                   | 1.5                 | V                  |
|                     |                                    | $V_{CC} = 2.3\text{ V to }2.7\text{ V}$ | $V_{CC} \times 0.7$ |                    |
|                     |                                    | $V_{CC} = 3\text{ V to }3.6\text{ V}$   | $V_{CC} \times 0.7$ |                    |
|                     |                                    | $V_{CC} = 4.5\text{ V to }5.5\text{ V}$ | $V_{CC} \times 0.7$ |                    |
| $V_{IL}$            | Low-level input voltage            | $V_{CC} = 2\text{ V}$                   | 0.5                 | V                  |
|                     |                                    | $V_{CC} = 2.3\text{ V to }2.7\text{ V}$ | $V_{CC} \times 0.3$ |                    |
|                     |                                    | $V_{CC} = 3\text{ V to }3.6\text{ V}$   | $V_{CC} \times 0.3$ |                    |
|                     |                                    | $V_{CC} = 4.5\text{ V to }5.5\text{ V}$ | $V_{CC} \times 0.3$ |                    |
| $V_I$               | Input voltage                      | 0                                       | 5.5                 | V                  |
| $V_O$               | Output voltage                     | 0                                       | $V_{CC}$            | V                  |
| $I_{OH}$            | High-level output current          | $V_{CC} = 2\text{ V}$                   | -50                 | $\mu\text{A}$      |
|                     |                                    | $V_{CC} = 2.3\text{ V to }2.7\text{ V}$ | -2                  | mA                 |
|                     |                                    | $V_{CC} = 3\text{ V to }3.6\text{ V}$   | -6                  |                    |
|                     |                                    | $V_{CC} = 4.5\text{ V to }5.5\text{ V}$ | -12                 |                    |
| $I_{OL}$            | Low-level output current           | $V_{CC} = 2\text{ V}$                   | 50                  | $\mu\text{A}$      |
|                     |                                    | $V_{CC} = 2.3\text{ V to }2.7\text{ V}$ | 2                   | mA                 |
|                     |                                    | $V_{CC} = 3\text{ V to }3.6\text{ V}$   | 6                   |                    |
|                     |                                    | $V_{CC} = 4.5\text{ V to }5.5\text{ V}$ | 12                  |                    |
| $\Delta t/\Delta v$ | Input transition rise or fall rate | $V_{CC} = 2.3\text{ V to }2.7\text{ V}$ | 200                 | ns/V               |
|                     |                                    | $V_{CC} = 3\text{ V to }3.6\text{ V}$   | 100                 |                    |
|                     |                                    | $V_{CC} = 4.5\text{ V to }5.5\text{ V}$ | 20                  |                    |
| $T_A$               | Operating free-air temperature     | -40                                     | 125                 | $^{\circ}\text{C}$ |

NOTE 4: All unused inputs of the device must be held at  $V_{CC}$  or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

### electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | TEST CONDITIONS                   | $V_{CC}$     | MIN          | TYP | MAX     | UNIT          |
|-----------|-----------------------------------|--------------|--------------|-----|---------|---------------|
| $V_{OH}$  | $I_{OH} = -50\text{ }\mu\text{A}$ | 2 V to 5.5 V | $V_{CC}-0.1$ |     |         | V             |
|           | $I_{OH} = -2\text{ mA}$           | 2.3 V        | 2            |     |         |               |
|           | $I_{OH} = -6\text{ mA}$           | 3 V          | 2.48         |     |         |               |
|           | $I_{OH} = -12\text{ mA}$          | 4.5 V        | 3.8          |     |         |               |
| $V_{OL}$  | $I_{OL} = 50\text{ }\mu\text{A}$  | 2 V to 5.5 V |              |     | 0.1     | V             |
|           | $I_{OL} = 2\text{ mA}$            | 2.3 V        |              |     | 0.4     |               |
|           | $I_{OL} = 6\text{ mA}$            | 3 V          |              |     | 0.44    |               |
|           | $I_{OL} = 12\text{ mA}$           | 4.5 V        |              |     | 0.55    |               |
| $I_I$     | $V_I = 5.5\text{ V or GND}$       | 0 to 5.5 V   |              |     | $\pm 1$ | $\mu\text{A}$ |
| $I_{CC}$  | $V_I = V_{CC}$ or GND, $I_O = 0$  | 5.5 V        |              |     | 20      | $\mu\text{A}$ |
| $I_{off}$ | $V_I$ or $V_O = 0$ to 5.5 V       | 0            |              |     | 5       | $\mu\text{A}$ |
| $C_i$     | $V_I = V_{CC}$ or GND             | 3.3 V        |              | 2   |         | pF            |
|           |                                   | 5 V          |              | 2   |         |               |



# SN74LV74A-Q1

## DUAL POSITIVE-EDGE-TRIGGERED D-TYPE FLIP-FLOP

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**timing requirements over recommended operating free-air temperature range,  $V_{CC} = 2.5\text{ V} \pm 0.2\text{ V}$  (unless otherwise noted) (see Figure 1)**

| PARAMETER                                  |                                         | $T_A = 25^\circ\text{C}$ |     | MIN | MAX | UNIT |
|--------------------------------------------|-----------------------------------------|--------------------------|-----|-----|-----|------|
|                                            |                                         | MIN                      | MAX |     |     |      |
| $t_w$ Pulse duration                       | PRE or $\overline{\text{CLR}}$ low      | 8                        |     | 9   |     | ns   |
|                                            | CLK                                     | 8                        |     | 9   |     |      |
| $t_{su}$ Setup time before CLK $\uparrow$  | Data                                    | 8                        |     | 9   |     | ns   |
|                                            | PRE or $\overline{\text{CLR}}$ inactive | 7                        |     | 7   |     |      |
| $t_h$ Hold time, data after CLK $\uparrow$ |                                         | 0.5                      |     | 0.5 |     | ns   |

**timing requirements over recommended operating free-air temperature range,  $V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$  (unless otherwise noted) (see Figure 1)**

| PARAMETER                                  |                                         | $T_A = 25^\circ\text{C}$ |     | MIN | MAX | UNIT |
|--------------------------------------------|-----------------------------------------|--------------------------|-----|-----|-----|------|
|                                            |                                         | MIN                      | MAX |     |     |      |
| $t_w$ Pulse duration                       | PRE or $\overline{\text{CLR}}$ low      | 6                        |     | 7   |     | ns   |
|                                            | CLK                                     | 6                        |     | 7   |     |      |
| $t_{su}$ Setup time before CLK $\uparrow$  | Data                                    | 6                        |     | 7   |     | ns   |
|                                            | PRE or $\overline{\text{CLR}}$ inactive | 5                        |     | 5   |     |      |
| $t_h$ Hold time, data after CLK $\uparrow$ |                                         | 0.5                      |     | 0.5 |     | ns   |

**timing requirements over recommended operating free-air temperature range,  $V_{CC} = 5\text{ V} \pm 0.5\text{ V}$  (unless otherwise noted) (see Figure 1)**

| PARAMETER                                  |                                         | $T_A = 25^\circ\text{C}$ |     | MIN | MAX | UNIT |
|--------------------------------------------|-----------------------------------------|--------------------------|-----|-----|-----|------|
|                                            |                                         | MIN                      | MAX |     |     |      |
| $t_w$ Pulse duration                       | PRE or $\overline{\text{CLR}}$ low      | 5                        |     | 5   |     | ns   |
|                                            | CLK                                     | 5                        |     | 5   |     |      |
| $t_{su}$ Setup time before CLK $\uparrow$  | Data                                    | 5                        |     | 5   |     | ns   |
|                                            | PRE or $\overline{\text{CLR}}$ inactive | 3                        |     | 3   |     |      |
| $t_h$ Hold time, data after CLK $\uparrow$ |                                         | 0.5                      |     | 0.5 |     | ns   |

**switching characteristics over recommended operating free-air temperature range,  $V_{CC} = 2.5\text{ V} \pm 0.2\text{ V}$  (unless otherwise noted) (see Figure 1)**

| PARAMETER | FROM (INPUT)                                       | TO (OUTPUT)         | LOAD CAPACITANCE     | $T_A = 25^\circ\text{C}$ |      |      | MIN | MAX | UNIT |
|-----------|----------------------------------------------------|---------------------|----------------------|--------------------------|------|------|-----|-----|------|
|           |                                                    |                     |                      | MIN                      | TYP  | MAX  |     |     |      |
| $f_{max}$ |                                                    |                     | $C_L = 50\text{ pF}$ | 30                       | 70   |      | 25  |     | MHz  |
| $t_{pd}$  | $\overline{\text{PRE}}$ or $\overline{\text{CLR}}$ | Q or $\overline{Q}$ | $C_L = 50\text{ pF}$ |                          | 13   | 17.4 | 1   | 20  | ns   |
|           | CLK                                                |                     |                      |                          | 14.2 | 20   | 1   | 23  |      |

**switching characteristics over recommended operating free-air temperature range,  $V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$  (unless otherwise noted) (see Figure 1)**

| PARAMETER | FROM (INPUT)                                       | TO (OUTPUT)         | LOAD CAPACITANCE     | $T_A = 25^\circ\text{C}$ |      |      | MIN | MAX | UNIT |
|-----------|----------------------------------------------------|---------------------|----------------------|--------------------------|------|------|-----|-----|------|
|           |                                                    |                     |                      | MIN                      | TYP  | MAX  |     |     |      |
| $f_{max}$ |                                                    |                     | $C_L = 50\text{ pF}$ | 50                       | 90   |      | 45  |     | MHz  |
| $t_{pd}$  | $\overline{\text{PRE}}$ or $\overline{\text{CLR}}$ | Q or $\overline{Q}$ | $C_L = 50\text{ pF}$ |                          | 9.2  | 15.8 | 1   | 18  | ns   |
|           | CLK                                                |                     |                      |                          | 10.2 | 15.4 | 1   | 18  |      |



# SN74LV74A-Q1

## DUAL POSITIVE-EDGE-TRIGGERED D-TYPE FLIP-FLOP

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**switching characteristics over recommended operating free-air temperature range,  $V_{CC} = 5\text{ V} \pm 0.5\text{ V}$  (unless otherwise noted) (see Figure 1)**

| PARAMETER  | FROM<br>(INPUT) | TO<br>(OUTPUT) | LOAD<br>CAPACITANCE  | $T_A = 25^\circ\text{C}$ |     |     | MIN | MAX | UNIT |
|------------|-----------------|----------------|----------------------|--------------------------|-----|-----|-----|-----|------|
|            |                 |                |                      | MIN                      | TYP | MAX |     |     |      |
| $f_{\max}$ |                 |                | $C_L = 50\text{ pF}$ | 90                       | 140 |     | 75  |     | MHz  |
| $t_{pd}$   | PRE or CLR      | Q or $\bar{Q}$ | $C_L = 50\text{ pF}$ |                          | 6.6 | 9.7 | 1   | 12  | ns   |
|            | CLK             |                |                      |                          | 7.2 | 9.3 | 1   | 13  |      |

**noise characteristics,  $V_{CC} = 3.3\text{ V}$ ,  $C_L = 50\text{ pF}$ ,  $T_A = 25^\circ\text{C}$  (see Note 5)**

| PARAMETER   |                                        | MIN  | TYP | MAX  | UNIT |
|-------------|----------------------------------------|------|-----|------|------|
| $V_{OL(P)}$ | Quiet output, maximum dynamic $V_{OL}$ |      | 0.1 | 0.8  | V    |
| $V_{OL(V)}$ | Quiet output, minimum dynamic $V_{OL}$ |      | 0   | -0.8 | V    |
| $V_{OH(V)}$ | Quiet output, minimum dynamic $V_{OH}$ |      | 3.2 |      | V    |
| $V_{IH(D)}$ | High-level dynamic input voltage       | 2.31 |     |      | V    |
| $V_{IL(D)}$ | Low-level dynamic input voltage        |      |     | 0.99 | V    |

NOTE 5: Characteristics are for surface-mount packages only.

**operating characteristics,  $T_A = 25^\circ\text{C}$**

| PARAMETER |                               | TEST CONDITIONS                            | $V_{CC}$ | TYP | UNIT |
|-----------|-------------------------------|--------------------------------------------|----------|-----|------|
| $C_{pd}$  | Power dissipation capacitance | $C_L = 50\text{ pF}$ , $f = 10\text{ MHz}$ | 3.3 V    | 21  | pF   |
|           |                               |                                            | 5 V      | 23  |      |

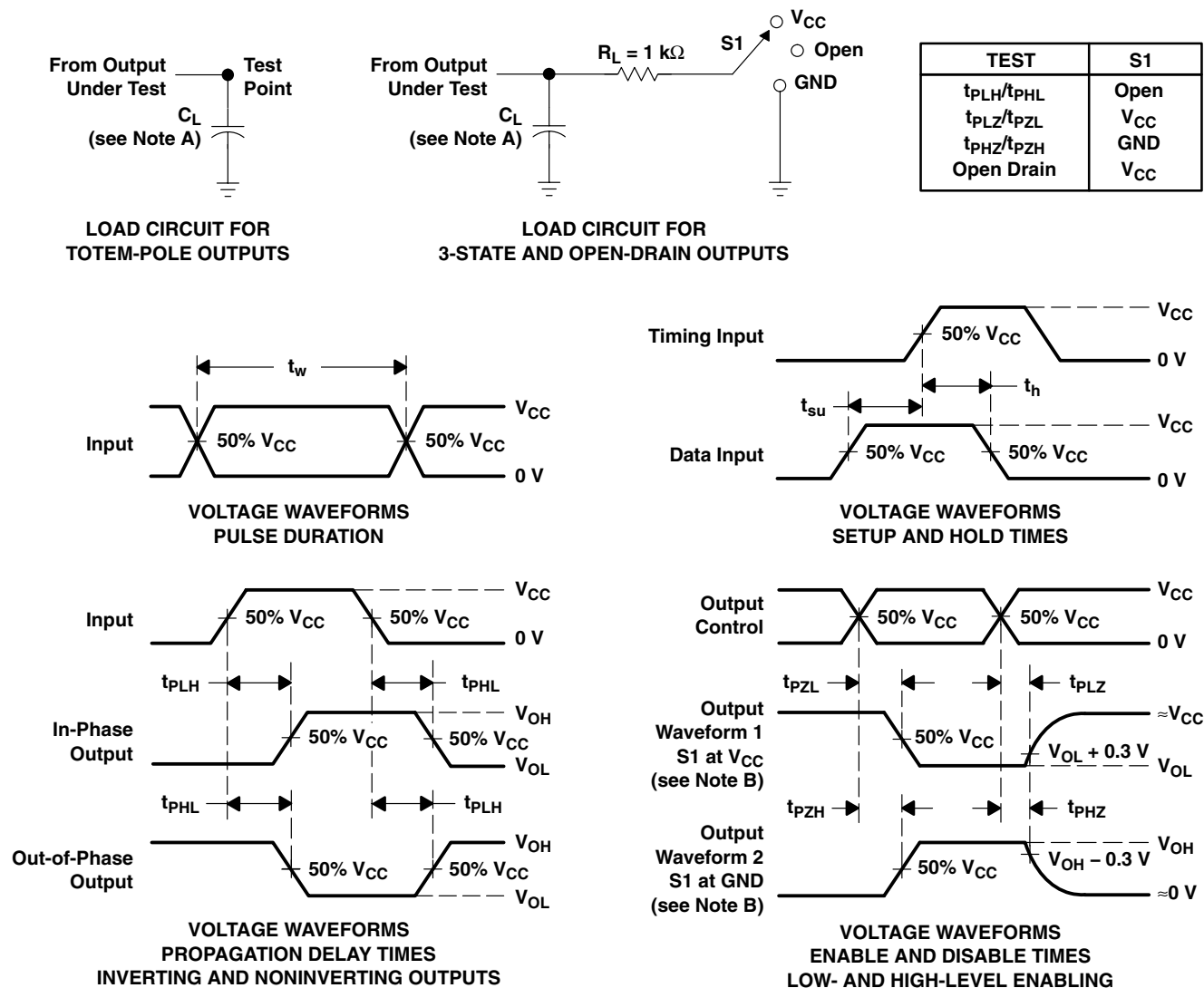


# SN74LV74A-Q1

## DUAL POSITIVE-EDGE-TRIGGERED D-TYPE FLIP-FLOP

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### PARAMETER MEASUREMENT INFORMATION



- NOTES:
- A.  $C_L$  includes probe and jig capacitance.
  - B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
  - C. All input pulses are supplied by generators having the following characteristics:  $PRR \leq 1\text{ MHz}$ ,  $Z_O = 50\ \Omega$ ,  $t_r \leq 3\text{ ns}$ ,  $t_f \leq 3\text{ ns}$ .
  - D. The outputs are measured one at a time, with one input transition per measurement.
  - E.  $t_{PLZ}$  and  $t_{PHZ}$  are the same as  $t_{dis}$ .
  - F.  $t_{PZL}$  and  $t_{PZH}$  are the same as  $t_{en}$ .
  - G.  $t_{PHL}$  and  $t_{PLH}$  are the same as  $t_{pd}$ .
  - H. All parameters and waveforms are not applicable to all devices.

Figure 1. Load Circuit and Voltage Waveforms

## PACKAGING INFORMATION

| Orderable Device  | Status<br>(1) | Package Type | Package<br>Drawing | Pins | Package<br>Qty | Eco Plan<br>(2)            | Lead/Ball Finish<br>(6) | MSL Peak Temp<br>(3) | Op Temp (°C) | Device Marking<br>(4/5) | Samples                 |
|-------------------|---------------|--------------|--------------------|------|----------------|----------------------------|-------------------------|----------------------|--------------|-------------------------|-------------------------|
| SN74LV74AQDRG4Q1  | ACTIVE        | SOIC         | D                  | 14   | 2500           | Green (RoHS<br>& no Sb/Br) | CU NIPDAU               | Level-1-260C-UNLIM   | -40 to 125   | LV74A                   | <a href="#">Samples</a> |
| SN74LV74AQDRQ1    | ACTIVE        | SOIC         | D                  | 14   | 2500           | Green (RoHS<br>& no Sb/Br) | CU NIPDAU               | Level-1-260C-UNLIM   | -40 to 125   | LV74A                   | <a href="#">Samples</a> |
| SN74LV74AQPWRG4Q1 | ACTIVE        | TSSOP        | PW                 | 14   | 2000           | Green (RoHS<br>& no Sb/Br) | CU NIPDAU               | Level-1-260C-UNLIM   | -40 to 125   | LV74A                   | <a href="#">Samples</a> |
| SN74LV74AQPWRQ1   | OBSOLETE      | TSSOP        | PW                 | 14   |                | TBD                        | Call TI                 | Call TI              | -40 to 125   |                         |                         |

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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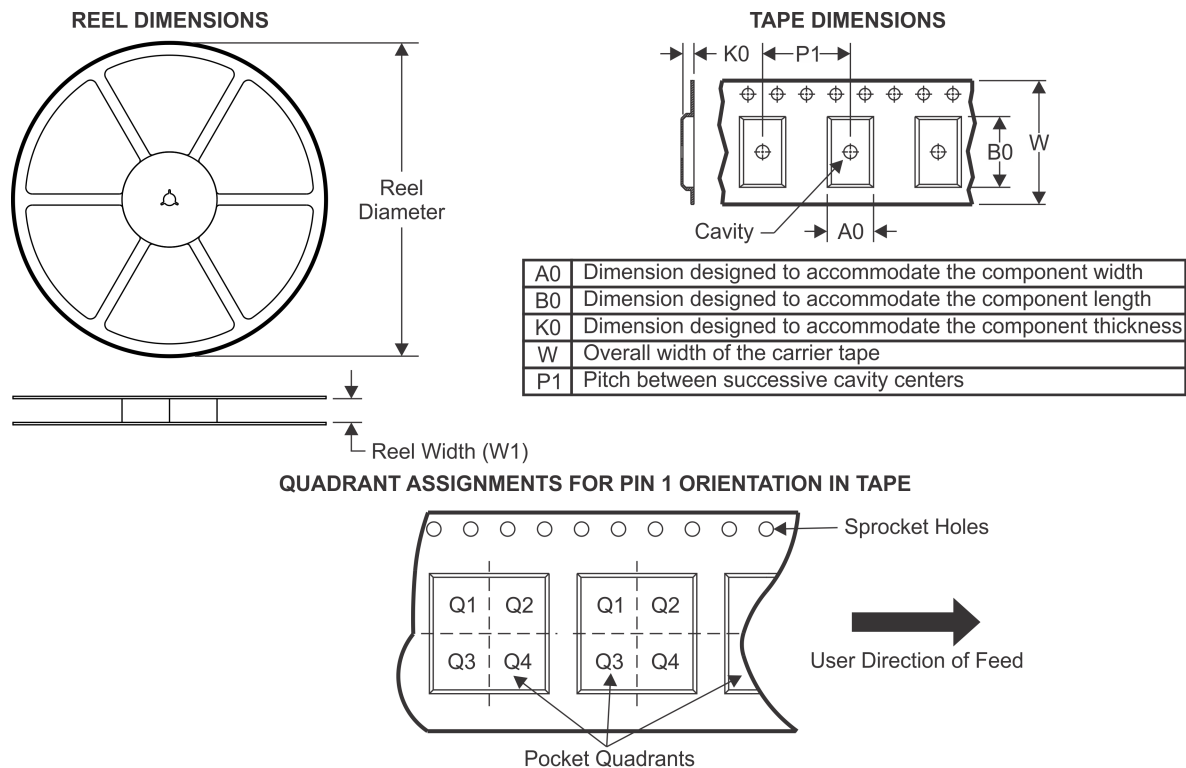
**OTHER QUALIFIED VERSIONS OF SN74LV74A-Q1 :**

- Catalog: [SN74LV74A](#)
- Enhanced Product: [SN74LV74A-EP](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Enhanced Product - Supports Defense, Aerospace and Medical Applications

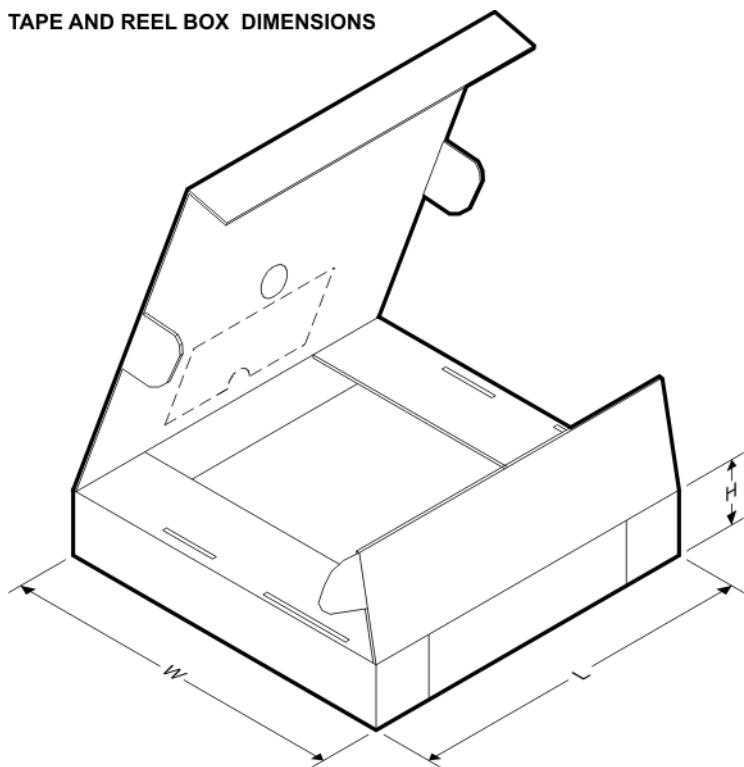


**TAPE AND REEL INFORMATION**


\*All dimensions are nominal

| Device            | Package Type | Package Drawing | Pins | SPQ  | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|-------------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| SN74LV74AQPWRG4Q1 | TSSOP        | PW              | 14   | 2000 | 330.0              | 12.4               | 6.9     | 5.6     | 1.6     | 8.0     | 12.0   | Q1            |

## TAPE AND REEL BOX DIMENSIONS

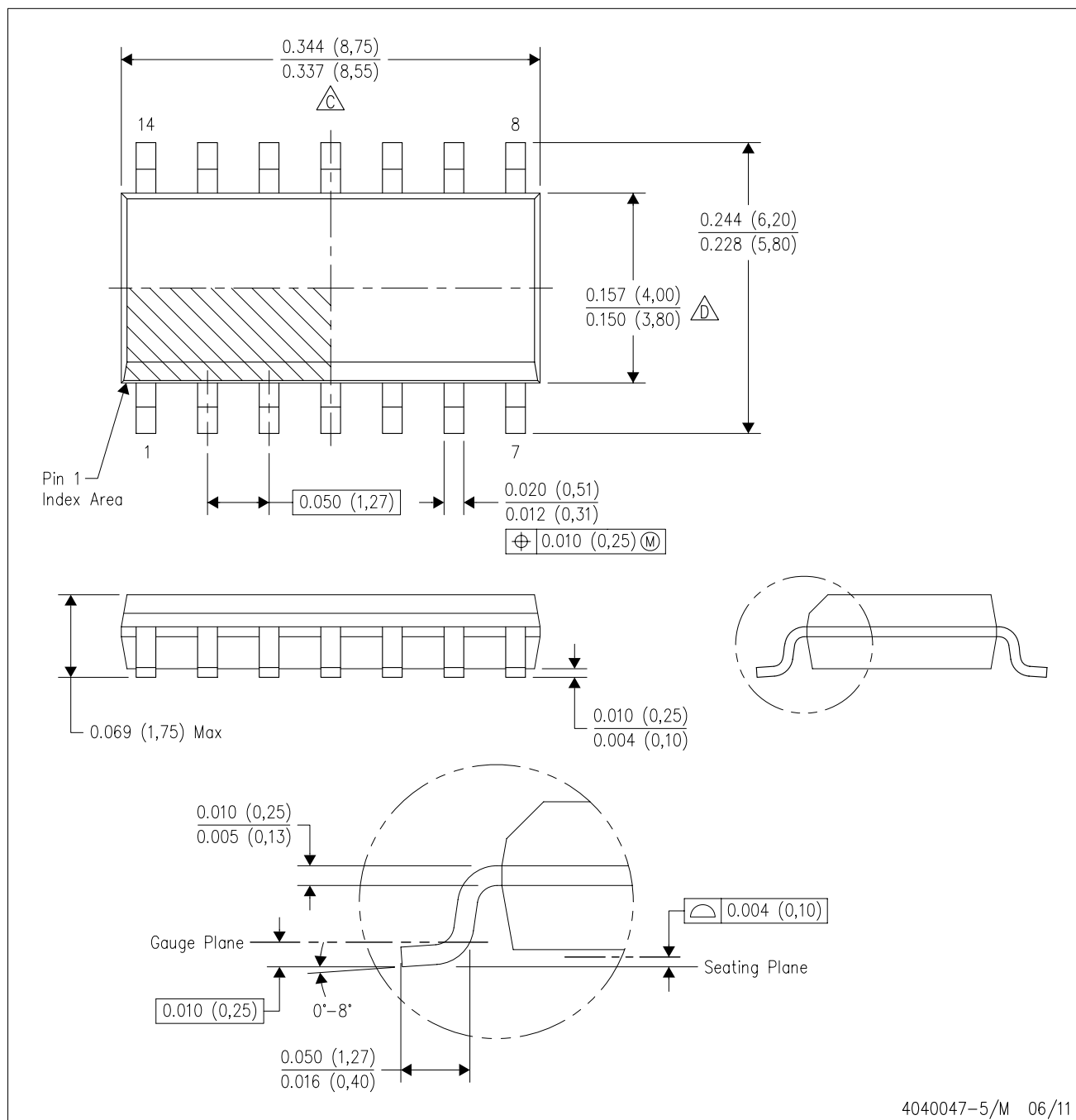


\*All dimensions are nominal

| Device            | Package Type | Package Drawing | Pins | SPQ  | Length (mm) | Width (mm) | Height (mm) |
|-------------------|--------------|-----------------|------|------|-------------|------------|-------------|
| SN74LV74AQPWRG4Q1 | TSSOP        | PW              | 14   | 2000 | 367.0       | 367.0      | 35.0        |

D (R-PDSO-G14)

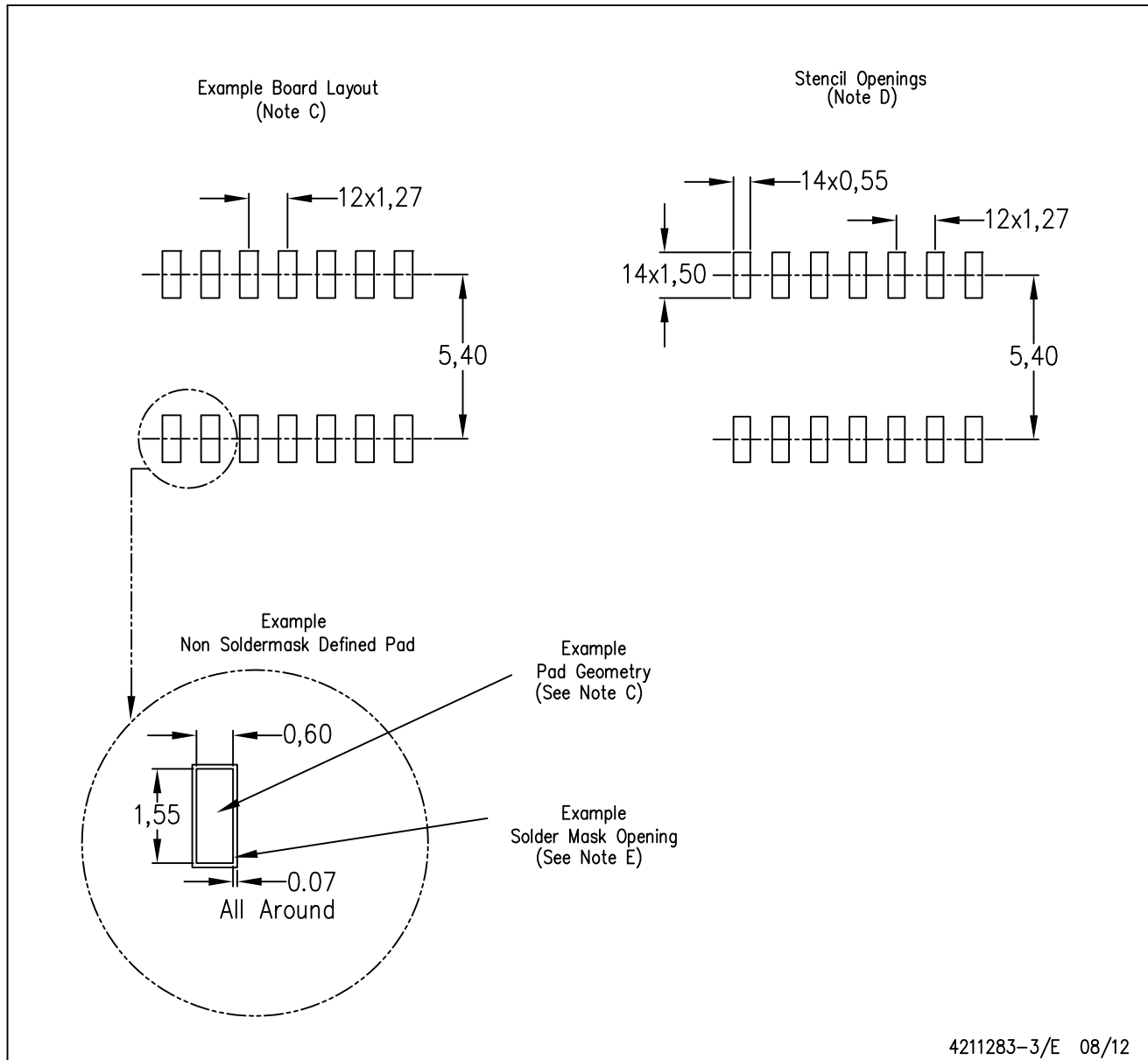
PLASTIC SMALL OUTLINE



NOTES: A. All linear dimensions are in inches (millimeters).  
 B. This drawing is subject to change without notice.  
 C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.  
 D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.  
 E. Reference JEDEC MS-012 variation AB.

D (R-PDSO-G14)

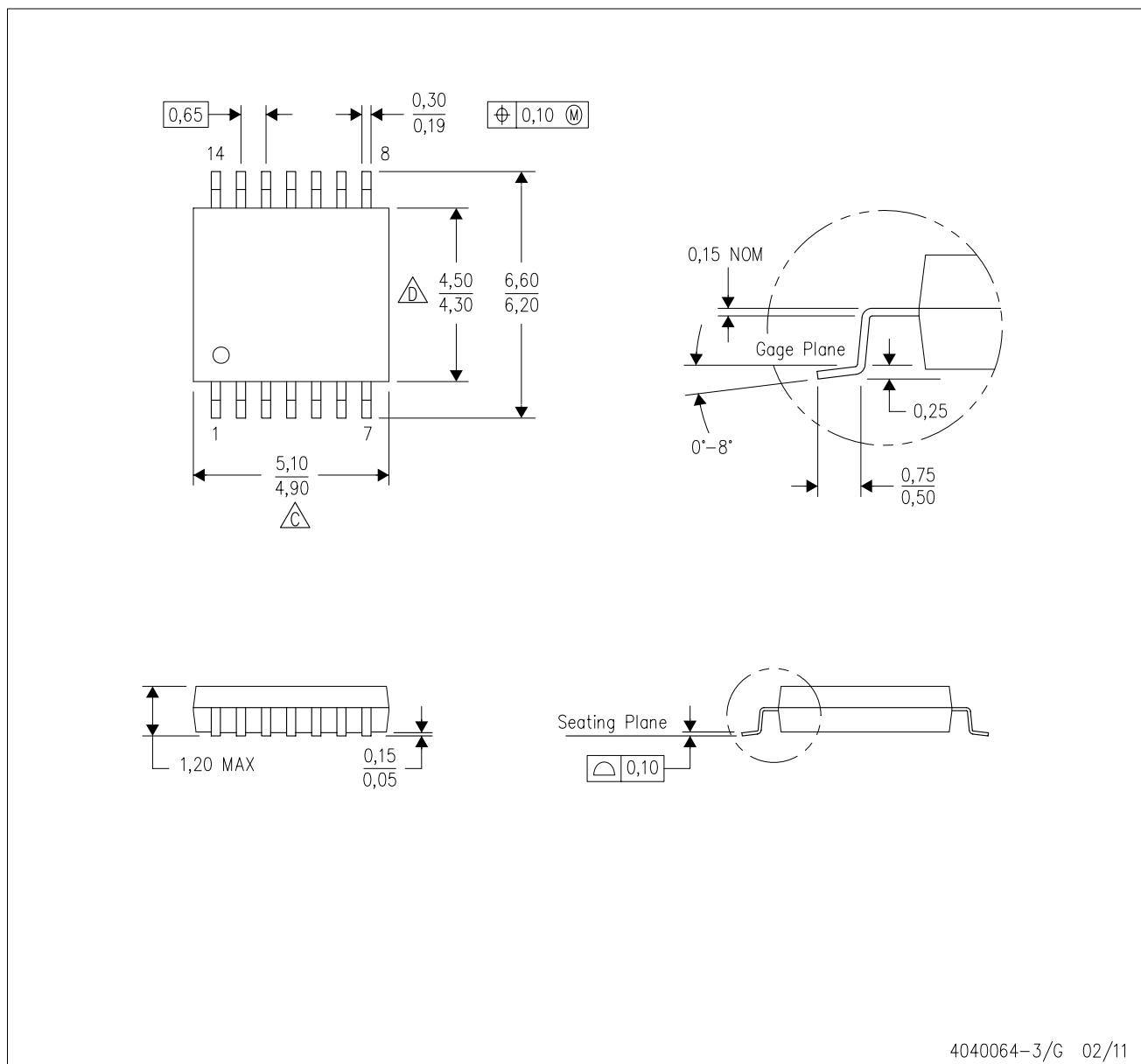
PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Publication IPC-7351 is recommended for alternate designs.
  - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
  - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

PW (R-PDSO-G14)

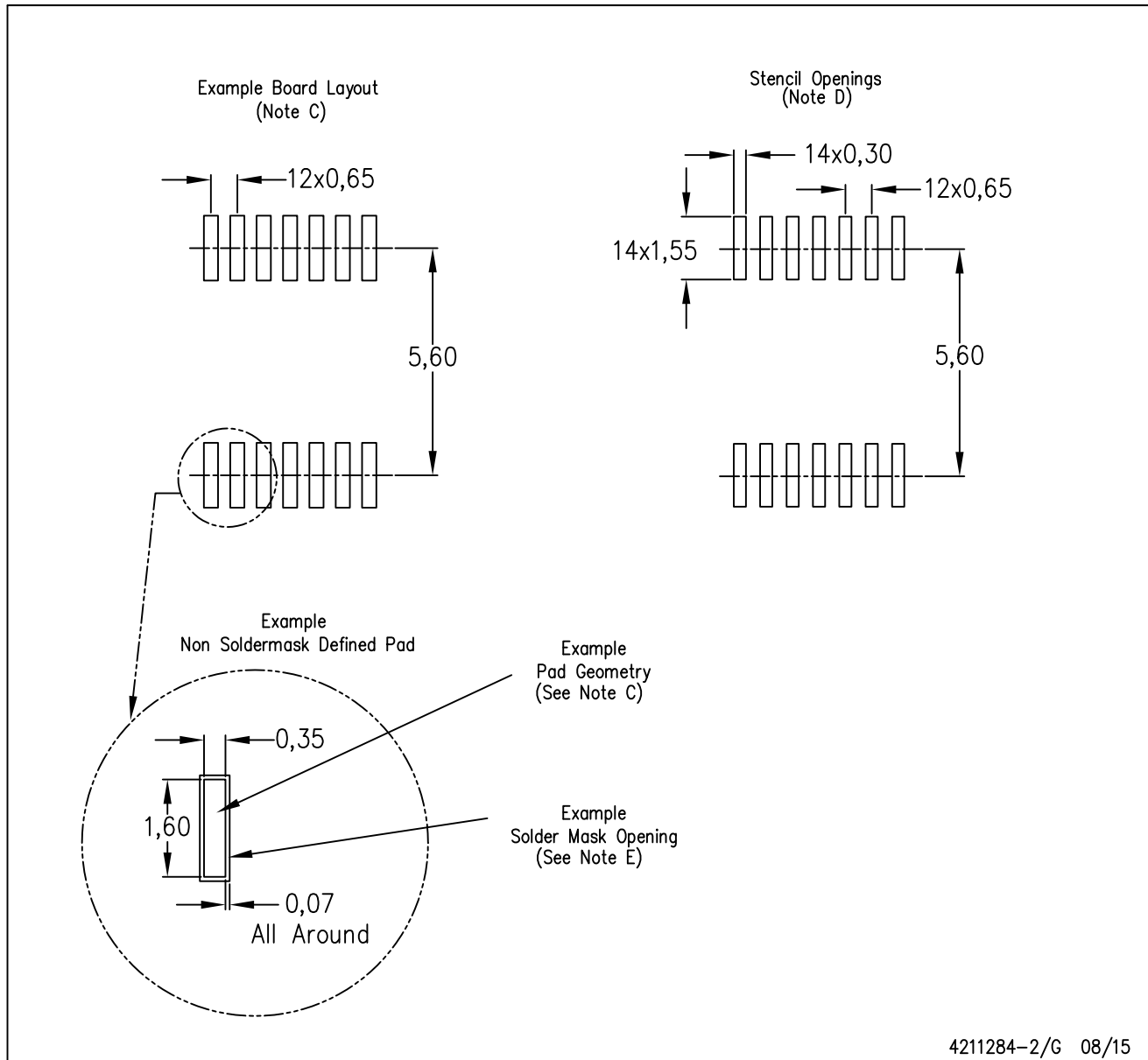
PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
  - B. This drawing is subject to change without notice.
  - C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
  - D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
  - E. Falls within JEDEC MO-153

PW (R-PDSO-G14)

PLASTIC SMALL OUTLINE



- NOTES:
- All linear dimensions are in millimeters.
  - This drawing is subject to change without notice.
  - Publication IPC-7351 is recommended for alternate designs.
  - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
  - Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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|                               |                                                                                          |
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