

TLC5618, TLC5618A PROGRAMMABLE DUAL 12-BIT DIGITAL-TO-ANALOG CONVERTERS

SLAS156G – JULY 1997 – REVISED APRIL 2001

- Programmable Settling Time to 0.5 LSB
2.5 μ s or 12.5 μ s Typ
- Two 12-Bit CMOS Voltage Output DACs in an 8-Pin Package
- Simultaneous Updates for DAC A and DAC B
- Single Supply Operation
- 3-Wire Serial Interface
- High-Impedance Reference Inputs
- Voltage Output Range . . . 2 Times the Reference Input Voltage
- Software Powerdown Mode
- Internal Power-On Reset
- TMS320 and SPI Compatible
- Low Power Consumption:
 - 3 mW Typ in Slow Mode,
 - 8 mW Typ in Fast Mode
- Input Data Update Rate of 1.21 MHz
- Monotonic Over Temperature
- Available in Q-Temp Automotive HighRel Automotive Applications Configuration Control/Print Support Qualification to Automotive Standards

applications

- Battery Powered Test Instruments
- Digital Offset and Gain Adjustment
- Battery Operated/Remote Industrial Controls
- Machine and Motion Control Devices
- Cellular Telephones

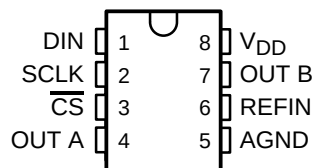
description

The TLC5618 is a dual 12-bit voltage output digital-to-analog converter (DAC) with buffered reference inputs (high impedance). The DACs have an output voltage range that is two times the reference voltage, and the DACs are monotonic. The device is simple to use, running from a single supply of 5 V. A power-on reset function is incorporated in the device to ensure repeatable start-up conditions.

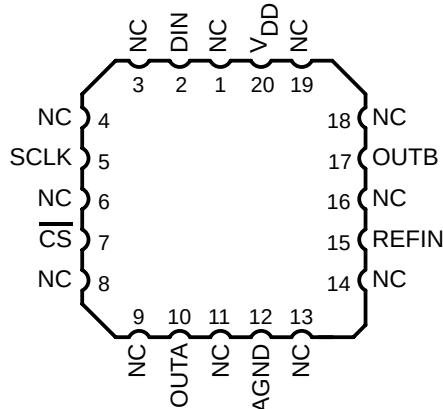
Digital control of the TLC5618 is over a 3-wire CMOS-compatible serial bus. The device receives a 16-bit word for programming and producing the analog output. The digital inputs feature Schmitt triggers for high noise immunity. Digital communication protocols include the SPI™, QSPI™, and Microwire™ standards.

Two versions of the device are available. The TLC5618 does not have an internal state machine and is dependent on all external timing signals. The TLC5618A has an internal state machine that counts the number of clocks from the falling edge of $\overline{CS}$ and then updates and disables the device from accepting further data inputs. The TLC5618A is recommended for TMS320 and SPI processors, and the TLC5618 is recommended only for SPI or 3-wire serial port processors. The TLC5618A is backward-compatible and designed to work in TLC5618 designed systems.

D, P, OR JG PACKAGE
(TOP VIEW)



FK PACKAGE
(TOP VIEW)



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

SPI and QSPI are trademarks of Motorola, Inc.
Microwire is a trademark of National Semiconductor Corporation.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

 **TEXAS
INSTRUMENTS**

POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

Copyright © 2001, Texas Instruments Incorporated
On products compliant to MIL-PRF-38535, all parameters are tested unless otherwise noted. On all other products, production processing does not necessarily include testing of all parameters.

TLC5618, TLC5618A PROGRAMMABLE DUAL 12-BIT DIGITAL-TO-ANALOG CONVERTERS

SLAS156G – JULY 1997 – REVISED APRIL 2001

description (continued)

The 8-terminal small-outline D package allows digital control of analog functions in space-critical applications. The TLC5618C is characterized for operation from 0°C to 70°C. The TLC5618I is characterized for operation from –40°C to 85°C. The TLC5618Q is characterized for operation from –40°C to 125°C. The TLC5618M is characterized for operation from –55°C to 125°C.

AVAILABLE OPTIONS

PACKAGE				
T _A	SMALL OUTLINE [†] (D)	PLASTIC DIP (P)	CERAMIC DIP (JG)	20 PAD LCC (FK)
0°C to 70°C	TLC5618CD TLC5618ACD	TLC5618CP TLC5618ACP	— —	— —
–40°C to 85°C	TLC5618ID TLC5618AID	TLC5618IP TLC5618AIP	— —	— —
–40°C to 125°C	TLC5618AQD	—	—	—
–55°C to 125°C	—	—	TLC5618AMJG	TLC5618AMFK

[†] The D package is available in tape and reel by adding R to the part number (e.g., TLC5618CDR)

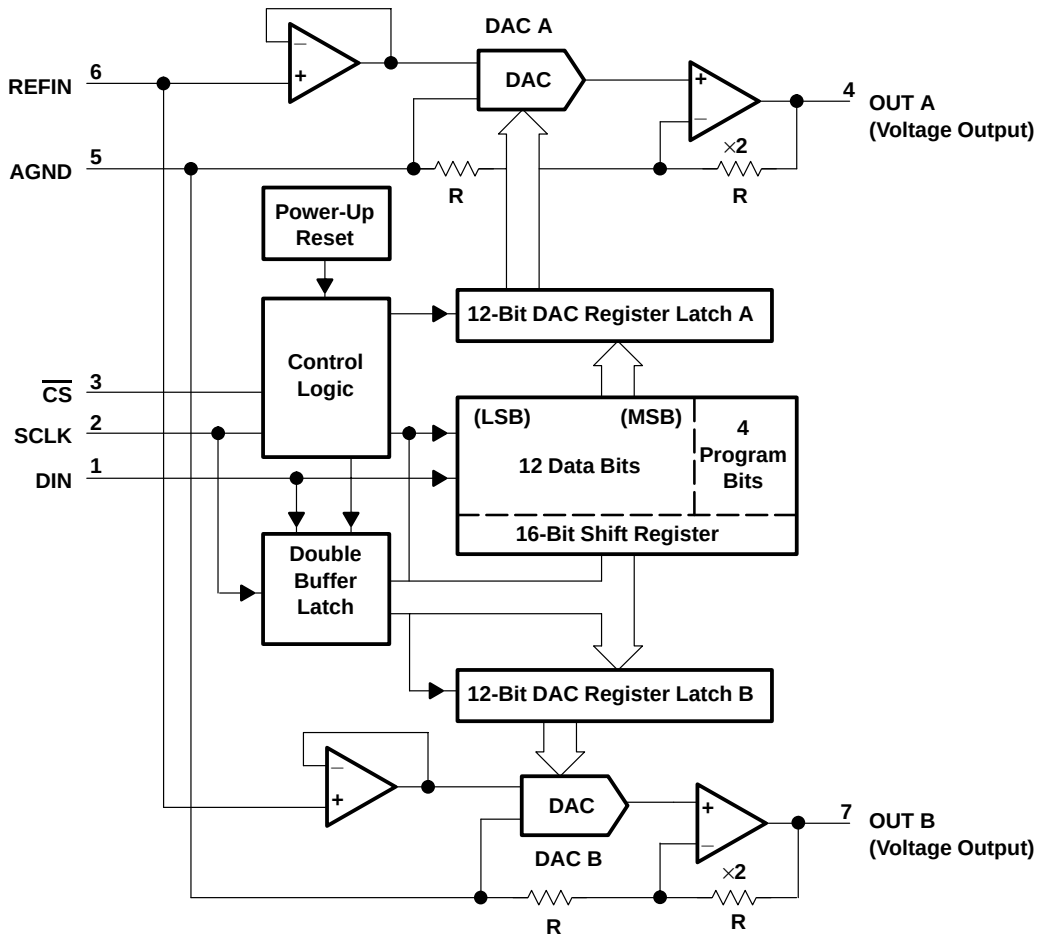
DEVICE	COMPATIBILITY
TLC5618	SPI, QSPI and Microwire
TLC5618A	TMS320Cxx, SPI, QSPI, and Microwire

TLC5618, TLC5618A

PROGRAMMABLE DUAL 12-BIT DIGITAL-TO-ANALOG CONVERTERS

SLAS156G – JULY 1997 – REVISED APRIL 2001

functional block diagram



Terminal Functions

TERMINAL NAME	NO.	I/O	DESCRIPTION
AGND	5		Analog ground
$\overline{\text{CS}}$	3	I	Chip select, active low
DIN	1	I	Serial data input
OUT A	4	O	DAC A analog output
OUT B	7	O	DAC B analog output
REFIN	6	I	Reference voltage input
SCLK	2	I	Serial clock input
V _{DD}	8		Positive power supply

TLC5618, TLC5618A PROGRAMMABLE DUAL 12-BIT DIGITAL-TO-ANALOG CONVERTERS

SLAS156G – JULY 1997 – REVISED APRIL 2001

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

Supply voltage (V_{DD} to AGND)	7 V
Digital input voltage range to AGND	– 0.3 V to $V_{DD} + 0.3$ V
Reference input voltage range to AGND	– 0.3 V to $V_{DD} + 0.3$ V
Output voltage at OUT from external source	$V_{DD} + 0.3$ V
Continuous current at any terminal	±20 mA
Operating free-air temperature range, T_A : TLC5618C, TLC5618AC	0°C to 70°C
TLC5618I, TLC5618AI	–40°C to 85°C
TLC5618AQ	–40°C to 125°C
TLC5618AM	–55°C to 125°C
Storage temperature range, T_{stg}	–65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	260°C

[†] Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

DISSIPATION RATING TABLE

PACKAGE	$T_A \leq 25^\circ\text{C}$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25^\circ\text{C}$ [‡]	$T_A = 70^\circ\text{C}$ POWER RATING	$T_A = 85^\circ\text{C}$ POWER RATING	$T_A = 125^\circ\text{C}$ POWER RATING
D	635 mW	5.08 mW/°C	407 mW	330 mW	—
FK	1375 mW	11.00 mW/°C	880 mW	715 mW	275 mW
JG	1050 mW	8.40 mW/°C	672 mW	546 mW	210 mW
P	1202 mW	9.61 mW/°C	769 mW	625 mW	—

[‡] This is the inverse of the traditional junction-to-ambient thermal resistance ($R\theta_{JA}$). Thermal resistances are not production tested and are for informational purposes only.

recommended operating conditions

		MIN	NOM	MAX	UNIT
Supply voltage, V_{DD}		4.5	5	5.5	V
High-level digital input voltage, V_{IH}	$V_{DD} = 5$ V	0.7 V_{DD}			V
Low-level digital input voltage, V_{IL}	$V_{DD} = 5$ V			0.3 V_{DD}	V
Reference voltage, V_{ref} to REFIN terminal		2	2.048	$V_{DD} - 1.1$	V
Load resistance, R_L		2			k Ω
Operating free-air temperature, T_A	TLC5618C, TLC5618AC	0		70	°C
	TLC5618I, TLC5618AI	–40		85	
	TLC5618AQ	–40		125	
	TLC5618AM	–55		125	

TLC5618, TLC5618A

PROGRAMMABLE DUAL 12-BIT DIGITAL-TO-ANALOG CONVERTERS

SLAS156G – JULY 1997 – REVISED APRIL 2001

electrical characteristics over recommended operating free-air temperature range, $V_{DD} = 5\text{ V} \pm 5\%$, $V_{ref}(REFIN) = 2.048\text{ V}$ (unless otherwise noted)

static DAC specifications

PARAMETER			TEST CONDITIONS		MIN	TYP	MAX	UNIT
Resolution					12			bits
Integral nonlinearity (INL), end point adjusted			V _{ref} (REFIN) = 2.048 V,	See Note 1			±4	LSB
Differential nonlinearity (DNL)			V _{ref} (REFIN) = 2.048 V,	See Note 2		±0.5	±1	LSB
E _{ZS}	Zero-scale error (offset error at zero scale)		V _{ref} (REFIN) = 2.048 V,	See Note 3			±12	mV
Zero-scale-error temperature coefficient			V _{ref} (REFIN) = 2.048 V,	See Note 4		3		ppm/°C
E _G	Gain error		V _{ref} (REFIN) = 2.048 V, See Note 5	C and I suffixes			±0.29	% of FS voltage
				Q and M suffixes			±0.60	
Gain error temperature coefficient			V _{ref} (REFIN) = 2.048 V,	See Note 6		1		ppm/°C
PSRR	Power-supply rejection ratio		Zero scale	See Notes 7 and 8	Slow		65	dB
			Gain				65	
			Zero scale		Fast		65	
			Gain				65	

- NOTES:
1. The relative accuracy or integral nonlinearity (INL) sometimes referred to as linearity error, is the maximum deviation of the output from the line between zero and full scale excluding the effects of zero code and full-scale errors.
 2. The differential nonlinearity (DNL) sometimes referred to as differential error, is the difference between the measured and ideal 1 LSB amplitude change of any two adjacent codes. Monotonic means the output voltage changes in the same direction (or remains constant) as a change in the digital input code.
 3. Zero-scale error is the deviation from zero voltage output when the digital input code is zero.
 4. Zero-scale-error temperature coefficient is given by: $E_{ZS} \text{ TC} = [E_{ZS}(T_{\max}) - E_{ZS}(T_{\min})]/V_{ref} \times 10^6/(T_{\max} - T_{\min})$.
 5. Gain error is the deviation from the ideal output ($V_{ref} - 1\text{ LSB}$) with an output load of $10\text{ k}\Omega$ excluding the effects of the zero-error.
 6. Gain temperature coefficient is given by: $E_G \text{ TC} = [E_G(T_{\max}) - E_G(T_{\min})]/V_{ref} \times 10^6/(T_{\max} - T_{\min})$.
 7. Zero-scale-error rejection ratio (E_{ZS}-RR) is measured by varying the V_{DD} from 4.5 V to 5.5 V dc and measuring the proportion of this signal imposed on the zero-code output voltage.
 8. Gain-error rejection ratio (E_G-RR) is measured by varying the V_{DD} from 4.5 V to 5.5 V dc and measuring the proportion of this signal imposed on the full-scale output voltage after subtracting the zero scale change.

OUT A and OUT B output specifications

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_O	Voltage output range	$R_L = 10\text{ k}\Omega$		0		$V_{DD} - 0.4$	V
Output load regulation accuracy		$V_O(\text{OUT}) = 4.096\text{ V}$,	$R_L = 2\text{ k}\Omega$			± 0.29	% of FS voltage
$I_{OSC}(\text{sink})$	Output short circuit sink current	$V_O(\text{A OUT}) = V_{DD}$, $V_O(\text{B OUT}) = V_{DD}$, Input code zero	Fast		38		mA
			Slow		23		
$I_{OSC}(\text{source})$	Output short circuit source current	$V_O(\text{A OUT}) = 0\text{ V}$, $V_O(\text{B OUT}) = 0\text{ V}$, Full-scale code	Fast		-54		mA
			Slow		-29		
$I_O(\text{sink})$	Output sink current	$V_O(\text{OUT}) = 0.25\text{ V}$			5		mA
$I_O(\text{source})$	Output source current	$V_O(\text{OUT}) = 4.2\text{ V}$			5		mA



TLC5618, TLC5618A

PROGRAMMABLE DUAL 12-BIT DIGITAL-TO-ANALOG CONVERTERS

SLAS156G – JULY 1997 – REVISED APRIL 2001

electrical characteristics over recommended operating free-air temperature range, $V_{DD} = 5\text{ V} \pm 5\%$, $V_{ref}(REFIN) = 2.048\text{ V}$ (unless otherwise noted) (continued)

reference input (REFIN)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_I Input voltage range		0		$V_{DD}-2$	V
R_i Input resistance			10		M Ω
C_i Input capacitance			5		pF
Reference feedthrough	REFIN = 1 V_{pp} at 1 kHz + 1.024 V dc (see Note 9)		-60		dB
Reference input bandwidth (f – 3 dB)	REFIN = 0.2 V_{pp} + 1.024 V dc	Slow	0.5		MHz
		Fast	1		

NOTE 9: Reference feedthrough is measured at the DAC output with an input code = 000 hex and a $V_{ref}(REFIN)$ input = 1.024 V dc + 1 V_{pp} at 1 kHz.

digital inputs (DIN, SCLK, $\overline{CS}$)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{IH} High-level digital input current	$V_I = V_{DD}$			± 1	μA
I_{IL} Low-level digital input current	$V_I = 0\text{ V}$			± 1	μA
C_i Input capacitance			8		pF

power supply

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{DD} Power supply current	$V_{DD} = 5.5\text{ V}$, No load, All inputs = 0 V or V_{DD}	Slow	0.6	1	mA
		Fast	1.6	2.5	
Power down supply current	D13 = 0 (see Table 2)		1		μA

operating characteristics over recommended operating free-air temperature range, $V_{DD} = 5\text{ V} \pm 5\%$, $V_{ref}(REFIN) = 2.048\text{ V}$ (unless otherwise noted)

analog output dynamic performance

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
SR+ Output slew rate, positive	$C_L = 100\text{ pF}$, $R_L = 10\text{ k}\Omega$, Code 32 to Code 4096, $V_{ref}(REFIN) = 2.048\text{ V}$, $T_A = 25^\circ\text{C}$, V_O from 10% to 90%	Slow	0.3	0.5	V/ μs
		Fast	2.4	3	
SR– Output slew rate, negative	$C_L = 100\text{ pF}$, $R_L = 10\text{ k}\Omega$, Code 4096 to Code 32, $V_{ref}(REFIN) = 2.048\text{ V}$, $T_A = 25^\circ\text{C}$, V_O from 10% to 90%	Slow	0.15	0.25	V/ μs
		Fast	1.2	1.5	
t_s Output settling time	$T_O \pm 0.5\text{ LSB}$, $R_L = 10\text{ k}\Omega$, $C_L = 100\text{ pF}$, See Note 10	Slow	12.5		μs
		Fast	2.5		
$t_{s(c)}$ Output settling time, code-to-code	$T_O \pm 0.5\text{ LSB}$, $R_L = 10\text{ k}\Omega$, $C_L = 100\text{ pF}$, See Note 11	Slow	2		μs
		Fast	2		
Glitch energy	DIN = All 0s to all 1s, $\overline{CS} = V_{DD}$, $f(SCLK) = 100\text{ kHz}$		5		nV–s
S/(N+D) Signal to noise + distortion	$V_{ref}(REFIN) = 1\text{ V}_{pp}$ at 1 kHz and 10 kHz + 1.024 V dc, Input code = 10 0000 0000		78		dB

NOTES: 10. Settling time is the time for the output signal to remain within $\pm 0.5\text{ LSB}$ of the final measured value for a digital input code change of 020 hex to 3FF hex or 3FF hex to 020 hex.

11. Settling time is the time for the output signal to remain within $\pm 0.5\text{ LSB}$ of the final measured value for a digital input code change of one count.



TLC5618, TLC5618A

PROGRAMMABLE DUAL 12-BIT DIGITAL-TO-ANALOG CONVERTERS

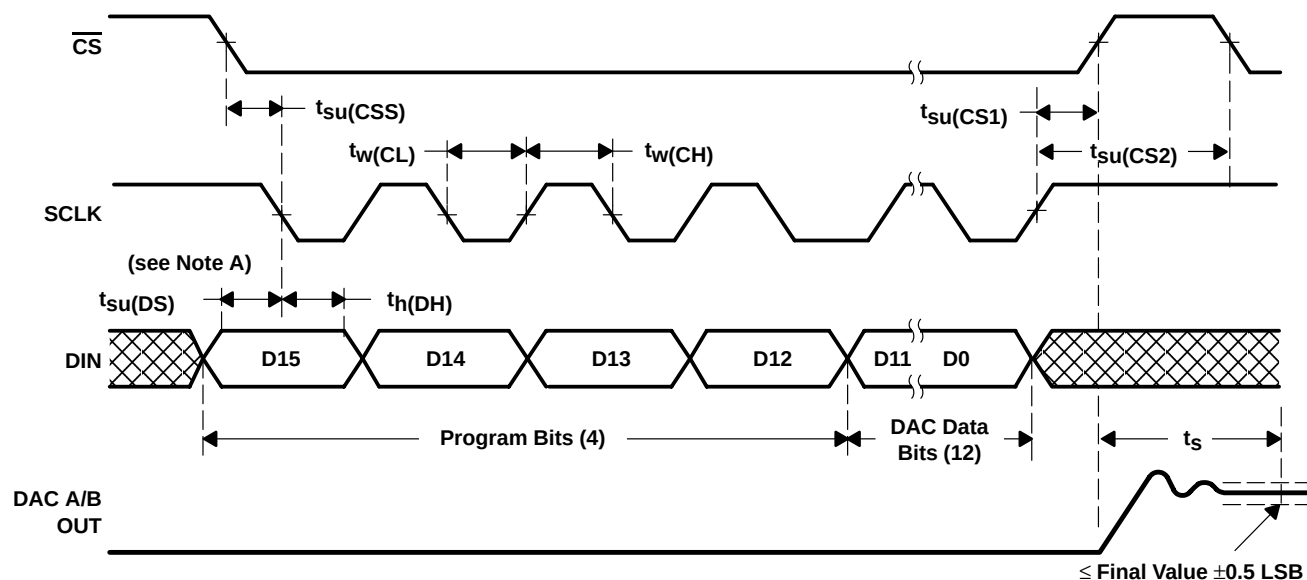
SLAS156G – JULY 1997 – REVISED APRIL 2001

operating characteristics over recommended operating free-air temperature range, $V_{DD} = 5\text{ V} \pm 5\%$, $V_{ref}(REFIN) = 2.048\text{ V}$ (unless otherwise noted) (continued)

digital input timing requirements

			MIN	NOM	MAX	UNIT
$t_{su}(DS)$	Setup time, DIN before SCLK low	C and I suffixes	5			ns
		Q and M suffixes	8			
$t_h(DH)$	Hold time, DIN valid after SCLK low		5			ns
$t_{su}(CSS)$	Setup time, $\overline{CS}$ low to SCLK low		5			ns
$t_{su}(CS1)$	Setup time, SCLK $\uparrow$ to $\overline{CS}$ $\uparrow$, external end-of-write		10			ns
$t_{su}(CS2)$	Setup time, SCLK $\uparrow$ to $\overline{CS}$ $\downarrow$, start of next write cycle		5 [†]			ns
$t_w(CL)$	Pulse duration, SCLK low		25			ns
$t_w(CH)$	Pulse duration, SCLK high		25			ns

[†] Not production tested for Q and M suffixes.



NOTE A: SCLK must go high after the 16th falling clock edge.

Figure 1. Timing Diagram for the TLC5618A

TLC5618, TLC5618A PROGRAMMABLE DUAL 12-BIT DIGITAL-TO-ANALOG CONVERTERS

SLAS156G – JULY 1997 – REVISED APRIL 2001

TYPICAL CHARACTERISTICS

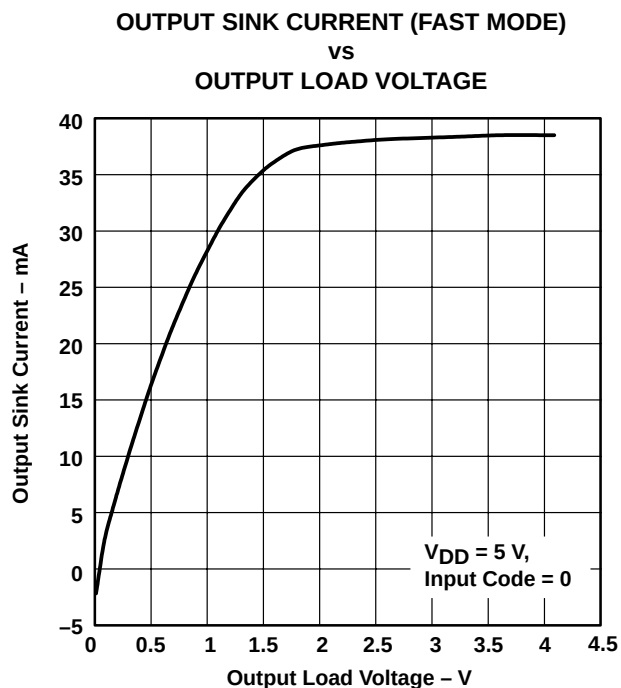


Figure 2

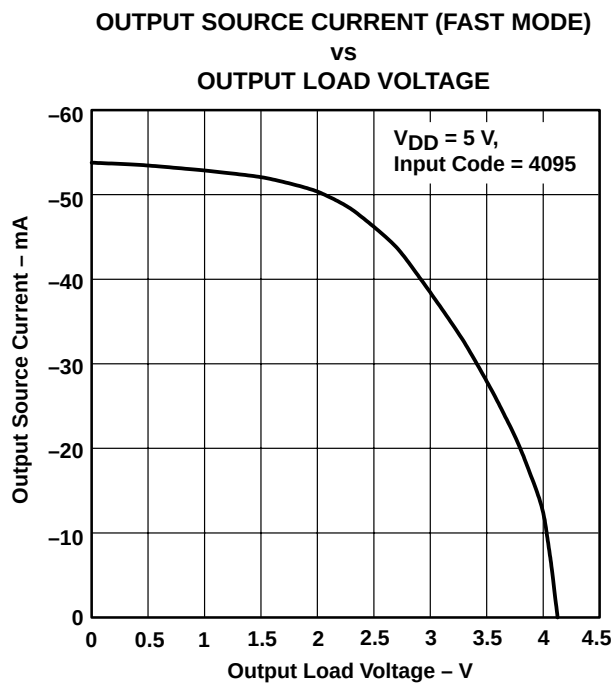


Figure 3

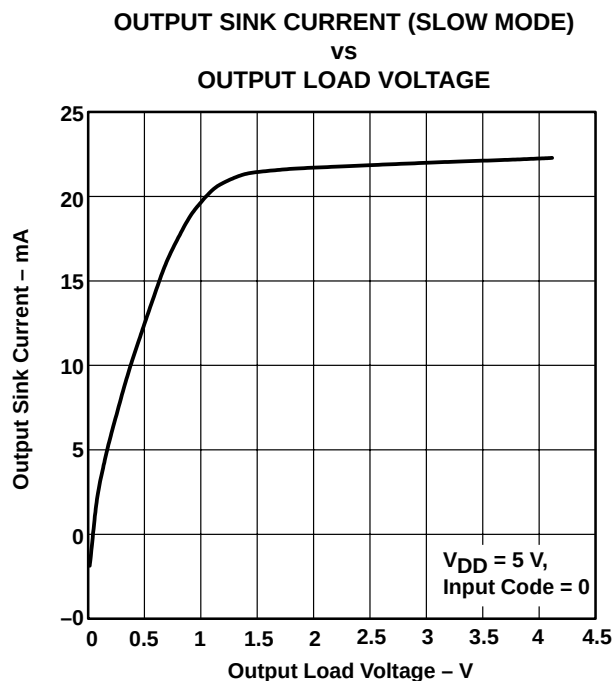


Figure 4

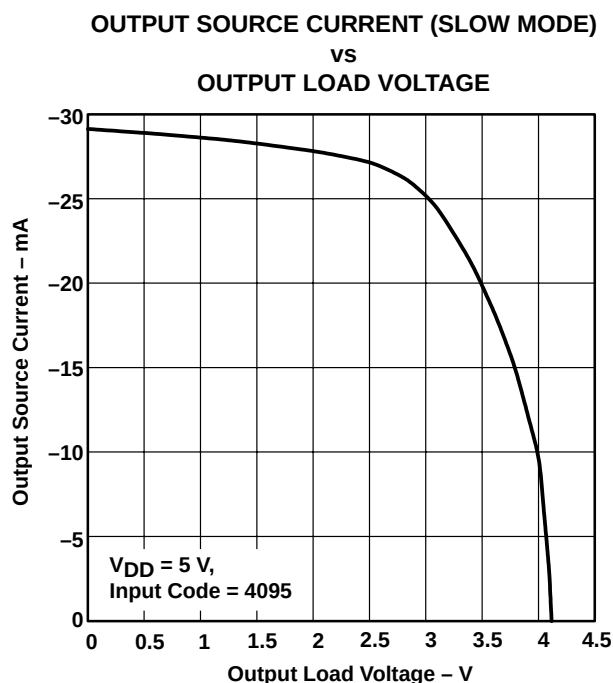


Figure 5

TYPICAL CHARACTERISTICS

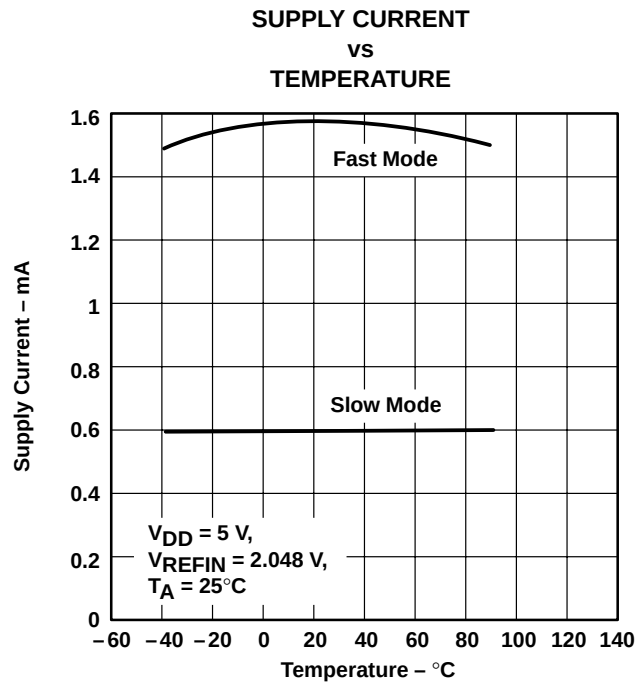


Figure 6

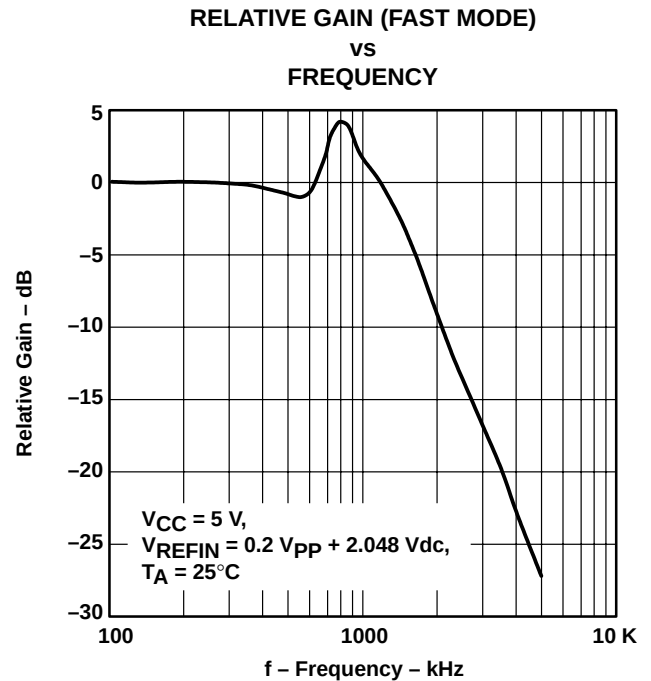


Figure 7

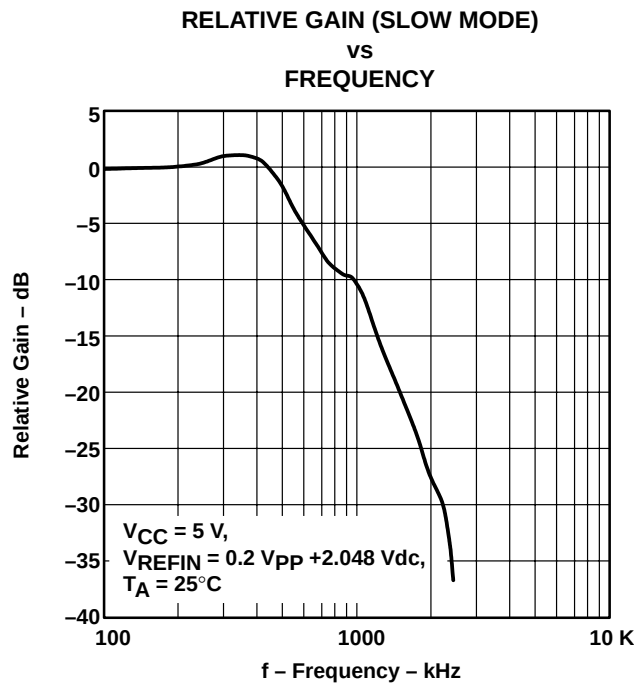


Figure 8

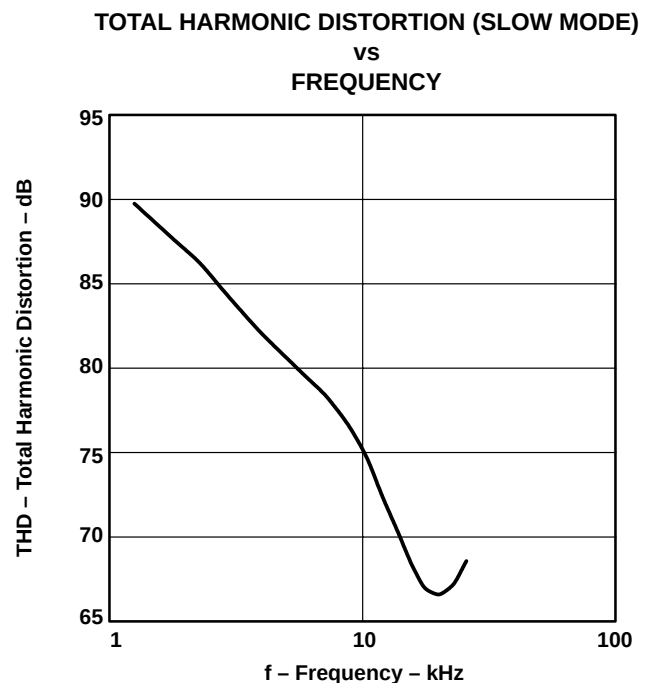


Figure 9

TLC5618, TLC5618A PROGRAMMABLE DUAL 12-BIT DIGITAL-TO-ANALOG CONVERTERS

SLAS156G – JULY 1997 – REVISED APRIL 2001

TYPICAL CHARACTERISTICS

TOTAL HARMONIC DISTORTION + NOISE (SLOW MODE)

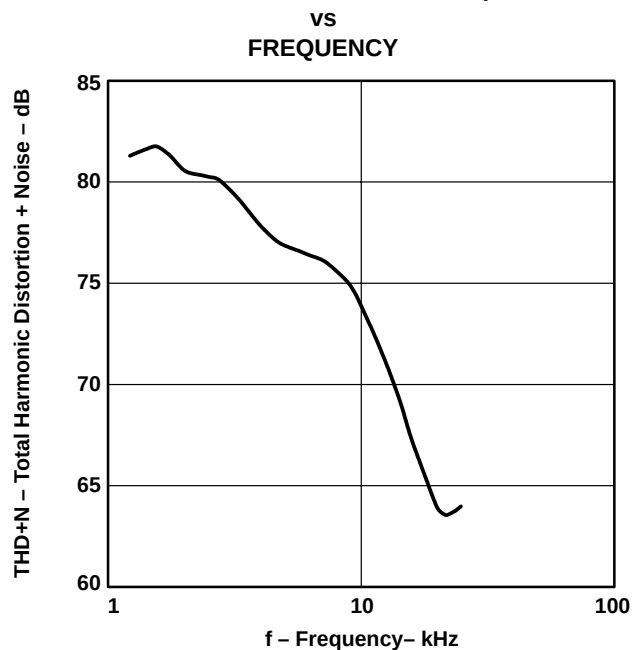


Figure 10

SIGNAL-TO-NOISE RATIO (SLOW MODE)

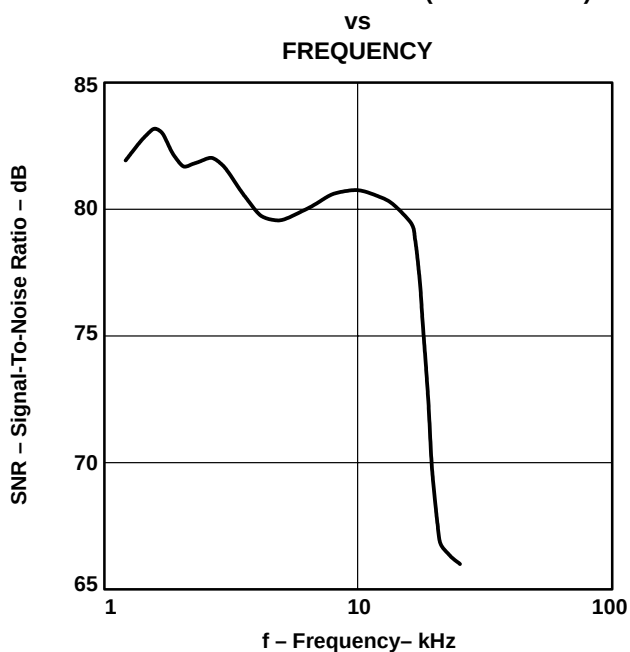


Figure 11

TOTAL HARMONIC DISTORTION (FAST MODE)

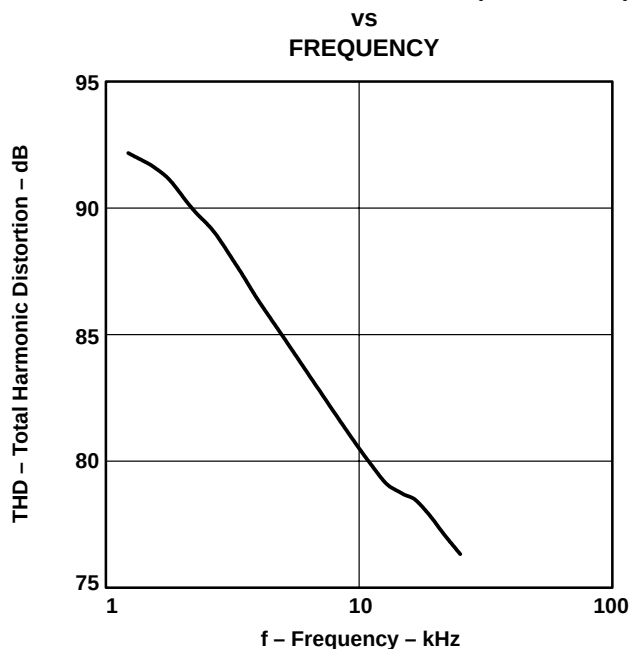


Figure 12

TOTAL HARMONIC DISTORTION + NOISE (FAST MODE)

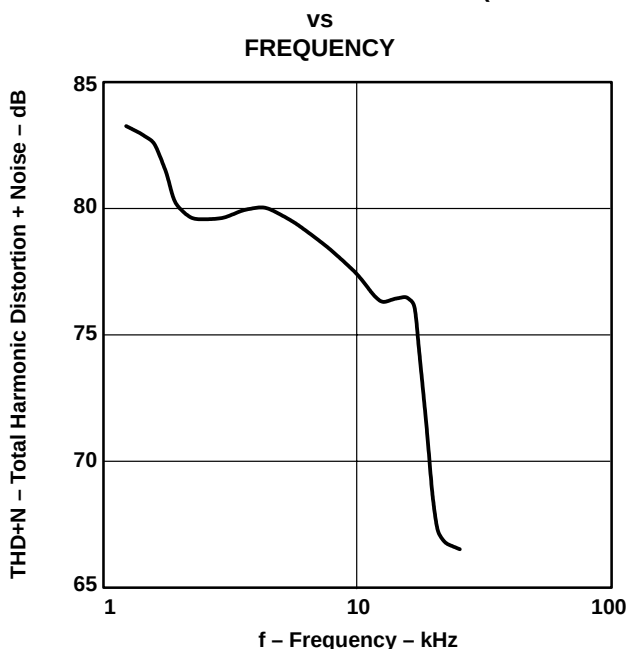


Figure 13

TYPICAL CHARACTERISTICS

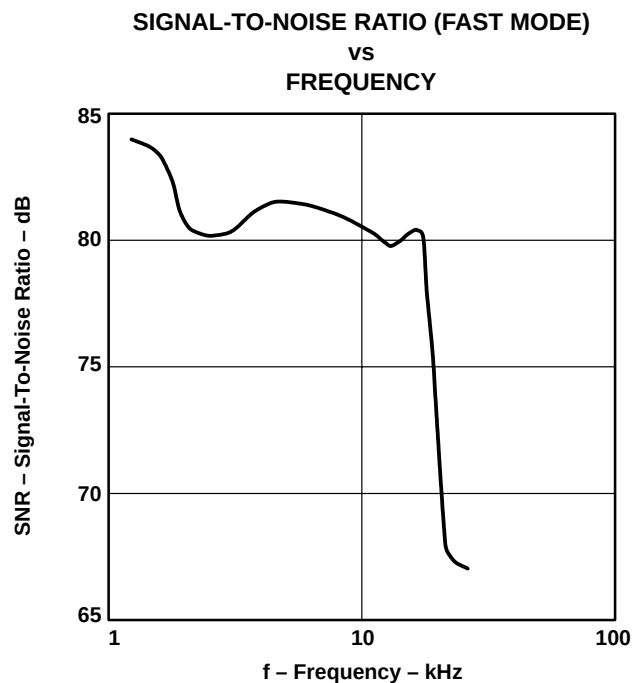


Figure 14

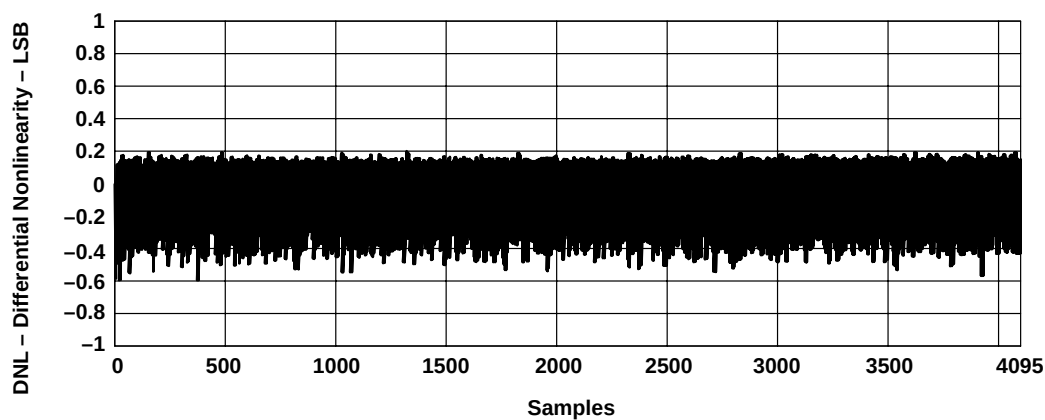


Figure 15. Differential Nonlinearity With Input Code

TLC5618, TLC5618A PROGRAMMABLE DUAL 12-BIT DIGITAL-TO-ANALOG CONVERTERS

SLAS156G – JULY 1997 – REVISED APRIL 2001

TYPICAL CHARACTERISTICS

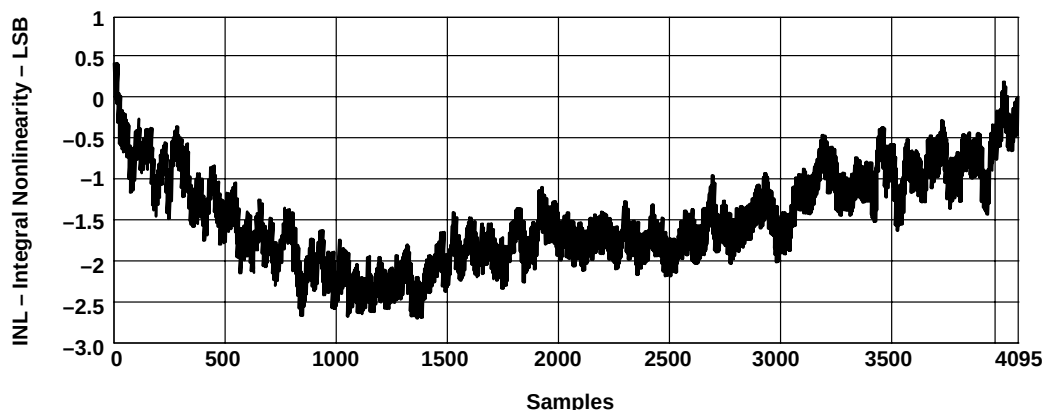


Figure 16. Integral Nonlinearity With Input Code

APPLICATION INFORMATION

general function

The TLC5618 uses a resistor string network buffered with an op amp to convert 12-bit digital data to analog voltage levels (see functional block diagram and Figure 17). The output is the same polarity as the reference input (see Table 1).

The output code is given by: $2(V_{REFIN}) \frac{CODE}{4096}$

An internal circuit resets the DAC register to all 0s on power up.

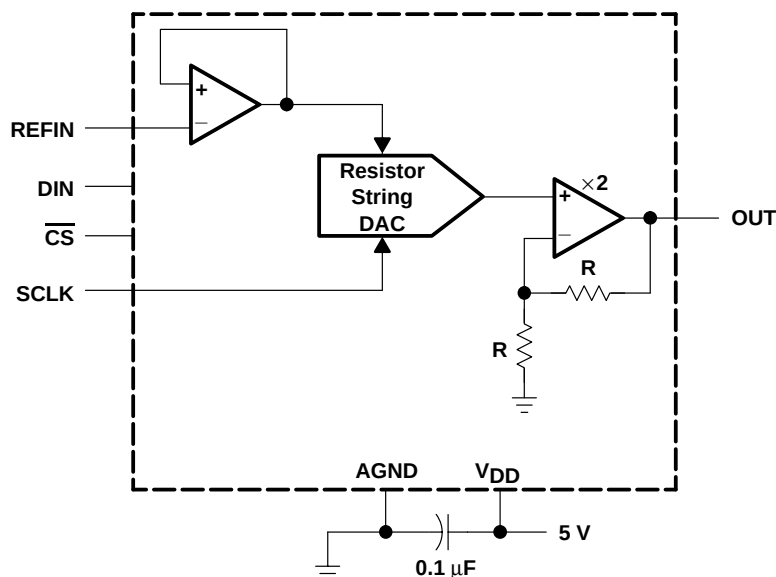


Figure 17. TLC5618 Typical Circuit

APPLICATION INFORMATION

Table 1. Binary Code Table (0 V to 2 V_{REFIN} Output), Gain = 2

INPUT			OUTPUT
1111	1111	1111	$2(V_{REFIN})\frac{4095}{4096}$
	:		:
1000	0000	0001	$2(V_{REFIN})\frac{2049}{4096}$
1000	0000	0000	$2(V_{REFIN})\frac{2048}{4096} = V_{REFIN}$
0111	1111	1111	$2(V_{REFIN})\frac{2047}{4096}$
	:		:
0000	0000	0001	$2(V_{REFIN})\frac{1}{4096}$
0000	0000	0000	0 V

buffer amplifier

The output buffer has a rail-to-rail output with short circuit protection and can drive a 2-kΩ load with a 100-pF load capacitance. Settling time is a software selectable 12.5 μs or 2.5 μs, typical to within ±0.5 LSB of final value.

external reference

The reference voltage input is buffered, which makes the DAC input resistance not code dependent. Therefore, the REFIN input resistance is 10 MΩ and the REFIN input capacitance is typically 5 pF, independent of input code. The reference voltage determines the DAC full-scale output.

logic interface

The logic inputs function with CMOS logic levels. Most of the standard high-speed CMOS logic families may be used.

serial clock and update rate

Figure 1 shows the TLC5618 timing. The maximum serial clock rate is:

$$f_{(SCLK)max} = \frac{1}{t_{w(CH)min} + t_{w(CL)min}} = 20 \text{ MHz}$$

The digital update rate is limited by the chip-select period, which is:

$$t_{p(CS)} = 16 \times (t_{w(CH)} + t_{w(CL)}) + t_{su(CS1)}$$

This equals an 810-ns or 1.23-MHz update rate. However, the DAC settling time to 12 bits limits the update rate for full-scale input step transitions.

TLC5618, TLC5618A PROGRAMMABLE DUAL 12-BIT DIGITAL-TO-ANALOG CONVERTERS

SLAS156G – JULY 1997 – REVISED APRIL 2001

APPLICATION INFORMATION

serial interface

When chip select ($\overline{CS}$) is low, the input data is read into a 16-bit shift register with the input data clocked in, most significant bit first. The falling edge of the SCLK input shifts the data into the input register.

The rising edge of $\overline{CS}$ then transfers the data to the DAC register. When $\overline{CS}$ is high, input data cannot be clocked into the input register.

The 16 bits of data can be transferred with the sequence shown in Figure 18.

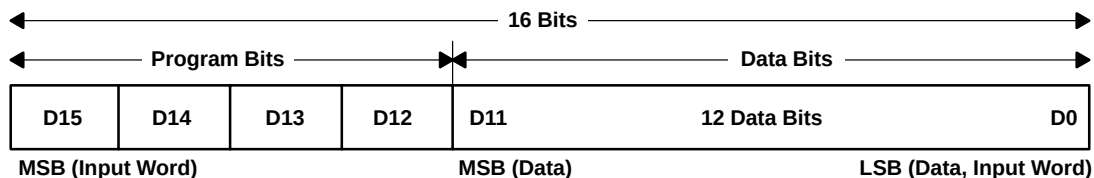


Figure 18. Input Data Word Format

Table 2 shows the function of program bits D15 – D12.

Table 2. Program Bits D15 – D12 Function

PROGRAM BITS				DEVICE FUNCTION
D15	D14	D13	D12	
1	X	X	X	Write to latch A with serial interface register data and latch B updated with buffer latch data
0	X	X	0	Write to latch B and double buffer latch
0	X	X	1	Write to double buffer latch only
X	0	X	X	12.5 μ s settling time
X	1	X	X	2.5 μ s settling time
X	X	0	X	Powered-up operation
X	X	1	X	Power down mode

function of the latch control bits (D15 and D12)

Three data transfers are possible. All transfers occur immediately after $\overline{CS}$ goes high and are described in the following sections.

latch A write, latch B update (D15 = high, D12 = X)

The serial interface register (SIR) data are written to latch A and the double buffer latch contents are written to latch B. The double buffer contents are unaffected. This program bit condition allows simultaneous output updates of both DACs.

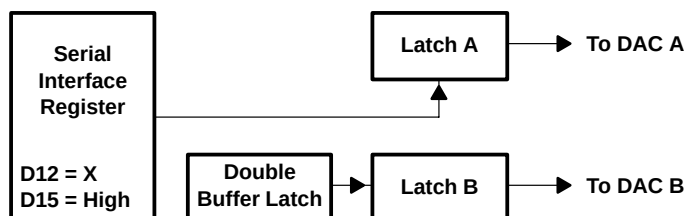


Figure 19. Latch A Write, Latch B Update

APPLICATION INFORMATION

latch B and double-buffer 1 write (D15 = low, D12 = low)

The SIR data are written to both latch B and the double buffer. Latch A is unaffected.

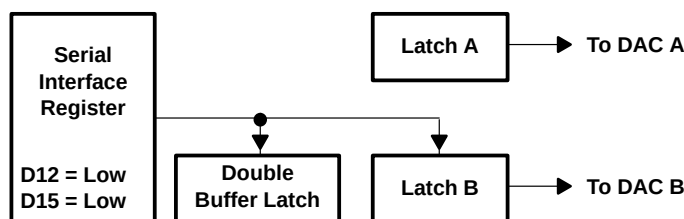


Figure 20. Latch B and Double-Buffer Write

double-buffer-only write (D15 = low, D12 = high)

The SIR data are written to the double buffer only. Latch A and B contents are unaffected.

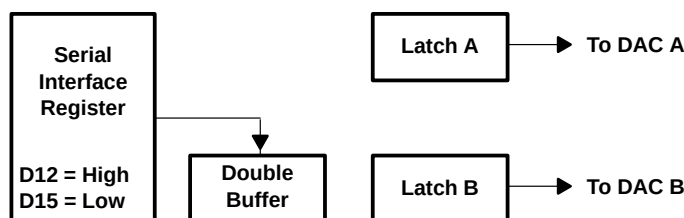


Figure 21. Double-Buffer-Only Write

purpose and use of the double buffer

Normally only one DAC output can change after a write. The double buffer allows both DAC outputs to change after a single write. This is achieved by the two following steps.

1. A double-buffer-only write is executed to store the new DAC B data without changing the DAC A and B outputs.
2. Following the previous step, a write to latch A is executed. This writes the SIR data to latch A and also writes the double-buffer contents to latch B. Thus both DACs receive their new data at the same time, and so both DAC outputs begin to change at the same time.

Unless a double-buffer-only write is issued, the latch B and double-buffer contents are identical. Thus, following a write to latch A or B with another write to latch A does not change the latch B contents.

operational examples

changing the latch A data from zero to full code

Assuming that latch A starts at zero code (e.g., after power up), the latch can be filled with 1s by writing (bit D15 on the left, D0 on the right)

1X0X 1111 1111 1111

to the serial interface. Bit D14 can be zero to select slow mode or one to select fast mode. The other X can be zero or one (don't care).

The latch B contents and the DAC B output are not changed by this write unless the double-buffer contents are different from the latch B contents. This can only be true if the last write was a double-buffer-only write.

TLC5618, TLC5618A

PROGRAMMABLE DUAL 12-BIT DIGITAL-TO-ANALOG CONVERTERS

SLAS156G – JULY 1997 – REVISED APRIL 2001

APPLICATION INFORMATION

changing the latch B data from zero to full code

Assuming that latch B starts at zero code (e.g., after power-up), the latch can be filled with 1s by writing (bit D15 on the left, D0 on the right).

0X00 1111 1111 1111

to the serial interface. Bit D14 can be zero to select slow mode or one to select fast mode. The data (bits D0 to D11) are written to both the double buffer and latch B.

The latch A contents and the DAC A output are not changed by this write.

double-buffered change of both DAC outputs

Assuming that DACs A and B start at zero code (e.g., after power-up), if DAC A is to be driven to mid-scale and DAC B to full-scale, and if the outputs are to begin rising at the same time, this can be achieved as follows:

First,

0d01 1111 1111 1111

is written (bit D15 on the left, D0 on the right) to the serial interface. This loads the full-scale code into the double buffer but does not change the latch B contents and the DAC B output voltage. The latch A contents and the DAC A output are also unaffected by this write operation.

Changing from fast to slow or slow to fast mode changes the supply current which can glitch the outputs, and so D14 (designated by d in the above data word) should be set to maintain the speed mode set by the previous write.

Next,

1X0X 1000 0000 0000

is written (bit D15 on the left, D0 on the right) to the serial interface. Bit D14 can be zero to select slow mode or one to select fast mode. The other X can be zero or one (don't care). This writes the mid-scale code (100000000000) to latch A and also copies the full-scale code from the double buffer to latch B. Both DAC outputs thus begin to rise after the second write.

DSP serial interface

Utilizing a simple 3-wire serial interface shown in Figure 22, the TLC5618A can be interfaced to TMS320 compatible serial ports. The 5618A has an internal state machine that will count 16 clocks after receiving a falling edge of $\overline{CS}$ and then disable further clocking in of data until the next falling edge is received on $\overline{CS}$. Therefore $\overline{CS}$ can be connected directly to the FS pins of the serial port and only the leading falling edge of the DSP will be used to start the write process. The TLC5618A is designed to be used with the TMS320Cxx DSP in burst mode serial port transmit operation.



APPLICATION INFORMATION

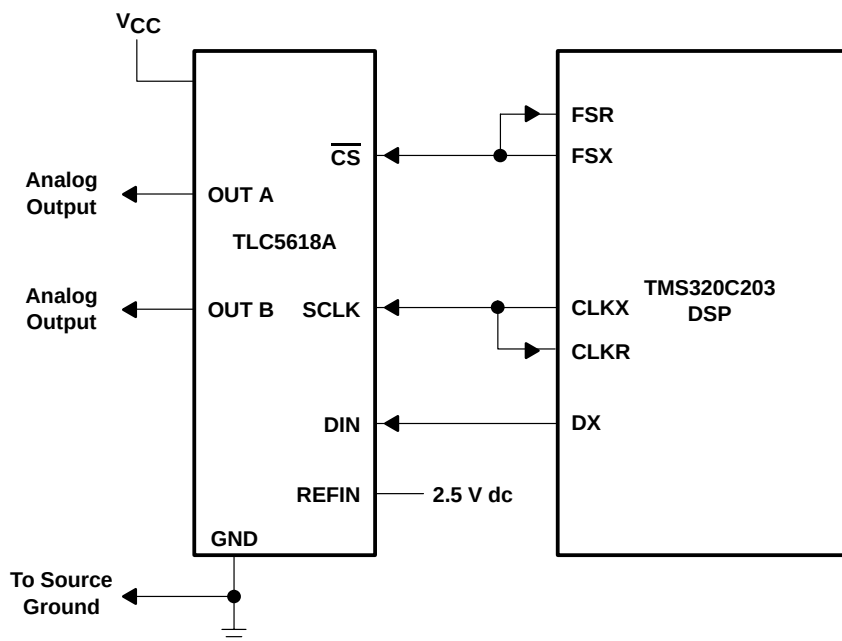


Figure 22. Interfacing The TLC5618A to the TMS320C203 DSP

general serial interface

Both the TLC5618 and TLC5618A are compatible with SPI, QSPI, or Microwire serial standards. The hardware connections are shown in Figures 23 and 24. The TLC5618A has an internal state machine that will count 16 clocks after the falling edge of $\overline{CS}$ and then internally disable the device. The internal edge is ORed together with $\overline{CS}$ so that the rising edge can be provided to $\overline{CS}$ prior to the occurrence of the internal edge to also disable the device.

The SPI and Microwire interfaces transfer data in 8-bit bytes, therefore, two write cycles are required to input data to the DAC. The QSPI interface, which has a variable input data length from 8 to 16 bits, can load the DAC input register in one write cycle.

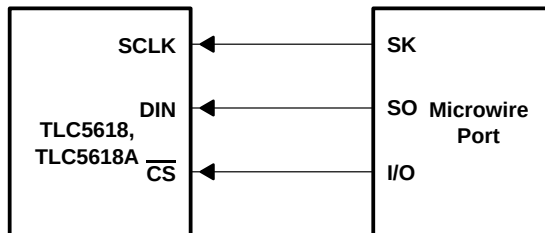


Figure 23. Microwire Connection

TLC5618, TLC5618A PROGRAMMABLE DUAL 12-BIT DIGITAL-TO-ANALOG CONVERTERS

SLAS156G – JULY 1997 – REVISED APRIL 2001

APPLICATION INFORMATION

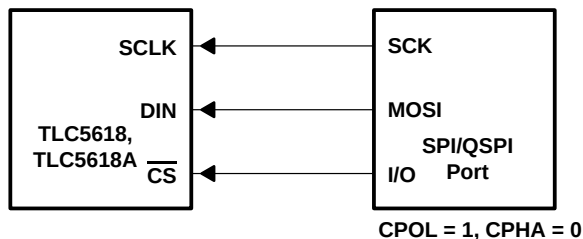


Figure 24. SPI/QSPI Connection

linearity, offset, and gain error using single end supplies

When an amplifier is operated from a single supply, the voltage offset can still be either positive or negative. With a positive offset, the output voltage changes on the first code change. With a negative offset the output voltage may not change with the first code depending on the magnitude of the offset voltage.

The output amplifier attempts to drive the output to a negative voltage. However, because the most negative supply rail is ground, the output cannot drive below ground and clamps the output at 0 V.

The output voltage then remains at zero until the input code value produces a sufficient positive output voltage to overcome the negative offset voltage, resulting in the transfer function shown in Figure 25.

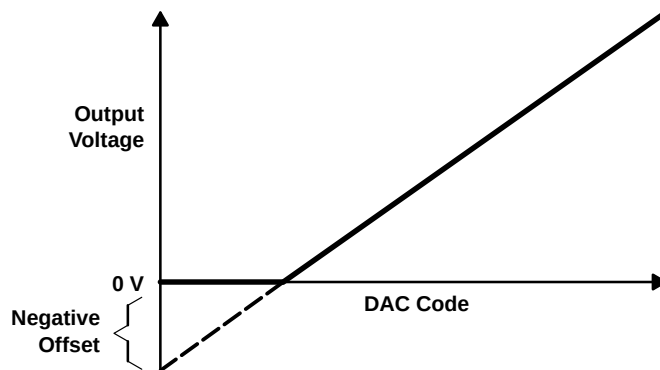


Figure 25. Effect of Negative Offset (Single Supply)

This offset error, not the linearity error, produces this breakpoint. The transfer function would have followed the dotted line if the output buffer could drive below the ground rail.

For a DAC, linearity is measured between zero-input code (all inputs 0) and full-scale code (all inputs 1) after offset and full scale are adjusted out or accounted for in some way. However, single supply operation does not allow for adjustment when the offset is negative due to the breakpoint in the transfer function. So the linearity is measured between full-scale code and the lowest code that produces a positive output voltage. The code is calculated from the maximum specification for the negative offset.

APPLICATION INFORMATION

power-supply bypassing and ground management

Printed-circuit boards that use separate analog and digital ground planes offer the best system performance. Wire-wrap boards do not perform well and should not be used. The two ground planes should be connected together at the low-impedance power-supply source. The best ground connection may be achieved by connecting the DAC AGND terminal to the system analog ground plane making sure that analog ground currents are well-managed.

A 0.1- μF ceramic bypass capacitor should be connected between V_{DD} and AGND and mounted with short leads as close as possible to the device. Use of ferrite beads may further isolate the system analog and digital power supplies.

Figure 26 shows the ground plane layout and bypassing technique.

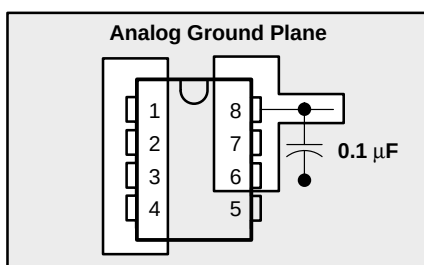


Figure 26. Power-Supply Bypassing

saving power

Setting the DAC register to all 0s minimizes power consumption by the reference resistor array and the output load when the system is not using the DAC.

ac considerations/analog feedthrough

Higher frequency analog input signals may couple to the output through internal stray capacitance. Analog feedthrough is tested by holding $\overline{\text{CS}}$ high, setting the DAC code to all 0s, sweeping the frequency applied to REFIN, and monitoring the DAC output.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
5962-9955702Q2A	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	-55 to 125	5962- 9955702Q2A TLC5618 AMFKB	Samples
5962-9955702QPA	ACTIVE	CDIP	JG	8	1	TBD	A42	N / A for Pkg Type	-55 to 125	9955702QPA TLC5618AM	Samples
TLC5618ACD	OBSOLETE	SOIC	D	8		TBD	Call TI	Call TI	0 to 70		
TLC5618ACDR	OBSOLETE	SOIC	D	8		TBD	Call TI	Call TI	0 to 70		
TLC5618ACP	OBSOLETE	PDIP	P	8		TBD	Call TI	Call TI	0 to 70		
TLC5618AID	OBSOLETE	SOIC	D	8		TBD	Call TI	Call TI	-40 to 85		
TLC5618AIDR	OBSOLETE	SOIC	D	8		TBD	Call TI	Call TI	-40 to 85		
TLC5618AIP	OBSOLETE	PDIP	P	8		TBD	Call TI	Call TI	-40 to 85		
TLC5618AMFKB	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	-55 to 125	5962- 9955702Q2A TLC5618 AMFKB	Samples
TLC5618AMJGB	ACTIVE	CDIP	JG	8	1	TBD	A42	N / A for Pkg Type	-55 to 125	9955702QPA TLC5618AM	Samples
TLC5618AQD	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	C5618A	Samples
TLC5618AQDG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM		C5618A	Samples
TLC5618AQDR	OBSOLETE	SOIC	D	8		TBD	Call TI	Call TI	-40 to 125		
TLC5618AQDRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM		C5618A	Samples
TLC5618CD	OBSOLETE	SOIC	D	8		TBD	Call TI	Call TI			
TLC5618CDR	OBSOLETE	SOIC	D	8		TBD	Call TI	Call TI			
TLC5618ID	OBSOLETE	SOIC	D	8		TBD	Call TI	Call TI			
TLC5618IDR	OBSOLETE	SOIC	D	8		TBD	Call TI	Call TI			

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

⁽²⁾ Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

⁽³⁾ MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

⁽⁴⁾ There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

⁽⁵⁾ Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

⁽⁶⁾ Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF TLC5618A, TLC5618AM :

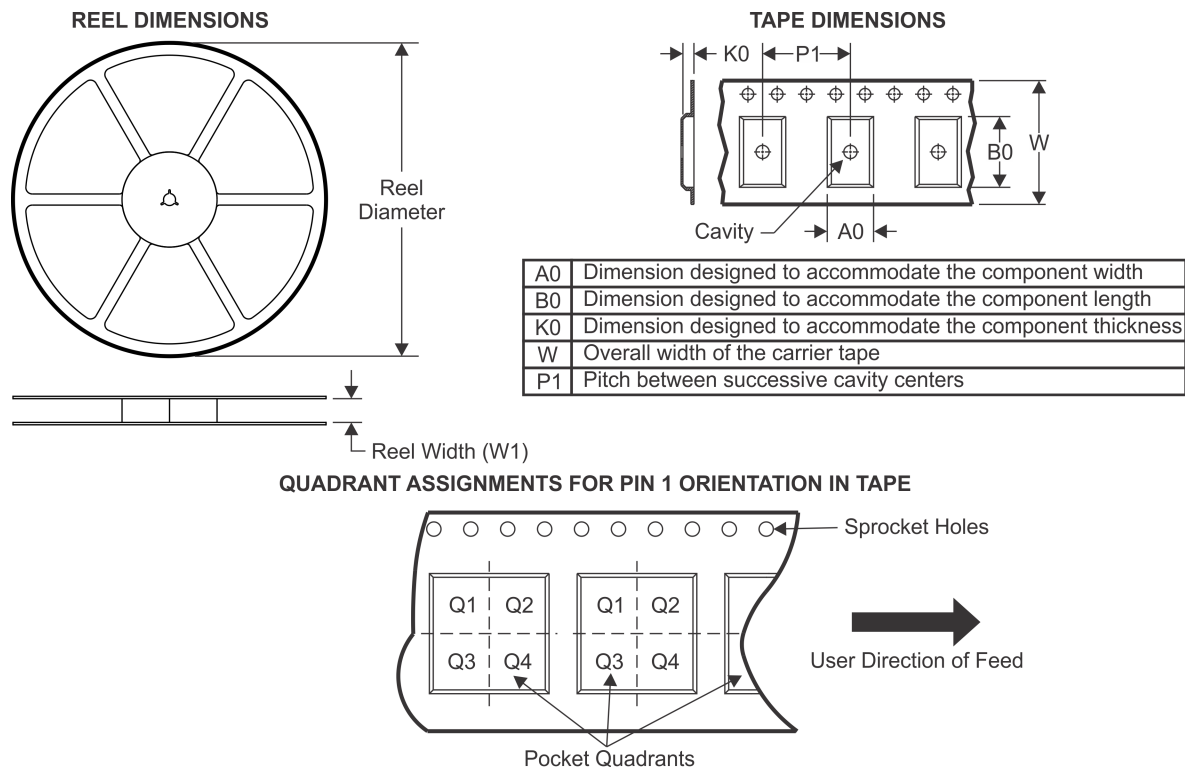
- Catalog: [TLC5618A](#)

- Military: [TLC5618AM](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product

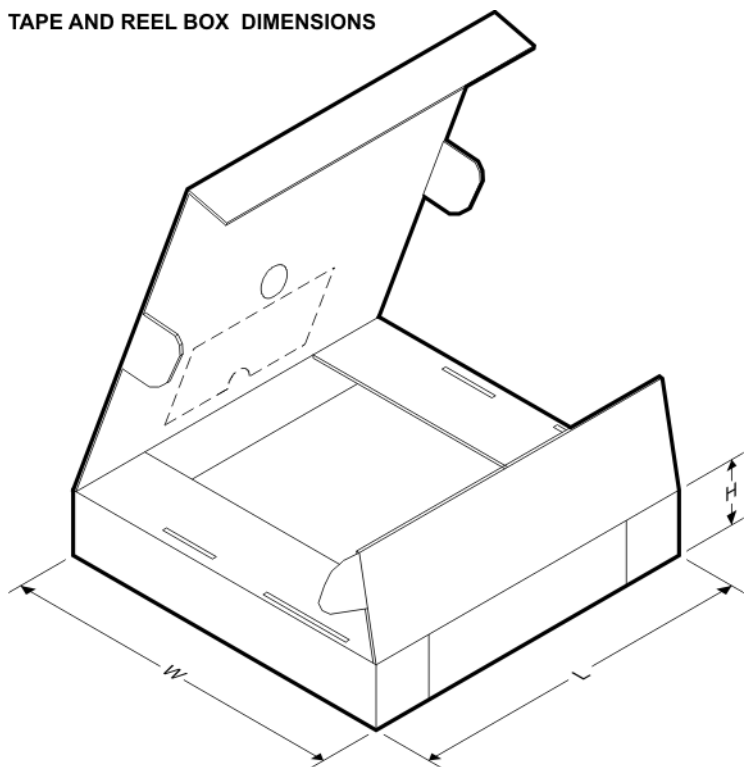
-
- Military - QML certified for Military and Defense Applications

TAPE AND REEL INFORMATION


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TLC5618AQDRG4	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TLC5618AQDRG4	SOIC	D	8	2500	367.0	367.0	38.0

IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, enhancements, improvements and other changes to its semiconductor products and services per JESD46, latest issue, and to discontinue any product or service per JESD48, latest issue. Buyers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All semiconductor products (also referred to herein as "components") are sold subject to TI's terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its components to the specifications applicable at the time of sale, in accordance with the warranty in TI's terms and conditions of sale of semiconductor products. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by applicable law, testing of all parameters of each component is not necessarily performed.

TI assumes no liability for applications assistance or the design of Buyers' products. Buyers are responsible for their products and applications using TI components. To minimize the risks associated with Buyers' products and applications, Buyers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right relating to any combination, machine, or process in which TI components or services are used. Information published by TI regarding third-party products or services does not constitute a license to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of significant portions of TI information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. TI is not responsible or liable for such altered documentation. Information of third parties may be subject to additional restrictions.

Resale of TI components or services with statements different from or beyond the parameters stated by TI for that component or service voids all express and any implied warranties for the associated TI component or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Buyer acknowledges and agrees that it is solely responsible for compliance with all legal, regulatory and safety-related requirements concerning its products, and any use of TI components in its applications, notwithstanding any applications-related information or support that may be provided by TI. Buyer represents and agrees that it has all the necessary expertise to create and implement safeguards which anticipate dangerous consequences of failures, monitor failures and their consequences, lessen the likelihood of failures that might cause harm and take appropriate remedial actions. Buyer will fully indemnify TI and its representatives against any damages arising out of the use of any TI components in safety-critical applications.

In some cases, TI components may be promoted specifically to facilitate safety-related applications. With such components, TI's goal is to help enable customers to design and create their own end-product solutions that meet applicable functional safety standards and requirements. Nonetheless, such components are subject to these terms.

No TI components are authorized for use in FDA Class III (or similar life-critical medical equipment) unless authorized officers of the parties have executed a special agreement specifically governing such use.

Only those TI components which TI has specifically designated as military grade or "enhanced plastic" are designed and intended for use in military/aerospace applications or environments. Buyer acknowledges and agrees that any military or aerospace use of TI components which have **not** been so designated is solely at the Buyer's risk, and that Buyer is solely responsible for compliance with all legal and regulatory requirements in connection with such use.

TI has specifically designated certain components as meeting ISO/TS16949 requirements, mainly for automotive use. In any case of use of non-designated products, TI will not be responsible for any failure to meet ISO/TS16949.

Products

Audio	www.ti.com/audio
Amplifiers	amplifier.ti.com
Data Converters	dataconverter.ti.com
DLP® Products	www.dlp.com
DSP	dsp.ti.com
Clocks and Timers	www.ti.com/clocks
Interface	interface.ti.com
Logic	logic.ti.com
Power Mgmt	power.ti.com
Microcontrollers	microcontroller.ti.com
RFID	www.ti-rfid.com
OMAP Applications Processors	www.ti.com/omap
Wireless Connectivity	www.ti.com/wirelessconnectivity

Applications

Automotive and Transportation	www.ti.com/automotive
Communications and Telecom	www.ti.com/communications
Computers and Peripherals	www.ti.com/computers
Consumer Electronics	www.ti.com/consumer-apps
Energy and Lighting	www.ti.com/energy
Industrial	www.ti.com/industrial
Medical	www.ti.com/medical
Security	www.ti.com/security
Space, Avionics and Defense	www.ti.com/space-avionics-defense
Video and Imaging	www.ti.com/video

TI E2E Community

e2e.ti.com