TPS24740
TPS24741
TPS24742

SLVSCV6A – JANUARY 2015 – REVISED FEBRUARY 2015

TPS2474x 2.5-V to 18-V High Performance Hot Swap and ORing Controller

Check for Samples: TPS24740, TPS24741, TPS24742

1 Features

- 2.5V to 18V Bus Operation (30V abs max)
- Programmable Protection Settings:
  - Current Limit: ±5% at 10mV
  - Fast Trip: ±10% at 20mV
  - Reverse Voltage: ±1mV at –1 mV
- Programable Response Time for Fast Trip and Reverse Voltage
- Programmable FET SOA Protection
- Dual Timer (Inrush/Fault)
- Interchangeable Hot Swap and ORing
- Analog Current Monitor (1% at 25mV)
- Status Flags for Faults and Power Good
- UV and OV Protection
- Independent EN for Hot Swap and ORing
- 4mm × 4mm 24-pin QFN
- 40 = Latch, 41 = Retry, 42 = Fast Latch Off

2 Applications

- Enterprise Storage
- Power Muxing
- Redundant Power Supplies
- Battery Back Up

3 Description

The TPS2474x is an integrated ORing and Hot Swap controller for 2.5 V to 18 V systems. It's precise and programmable protection settings aid in the design of high power, high availability systems where isolating faults is critical.

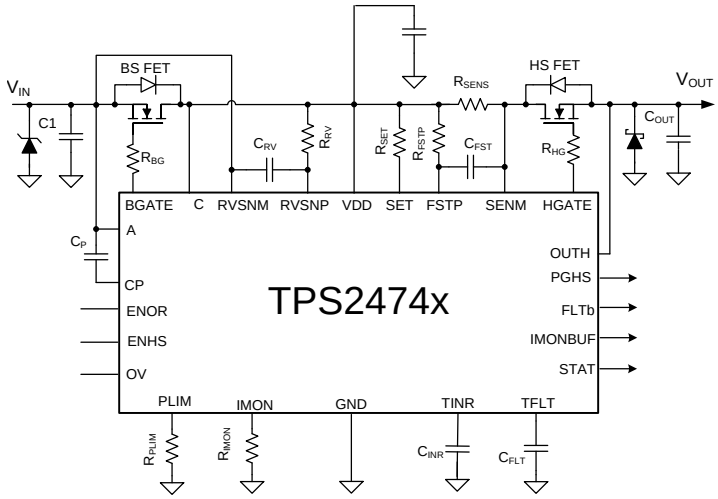
Programmable current limit, fast shut down, and fault timer protect the load and supply during fault conditions such as a hot - short. The fast shutdown threshold and response time can be tuned to ensure a fast response to real faults, while avoiding nuisance trips. Programmable SOA (Safe Operating Area) protection and the inrush timer keep the MOSFET safe under all operating conditions. After asserting a power good, TPS2474x runs the fault timer during over-current events, but doesn't current limit. It shuts down after the fault timer expires. Two independent timers (inrush/fault) allow the user to customize protection based on system requirements. The ORing function of the TPS2474x allows the user to program the reverse voltage threshold and response time to aid in the design of redundant power supply systems.

Device Information(1)

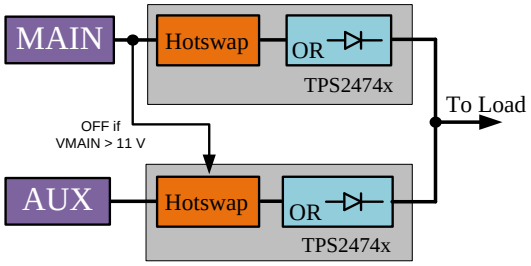
PART NUMBER	PACKAGE	BODY SIZE (NOM)
TPS24740 TPS24741 TPS24742	VQFN (24)	4.00 mm x 4.00 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

4 Simplified Schematics



TPS2474x in Priority Muxing



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5 Revision History

Changes from Original (January 2015) to Revision A **Page**

- Published full Production Data sheet to include *Specification* tables, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section ... 4

6 Device Comparison Table

PART NUMBER(1)	LATCH / RETRY OPTION
TPS24740	Latch
TPS24741	Auto – Retry
TPS24742	Fast Latch Off

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.

7 Pin Configuration and Functions

QFN 24-Pin with Thermal Pad
RGE Package
Top View

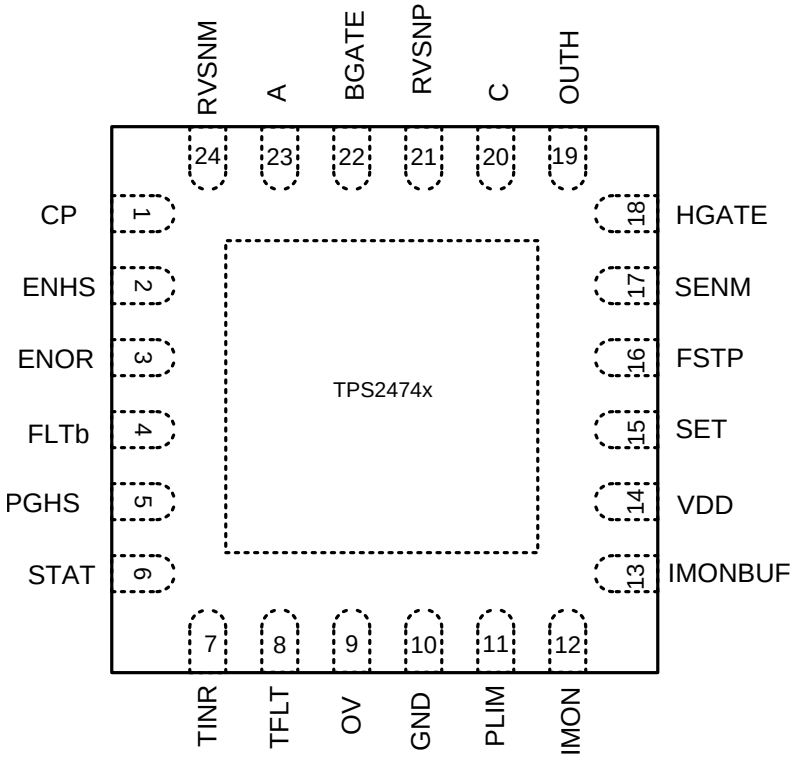


Table 1. Pin Functions

PIN		TYPE(1)	DESCRIPTION
NAME	NO.		
A	23	I/P	Voltage sense input that connects to the OR MOSFET's body diode's anode. Connect to the OR MOSFET source in the typical configuration. A pin is used to supply power to the ORing block of the TPS2474x under certain biasing conditions.
BGATE	22	O	Connect to the gate of the external OR MOSFET. Controls the OR MOSFET to emulate a low forward-voltage diode.
C	20	I/P	Voltage sense input that connects to the OR MOSFET's body diode's cathode. Connect to the OR MOSFET drain in the typical configuration. C pin is used to supply power to the ORing block of the TPS2474x under certain biasing conditions.
CP	1	I/O	Connect a storage capacitor from CP to A for fast turn-on of blocking Gate.
ENHS	2	I	Active-high enable input of Hot-swap. Logic input. Connects to resistor divider.
ENOR	3	I	Active-high enable input of Oring. Logic input. Connects to resistor divider.

(1) I = Input; O = Output ; P = Power

Table 1. Pin Functions (continued)

PIN		TYPE(1)	DESCRIPTION
NAME	NO.		
FLTb	4	O	Active-low, open-drain output indicating various faults.
FSTP	16	I	Fast trip programming set pin for hot-swap. Connect R_{FSTP} from the positive terminal of the Hot Swap sense resistor to the FSTP pin.
GND	10	–	Ground.
HGATE	18	O	Gate driver output for external Hot Swap MOSFET.
IMON	12	I/O	Analog current monitor and load current limit program point. Connect R_{IMON} to ground.
IMONBUF	13	O	Voltage output proportional to the load current (0V–3.0V).
OUTH	19	I	Output voltage sensor for monitoring Hot Swap MOSFET power. Connects to the source terminal of the hot-swap N channel MOSFET.
OV	9	I	Overvoltage comparator input. Connects to resistor divider. HGATE and BGATE are pulled low when OV exceeds the threshold. Connect to ground when not used.
PGHS	5	O	Active-high, open-drain power-good indicator.
PLIM	11	I	Power-limiting programming pin. A resistor from this pin to GND sets the maximum power dissipation for the Hot Swap FET.
RVSNP	21	I	Positive input of the reverse voltage comparator. Connect a resistor from RVSNP to C to set the reverse voltage trip point of the blocking FET.
RVSNM	24	I	Negative input of the reverse voltage comparator.
SENM	17	I	Current-sensing input for the sensing resistor. Directly connects to the negative terminal of the sensing resistor.
SET	15	I	Current-limit programming set pin for hot-swap. A resistor is connected from positive terminal of the sensing resistor.
STAT	6	O	High when BGATE is ON.
TFLT	8	I/O	Fault timer, which runs when the device goes from regular operation to an over-current condition.
TINR	7	I/O	Inrush timer, which runs during the inrush operation (start-up) if the part is in current limit or power limit.
VDD	14	P	Power Supply.

8 Specifications

8.1 Absolute Maximum Ratings

Unless otherwise noted, these apply over recommended operating junction temperature: -40°C ≤ T_J ≤ 125°C. (1)

		MIN	MAX	UNIT
Input Voltage	CP, BGATE	–0.3	40	V
	VDD,SET, FSTP,SENM, OUTH, C, RVSNP, RVSNM, A, ENHS, ENOR, FLTb, PGHS, OV, STAT	–0.3	30	V
	CP, BGATE to A	–0.3	12	V
	HGATE to OUTH	–0.3	15	V
	SET to VDD	–0.3	0.3	V
	SENM, FSTP to VDD	–0.6	0.3	V
	A to C	–30	7	V
	RVSNM, to A, C, RVSNP RVSNP to A, C, RVSNM	–30	30	V
	TINR, TFLT, PLIM, IMON,	–0.3	3.6	V
	IMONBUF	–0.3	7	V
Sink Current	FLTb, PGHS, STAT		5	mA
Source Current	IMON, IMONBUF		5	mA
Storage temperature range, T_{stg}		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

8.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$ (1)	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 (2)	±1500	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101 (3)	±500	

(1) Electrostatic discharge (ESD) measures device sensitivity and immunity to damage caused by assembly line electrostatic discharges into the device.
(2) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(3) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

8.3 Recommended Operating Conditions

These apply over recommended operating junction temperature: -40°C ≤ T_J ≤ 125°C.

		MIN	MAX	UNIT
Input voltage	VDD, SENM, SET (1), FSTP	2.5	18	V
	ENHS, ENOR, FLTb, PGHS, STAT, OUTH	0	18	
	A, C, RVSNM, RVSNP; (2)	0.7	18	
Sink current	FLTb, PGHS, STAT	0	2	mA
Source current	IMON	0	1	mA
External resistance	PLIM	4.99	500	kΩ
	IMON	1	6	kΩ
	RVSNP	10	1000	Ω
	FSTP	10	4000	Ω
	SET	10	400	Ω
R_{IMON} / R_{SET}	w/o R_{STBL} (3)	10	70	
	With appropriate R_{STBL}	3	10	
External capacitor	CP, FSTP, RVSNP	1	1000	nF
	HGATE, BGATE (4)	0	1	µF
	TINR, TFLT	1		nF
	IMON		30	pF
	IMONBUF		100	pF
Operating junction temperature, T_J		–40	125	°C

(1) Do not apply voltage to these pins.
(2) For the HS then ORing application these pins may be below the recommended minimum during start-up. The part is designed to function properly under these scenarios. However the part should not be used with a bus voltage below the recommended voltage.
(3) Refer to R_{STBL} Requirement for R_{IMON} / R_{SET} < 10 describe in section Select R_{SNS} and $V_{SNS,CL}$ Setting.
(4) External capacitance tied to HGATE, BGATE should be in series with a resistor no less than 1kΩ.

8.4 Thermal Information

THERMAL METRIC (1)		TPS24740, TPS24741, TPS24742	UNIT
		RGE (24 PINS)	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	34.6	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	38.4	
$R_{\theta JB}$	Junction-to-board thermal resistance	12.9	
ψ_{JT}	Junction-to-top characterization parameter	0.5	
ψ_{JB}	Junction-to-board characterization parameter	12.9	
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	3.2	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

8.5 Electrical Characteristics

Unless otherwise noted these limits apply to the following: -40°C ≤ T_J ≤ 125°C; 2.5V < V_{VDD} , V_{OUTH} < 18V; 0.7 V < V_A , V_C , V_{RVSNM} < 18 V; V_{ENHS} = V_{ENOR} = 2 V, V_{OV} = 0 V; V_{BGATE}, V_{HGATE}, V_{PGHS}, V_{STAT}, V_{FLTb}, and $V_{IMONBUF}$ are floating; C_{CP} = 100 nF, C_{INR} = 1 nF, C_{FLT} = 1 nF, R_{SET} = 44.2 Ω, R_{IMON} = 2.98 kΩ, R_{FSTP} = 200 Ω, R_{RV} = 200 Ω, and R_{PLIM} = 52 kΩ.

PARAMETER		TEST CONDITION	MIN	TYP	MAX	UNIT
INPUT SUPPLY (VDD)						
V_{UVR}	UVLO threshold, rising		2.2	2.32	2.45	V
V_{UVhyst}	UVLO hysteresis			0.1		V
I_{QON}	Supply current: I_{VDD}+I_A+I_C+ I_{OUTH}	Device on, V_{ENHS} = V_{ENOR} = 2V		4.2	6	mA
HOT SWAP FET ENABLE (ENHS)						
V_{ENHS}	Threshold voltage, rising		1.3	1.35	1.4	V
$V_{ENHShyst}$	Hysteresis			50		mV
I_{ENHS}	Input Leakage Current	0 ≤ V_{ENHS} ≤ 30V	–1		1	µA
BLOCKING (ORING) FET ENABLE (ENOR)						
V_{ENOR}	Threshold voltage, rising		1.3	1.35	1.4	V
$V_{ENORhyst}$	Hysteresis			50		mV
I_{ENOR}	Input leakage current	0 V ≤ V_{ENOR} ≤ 30V	–1	0	1	µA
OVER VOLTAGE (OV)						
V_{OVR}	Threshold voltage, rising		1.3	1.35	1.4	mV
V_{OVhyst}	Hysteresis			50		mV
I_{OV}	Input leakage current	0 ≤ V_{OV} ≤ 30V	–1		1	µA
POWER LIMIT PROGRAMING (PLIM)						
$V_{PLIM,BIAS}$	Bias voltage	Sourcing 10µA	0.66	0.675	0.69	V
$V_{IMON,PL}$	Regulated IMON voltage during power limit	R_{PLIM} = 52 kΩ; $V_{SENM-OUTH}$=12V;	114.75	135	155.25	mV
		R_{PLIM} = 105 kΩ; $V_{SENM-OUTH}$=12V;	56.95	67	77.05	
		R_{PLIM} = 261 kΩ; $V_{SENM-OUTH}$=12V;	18.9	27	35.1	
		R_{PLIM} = 105 kΩ; $V_{SENM-OUTH}$=2V;	341.7	402	462.3	
		R_{PLIM} = 105 kΩ; $V_{SENM-OUTH}$=18V;	38.25	45	51.75	
SLOW TRIP THRESHOLD (SET)						
V_{OS_SET}	Input referred offset (V_{SNS} to V_{IMON} scaling)	R_{SET} = 44.2Ω; R_{IMON}=3kΩ to 1.2kΩ (corresponds to $V_{SNS,CL}$=10mV to 25mV)	–150		150	µV
V_{GE_SET}	Gain error (V_{SNS} to V_{IMON} scaling)(1)		–0.4%		0.4%	
FAST TRIP THRESHOLD PROGRAMMING (FSTP)						
I_{FSTP}	FSTP input bias current	V_{FSTP}=12V	95	100	105	µA
$V_{FASTRIP}$	Fast trip threshold	R_{FSTP} = 200 Ω, V_{SNS} when V_{HGATE} ↓	18	20	22	mV
		R_{FSTP} = 1 kΩ, V_{SNS} when V_{HGATE} ↓	95	100	105	
		R_{FSTP} = 4 kΩ, V_{SNS} when V_{HGATE} ↓	380	400	420	
CURRENT MONITOR and CURRENT LIMIT PROGRAMING (IMON)						
$V_{IMON,CL}$	Slow trip threshold at summing node	V_{IMON}↑, when I_{TFLT} starts sourcing	660	675	690	mV
CURRENT MONITOR (IMONBUF)						
$V_{OS\_IMONBUF}$	Buffer offset	V_{IMON} = 50mV to 675mV, Input referred	–3	0	3	mV
$GAIN_{IMONBUF}$	Buffer voltage gain	$\Delta V_{IMONBUF}$F / ΔV_{IMON}	2.97	2.99	3.01	V
$BW_{IMONBUF}$	Buffer closed loop bandwidth	$C_{IMONBUF}$ = 75pF		1		MHz

(1) Specified by characterization, not production tested.

Electrical Characteristics (continued)

Unless otherwise noted these limits apply to the following: -40°C ≤ T_J ≤ 125°C; 2.5V < V_{VDD} , V_{OUTH} < 18V; 0.7 V < V_A , V_C , V_{RVSNM} < 18 V; V_{ENHS} = V_{ENOR} = 2 V, V_{OV} = 0 V; V_{BGATE}, V_{HGATE}, V_{PGHS}, V_{STAT}, V_{FLTb}, and $V_{IMONBUF}$ are floating; C_{CP} = 100 nF, C_{INR} = 1 nF, C_{FLT} = 1 nF, R_{SET} = 44.2 Ω, R_{IMON} = 2.98 kΩ, R_{FSTP} = 200 Ω, R_{RV} = 200 Ω, and R_{PLIM} = 52 kΩ.

PARAMETER		TEST CONDITION	MIN	TYP	MAX	UNIT
HOT SWAP GATE DRIVER (HGATE)						
V_{HGATE}	HGATE output voltage	5 ≤ V_{VDD} ≤ 16V; measure $V_{HGATE-OUTH}$	12	13.6	15.5	V
		2.5V <V_{VDD} < 5V; 16V <V_{VDD} < 20V measure $V_{HGATE-OUTH}$	7	7.95	15	V
$V_{HGATEmax}$	Clamp voltage	Inject 10µA into HGATE, measure $V_{(HGATE\ –\ OUTH)}$	12	13.9	15.5	V
$I_{HGATEsrc}$	Sourcing current	$V_{HGAT-OUTH}$ = 2V-10V	44	55	66	µA
$I_{HGATEfastSink}$	Sinking current for fast trip	$V_{HGATE-OUTH}$ = 2V -15V; $V_{(FSTP\ –\ SENM)}$ = 20mV	0.45	1	1.6	A
$I_{HGATEsustSink}$	Sustained sinking current	Sustained, $V_{HGATE-OUTH}$ = 2V – 15V; V_{ENHS} = 0	30	44	60	mA
CURRENT SENSE NEGATIVE INPUT (SENM)						
I_{SENM}	Input bias current	V_{SENM} = 12V		15	20	µA
INRUSH TIMER (TINR)						
$I_{TINRsrc}$	Sourcing current	V_{TINR} = 0V, In power limit or current limit	8	10.25	12.5	µA
$I_{TINRsink}$	Sinking current	V_{TINR} = 2V, In regular operation	1.5	2	2.5	µA
V_{TINRup}	Upper threshold voltage	Raise V_{TINR} until HGATE starts sinking	1.3	1.35	1.4	V
V_{TINRlr}	Lower threshold voltage	Raise V_{TINR} to 2V. Reduce V_{TINR} until I_{TINR} is sourcing.	0.33	0.35	0.37	v
R_{TINR}	Bleed down resistance	V_{VDD} = 0V, V_{TINR} = 2V	70	104	130	kΩ
$I_{TINR-PD}$	Pulldown current	V_{TINR} = 2V, when V_{ENHS} = 0V	2	4.2	7	mA
$V_{IMON,TINR}$	See (2)	R_{PLIM} = 52kΩ, V_{SENM} = 12V, V_{OUTH} = 0 V. Raise IMON voltage and record IMON when TINR starts sourcing current	47.75	90	132.25	mV
$V_{IMON,PL}$	See (2)	R_{PLIM} = 52kΩ, V_{SENM} = 12V, V_{OUTH} = 0 V. Raise IMON voltage and record IMON when I_{HGATE} starts sinking current.	114.75	135	155.25	mV
$\Delta V_{IMON,TINR}$	See (2)	R_{PLIM} = 52kΩ, V_{SENM} = 12V, V_{OUTH} = 0 V. $\Delta V_{IMON,TINR}$ = $V_{IMON,PL}$ – $V_{IMON,TINR}$	23	45	67	mV
FAULT TIMER (TFLT)						
$I_{TFLTsrc}$	Sourcing current	V_{TFLT} = 0V, PGHS is high and in overcurrent	8	10.25	12.5	µA
$I_{TFLTsink}$	Sinking current	V_{TFLT} = 2V, Not in overcurrent	1.5	2	2.5	µA
V_{TFLTup}	Upper threshold voltage	Raise V_{TFLT} until HGATE starts sinking	1.3	1.35	1.4	V
R_{TFLT}	Bleed down resistance	V_{VDD} = 0V, V_{TFLT} = 2V	70	104	130	kΩ
$I_{TFLT-PD}$	Pulldown current	V_{TFLT} = 2V, when V_{ENHS} = 0V	2	5.6	7	mA
HOT SWAP OUTPUT (OUTH)						
$I_{OUTH,\ BIAS}$	Input bias current	V_{OUTH} = 12V		30	70	µA
CHARGE PUMP FOR BGATE (CP)						
I_{CP}	CP Equivalent charging resistance	V_A = 12 V , 1mA CP current	5	8.7	12.5	kΩ
V_{CP}	CP Output voltage	Max(V_A, V_C, V_{VDD}) > 6 V, Measure V_{CP-A}	9	10	11	V
		6V > Max(V_A, V_C, V_{VDD}) > 4V, Measure V_{CP-A}	5	5.9	11	
		Max(V_A, V_C, V_{VDD}) = 2.5 V, Measure V_{CP-A}	8	9.8	11	
BLOCKING/ORING GATE DRIVER (BGATE)						
I_{BGATE_CHRG}	BGATE Pull up current	V_{AC} = 20mV, pulse		30		mA
		V_{AC} = 20mV, sustained	0.2	0.3	0.4	mA
$I_{BGATEsustSink}$	BGATE Sinking current	Fast turnoff, $V_{BGATE-A}$ = 7V	0.4	0.9	1.4	A
		Sustained, $V_{BGATE-A}$ = 2V to 11V	19	35	65	mA

(2) For more detail on the definition and usage of these parameters refer to section Using SoftStart – I_{HGATE} and TINR Considerations.

Electrical Characteristics (continued)

Unless otherwise noted these limits apply to the following: -40°C ≤ T_J ≤ 125°C; 2.5V < V_{VDD} , V_{OUTH} < 18V; 0.7 V < V_A , V_C , V_{RVSNM} < 18 V; V_{ENHS} = V_{ENOR} = 2 V, V_{OV} = 0 V; V_{BGATE}, V_{HGATE}, V_{PGHS}, V_{STAT}, V_{FLTb}, and $V_{IMONBUF}$ are floating; C_{CP} = 100 nF, C_{INR} = 1 nF, C_{FLT} = 1 nF, R_{SET} = 44.2 Ω, R_{IMON} = 2.98 kΩ, R_{FSTP} = 200 Ω, R_{RV} = 200 Ω, and R_{PLIM} = 52 kΩ.

PARAMETER		TEST CONDITION	MIN	TYP	MAX	UNIT
BLOCKING/ORing ANODE (A)						
I_A	Input current(3)	2.5 V ≤ V_A ≤ 18V			3	mA
V_{A_UVLO}	Undervoltage lockout	V_A increasing and V_{VDD}=V_C=0.7V	1.85	1.93	2.05	V
$V_{A\_UVLO\_hyst}$	Undervoltage lockout hysteresis			0.1		V
BLOCKING/ORing CATHODE (C)						
I_C	Input current(3)	2.5 V ≤ V_C ≤ 18V			3	mA
V_{C_UVLO}	Undervoltage lockout	V_C increasing and V_{DD}=V_A=0.7V	1.85	1.93	2.05	V
V_{C_UVHyst}	Hysteresis			100		mV
V_{FWDTH}	Forward turn-on voltage	Measure V_{AC} when V_{BGATE} ↑	7.5	10	12.5	mV
POSITIVE INPUT OF REVERSE VOLTAGE COMPARATOR (RVSNP)						
I_{RVSNP}	RVSNP Input bias current	V_{RVSNP} = 12V, sinking current; 0.7V < V_A, V_{RVSNM} < 20V	93	99	105	µA
$V_{RVTRIP1}$	Reverse Comparator Offset	R_{RV}=10Ω, Measure $V_{RVSNP-RVSNM}$, when BGATE↓	-1	0	1	mV
NEGATIVE INPUT OF REVERSE VOLTAGE COMPARATOR (RVSNM)						
I_{RVSNM}	Leakage current		–2		2	µA
FAULT INDICATOR (FLTb)						
V_{OL_FLTb}	Output low voltage	Sinking 2 mA		0.11	0.25	V
I_{FLTb}	Input Leakage Current	V_{FLTb} = 0V, 30V	–1	0	1	µA
V_{HSFLT_IMON}	V_{IMON} threshold to detect Hot Swap FET short	V_{ENHS} = 0V, Measured V_{IMON} ↑ to GND when FLTb ↓	88	101	115	mV
V_{HSFL_hyst}	Hysteresis			25		mV
$V_{BFET,\ OPEN,\ FLT}$	A-C threshold to detect OPEN Blocking/ORing FET fault	V_{ENOR}=3V, Measure V_{A-C} to FLTb↓, V_{CP-A} > 7V	350	410	490	mV
V_{CP_FLT}	CP fault threshold	Measure V_{CP-A} ↓ when FLTb↓, 4V ≤ V_{VDD} < 18V	5	5.5	6	V
		Measure V_{CP-A} ↓ when FLTb↓, 2.5V < V_{VDD} < 4V	3.3	3.75	4.2	V
$V_{CP,\ FLT,\ hyst}$	Hysteresis	4V ≤ V_{VDD} < 18V		1.5		V
		2.5V < V_{VDD} < 4V		1.1		V
HOT SWAP POWER GOOD OUTPUT (PGHS)						
V_{PGHSth}	PGHS Threshold	Measure $V_{SENM-OUTH}$ ↓ when PGHS↑	170	270	375	mV
$V_{PGHShyst}$	PGHS hysteresis	$V_{SENM-OUTH}$ ↑		80		mV
V_{OL_PGHS}	PGHS Output low voltage	Sinking 2mA		0.11	0.25	V
I_{PGHS}	PHGS Input leakage current	V_{PGHS}=0V to 30V	–1	0	1	µA
STATUS INDICATOR (STAT)						
V_{STATon}	Status ON threshold	4V ≤ V_{VDD} < 20V , Measure $V_{BGATE\ -\ A}$ ↑, when STAT↑	5	6	7	V
		2.5V < V_{VDD} < 4V , Measure $V_{BGATE\ -\ A}$ ↑, when STAT↑	3.6	4	4.4	V
$V_{STAToff}$	Status OFF threshold	4V < V_{VDD} < 20V , Measure $V_{BGATE\ -\ A}$ ↓, when STAT↓	4	5	6	V
		2.5V <V_{VDD} < 4V , Measure $V_{BGATE\ -\ A}$ ↑, when STAT↑	2	2.7	3.4	V
$V_{STAT,LOWoff}$	STAT Output low voltage	Sinking 2 mA		0.11	0.25	V
$I_{STAT,LEAK}$	STAT Input leakage current	V_{STAT} = 0 V, 30 V	–1	0	1	µA
THERMAL SHUTDOWN (OTSD)						
T_{OTSD}	Thermal shutdown threshold	Temperature rising		140		°C
$T_{OTSD,HYST}$	Hysteresis			10		°C

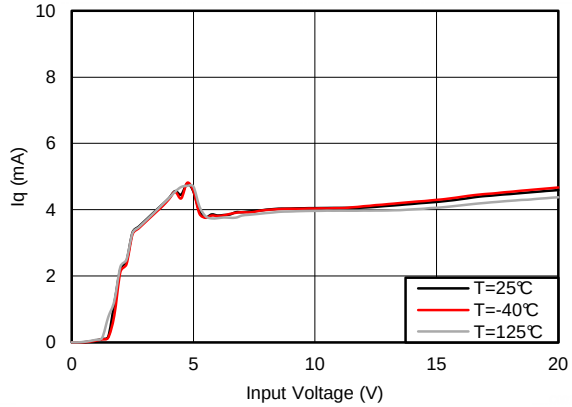
(3) The TPS2474x is set up to be powered from A, C, or VDD depending on the biasing condition. See Internal Power ORing of TPS24740 To obtain the total current draw from A, C, VDD, and OUTH refer to the spec for Input Supply (VDD)..

8.6 Timing Requirements

PARAMETER		TEST CONDITION	MIN	TYP	MAX	UNIT
INPUT SUPPLY (VDD)						
$DEGL_{UVLO}$	UVLO deglitch	Both rising and falling		14		µs
HOT SWAP FET ENABLE (ENHS)						
$DEGL_{ENHS}$	Deglitch time	Both rising and falling	2.2	3.8	5.5	µs
BLOCKING (ORING) FET ENABLE (ENOR)						
$DEGL_{ENOR}$	Deglitch time	Both rising and falling	1.7	3.5	5	µs
OVER VOLTAGE (OV)						
$DEGL_{OV}$	Deglitch time	Both rising and falling	2.2	3.9	5.7	µs
HOT SWAP GATE DRIVER (HGATE)						
$t_{HGATEdly}$	Turn on delay	CP ↑ to I_{HGATE} sourcing		1.9		ms
FAST TRIP (FSTP)						
$t_{FastOffDly}$	Fast turn-off delay	$V_{(FSTP\ -\ SENM)}$: –5mV to 5mV, C_{HGATE} = 0 pF		600		ns
		$V_{(FSTP\ -\ SENM)}$: -20mV to 20mV C_{HGATE} = 0 pF		300		
$t_{FastOffDur}$	Strong pull down current duration		53	63	73	µs
INRUSH TIMER (TINR)						
N_{RETRY}	Number of TINR cycles before retry	TPS24741 only		64		
$RETRY_{DUTY}$	Retry duty cycle	T_{INR} not connected to T_{FLT}		0.35%		
		T_{INR} connected to T_{FLT}		0.7%		
BLOCKING/OR_{ING} GATE DRIVER (BGATE)						
$t_{FastOffDur}$	Strong pull down current duration		10	15	20	µs
$t_{FastOnDur}$	Strong pull up current duration		10	20	30	µs
POSITIVE INPUT OF REVERSE VOLTAGE COMPARATOR (RVSNP)						
$t_{FastOffDly}$	Turn-off delay	$V_{(RVSNP\ -RVSNM)}$ = –5mV → 5mV, C_{BGATE} = 0 pF		340		ns
		$V_{(RVSNP\ -RVSNM)}$ = –20mV → +20mV, C_{BGATE} = 0 pF		150		
FAULT INDICATOR (FLTb)						
t_{FLT_degl}	HS / OR Fault Deglitch	Both HS and ORing faults	2.2	3.9	5.3	ms
$t_{FLT\_CP\_degl}$	CP fault deglitch		26.5	32	37.2	ms
HOT SWAP POWER GOOD OUTPUT (PGHS)						
$t_{PGHSdegl}$	PGHS deglitch time	Rising	0.7	1	1.3	ms
		Falling	7	8	9	
STATUS INDICATOR (STAT)						
$t_{STATdegl}$	STAT Delay (deglitch) time	Rising or falling edge	0.4	0.95	1.5	ms

8.7 Typical Characteristics

Unless otherwise noted these limits apply to the following: V_{VDD} = V_A = V_C = V_{RVSNM} = V_{OUTH} = 12 V; V_{ENHS} = V_{ENOR} = 2 V, V_{OV} = 0 V; V_{BGATE}, V_{HGATE}, V_{PGHS}, V_{STAT}, V_{FLTb}, and $V_{IMONBUF}$ are floating; C_{CP} = 100 nF, C_{INR} = 1 nF, C_{FLT} = 1 nF, R_{SET} = 44.2 Ω, R_{IMON} = 2.98 kΩ, R_{FSTP} = 200 Ω, R_{RV} = 200 Ω, and R_{PLIM} = 52 kΩ.



Iq = I_{VDD} + I_A + I_C + I_{OUTH}

Figure 1.

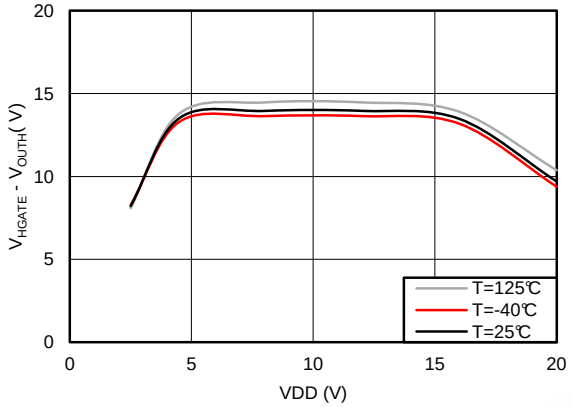


Figure 2.

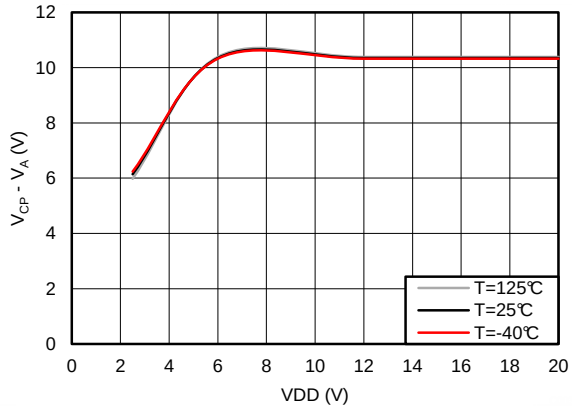
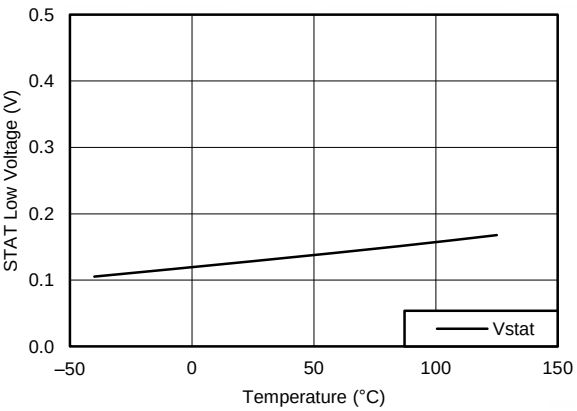
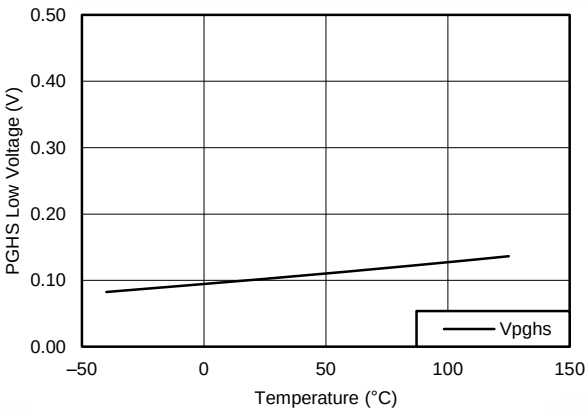


Figure 3.



I_{STAT} = 2mA

Figure 4.



I_{PGHS} = 2mA

Figure 5.

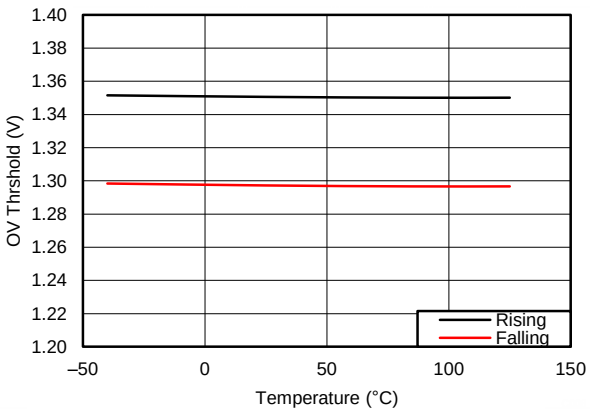


Figure 6.

Typical Characteristics (continued)

Unless otherwise noted these limits apply to the following: V_{VDD} = V_A = V_C = V_{RVSNM} = V_{OUTH} = 12 V; V_{ENHS} = V_{ENOR} = 2 V, V_{OV} = 0 V; V_{BGATE}, V_{HGATE}, V_{PGHS}, V_{STAT}, V_{FLTb}, and $V_{IMONBUF}$ are floating; C_{CP} = 100 nF, C_{INR} = 1 nF, C_{FLT} = 1 nF, R_{SET} = 44.2 Ω, R_{IMON} = 2.98 kΩ, R_{FSTP} = 200 Ω, R_{RV} = 200 Ω, and R_{PLIM} = 52 kΩ.

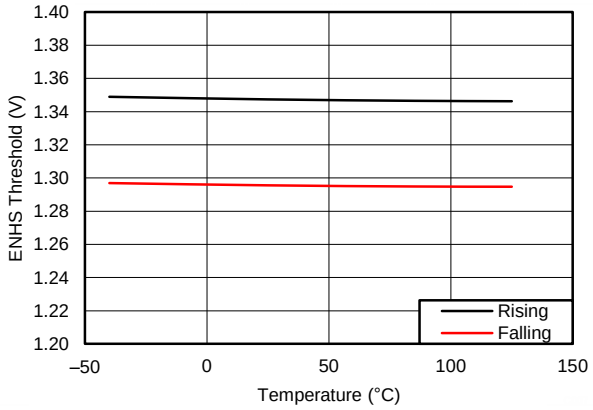


Figure 7.

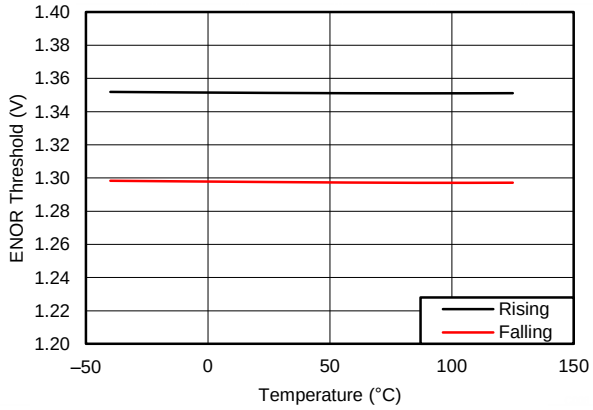
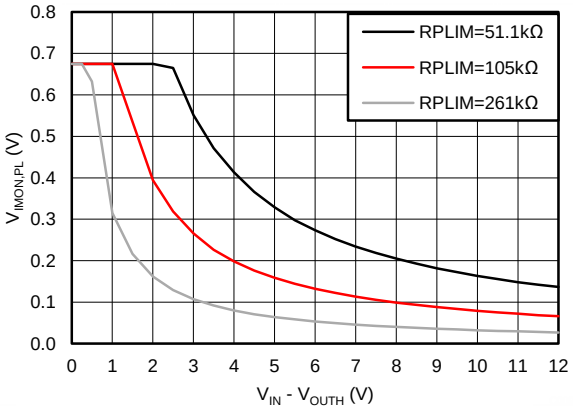
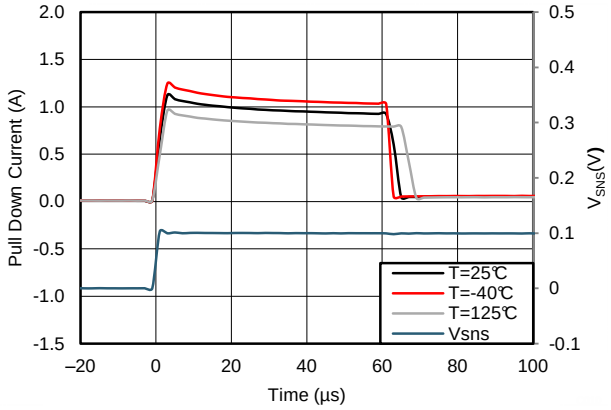


Figure 8.



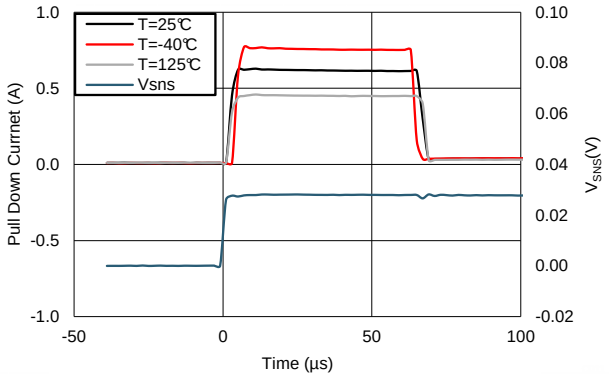
V_{IMON} during Power Limiting

Figure 9.



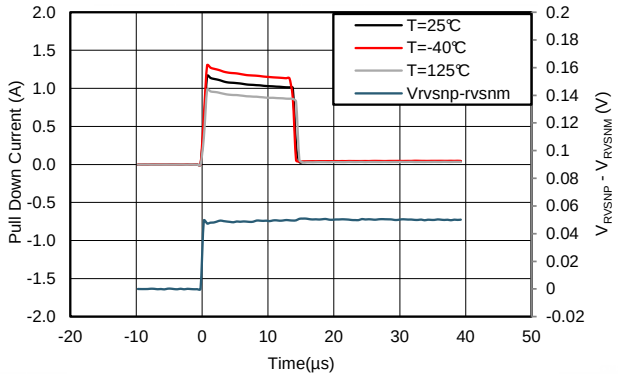
V_{HGATE} - V_{OUTH} = 10V

Figure 10.



V_{HGATE} - V_{OUTH} = 2V

Figure 11.



V_{BGATE} - V_A = 10V

Figure 12.

Typical Characteristics (continued)

Unless otherwise noted these limits apply to the following: V_{VDD} = V_A = V_C = V_{RVSNM} = V_{OUTH} = 12 V; V_{ENHS} = V_{ENOR} = 2 V, V_{OV} = 0 V; V_{BGATE}, V_{HGATE}, V_{PGHS}, V_{STAT}, V_{FLTb}, and $V_{IMONBUF}$ are floating; C_{CP} = 100 nF, C_{INR} = 1 nF, C_{FLT} = 1 nF, R_{SET} = 44.2 Ω, R_{IMON} = 2.98 kΩ, R_{FSTP} = 200 Ω, R_{RV} = 200 Ω, and R_{PLIM} = 52 kΩ.

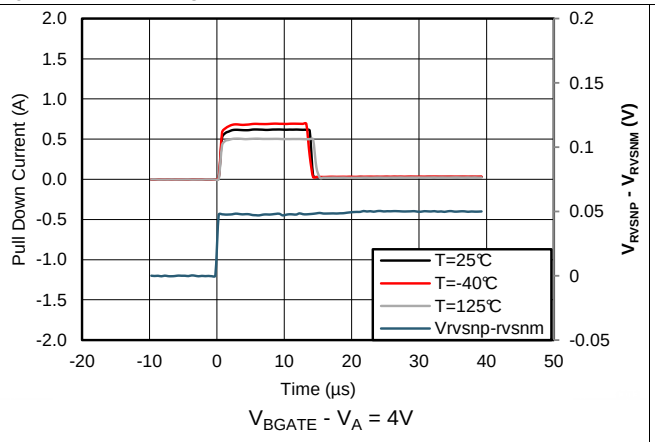


Figure 13.

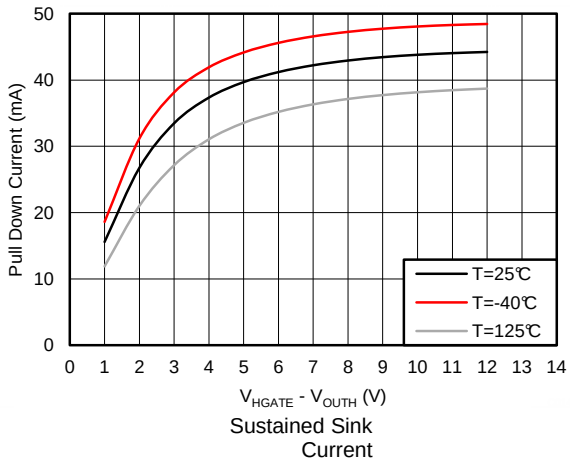


Figure 14.

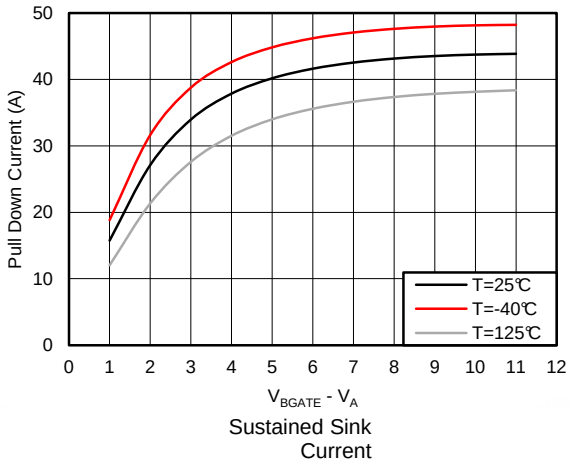


Figure 15.

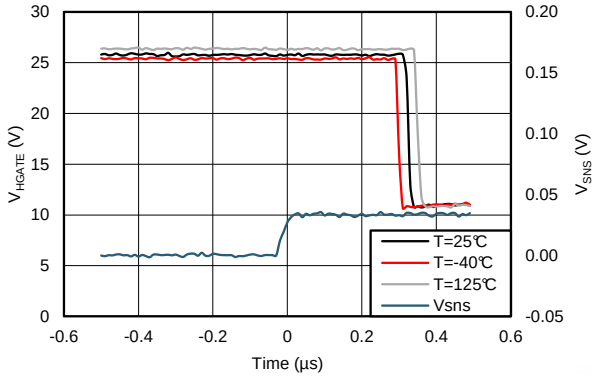


Figure 16.

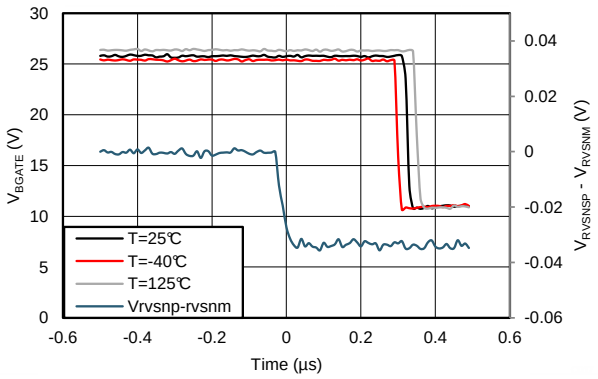


Figure 17.

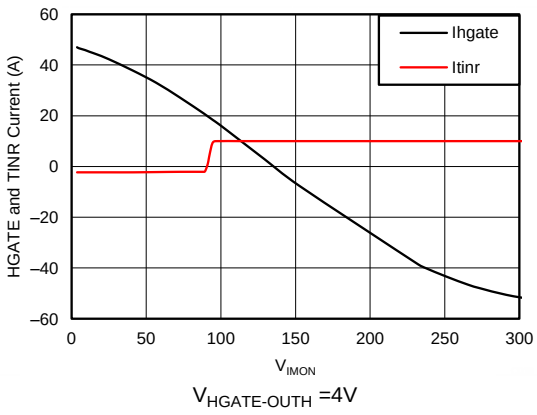


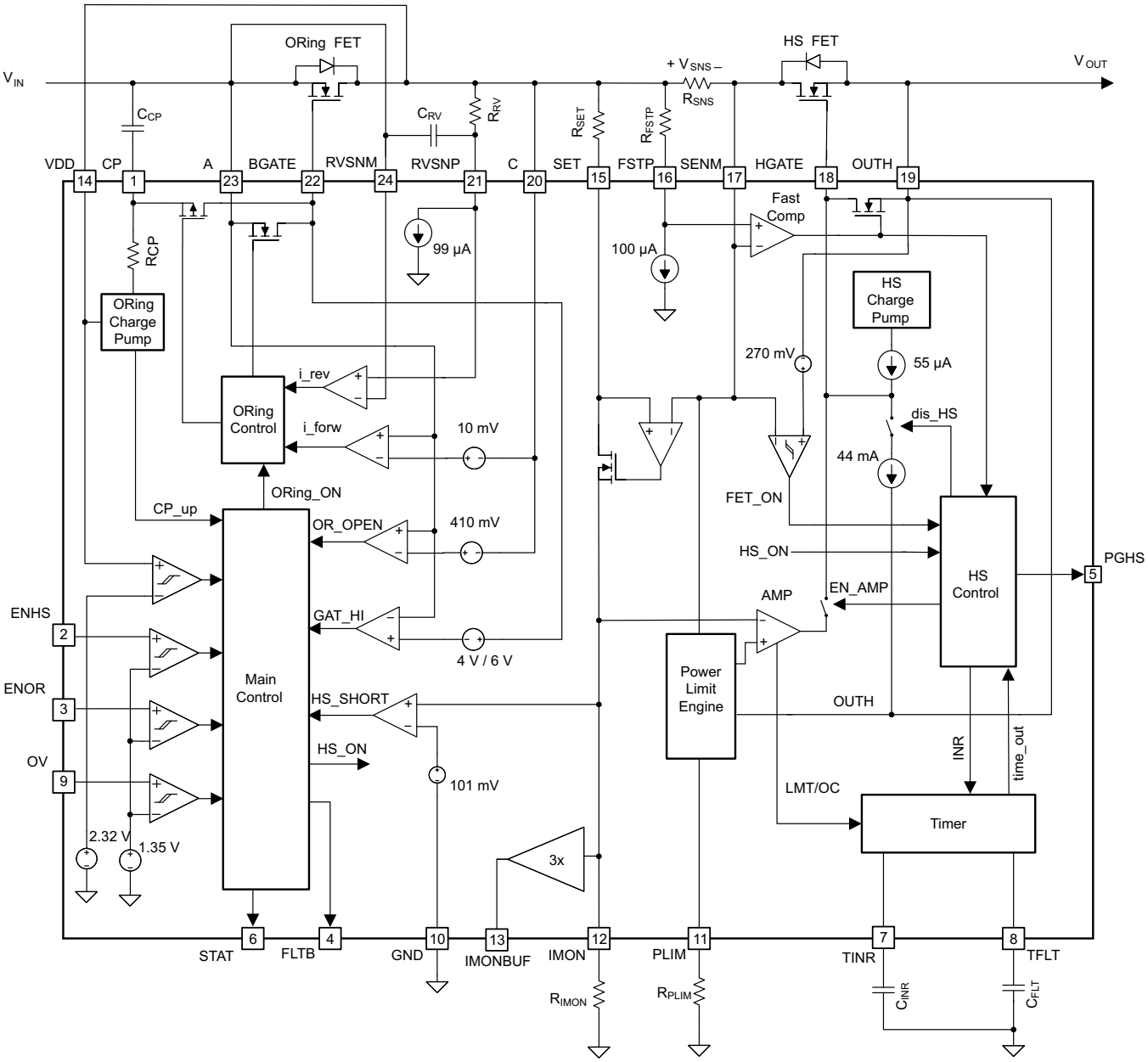
Figure 18.

9 Detailed Description

9.1 Overview

TPS2474x is a Hot Swap and ORing controller with many programmable settings. In addition the ORing and Hot Swap blocks are set-up independently, which allows for the interchangeable order of Hot Swap and ORing. For the ORing controller the RVSNM and RVSNP serve as a way to program the reverse voltage threshold and sense the reverse voltage. The Hot Swap features a programmable current limit, power limit, and fast trip threshold. It also has dual timers: one for inrush and one during over current faults. Finally it features an analog current monitor that can be used to provide current information to a microcontroller.

9.2 Functional Block Diagram



9.3 Feature Description

9.3.1 Internal Power ORing of TPS24740

The ORing function of the TPS2474x runs from an internal bus (V_{INT}), which is derived from ORing A, C, and VDD. This ensures that the TPS2474x can stay powered and functions properly, even if the input or output are shorted to GND. The ORing function's UVLO is derived based on the V_{INT} rail. This does mean that the part can draw up to 3 mA from the A or C pin. Hence it is recommended to keep traces to these pins fairly short and to avoid adding resistors in the path.

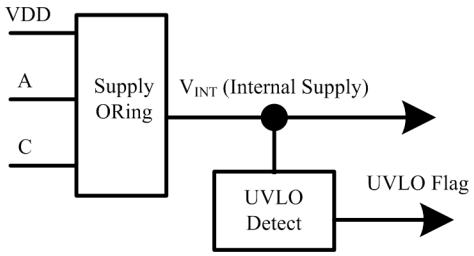


Figure 19. Power ORing

9.3.2 Enable and Over-voltage Protection

Both the Hot Swap section and the ORing section can be independently enabled with the ENHS and ENOR pins respectively. The part is enabled when the pin voltage exceeds 1.35V and is disabled when the pin voltage falls under 1.3V providing 50mV of hysteresis. A resistor divider can be connected to these pins to turn on the TSP2474x at a certain bus voltage. Both the ORing and the Hot Swap FETs will be turned off if the OV pin exceeds 1.35V.

9.3.3 Current Limit and Power Limit During Start-up

The current limit and power limit of the TPS2474x are programmable to protect the load, power supply, and the Hot Swap MOSFET. During start-up the active control loop will regulate the gate to ensure that the current through the MOSFET and the power dissipation of the MOSFET is below their respective pre-programmed thresholds. The maximum current allowed through the MOSFET (I_{LIM}) is determined with Equation 1. $I_{LIM,CL}$ is the programmed current limit, P_{LIM} is the programmed power limit, and V_{DS} is the drain to source voltage across the Hot Swap MOSFET.

$$I_{LIM} = MIN\left(I_{LIM,CL}, \frac{P_{LIM}}{V_{DS}}\right) \quad (1)$$

This results in an IV curve shown in Figure 20. $I_{LIM,PL}$ denotes the maximum allowed MOSFET current (I_{DS}) when the part is in power limit. As V_{DS} increases, $I_{LIM,PL}$ decreases and $I_{LIM,PL,MIN}$ denotes the lowest $I_{LIM,PL}$, which occurs at the largest V_{DS} ($V_{DS,MAX}$). The TPS2474x enforce this by regulating the voltage across R_{SNS} (V_{SNS}). $V_{SNS,PL}$ denotes V_{SNS} when power limiting is active. Similarly to $I_{LIM,PL}$, $V_{SNS,PL}$ decreases as V_{DS} increases and $V_{SNS,PL,MIN}$ corresponds to the lowest $V_{SNS,PL}$, which occurs at $V_{DS,MAX}$. $V_{SNS,CL}$ is a current limiting sense voltage, which is programmable in the TPS2474x.

Feature Description (continued)

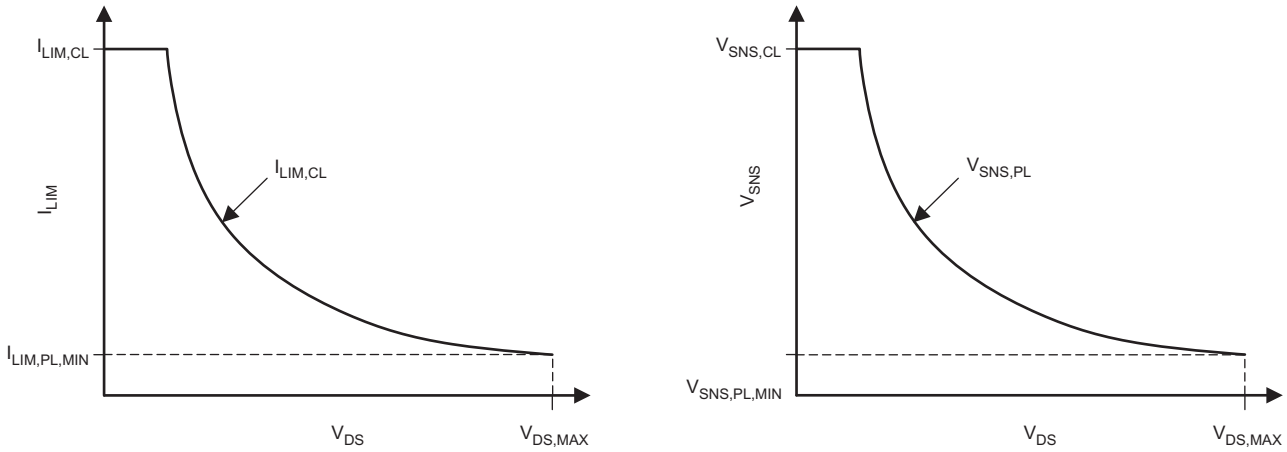


Figure 20. Current vs V_{DS} and V_{SNS} vs V_{DS} Programmed by Power Limit Engine

The current and power limit can be programmed using the equations below.

$$V_{SNS,CL} = \frac{0.675 \times R_{SET}}{R_{IMON}} \quad (2)$$

$$I_{LIM,CL} = \frac{V_{SNS,CL}}{R_{SNS}} = \frac{0.675 \times R_{SET}}{R_{IMON} \times R_{SNS}} \quad (3)$$

$$P_{LIM} = \frac{84375 \times R_{SET}}{R_{PLIM} \times R_{SNS} \times R_{IMON}} \quad (4)$$

Note, that the error is largest at $V_{SNS,PL,MIN}$ due to offset of the internal amplifier. Also the operation at $V_{DS,MAX}$ is most critical because it corresponds to the short circuit condition and has the biggest impact on start time. Thus it is critical to consider $V_{SNS,PL,MIN}$ during design. Equation 5 shows the relationship of $V_{SNS,PL,MIN}$ as a function of P_{LIM}, $I_{LIM,CL}$, $V_{SNS,CL}$, and $V_{DS,MAX}$. Note that $I_{LIM,CL}$ and $V_{DS,MAX}$ are usually determined by the system requirements. The designer will have control over P_{LIM} and $V_{SNS,CL}$. In general, there will be a desire to reduce the power limit to allow for smaller MOSFETs and to reduce the $V_{SNS,CL}$ to improve efficiency (lower R_{SNS}). However, this will also reduce $V_{SNS,PL,MIN}$ and the designer should ensure that it's above the miminum recommended value of 1.5mV.

$$V_{SNS,PL,MIN} = \frac{P_{LIM} \times V_{SNS,CL}}{V_{DS,MAX} \times I_{LIM,CL}} \quad (5)$$

9.3.4 Two Level Protection During Regular Operation

After the TPS2474x has gone through start-up it will no longer actively control HGATE. Instead it will run the timer when the current is between the current limit and the fast trip threshold. Once the timer has expired the gate will be pulled down. If the current ever exceeds the fast trip threshold, HGATE will be pulled down immediately.

9.3.5 Dual Timer (TFLT and TINR)

TPS2474x has two timer pins to allow the user to customize the protection. The TINR pin sources 10.25 µA when the device is in start-up mode and is actively regulating the gate to limit the MOSFET power or current. It sinks 2 µA otherwise. The TFLT pin sources 10.25 µA when the device is in regular operation and the FET current exceeds the current limit. It sinks 2 µA otherwise. If either of the timer pins exceeds 1.35, the TPS2474x times out. The TPS24740 and TPS24742 latches off. The TPS24741 goes through 64 cycles of TINR and attempts to start-up again.

Feature Description (continued)

Since the TINR usually runs when the MOSFET is being stressed, TINR should be sized to maintain the FET within its SOA. In general TFLT runs when the load is drawing more current than expected, which can stress the load and the power supply. Thus TFLT should be programmed to have the right protection settings for the power supply and the load. In some systems the load is allowed to draw current above the current limit for a prolonged time. In that case a large TFLT is required, but a short TINR may still be desired to minimize the worst case FET stress. In other applications a long TINR may be required to due to large downstream capacitances, but drawing excessive current from the power supply for more than 5ms is not desired. In that case a short TFLT and a long TINR should be used. Finally, many applications can use the same TINR and TFLT setting, in which case the pins can be tied together and a single capacitor can be used. The two different options are shown in Figure 21.

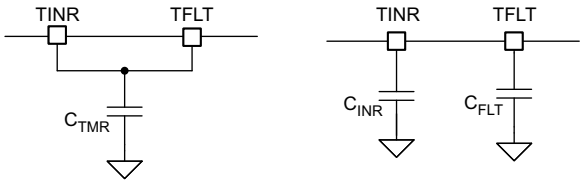


Figure 21. Timer Configurations

If two separate timer capacitors are used their values can be computed with Equation 6 and Equation 7:

$$C_{INR} = 7.59\ \mu F \times T_{INR} \quad (6)$$

$$C_{FLT} = 7.59\ \mu F \times T_{FLT} \quad (7)$$

If a single capacitor is used C_{TMR} can be computed with Equation 8.

$$C_{TMR} = 6.11\ \mu F \times T_{TMR} \quad (8)$$

9.3.6 Using SoftStart – I_{HGATE} and TINR Considerations

During start-up the TPS2474x regulates the HGATE to keep the FET power dissipation within P_{LIM}. This is accomplished by an amplifier that monitors the IMON voltage and an internal reference voltage. The TPS24740 will source current into HGATE if V_{IMON} is lower than the reference voltage and will sink current into HGATE if V_{IMON} is above the reference voltage. In steady state, the V_{IMON} will be regulated to the $V_{IMON,PL}$ point, where I_{HGATE} equals zero. Note that $V_{IMON,PL}$ is determined by R_{PLIM} and the $V_{SENM\ –\ VOUTH}$.

The same amplifier feeds into the inrush timer circuitry to run the timer when the part is in power limit. The V_{IMON} threshold at which the timer starts to source current is denoted as $V_{IMON,\ TINR}$. Note that $V_{IMON,TINR}$ is lower than $V_{IMON,PL}$ to account for tolerances and ensure that the timer is always active when the device is in power limit. The difference between the two thresholds is defined as $\Delta V_{IMON,\ TINR}$. A typical curve of the I_{HGATE} and I_{TINR} is available in the typical characteristics section.

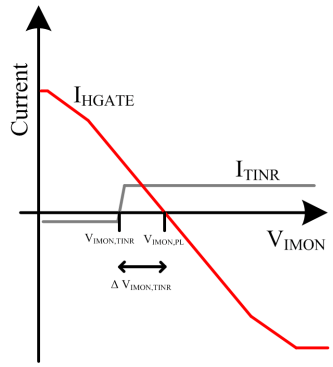


Figure 22. I_{HGATE} Current and TINR Relationship

Feature Description (continued)

It is critical to consider $\Delta V_{IMON,\ TINR}$ and Figure 22 if a soft start circuit is used. Typically, the soft start is implemented by limiting the gate dv/dt with a capacitor, which in turn limits the inrush current to the output capacitor. Often times, the inrush current is kept below $I_{LIM,PL}$ to keep the timer from running. Note that the $I_{LIM,PL}$ is based on the $V_{IMON,PL}$ threshold and thus TINR can be activated even if the inrush current is below $I_{LIM,PL}$. To prevent the timer from running unintentionally, it's important that the minimum power limit (typical P_{LIM} - tolerance) is above $P_{LIM,MIN,SS}$, which can be computed as shown in Equation 9 below. As an example, consider the usage case where the maximum inrush current ($I_{INR,MAX}$) is 2A, the maximum input voltage ($V_{IN,MAX}$) is 13V and R_{SET}, R_{IMON}, and R_{SNS} are 100Ω, 2.7kΩ, and 1mΩ respectively. For that case the power limit should be set to at least 58.3 W + P_{LIM} tolerance to ensure that the inrush timer does not run.

$$P_{LIM,MIN,\ SS} = (I_{INR,MAX} + \Delta V_{IMON,TINR,MAX} \times \frac{R_{SET}}{R_{IMON} \times R_{SNS}}) \times V_{IN,MAX}$$

$$= \left(2A + 67mV \times \frac{100\Omega}{2.7k\Omega \times 1m\Omega}\right) \times 13V = 58.3W \quad (9)$$

9.3.7 Three Options for Response to a Fast Trip

The TPS24740, TPS24741, and TPS24742 have difference responses to a fast trip event to accommodate different design requirements. When the current exceeds the fast trip threshold, the gate is quickly pulled down to minimize damage that can be caused due to a short circuit. Figure 23 shows the response of the variate devices options to a Hotshort on the output. The TPS24740 (latch) attempts to re-start once after the hot-short is observed and then stay off. The TPS24741 continuously retries with a duty cycle of ~0.5% (0.7% if TFLT and TINR are connected, 0.35% if TFLT and TINR are not connected); and, the TPS24742 shuts off and never retries again. In general the TPS24742 (Fast/immediate Latch Off) places the least amount of stress on the MOSFET, but is the least likely to recover from a nuisance trip.

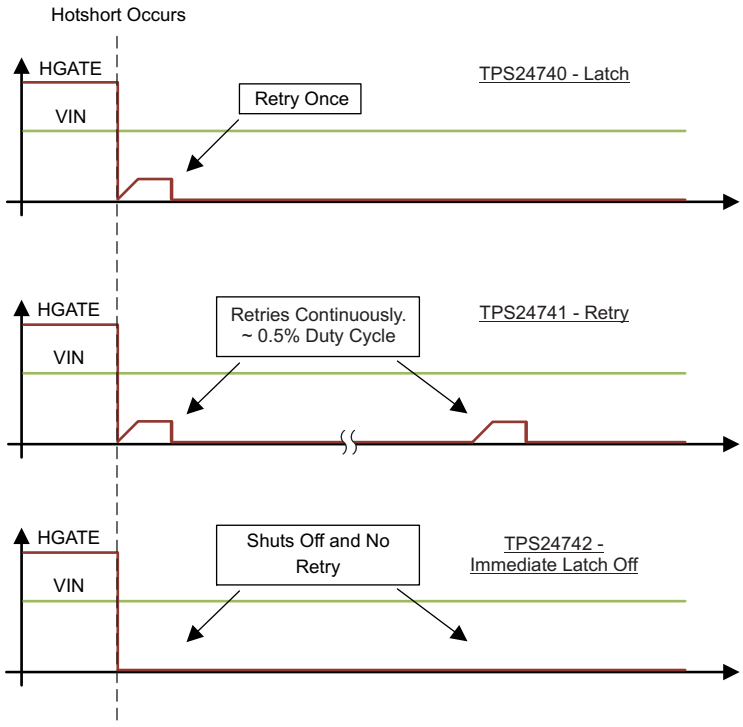


Figure 23. TPS24740/1/2 Response to a Short Circuit

Feature Description (continued)

9.3.8 Programmable Reverse Voltage Threshold

The TPS2474x has a programmable reverse voltage threshold. An internal comparator detects a reverse current condition when RVSNP is above RVSNM. This signal is used to shut off the ORing MOSFET. R_{RV} along with a 99µA current source pre-bias RVSNP to below the real source voltage of the MOSFET and effectively set the reverse voltage threshold. C_{RV} along with R_{RV} filters transients across the drain to source of the ORing FET.

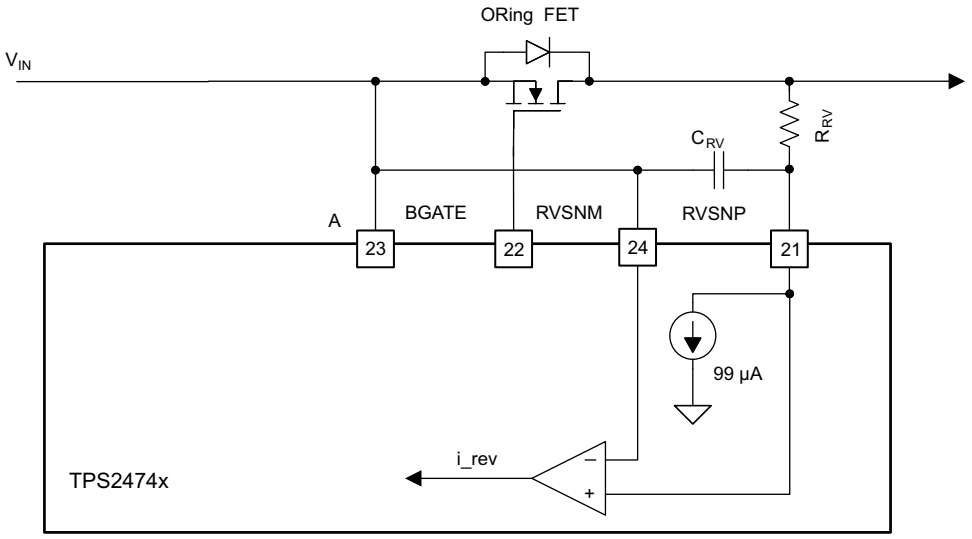


Figure 24. Programming and Sensing Reverse Voltage

Note that the RVSNM and RVSNP can be connected at various places. One option is to connect it across the drain to source of the ORing FET (Figure 24), which would result in a reverse current threshold of V_{RV}/R_{DSON}. Another option is to connect across the R_{SNS} as shown in Figure 25. This could be useful if a precise threshold is desired and R_{SNS} is larger than the R_{DSON} of the ORing FET.

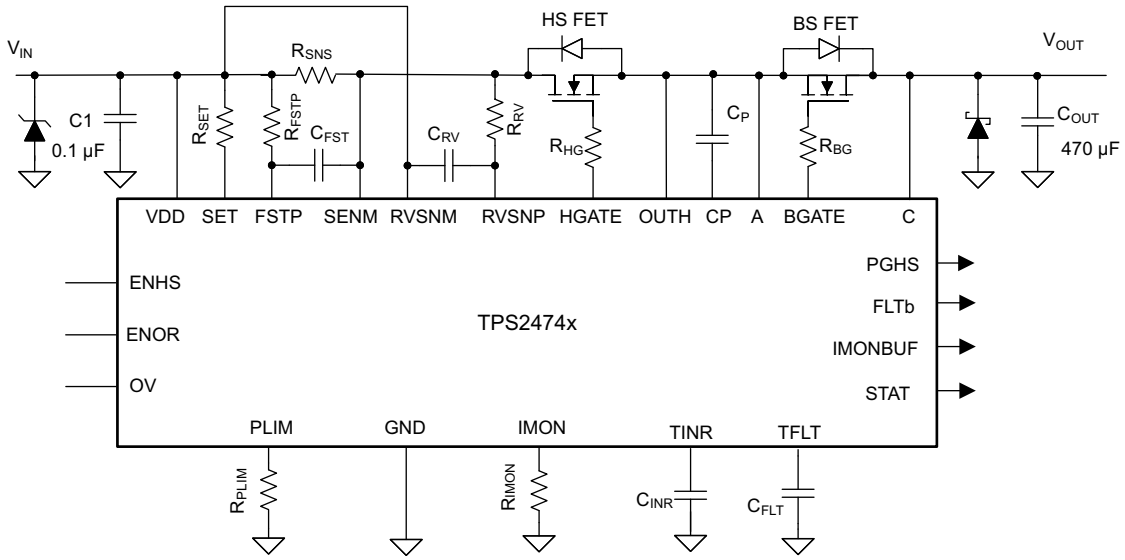


Figure 25. Sensing Reverse Voltage Across Hot Swap Sense Resistor

Feature Description (continued)

9.3.9 Analog Current Monitor

The TPS2474x also features two analog current monitoring outputs: IMON and IMONBUF. Each has their own advantages and disadvantages. The IMON is more accurate, because it doesn't have the error added from the second stage. However it is a high impedance output and leakage current on that node would result in monitoring error. In addition it can only support 30pF of capacitance and its full scale range is 675mV (this is where current limit kicks in). The IMONBUF takes the IMON signal and buffers it 3x. This introduces more error, but the output is low impedance, has a larger full scale range, and can drive up to 100pF of capacitance.

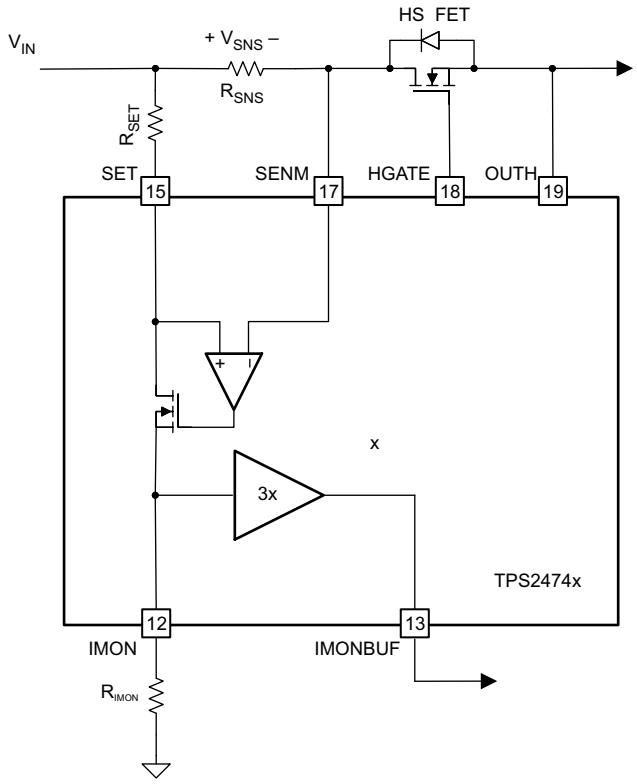


Figure 26. Current Monitoring Circuitry

9.3.10 Power Good Flag

The TPS2474x has a power good flag, which should be used to turn on downstream DC/DC converters. This reduces the stress on the Hot Swap MOSFET during start-up. The PGHS pin of the TPS2474x is asserted (with 1 ms deglitch) when both:

- Hot Swap is enabled and
- VDS of Hot Swap MOSFET is below 240 mV.

PGHS is de-asserted (with 8 ms deglitch) when either:

- Hot Swap is disabled.
- VDS of Hot Swap MOSFET is above 310 mV
- In an overcurrent condition that causes the timer to time out and latch off.

9.3.11 ORing MOSFET Status Indicator

The TPS2474x, features a STAT flag that indicates whether the BGATE (ORing FET driver) is ON or OFF. In general it is good practice to have the ORing FETs ON before drawing any significant load to prevent the ORing FET from overheating.

Feature Description (continued)

9.3.12 Fault Reporting

TPS 2474x will assert a fault by pulling down on the FLTb pin if any of the following occur:

- Hot Swap MOSFET Shorted Fault (ENHS = LO, but VIMON > 101 mV)
- Hot Swap timer times out.
- ORing MOSFET Open Fault (ENOR = HI, CP up, but V_{AC} > 410 mV)
- CP is down for more than 32 ms
- Over Temperature Shut Down (OTSD)

Figure 27 shows the logic for the fault conditions.

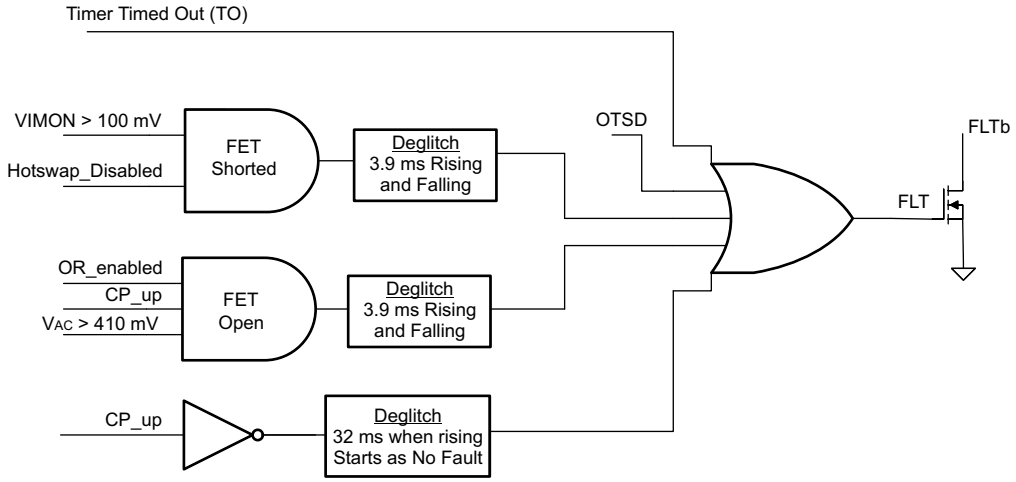


Figure 27. Logic for Fault Reporting

9.4 Device Functional Modes

The Hot Swap and ORing section of the TPS2474x are for the most part independent. The only exception is that the Hot Swap is gated by the charge pump being up. This ensures that the ORing FET is ON before the Hot Swap turns on to avoid a possible glitch from a fast ORing turn on.

9.4.1 ORing Functional Modes

Figure 28 shows the state machine for the ORing portion of the controller. It has three modes listed below:

- **Precharge CP:** Here the TPS2474x charges the CP node before beginning regular operation. This state is entered after POR/UVLO or if the CP voltage falls below 3.7V. Whenever the CP voltage is above 5.5V the FET OFF state is entered
- **FET OFF:** In this state the ORing FET is OFF and is pulled down to A with a 35mA current source. If a forward voltage drop is detected across the FET (V_{AC} > 10mV) the TPS2474x enters the FET ON state. There is a 30mA fast pull up that lasts 20µs, followed by a sustained 0.3 mA pull up.
- **FET ON:** In this state the ORing FET is pulled up to the CP voltage. If reverse current is detected (RVSNP > RVSNM) the TPS2474x will enter the OFF state. There is a 0.9A pull down current that lasts 15 µs, followed by a sustained 35mA pull down.

Device Functional Modes (continued)

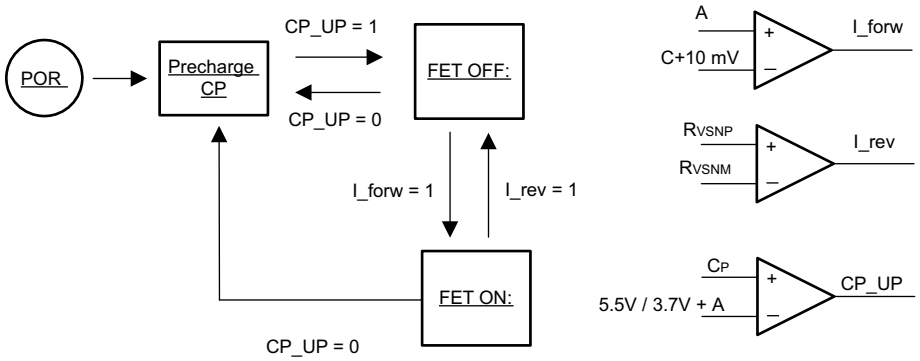


Figure 28. ORing State Machine

9.4.2 Hot Swap Functional Modes

The state machine for the Hot Swap section is shown in Figure 29. After a POR / UVLO event the Hot Swap waits 1.9ms after the charge pump is up before starting up. Once operational the Hot Swap has the following functional modes:

- **Inrush Mode (INR):** In this state the Hot Swap controller is actively regulating the HGATE to meet the current limit and power limit settings. The inrush timer is running if the controller is in power or current limiting. If the inrush timer times out the gate will be pulled down. The TPS24740 and TPS24742 will go to latched mode and TPS24741 will go into retry mode.
- **Regular Operation Mode (REG):** In this mode everything is operating properly so both the timers are discharged and the HGATE is high. If there is an overcurrent condition (V_{SNS} > $V_{SNS,CL}$), the device will go into fault mode. If there is a fast trip condition (V_{SNS} > V_{FSTP}), the gate will be pulled down with a 1A / 63 µs pulse. The TPS24742 will go to the latched state and the TPS24740 and TPS24741 will go back to inrush for a retry.
- **Fault Mode (FLT):** In this mode the TPS2474x runs the fault timer. Once the timer expires the TPS24740 and TPS24742 will go to latch mode while TPS24741 will go to retry mode. If the overcurrent condition is removed the controller will go back to the regular operation mode.
- **Latched Mode (Latched):** In the latched mode the HGATE is low, the timer is being discharged, and the FLTb is asserted. If there is a rising edge on ENHS the part will discharge the timers and go to the inrush mode.
- **Retry Mode (Retry):** Here the part charges and discharges the inrush timer 64 times before attempting another retry.

Device Functional Modes (continued)

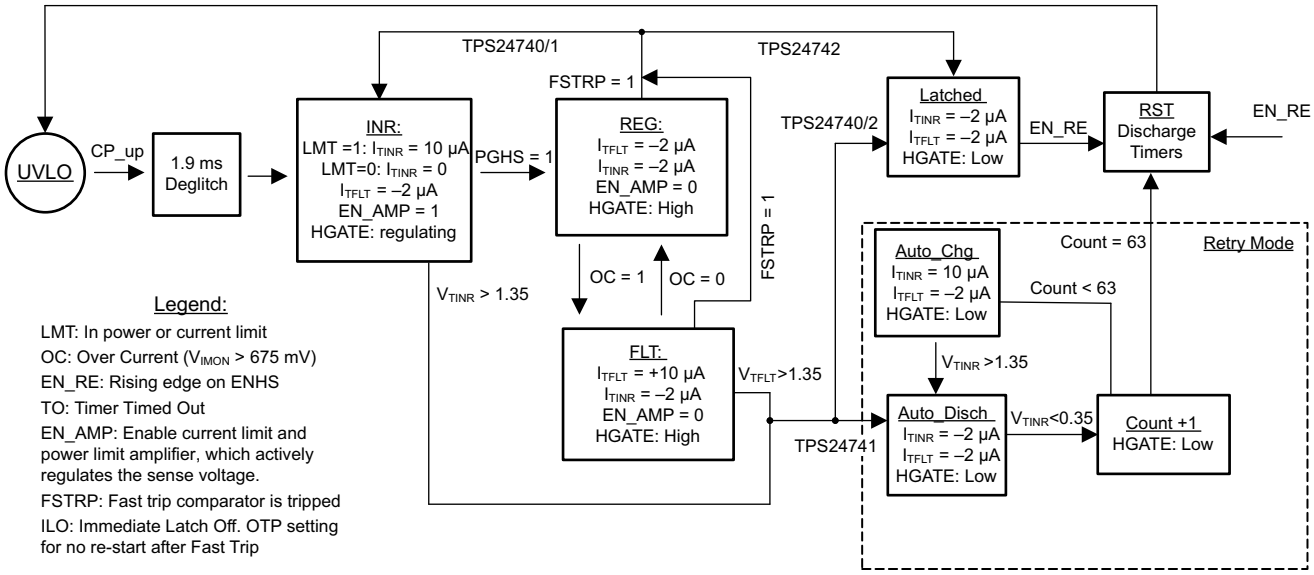


Figure 29. Hot Swap State Machine

10 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

10.1 Application Information

The TPS2474x controls an ORing MOSFET and a Hot Swap MOSFET to provide complete protection in redundant systems. The two sections are mostly independent and the Hot Swap and ORing settings can be chosen independently. In addition the TPS2474x supports various system level configurations shown in System Examples. Since the ORing and Hot Swap control are independent the design procedure shown in the Typical Application section can be used for these different configurations as well. Note that the component selection can often be iterative; and, it is recommended to use the publically available excel calculators to crunch the numbers. See Tools & Software link on the Product folder.

10.2 Typical Application

Two application examples are provided. The first one is an OR then Hot Swap 30A design with a current monitoring requirement, which uses the TPS24740. The second design is a Hot Swap then ORing 40A design with a transient load requirement and a large output capacitor that uses the TPS24742. Note that there are a lot of calculations necessary for these designs and it is easy to make mistakes. For this reason it is recommended to use TI design calculators, which follow a very similar procedure. See Tools & Software link on the Product folder. These written examples should be used as reference to better understand the calculations implemented in the design calculators.

10.2.1 30A Single channel OR then Hot Swap With Current Monitoring

Figure 30 shows the application schematic for a single channel OR then Hot Swap configuration.

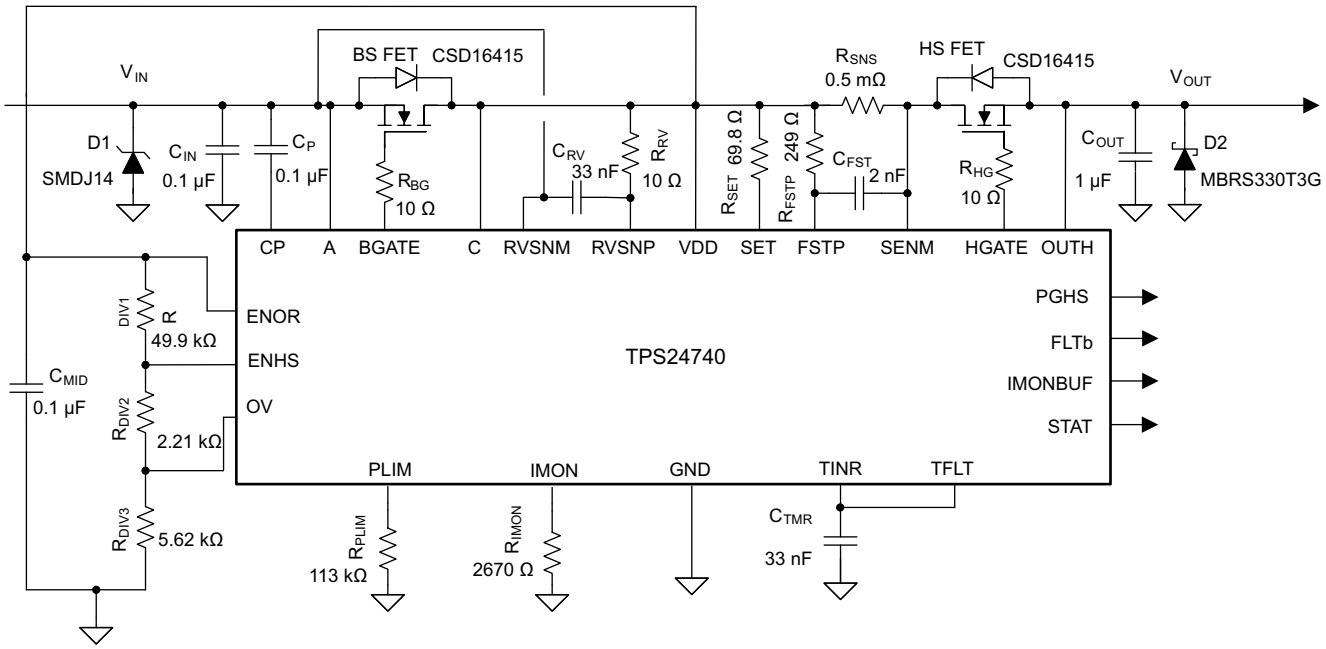


Figure 30. Application Schematic for ORing then Hot Swap

Typical Application (continued)

10.2.2 Design Requirements

Table 2 summarizes the design parameters that must be known before designing a Hot Swap circuit. When charging the output capacitor through the Hot Swap MOSFET, the FET's total energy dissipation equals the total energy stored in the output capacitor ($1/2CV^2$). Thus both the input voltage and output capacitance determines the stress experienced by the MOSFET. The maximum load current drives the current limit and sense resistor selection. In addition, the maximum load current, maximum ambient temperature, and the thermal properties of the PCB ($R_{\theta CA}$) drives the selection of the MOSFET R_{DSON} and the number of MOSFETs used. $R_{\theta CA}$ is a strong function of the layout and the amount of copper that is connected to the drain of the MOSFET. Air cooling also reduces $R_{\theta CA}$. It is also important to know if there are any transient load requirements. Finally, whether current monitoring is needed and its accuracy requirement drives the selection of R_{SNS}, R_{IMON}, and R_{SET}.

Table 2. Design Requirements for 30A ORing then Hot Swap

DESIGN PARAMETER	EXAMPLE VALUE
Input voltage range	11 V – 13 V
Maximum DC load current	30A
Maximum Output Capacitance of the Hot Swap	1500 µF
Maximum Ambient Temperature	55°C
Minimum Ambient Temperature	0°C
MOSFET $R_{\theta CA}$ (function of layout)	30°C/W
Transient load requirement	No
Pass "Hot-Short" on Output?	Yes
Pass a "Start into short"?	Yes
Is the load off until PG asserted?	Yes
Current Monitoring Required (accuracy?)	Yes (<2.5% full scale)
IC used	TPS24740

10.2.3 Detailed Design Procedure

10.2.3.1 Select R_{SNS} and $V_{SNS,CL}$ Setting

TPS2474x has a programmable $V_{SNS,CL}$ with a recommended range of 10 mV to 67.5 mV. It can be used with a $V_{SNS,CL}$ up to 200 mV, but that requires a resistor (R_{STBL}) between SET and SENM to ensure stability of an internal loop. R_{STBL} should be set larger than R_{IMON} x R_{SET} / (10xR_{SET}- R_{IMON}). This is shown in Figure 31.

For the majority of applications 25mV (R_{STBL} is not needed) is a good starting target for $V_{SNS,CL}$. Targeting a current limit of 35A to allow margin for the load, the sense resistor can be calculated as follows

$$R_{SNS,CLC} = \frac{V_{SNS,TGT}}{I_{LIM}} = \frac{25\ mV}{35\ A} = 0.71\ m\Omega \quad (10)$$

Since 0.71 mΩ resistors aren't available, the closest standard resistor should be chosen. To have better efficiency, a 0.5 mΩ resistor is chosen. Next the $V_{SNS,CL}$ should be computed based on the actual R_{SNS} and then used to compute R_{SET} and R_{IMON}. R_{SET} is chosen to target 250 µA of current through SET and IMON pins during current limit.

$$V_{SNS,CL} = I_{LIM} \times V_{SNS,CL} = 35\ A \times 0.5\ m\Omega = 17.5\ mV \quad (11)$$

$$R_{SET,CLC} = \frac{V_{SNS,CL}}{250\ \mu A} = 70\ \Omega \quad (12)$$

Choose R_{SET} to equal 69.8Ω, which is the closest available standard resistor. Next obtain the calculated R_{IMON} ($R_{IMON,CLC}$) as follows:

$$R_{IMON,CLC} = \frac{R_{SET} \times 675\ mV}{V_{SNS,CL}} = \frac{69.8\ \Omega \times 675\ mV}{17.5\ mV} = 2.692\ k\Omega \quad (13)$$

Choose 2.67kΩ resistor for R_{IMON}, which is the closest available standard resistor. Since precision current monitoring is desired, 0.1% resistors were used for R_{IMON} and for R_{SET} and a 4 terminal sense resistor (WSL4026L5000) was used for R_{SNS}.

$$I_{LIM,CL} = \frac{0.675\ V \times R_{SET}}{R_{IMON} \times R_{SNS}} = \frac{0.675\ V \times 69.8\ \Omega}{2.67\ k\Omega \times 0.5\ m\Omega} = 35.3\ A \quad (14)$$

$$V_{IMON,GAIN} = \frac{R_{IMON} \times R_{SNS}}{R_{SET}} = \frac{0.5\ m\Omega \times 2.67\ k\Omega}{69.8} = 19.13\ mV / A \quad (15)$$

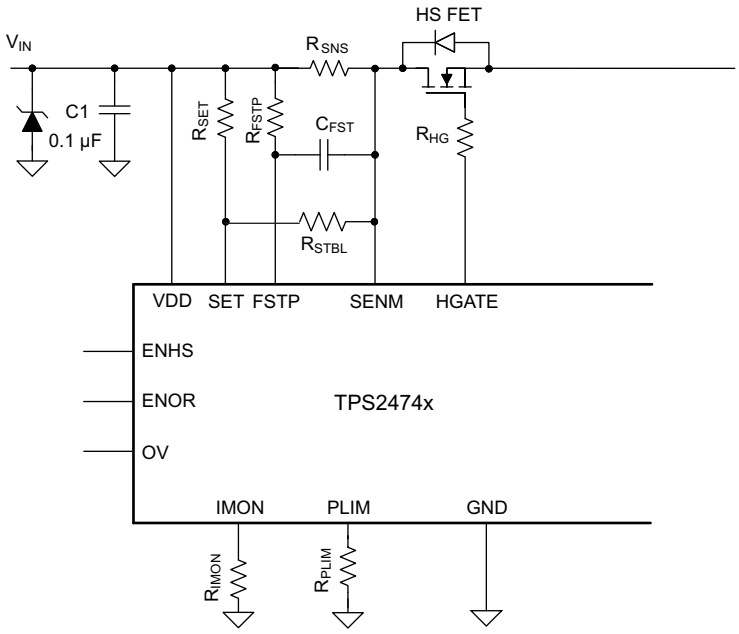


Figure 31. Adding R_{STBL} for $V_{SNS,CL}$ > 67.5mV

10.2.3.2 Selecting the Fast Trip Threshold and Filtering

The TPS2474x allows the user to program the fast trip threshold. When this threshold is exceeded the gate is quickly pulled down. C_{FSTP} can be added to include some filtering into the comparator. The selection of the fast trip threshold and filtering is influenced by the systems environment and requirements. In general picking a larger threshold and larger filtering time will result in more immunity to nuisance trips, but also a slower response (possibly inadequate) to real fault conditions. It's best to fine tune these threshold after testing the real system. As a starting point it is recommended to set the fast trip threshold at least 1.25x larger than then current limit. For this design example a 50A fast trip threshold along with a 500ns filtering time constant were targeted. The value for R_{FSTP} and C_{FSTP} can be computed as shown below:

$$R_{FSTP} = \frac{I_{FSTP} \times R_{SNS}}{100\ \mu A} = \frac{50\ A \times 0.5\ m\Omega}{100\ \mu A} = 250\ \Omega \quad (16)$$

$$C_{FSTP} = \frac{t_{FSTP}}{R_{FSTP}} = \frac{500\ ns}{250\ \Omega} = 2\ nF \quad (17)$$

The next closest standard resistor and capacitor values should be chosen. In this case R_{FSTP} = 249Ω and C_{FSTP}=2nF.

10.2.3.3 Selecting the Hot Swap FET(s)

It is critical to select the correct MOSFET for a Hot Swap design. The device must meet the following requirements:

- The V_{DS} rating should be sufficient to handle the maximum system voltage along with any ringing caused by transients. For most 12V systems a 25 V or 30V FET is a good choice.
- The SOA of the FET should be sufficient to handle all usage cases: start-up, hot-short, start into short.
- R_{DSON} should be sufficiently low to maintain the junction and case temperature below the maximum rating of the FET. In fact, it is recommended to keep the steady state FET temperature below 125°C to allow margin to handle transients.
- Maximum continuous current rating should be above the maximum load current and the pulsed drain current must be greater than the current threshold of the circuit breaker. Most MOSFETs that pass the first three requirements will also pass these two.
- A V_{GS} rating of +16 V is required, because the TPS2474x can pull up the gate as high as 15.5 V above source.

For this design the CSD16415Q was selected for its low R_{DSON} and superior SOA. After selecting the MOSFET, the maximum steady state case temperature can be computed as follows:

$$T_{C,MAX} = T_{A,MAX} + R_{\theta CA} \times I^2_{LOAD,MAX} \times R_{DSON}(T_J) \tag{18}$$

Note that the R_{DSON} is a strong function of junction temperature, which for most MOSFETS will be very close to the case temperature. A few iterations of the above equations may be necessary to converge on the final R_{DSON} and $T_{C,MAX}$ value. According to the CSD16415Q datasheet, its R_{DSON} is about 1.3x greater at 100°C compared to room temperature. The equation below uses this R_{DSON} value to compute the $T_{C,MAX}$. Note that the computed $T_{C,MAX}$ is close to the junction temperature assumed for R_{DSON}. Thus no further iterations are necessary.

$$T_{C,MAX} = 55°C + 30° \frac{C}{W} \times (30A)^2 \times (1.3 \times 1\,m\Omega) = 90.1°C \tag{19}$$

10.2.3.4 Select Power Limit

In general, a lower power limit setting is preferred to reduce the stress on the MOSFET. However, at low power limit levels both the V_{SNS} and V_{IMON} become very low, which results in more error caused by offsets. It is recommended to keep V_{SNS} above 1.5mV and V_{IMON} above 27mV to ensure reasonable accuracy of the power limit engine. Based on these requirements the minimum power limit can be computed as seen in Equation 20.

$$P_{LIM,MIN} = \frac{V_{IN,MAX}}{R_{SNS}} \times MIN\left(V_{SNS,MIN}, \frac{V_{IMON,MIN} \times R_{SET}}{R_{IMON}}\right)$$
$$= \frac{13\ V}{0.5\ m\Omega} \times MIN\left(1.5\ mV, \frac{27\ mV \times 69.8\ \Omega}{2.67\ k\Omega}\right) = 39\ W \tag{20}$$

In most applications the power limit can be set to $P_{LIM,MIN}$ using Equation 21. Here R_{SNS} and R_{PWR} are in Ωs and P_{LIM} is in Watts.

$$R_{PLIM} = \frac{84375 \times R_{SET}}{R_{SNS} \times R_{IMON} \times P_{LIM}} = \frac{84375 \times 69.8\ \Omega}{0.5\ m\Omega \times 2.67\ k\Omega \times 39} = 113.1\ k\Omega \tag{21}$$

The closest available resistor should be selected. In this case it is a 113 kΩ.

10.2.3.5 Set Fault Timer

The inrush timer runs when the Hot Swap is in power limit or current limit, which is the case during start-up. Thus the timer has to be sized large enough to prevent a time-out during start-up. If the part starts directly into current limit ($I_{LIM} \times V_{IN} < P_{LIM}$) the maximum start time can be computed with Equation 22:

$$t_{start,max} = \frac{C_{OUT} \times V_{IN,MAX}}{I_{LIM}} \tag{22}$$

For most designs (including this example) $I_{LIM} \times V_{IN} > P_{LIM}$ so the Hot Swap will start in power limit and transition into current limit. In that case the maximum start time can be computed as seen in Equation 23:

$$t_{start,max} = \frac{C_{OUT}}{2} \times \left[\frac{V^2_{IN,MAX}}{P_{LIM}} + \frac{P_{LIM}}{I^2_{LIM}}\right] = \frac{1500\ \mu F}{2} \times \left[\frac{(13\ V)^2}{39\ W} + \frac{39\ W}{(35\ A)^2}\right] = 3.27ms \tag{23}$$

Note that the above start-time is based on typical current limit and power limit values. To ensure that the timer never times out during start-up it is recommended to set the fault time (TINR) to be 1.5x $t_{start,max}$ or 4.9 ms. This will account for the variation in power limit, timer current, and timer capacitance.

Next the design should decide if having equal TINR and TFLT is acceptable. If there is no transient load requirement this is usually fine. For this example the same capacitor is connected to both TINR and TFLT to save on BOM cost. In this case the time out (T_{TMR}) should be set based on the TINR requirements. When these pins are connected the C_{TMR} can be computed as follows:

$$C_{TMR} = 6.11\ \mu F \times T_{TMR} = 6.11\ \mu F \times 4.9\ ms = 29.9\ nF \quad (24)$$

The next largest available C_{TMR} is chosen as 33nF. Once the C_{TMR} is chosen the actual programmed time out can be computed as seen in Equation 25.

$$T_{TMR} = \frac{C_{TMR}}{6.11\ \mu F} = \frac{33\ nF}{6.11\ \mu F} = 5.4\ ms \quad (25)$$

10.2.3.6 Check MOSFET SOA

Once the power limit and fault timer are chosen, it is critical to check that the FET remains within its SOA during all test conditions. For this design example the TPS24740 is used, which retries once during a hot-short.

During a “Hot-Short” the circuit breaker trips and the TPS24740 re-starts into power limit until the timer runs out. In the worst case the MOSFET’s V_{DS} will equal $V_{IN,MAX}$, I_{DS} will equal P_{LIM} / $V_{IN,MAX}$ and the stress event will last for T_{TMR}. For this design example the MOSFET will have 13 V, 3 A across it for 5.6 ms.

Based on the SOA of the CSD16415Q, it can handle 13 V, 100 A for 1 ms and it can handle 13 V, 15 A for 10 ms. The SOA for 5.6 ms can be extrapolated by approximating SOA vs time as a power function as shown in Equation 26:

$$I_{SOA}(t) = a \times t^m$$

$$m = \frac{\ln\left(I_{SOA}(t_1) / I_{SOA}(t_2)\right)}{\ln(t_1 / t_2)} = \frac{\ln\left(\frac{100\ A}{15\ A}\right)}{\ln\left(\frac{1\ ms}{10\ ms}\right)} = -0.82$$

$$a = \frac{I_{SOA}(t_1)}{t_1^m} = \frac{100\ A}{(1\ ms)^{-0.82}} = 100\ A \times (ms)^{0.82}$$

$$I_{SOA}(5.4\ ms) = 100\ A \times (ms)^{0.82} \times (5.4\ ms)^{-0.82} = 25.1\ A \quad (26)$$

Note that the SOA of a MOSFET is specified at a case temperature of 25°C, while the case temperature can be much hotter during a hot-short. The SOA should be de-rated based on $T_{C,MAX}$ using Equation 27:

$$I_{SOA}(5.4\ ms, T_{C,MAX}) = I_{SOA}(5.4\ ms, 25°C) \times \frac{T_{J,ABSMAX} - T_{C,MAX}}{T_{J,ABSMAX} - 25°C} = 25.1\ A \times \frac{150°C - 90.1°C}{150°C - 25°C} = 12\ A \quad (27)$$

Based on this calculation the MOSFET can handle 11.67 A, 13 V for 5.6 ms at elevated case temperature, but is only required to handle 3A (39 W / 13 V) during a hot-short. Thus there is good margin and this will be a robust design. In general, it is recommended that the MOSFET can handle 1.3x more than what is required during a hot-short. This provides margin to cover the variance of the power limit and fault time.

10.2.3.7 Choose ORing MOSFET

When selecting the ORing MOSFET the considerations are similar to the Hot Swap MOSFET, but the SOA is no longer critical. In addition the lower R_{DSON} is not always ideal, because that would result in a larger reverse current for the same reverse voltage threshold. Of course a lower R_{DSON} would provide better efficiency. For consistency sake a single CSD16415Q FET was used for the ORing section as well. It is important to check its steady state temperature at max load using the same equation that was used for the Hot Swap.

$$T_{C,MAX} = 55°C + 30° \frac{C}{W} \times (30A)^2 \times (1.3 \times 1\ m\Omega) = 90.1°C \quad (28)$$

10.2.3.8 Choose Reverse Current Threshold and Filtering

When setting the reverse current threshold, it is often desired to set a very low value to minimize the maximum DC reverse current. However, the accuracy of the reverse voltage threshold should be considered. The TPS2474x has a 1mV offset on the reverse voltage comparator. Thus setting a very low reverse voltage setting can result in some boards to trip at positive current. This would lead to oscillations at zero load condition as the ORing gate turns ON and OFF, which is typically not desired. Note that applications that always have a significant forward current will not experience this problem.

For this design example a reverse voltage of 1.5mV was targeted to keep the threshold low, but to also ensure that the device never trips at positive current. Just like the filtering on the fast trip threshold for the Hot Swap, the optimum time constant for filtering the reverse voltage threshold will depend on the system environment and requirements. Again, this is a trade-off between avoiding nuisance trips and a fast response to actual faults. In general a 500ns time constant is a good starting point. Based on these target thresholds, R_{RV} and C_{RV} can be computed using Equation 29 and Equation 30.

$$R_{RV} = \frac{V_{RV}}{99\ \mu A} = \frac{1.5\ mV}{99\ \mu A} = 15.2\ \Omega \tag{29}$$

$$C_{RV} = \frac{t_{RV}}{R_{RV}} = \frac{500\ ns}{15.2\ \Omega} = 32.9\ nF \tag{30}$$

Choose closest available standards values: R_{RV} = 15Ω and C_{RV} = 33nF.

10.2.3.9 Choose Under Voltage and Over Voltage Settings

The TPS2474x has comparators with 1.35V threshold on the ENHS, ENOR, and OV pins. A resistor divider can be used to set Undervoltage and Overvoltage thresholds for the bus. For this design example 10V and 14V were chosen as the limits to allow some margin for the 11V to 13V input bus. Once these limits are known, R_{DIV2} and R_{DIV3} can be computed using Equation 31, Equation 32, and Equation 33. R_{DIV1} was set to 49.9 kΩ, which keeps the power consumption reasonably low without being too susceptible to leakage currents.

$$R_{DIV2,3} = R_{DIV2} + R_{DIV3} = \frac{R_{DIV1} \times 1.35\ V}{V_{UV} - 1.35\ V} = \frac{49.9\ k\Omega \times 1.35\ V}{10\ V - 1.35\ V} = 7.79\ k\Omega \tag{31}$$

$$R_{DIV3} = \frac{\left(R_{DIV1} + R_{DIV2,3}\right) \times 1.35\ V}{V_{OV}} = \frac{\left(49.9\ k\Omega + 7.79\ k\Omega\right) \times 1.35\ V}{14\ V} = 5.56\ k\Omega \tag{32}$$

$$R_{DIV2} = R_{DIV2,3} - R_{DIV1} = 7.79\ k\Omega - 5.56\ k\Omega = 2.23\ k\Omega \tag{33}$$

Choose closest available standard 1% resistors: R_{DIV2} = 2.21 kΩ and R_{DIV3} = 5.62 kΩ. The actual Under Voltage and Over Voltage settings can be computed for the chosen resistors as shown in Equation 34 and Equation 35:

$$V_{UV\_act} = 1.35V \times \frac{R_{DIV1} + R_{DIV2} + R_{DIV3}}{R_{DIV2} + R_{DIV3}} = 1.35\ V \times \frac{2.21\ k\Omega + 5.62\ k\Omega + 49.9\ k\Omega}{2.21\ k\Omega + 5.62\ k\Omega} = 9.95\ V \tag{34}$$

$$V_{OV\_act} = 1.35\ V \times \frac{R_{DIV1} + R_{DIV2} + R_{DIV3}}{R_{DIV3}} = 1.35\ V \times \frac{2.21\ k\Omega + 5.62\ k\Omega + 49.9\ k\Omega}{5.62\ k\Omega} = 13.87\ V \tag{35}$$

10.2.3.10 Selecting C_{IN}, C_{OUT}, and C_{MIDDLE}

It is recommended to add ceramic bypass capacitors to help stabilize the voltages on the input, output, and the intermediate node. Since C_{IN} and C_{MIDDLE} will be charged directly on hot-plug, their value should be kept small. 0.1µF is a good target. Since C_{OUT} doesn't get charged during hot-plug, a larger value such as 1 µF could be used.

10.2.3.11 Selecting D1 and D2

During hot plug and hot short events there could be significant transients on the input and output of the hotswap that could cause operation outside of the IC specifications. To ensure reliable operation a TVS on the input and a Schottky diode on the output are recommended. In this example a SMDJ14A and MBRS330T3G are used.

10.2.3.12 Ensuring Stability

For most applications, the TPS2474x is stable whithout any additional components. However in some cases additional $C_{GS,EXT}$ is required as shown in Figure 32 to help stabilize the current and power limit loop. Typically this is for low current limits and low sense voltages. It is easy to check whether these extra components are needed using the equations below. Note that the transconductance (also referred to as g_m and g_{fs}) of the FET will vary based on the current and thus g_m' is used in the equations as a normalizing parameter. The CSD16415 has a gm of 168 siemens at 40A of I_{DS}, resulting in g_m' of 26.56. For this example, $C_{GS,MIN}$ was computed to be 0.9nF, while the C_{ISS} of the CSD16415 is 3.15nF providing plenty of margin for the design. In general it is recommended to have a 2x margin from the typical C_{ISS} and $C_{GS,MIN}$ to account for any variation that the FET would have. If the C_{ISS} of the MOSFET isn't large enough an external RC should be added as shown in the figure below. Note that if parallel FETs are used $C_{GS,MIN}$ (per FET) is reduced by square root of two or by 1.41.

$$C_{GS,MIN} = 6.54 \times 10^{-12} \times gm' \times \left(\frac{R_{IMON}}{R_{SET}}\right)^{1.5} \times \sqrt{R_{SNS}} \tag{36}$$

$$g_m' = \frac{g_m(I_{DS})}{\sqrt{I_{DS}}} = \frac{168}{\sqrt{40}} = 26.56 \tag{37}$$

$$C_{GS,MIN} = 6.54 \times 10^{-12} \times 26.56 \times \left(\frac{2.67k}{69.8}\right)^{1.5} \times \sqrt{0.5m} = 0.9nF \tag{38}$$

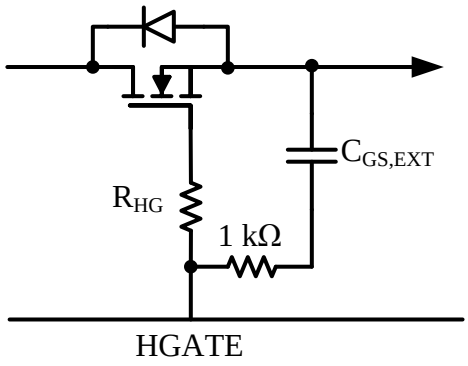


Figure 32. Ensuring Stability

10.2.3.13 Compute Tolerances

After finishing a design it is often desired to know the variations of each setting. Often times there are multiple error sources and there are two common ways to analyze the circuit. One is worst case, which adds all of the error sources. The other one is root mean square (RMS), which is less conservative. When error sources are independent using the RMS method provides a more statistically accurate view of the tolerances. This method is used in this section. Note that the error calculations are quite long and tedious and it is recommended to use TI's excel tools, which support both worst case and RMS analysis. For this example the tolerances in Table 3 are assumed. See Tools & Software link on the Product folder.

Table 3. Component Tolerances

COMPONENTS	TOLERANCE
R_{IMON} and R_{SET}	0.1%
R_{SNS}	1%
R_{DIV1}, R_{DIV2}, R_{DIV3}, R_{PLIM}, R_{FST},	1%
C_{TMR}	10%

First, the tolerance of the current monitoring and current limit is computed.

There are 5 error sourcing contributing to the current monitoring accuracy on the IMON pin: tolerance of R_{SET} (ER_{SET}), tolerance of R_{IMON} (ER_{IMON}), tolerance of R_{SNS} (ER_{SNS}), the IC gain error (ER_{GAIN}), and the IC offset error (ER_{OS}). All of these errors are in % with the exception of the offset error. To get a percent error due to the offset error ($ER_{OS\%}$) simply divide the offset by the sense voltage. For the TPS2474x, ER_{GAIN} is 0.4%, and ER_{OS} is 150 µV.

Based on these values the full scale ($I_{FS,ERR,IMON}$) and 20% of full scale ($I_{20FS,ERR,IMON}$) current monitoring accuracy at the Imon pin can be computed with Equation 39 and Equation 40.

$$I_{FS,ERR,IMON} = \sqrt{(ER_{SET})^2 + (ER_{SNS})^2 + (ER_{IMON})^2 + (ER_{GAIN})^2 + \left(\frac{ER_{OS}}{R_{SNS} \times I_{LIM}}\right)^2}$$
$$= \sqrt{0.1\%^2 + 1\%^2 + 0.1\%^2 + 0.4\%^2 + (150\ \mu V / 17.7\ mV)^2} = 1.4\% \quad (39)$$

$$I_{20FS,ERR,IMON} = \sqrt{(ER_{SET})^2 + (ER_{SNS})^2 + (ER_{IMON})^2 + (ER_{GAIN})^2 + \left(\frac{ER_{OS}}{R_{SNS} \times 0.2 \times I_{LIM}}\right)^2} = 4.4\% \quad (40)$$

Note that the TPS24740 detects the current limit when the IMON pin exceeds 675 mV. Thus the current limit error $I_{LIM,ER}$ is a combination of the $I_{FS,ERR,IMON}$ and the current limit error at the IMON pin ($I_{LIM,ERR,IMON}$). The 675 mV threshold varies up to 15 mV so $I_{LIM,ERR,IMON}$ is 2.3% and the current limit error can be computed as seen in Equation 41:

$$I_{LIM,ERR} = \sqrt{(I_{FS,ERR,IMON})^2 + (I_{LIM,ERR,IMON})^2} = \sqrt{1.4\%^2 + 2.3\%^2} = 2.7\% \quad (41)$$

If the current is monitored at the IMONBUF pin, there is additional error introduced due to the internal buffer, which has a gain error of 0.66% ($ER_{OS,BUF}$) and an offset error of 3mV ($ER_{OS,BUF}$) referred to the IMON pin. Note that V_{IMON} equals 675 mV at full scale and 135 mV at 20% of full scale. Thus the total current monitoring error at the IMONBUF pin for full scale ($I_{FS,ERR,IMONBUF}$) and 20% of full scale ($I_{20FS,ERR,IMONBUF}$) can be found using Equation 42 and Equation 43 :

$$I_{FS,ERR,IMONBUF} = \sqrt{(I_{FS,ERR,IMON})^2 + (ER_{GAIN,BUF})^2 + \left(\frac{ER_{OS,BUF}}{675\ mV}\right)^2}$$
$$= \sqrt{1.4\%^2 + 0.66\%^2 + \left(\frac{3\ mV}{675\ mV}\right)^2} = 1.6\% \quad (42)$$

$$I_{20FS,ERR,IMONBUF} = \sqrt{(I_{20FS,ERR,IMON})^2 + (ER_{GAIN,BUF})^2 + \left(\frac{ER_{OS,BUF}}{135mV}\right)^2}$$
$$= \sqrt{4.4\%^2 + 0.66\%^2 + \left(\frac{3mV}{135mV}\right)^2} = 5.0\% \quad (43)$$

Next the power limit error is computed. This error is made up of three sources: the error from external components (ERR_{COMP}), the error when translating the sense voltage to IMON ($I_{PL,ERR,IMON}$), and the error of the power limit engine at IMON ($ERR_{IMON,PL}$). Both ERR_{SNS} and $ERR_{IMON,\ PL}$ are a function of the operating point of the power limit engine. Note that this error is greatest at largest V_{DS}, since $V_{SNS,PL}$ is smallest (refer to Figure 20). For this example V_{DS} is largest when V_{IN} = 13 V (maximum V_{IN}) and V_{OUT} = 0 V and thus the error is computed at this operating point. The sense voltage (V_{SNS}) and the voltage at the IMON pin (V_{IMON}) should be computed for this operating point using Equation 44 and Equation 45:

$$V_{SNS} = \frac{P_{LIM} \times R_{SNS}}{V_{DS}} = \frac{39\ W \times 0.5\ m\Omega}{13\ V} = 1.5\ mV \quad (44)$$

$$V_{IMON} = \frac{V_{SNS} \times R_{IMON}}{R_{SET}} = \frac{1.5\ mV \times 2670\ \Omega}{69.8\ \Omega} = 57.4\ mV \quad (45)$$

The $I_{PL,ERR,IMON}$ can be computed similarly to $I_{FS,ERR,IMON}$ using Equation 46.

$$I_{PL,ERR,IMON} = \sqrt{(ER_{GAIN})^2 + \left(\frac{ER_{OS}}{V_{SNS}}\right)^2} = \sqrt{(0.4\%)^2 + \left(\frac{150\ \mu V}{1.5\ mV}\right)^2} = 10\% \quad (46)$$

The tolerance of the power limit engine is specified at three V_{IMON} points in the datasheet: 135 mV (±20.3 mV), 67.5 mV (±10.1 mV), and 27 mV (±8.1 mV). To get the % error at the real operating point, the absolute error should be extrapolated and divided by V_{IMON} as shown in Equation 47. This is graphically depicted in Figure 33.

$$ERR_{IMON,PL} = \frac{8.1\ mV + (57.4\ mV - 27\ mV) \times \frac{10.1\ mV - 8.1\ mV}{67.5\ mV - 27\ mV}}{57.4\ mV} = 16.7\% \quad (47)$$

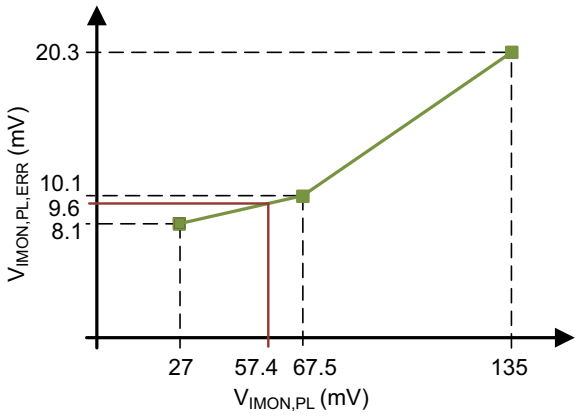


Figure 33. Extrapolating Power Limit Error

Once $ERR_{IMON,PL}$ and $I_{PL,ERR,IMON}$ are known the total power limit error ($PL_{ERR,TOT}$) can be computed using Equation 48. The component error comes from R_{SNS} (1%), R_{PLIM} (1%), R_{SET} (0.1%), and R_{IMON} (0.1%) resulting in a total component error of 1.4%.

$$PL_{ERR,TOT} = \sqrt{(ERR_{IMON,PL})^2 + (I_{PL,ERR,IMON})^2 + (ERR_{COMP})^2}$$
$$= \sqrt{(16.7\%)^2 + (10\%)^2 + (1.4\%)^2} = 19.5\% \quad (48)$$

After computing the fast trip voltage threshold to be 24.9 mV (100 µA × 249 Ω), the fast trip threshold error resulting from the IC ($FST_{ERR,\ IC}$) can be computed using a similar extrapolation method as used for power limit. The component error of R_{SNS} and R_{FST} should be added to obtain the total fast trip error ($FST_{ERR,TOT}$) shown in Equation 49 and Equation 50 below.

$$FST_{ERR,IC} = \frac{2\ mV + (24.9\ mV - 20\ mV) \times \frac{5\ mV - 2\ mV}{100\ mV - 20\ mV}}{24.9\ mV} = 8.8\% \quad (49)$$

$$FST_{ERR,TOT} = \sqrt{(8.8\%)^2 + (1\%)^2 + (1\%)^2} = 8.9\% \quad (50)$$

The IC error of the UV/OV threshold is always 3.7% (0.05 V/1.35 V). Assuming that all resistors have a 1% error the component error is 1.41% (2 resistors). When using the RMS method the total error is 4%. For the timer error, the IC contributes 22% and 10% comes from the component. When using the RMS method the total error becomes 24.1%.

Table 4 summarizes the final tolerances of the design:

Table 4. Design Tolerances

SETTINGS	ACCURACY
Current Limit	2.7%
Fast Trip	8.9%
Power Limit	19.5%
Timer	24.1%
UV/OV	4.0%
Current Monitoring at IMON (Full Scale)	1.4%
Current Monitoring at IMON (20% of Full Scale)	4.4%
Current Monitoring at IMONBUF (Full Scale)	1.6%
Current Monitoring at IMONBUF (20% of Full Scale)	5.0%

10.2.4 Application Curves

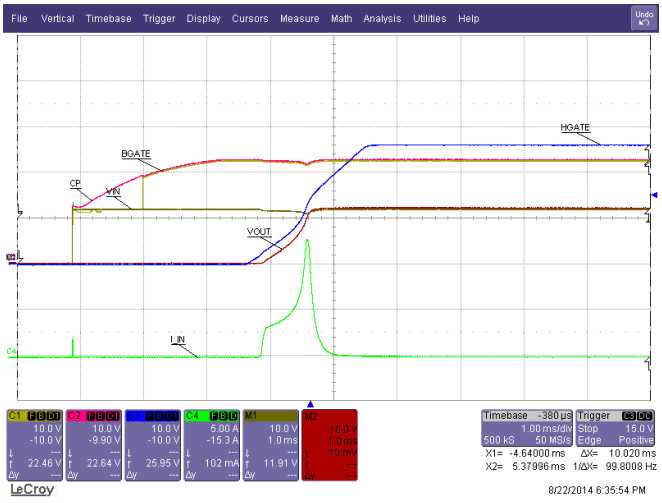


Figure 34. Start up (C_{OUT}= 440 µF)

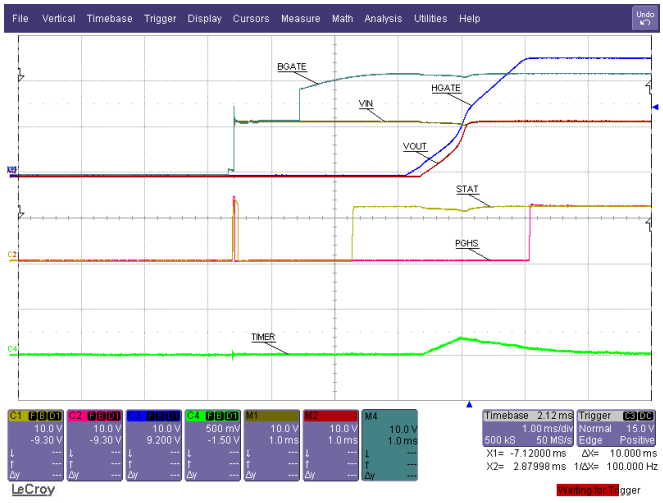


Figure 35. Start up (C_{OUT}= 440 µF)

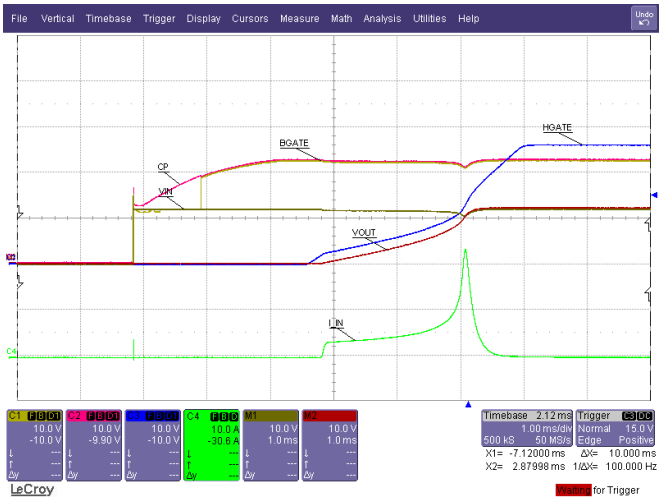


Figure 36. Start up (C_{OUT}=1500 µF)

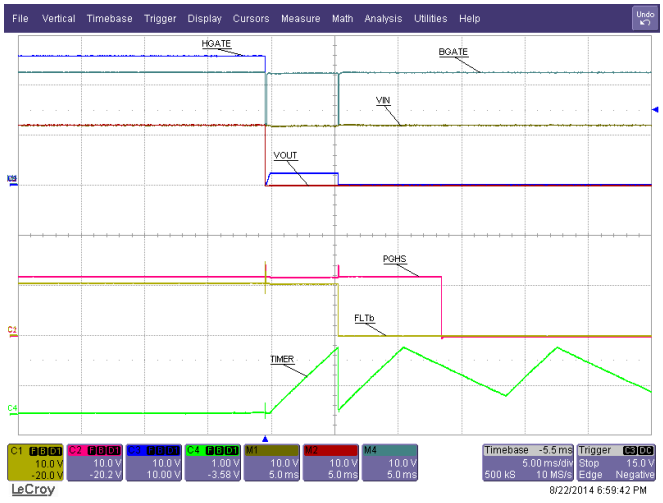


Figure 37. Hot Short on V_{OUT} (zoomed out)

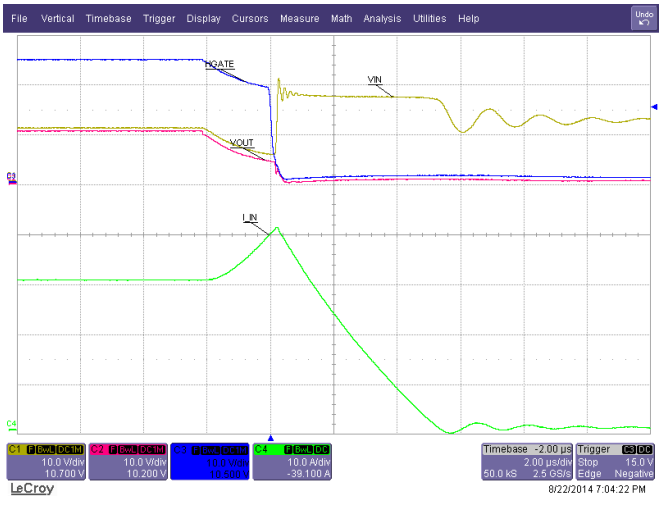


Figure 38. Hot Short on V_{OUT} (zoomed in)

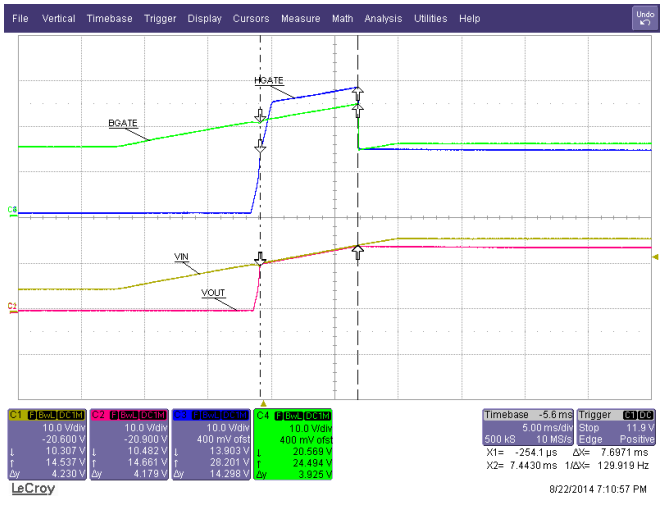


Figure 39. Under/Over Voltage with V_{IN} Rising

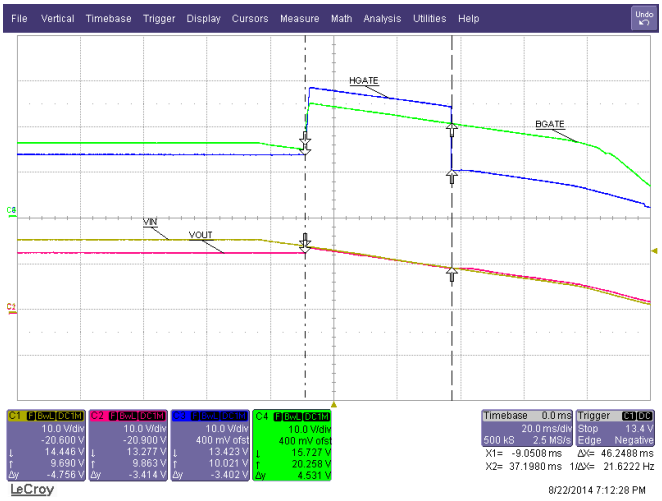


Figure 40. Under/Over Voltage with V_{IN} Falling

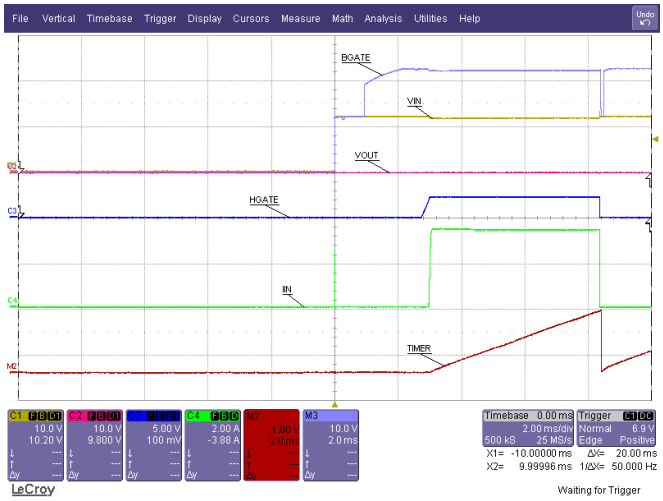


Figure 41. Start Up with V_{OUT} Shorted

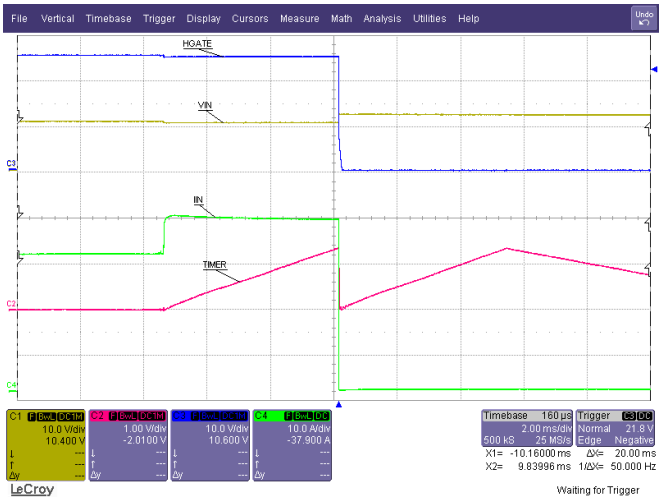


Figure 42. Load Step 32A to 40A

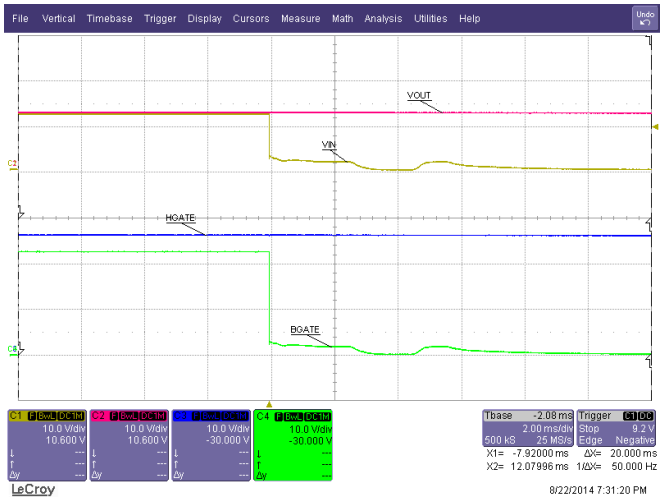


Figure 43. Hot – Short on V_{IN}

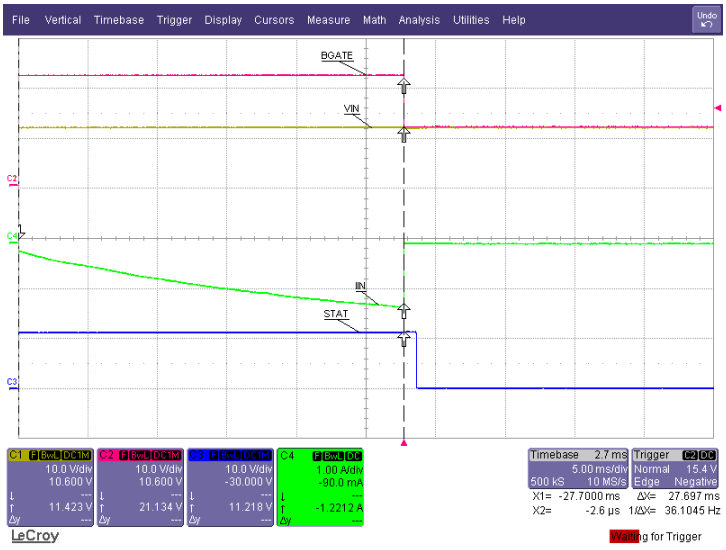


Figure 44. Gradual Reverse Current

10.2.5 40 A Single Channel Hot Swap then ORing

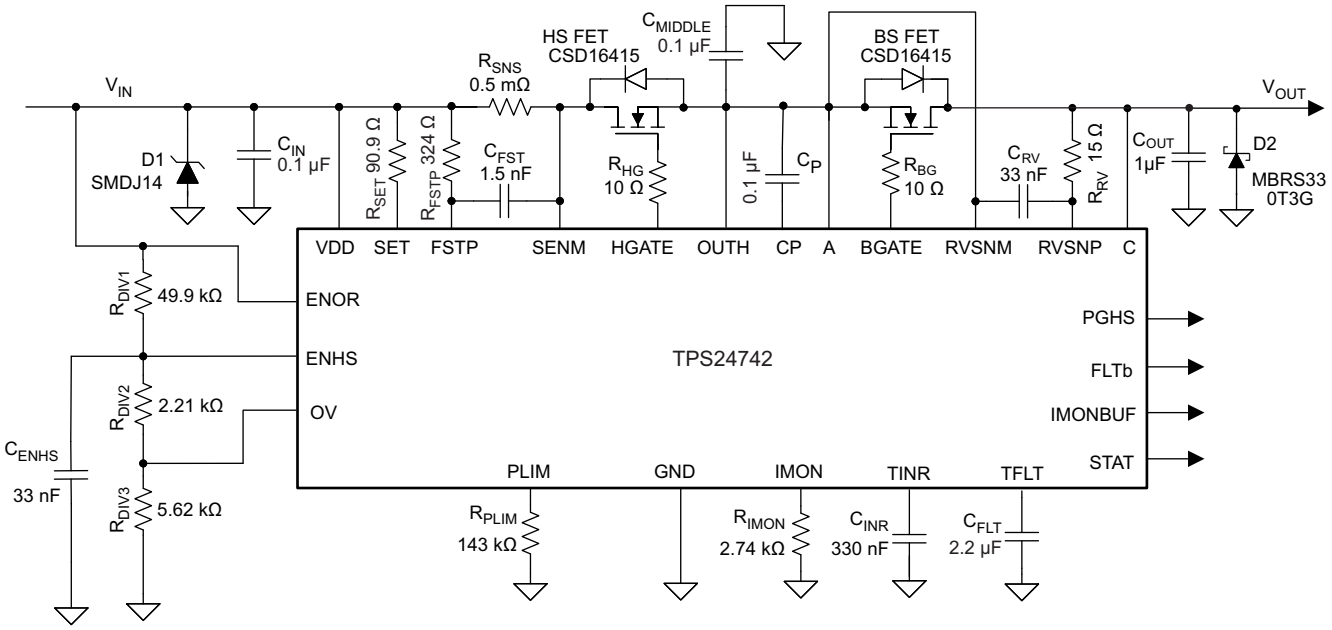


Figure 45. Application Schematic for Hot Swap then ORing

10.2.5.1 Design Requirements

This second design example is similar to the first one, but has a few key differences. First of all, the maximum output capacitance is much larger, and the maximum current is also larger, which puts more stress on the MOSFET. On the flip side, the TPS24742 IC is used, which results in less MOSFET stress during a hot-short event, because there is no restart. Finally, there is a requirement that the design should allow for 60A to pass through for 200 ms without shutting down. This requires the use of two timers. In addition, there is no requirement for accurate current monitoring and hence it's not necessary to use a 4 terminal sense resistor.

Table 5. Design Requirements for 40A ORing then Hot Swap

DESIGN PARAMETER	EXAMPLE VALUE
Input voltage range	11 V – 13 V
Maximum DC load current	40A
Maximum Output Capacitance of the Hot Swap	10,000 µF
Maximum Ambient Temperature	55°C
MOSFET $R_{\theta CA}$ (function of layout)	30°C/W
Transient load requirement	Yes, 60A for 200ms
Pass "Hot-Short" on Output?	Yes
Pass a "Start into short"?	Yes
Is the load off until PG asserted?	Yes
IC used	TPS24742
Current Monitoring Required	No
Can a hot board be unplugged and plugged back in?	No

10.2.5.2 Design Procedure

10.2.5.2.1 Select R_{SNS} and $V_{SNS,CL}$ Setting

Similarly to the previous design example, 25mV is used as a starting target for $V_{SNS,CL}$. Targeting a current limit of 45A to allow margin for the load, the sense resistor can be computed as follows:

$$R_{SNS,CLC} = \frac{V_{SNS,TGT}}{I_{LIM}} = \frac{25\ mV}{45\ A} = 0.55\ m\Omega \quad (51)$$

Since 0.55 mΩ resistors aren't available, the closest standard resistor should be chosen. To have better efficiency, a 0.5 mΩ resistor is chosen. Next the $V_{SNS,CL}$ should be computed based on the actual R_{SNS} and then used to compute R_{SET} and R_{IMON}. R_{SET} is chosen to target 250 µA of current through SET and IMON pins during current limit.

$$V_{SNS,CL} = I_{LIM} \times V_{SNS,CL} = 45\ A \times 0.5\ m\Omega = 22.5\ mV \quad (52)$$

$$R_{SET,CLC} = V_{SNS,CL}/250\ \mu A = 90\ \Omega \quad (53)$$

Chose R_{SET} to equal 90.9Ω, which is the closest available standard resistor. Next obtain the calculated R_{IMON} ($R_{IMON,CLC}$) as follows:

$$R_{IMON,CLC} = \frac{R_{SET} \times 675\ mV}{V_{SNS,CL}} = \frac{90.9\ \Omega \times 675\ mV}{22.5\ mV} = 2.727\ k\Omega \quad (54)$$

Choose 2.74kΩ resistor for R_{IMON}, which is the closest available standard resistor. Since precision current monitoring is not needed 1% resistors were used for R_{IMON} and for R_{SET} and a 2 terminal sense resistor (HCS2512FTL500) was used for R_{SNS}.

Finally, compute the actual current limit ($I_{LIM,CL}$) :

$$I_{LIM,CL} = \frac{0.675\ V \times R_{SET}}{R_{IMON} \times R_{SENSE}} = \frac{0.675\ V \times 90.9\ \Omega}{2.74\ k\Omega \times 0.5\ m\Omega} = 44.8\ A \quad (55)$$

10.2.5.2.2 Selecting the Fast Trip Threshold and Filtering

The TPS2474x allows the user to program the fast trip threshold. When this threshold is exceeded the gate is quickly pulled down. C_{FSTP} can be added to include some filtering into the comparator. The selection of the fast trip threshold and filtering is influenced by the systems environment and requirements. In general picking a larger threshold and larger filtering time will result in more immunity to nuisance trips, but also a slower response (possibly inadequate) to real fault conditions. It's best to fine tune these threshold after testing the real system. As a starting point it is recommended to set the fast trip threshold at least 1.25x larger than then current limit. For this design example a 65A fast trip threshold along with a 500ns filtering time constant were targeted to make sure that the 60A load transient can be passed. The value for R_{FSTP} and C_{FSTP} can be computed as shown in Equation 56 and Equation 57:

$$R_{FSTP,CLC} = \frac{I_{FSTP} \times R_{SNS}}{100\ \mu A} = \frac{65\ A \times 0.5\ m\Omega}{100\ \mu A} = 325\ \Omega \quad (56)$$

$$C_{FSTP} = \frac{t_{FSTP}}{R_{FSTP}} = \frac{500\ ns}{324\ \Omega} = 1.54\ nF \quad (57)$$

The next closest standard resistor and capacitor values should be chosen. In this case R_{FSTP} = 324Ω and C_{FSTP}=1.5nF.

10.2.5.2.3 Selecting the Hot Swap FET

It is critical to select the correct MOSFET for a Hot Swap design. The device must meet the following requirements:

- The V_{DS} rating should be sufficient to handle the maximum system voltage along with any ringing caused by transients. For most 12V systems a 25 V or 30V FET is a good choice.
- The SOA of the FET should be sufficient to handle all usage cases: start-up, hot-short, start into short.
- R_{DSON} should be sufficiently low to maintain the junction and case temperature below the maximum rating of the FET. In fact, it is recommended to keep the steady state FET temperature below 125°C to allow margin to handle transients.
- Maximum continuous current rating should be above the maximum load current and the pulsed drain current must be greater than the current threshold of the circuit breaker. Most MOSFETs that pass the first three requirements will also pass these two.

- A V_{GS} rating of +16 V is required, because the TPS2474x can pull up the gate as high as 15.5 V above source.

For this design the CSD16415Q was selected for its low R_{DSON} and superior SOA. After selecting the MOSFET, the maximum steady state case temperature can be computed as seen in Equation 58:

$$T_{C,MAX} = T_{A,MAX} + R_{\theta CA} \times I^2_{LOAD,MAX} \times R_{DSON}(T_J) \quad (58)$$

Note that the R_{DSON} is a strong function of junction temperature, which for most MOSFETS will be very close to the case temperature. A few iterations of the above equations may be necessary to converge on the final R_{DSON} and $T_{C,MAX}$ value. According to the CSD16415Q datasheet, its R_{DSON} is about 1.4 × greater at 120°C compared to room temperature. Equation 59 uses this R_{DSON} value to compute the $T_{C,MAX}$. Note that the computed $T_{C,MAX}$ is close to the junction temperature assumed for R_{DSON}. Thus no further iterations are necessary.

$$T_{C,MAX} = 55°C + 30° \frac{C}{W} \times (40A)^2 \times (1.4 \times 1\,m\Omega) = 122.2°C \quad (59)$$

10.2.5.2.4 Select Power Limit

In general, a lower power limit setting is preferred to reduce the stress on the MOSFET. However, at low power limit levels both the V_{SNS} and V_{IMON} become very low, which results in more error caused by offsets. It is recommended to keep V_{SNS} above 1.5mV and V_{IMON} above 27mV to ensure reasonable accuracy of the power limit engine. Based on these requirements the minimum power limit can be computed as shown in Equation 60:

$$P_{LIM,MIN} = \frac{V_{IN,MAX}}{R_{SNS}} \times MIN\left(V_{SNS,MIN}, \frac{V_{IMON,MIN} \times R_{SET}}{R_{IMON}}\right)$$
$$= \frac{13\ V}{0.5\ m\Omega} \times MIN\left(1.5\ mV, \frac{27\ mV \times 90.9\ \Omega}{2.74\ k\Omega}\right) = 39\ W \quad (60)$$

In most applications the power limit can be set to $P_{LIM,MIN}$ using the equation below. Here R_{SNS} and R_{PWR} are in Ωs and P_{LIM} is in Watts.

$$R_{PLIM} = \frac{84375 \times R_{SET}}{R_{SNS} \times R_{IMON} \times P_{LIM}} = \frac{84375 \times 90.9\ \Omega}{0.5\ m\Omega \times 2.74\ k\Omega \times 39} = 143.5\ k\Omega \quad (61)$$

The closest available resistor should be selected. In this case it is a 143 kΩ.

10.2.5.2.5 Set Fault Timer

The inrush timer runs when the Hot Swap is in power limit or current limit, which is the case during start-up. Thus the timer has to be sized large enough to prevent a time-out during start-up. If the part starts directly into current limit ($I_{LIM} \times V_{IN} < P_{LIM}$) the maximum start time can be computed with Equation 62:

$$t_{start,max} = \frac{C_{OUT} \times V_{IN,MAX}}{I_{LIM}} \quad (62)$$

For most designs (including this example) $I_{LIM} \times V_{IN} > P_{LIM}$ so the Hot Swap will start in power limit and transition into current limit. In that case the maximum start time can be computed as seen in Equation 63:

$$t_{start,max} = \frac{C_{OUT}}{2} \times \left[\frac{V^2_{IN,MAX}}{P_{LIM}} + \frac{P_{LIM}}{I^2_{LIM}}\right] = \frac{10000\ \mu F}{2} \times \left[\frac{(13\ V)^2}{39\ W} + \frac{39\ W}{(45\ A)^2}\right] = 21.76\ ms \quad (63)$$

Note that the above start time is based on typical current limit and power limit values. To ensure that the timer never times out during start-up it is recommended to set the fault time (TINR) to be 1.5x $t_{start,max}$ or 32.6 ms. This will account for the variation in power limit, timer current, and timer capacitance.

Next the designer should decide if having equal TINR and TFLT is acceptable. Note that to pass the load transient the fault timer needs to be longer than 200 ms. If the inrush time is this long, it will place too much stress on the MOSFET during a start into short. For this reason, it's ideal to have two separate timers. To ensure proper start up and to pass the load transient a target inrush time ($T_{INR,TGT}$) of 32.6 ms and a target fault time ($T_{FLT,TGT}$) of 250ms is used. $C_{INR,CLC}$ and $C_{FLT,CLC}$ is computed as seen in Equation 64 and Equation 65 :

$$C_{INR,CLC} = 7.59\ \mu F \times T_{INR,TGT} = 7.59\ \mu F \times 32.6\ ms = 247\ nF \quad (64)$$

$$C_{FLT,CLC} = 7.59\ \mu F \times T_{FLT,TGT} = 7.59\ \mu F \times 250\ ms = 1898\ nF \quad (65)$$

The next largest available C_{INR} is chosen as 330nF and the next largest available C_{FLT} is chosen as 2.2µF

Next, the actual T_{INR} and T_{FLT} can be computed as shown below: Once C_{TMR} and C_{FLT} is chosen the actual programmed time out can be computed as shown in Equation 66 and Equation 67.

$$T_{INR} = \frac{C_{INR}}{7.407\ \mu F} = \frac{330\ nF}{7.59\ \mu F} = 43.5\ ms \quad (66)$$

$$T_{FLT} = \frac{C_{FLT}}{7.407\ \mu F} = \frac{2.2\ \mu F}{7.59\ \mu F} = 290\ ms \quad (67)$$

10.2.5.2.6 Check MOSFET SOA

Once the power limit and fault timer are chosen, it's critical to check that the FET will stay within its SOA during all test conditions. For this design example the TPS24742 is used, which does not retry during a hot-short. Thus the worst condition is a start-up with output shorted to GND. In this case the TPS24742 will start into a power limit and regulate at that point for 43.5 ms (T_{INR}). Based on the SOA of the CSD16415Q, it can handle 13 V, 15 A for 10 ms and it can handle 13 V, 4 A for 100 ms. The SOA for 43.5 ms can be extrapolated by approximating SOA vs time as a power function as shown in Equation 68:

$$I_{SOA}(t) = a \times t^m$$

$$m = \frac{\ln\left(I_{SOA}(t_1)/I_{SOA}(t_2)\right)}{\ln(t_1/t_2)} = \frac{\ln\left(\frac{15\ A}{4\ A}\right)}{\ln\left(\frac{10\ ms}{100\ ms}\right)} = -0.57$$

$$a = \frac{I_{SOA}(t_1)}{t_1^m} = \frac{15\ A}{(10\ ms)^{-0.57}} = 56.25\ A \times (ms)^{0.57}$$

$$I_{SOA}(43.5\ ms) = 56.25\ A \times (ms)^{0.57} \times (43.5\ ms)^{-0.57} = 6.55\ A \quad (68)$$

Note that the SOA of a MOSFET is specified at a case temperature of 25°C, while the case temperature can be hotter during a start into a short. It is important to understand the hottest temperature that a MOSFET can be during a start-up ($T_{C,\ MAX,\ START}$). If a board has been off for a while and then it's turned on $T_{A,\ MAX}$ is a good estimate for $T_{C,MAX,\ START}$. However, if a board is on and then gets power cycled $T_{C,MAX}$ should be used for $T_{C,MAX,START}$. This will depend on system requirements. For this design example it is assumed that the board can only be plugged in cold and $T_{A,MAX}$ is used to estimate $T_{C,MAX,START}$.

$$I_{SOA}(43.5\ ms, T_{C,MAX,START}) = I_{SOA}(43.5\ ms,\ 25°C) \times \frac{T_{J,ABSMAX} - T_{A,MAX}}{T_{J,ABSMAX} - 25°C}$$

$$= 6.55\ A \times \frac{150°C - 55°C}{150°C - 25°C} = 4.98\ A \quad (69)$$

Based on this calculation the MOSFET can handle 4.98 A, 13 V for 43.5 ms at 55°C elevated case temperature, but is only required to handle 3A during a hot-short. Thus there is good margin and this will be a robust design. In general, it is recommended that the MOSFET can handle 1.3x more than what is required during a worst case operating condition. This provides margin to cover the variance of the power limit and fault time.

10.2.5.2.7 Checking Stability of Hot Swap Loop

Using the same method as shown for the OR then Hot Swap example, Ensuring Stability, the minimum required C_{GS} is computed to be 0.6 nF. Again the C_{ISS} is 3.1nF and there is plenty of margin to ensure stability.

10.2.5.2.8 Choose ORing MOSFET

When selecting the ORing MOSFET, the considerations are similar to the Hot Swap MOSFET, but the SOA is no longer critical. In addition the lower R_{DSON} is not always ideal, because that would result in a larger reverse current for the same reverse voltage threshold. Of course a lower R_{DSON} would provide better efficiency. For consistency sake a single CSD16415Q FET was used for the ORing section as well. It's important to check its steady state temperature at max load using the same equation that was used for the Hot Swap.

$$T_{C,MAX} = 55°C + 30°\frac{C}{W} \times (40\ A)^2 \times (1.4 \times 1\ m\Omega) = 122.2°C \quad (70)$$

10.2.5.2.9 Choose Reverse Current Threshold and Filtering

Same settings were used as the previous design example.

10.2.5.2.10 Choose Under Voltage and Over Voltage Settings

Same settings were used as the previous design example.

10.2.5.2.11 Selecting C_{IN}, C_{OUT}, C_{MIDDLE}, and Transient Protection

Same settings were used as the previous design example

10.2.5.2.12 Adding C_{ENHS}

When the ENHS pulled below its threshold and raised back up the IC will reset. Note that during a hot short the input voltage can easily droop below the UV threshold and cycle the ENHS pin. For the TPS24740 and TPS24741 IC's this will not cause any issues. However, when using the TPS24742 the cycling of the ENHS will result in the IC attempting to restart, which is undesired (this is the main reason why someone would use the TPS24742). To avoid this behavior a capacitor should be added to the ENHS to provide filtering. For this example 33 nF was chosen.

10.2.5.3 Application Curves

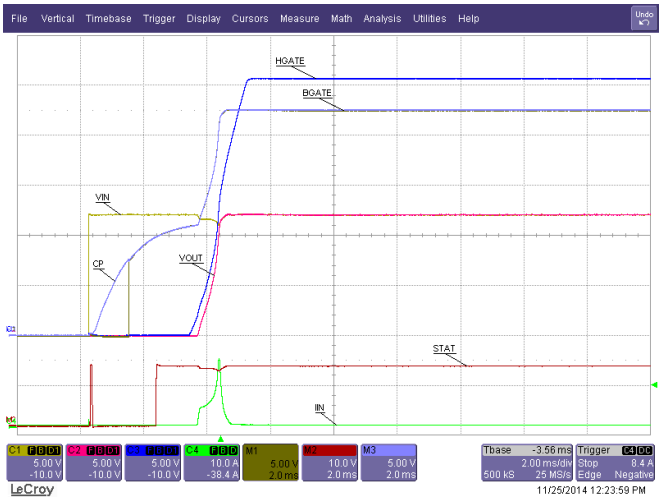


Figure 46. Start up (C_{OUT}=440µF)

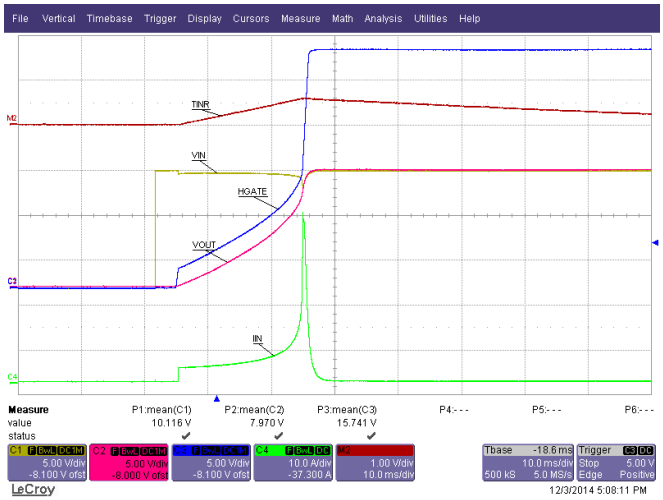


Figure 47. Start up (C_{OUT}=10,000µF, V_{IN} = 13V)

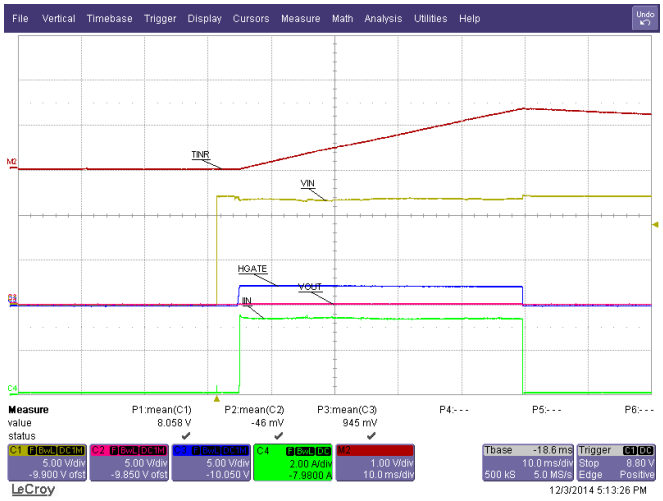


Figure 48. Start up Into Short on V_{OUT}

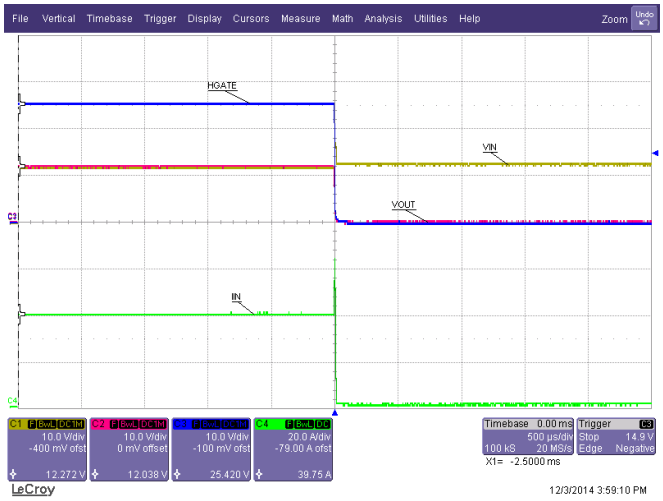


Figure 49. Hot Short on V_{OUT}

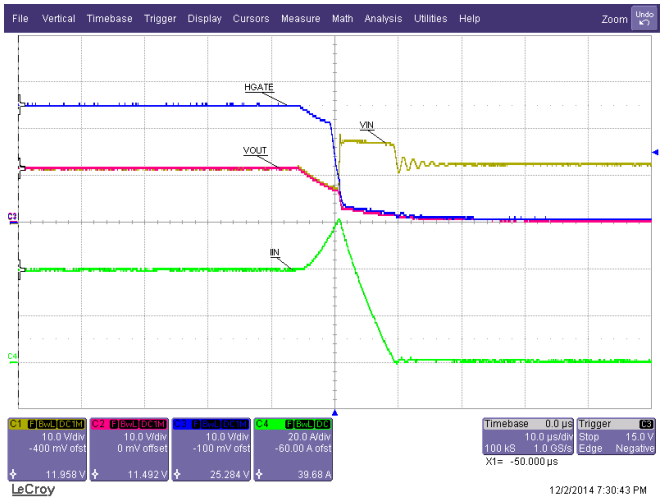


Figure 50. Hot – Short on V_{OUT}(zoomed in)

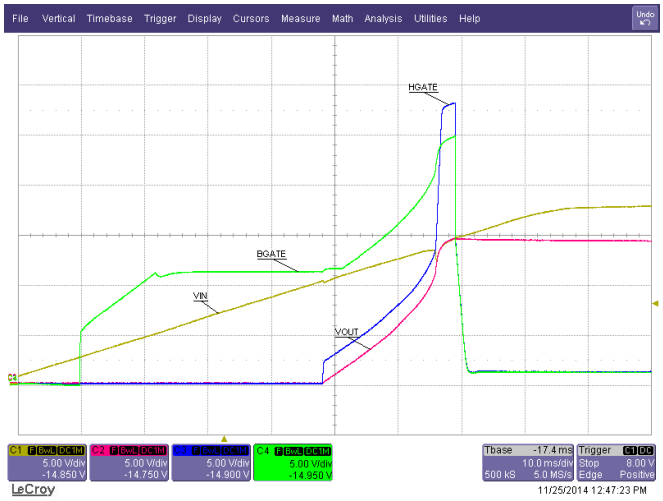


Figure 51. Under/Over Voltage with V_{IN} Rising

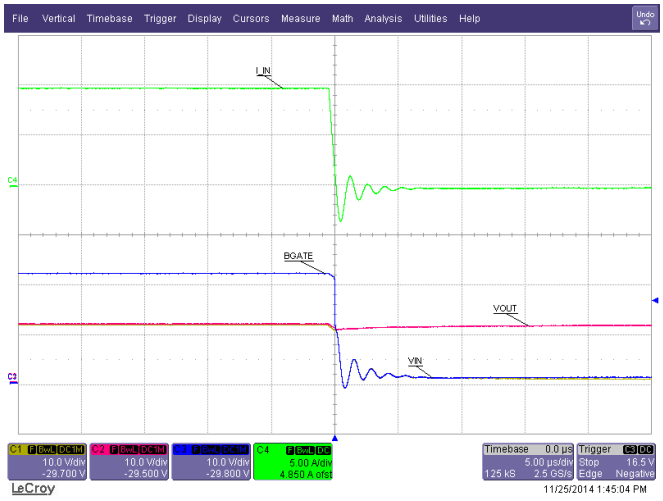


Figure 52. Short Vin (I_{LOAD} = 10A)

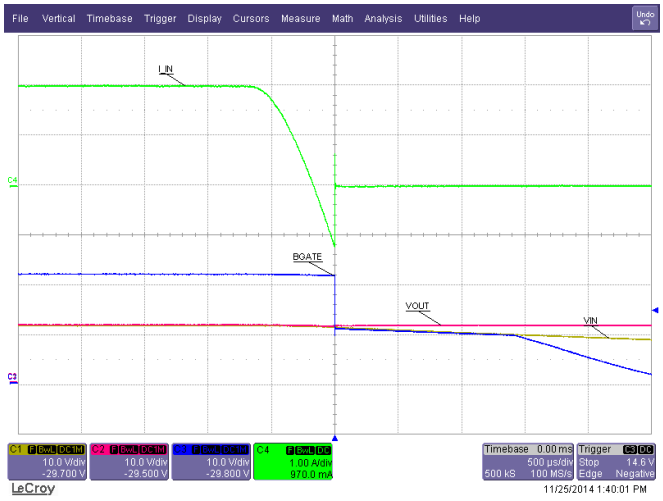


Figure 53. Gradual Reverse Current

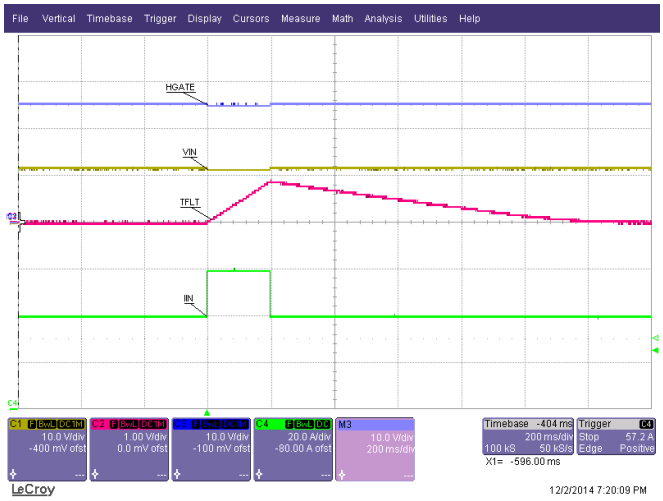


Figure 54. 60A Load Step for 200 ms

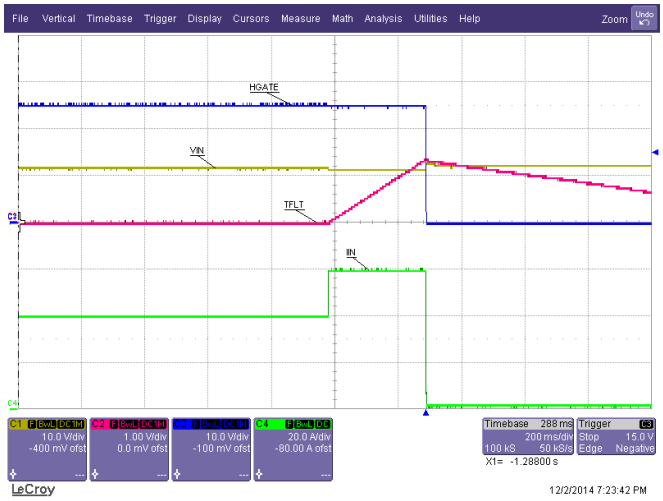


Figure 55. Load Step 40A to 60A

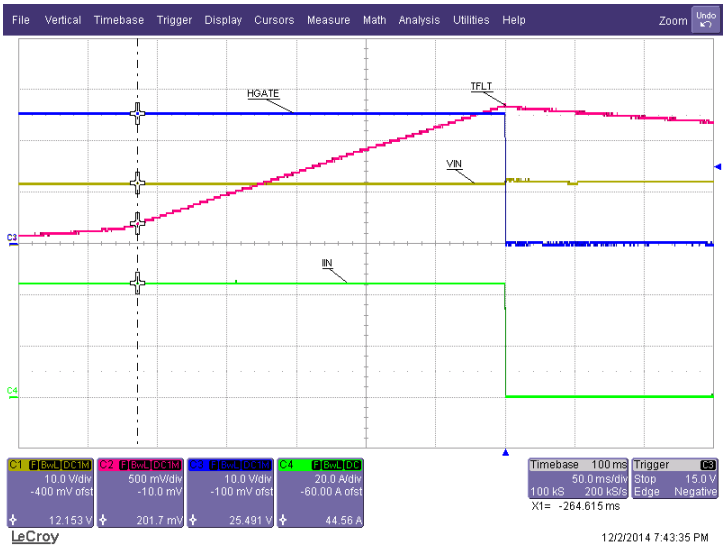


Figure 56. Gradual Overcurrent

10.3 System Examples

The TPS2474x is a flexible Hot Swap and ORing controller that can supports many redundant configurations. The following section goes through the various system level configurations and the advantages of each one. It also shows how the TPS2474x will behave under system level tests.

10.3.1 TPS2474x in Battery Back Up

Some battery back-up units are set up to support both charging and discharging from the same terminal. In this case a configuration shown in Figure 57 can be used. In normal operation the load is power from the AC/DC, while the BBU is charged from the mid-point. The Hot Swap will provide inrush and fault protection to the load. If the AC/DC fails the ORing will prevent the reverse current to the AC/DC and the load will get powered from the BBU.

System Examples (continued)

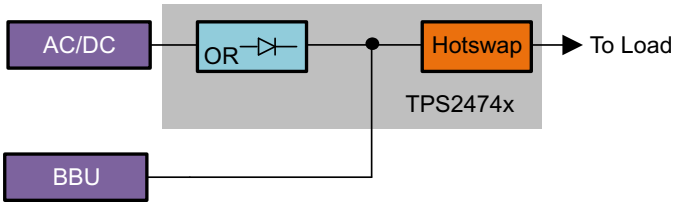


Figure 57. Block Diagram for Hot Swap and ORing in BBU Applications

Figure 58 shows the schematic for this implementation. It is important to connect VDD to the mid-point to ensure that the IC has power even if V_{IN} goes away. In addition the ENHS pin should be based on the mid-point voltage to ensure that the Hot Swap stays ON even if the V_{IN} power goes away.

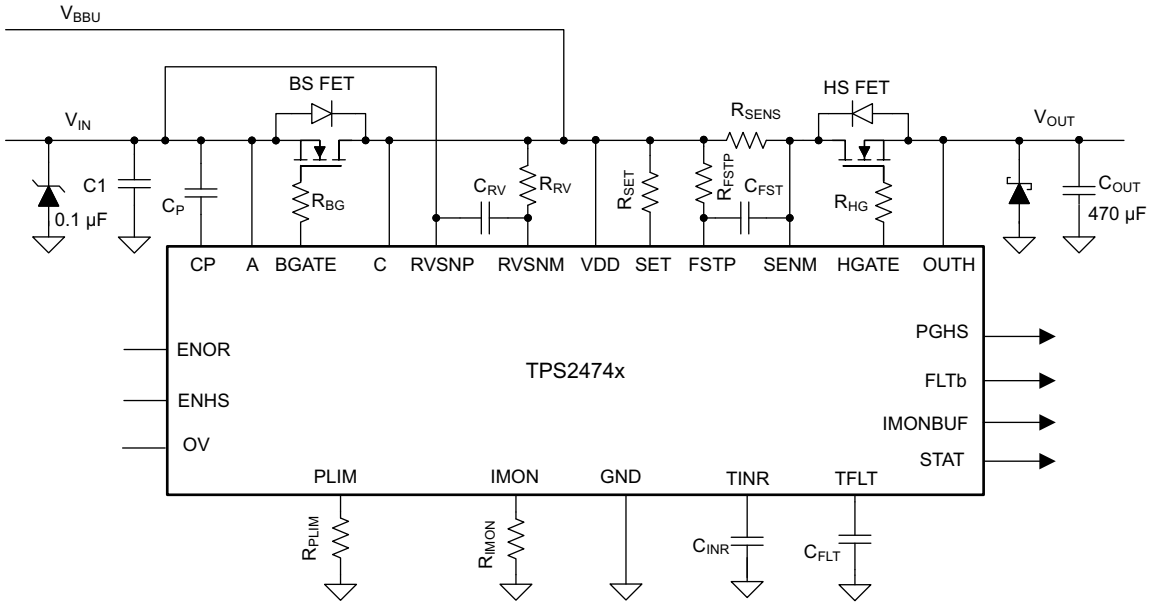


Figure 58. Application Schematic for TPS2474x in BBU Applications

Figure 59 shows a switch over from the AC/DC power (V_{IN}) to BBU power with a 12A load. The BBU is modeled as drawing 4A when V_{MIDDLE} > 12V and supplying up to 20A when V_{MIDDLE} < 12V. Note that when V_{IN} collapses the BBU current goes from negative to positive and the BGATE goes down to prevent the AC/DC from draining power from the BBU.

System Examples (continued)

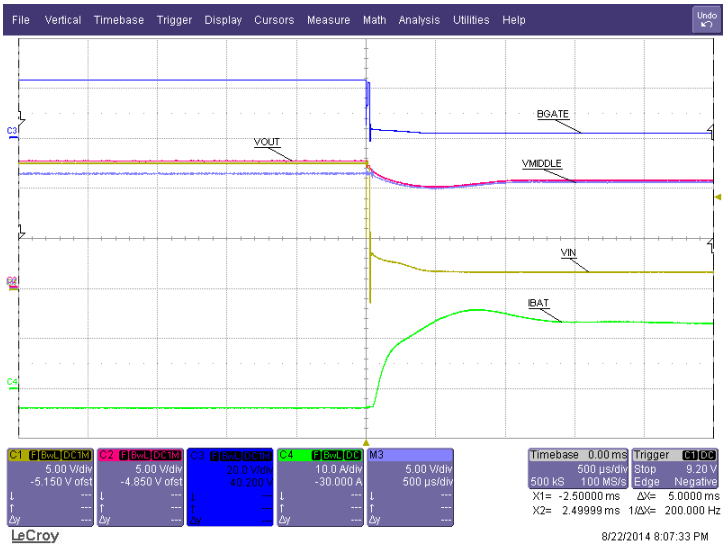


Figure 59. Switch Over to Battery Power

10.3.2 TPS2474x in Priority Muxing

Priority muxing is used in the following scenario:

1. The system should be powered from Main when it's present
2. The system should be powered from Auxiliary when Main goes away.
3. Auxiliary voltage may be above the Main voltage.
4. The system should support a short to ground on both Main and Aux.

Due to condition 3, the 2 supplies can't be simply ORed together because the load could start drawing power from AUX. That's why an additional Hot Swap is required on the AUX rail to prevent the forward current flow. The OV pin of the TPS2474x can be used to keep the Auxiliary Hot Swap OFF unless the voltage on MAIN falls below a certain threshold.

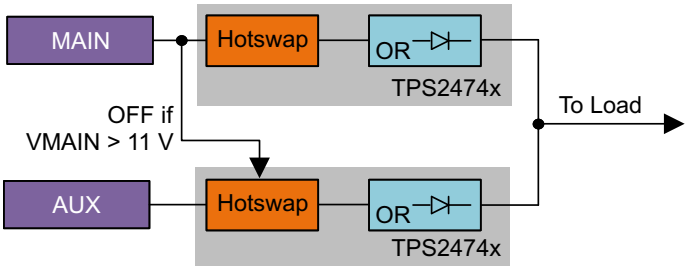


Figure 60. Block Diagram for Priority Muxing

System Examples (continued)

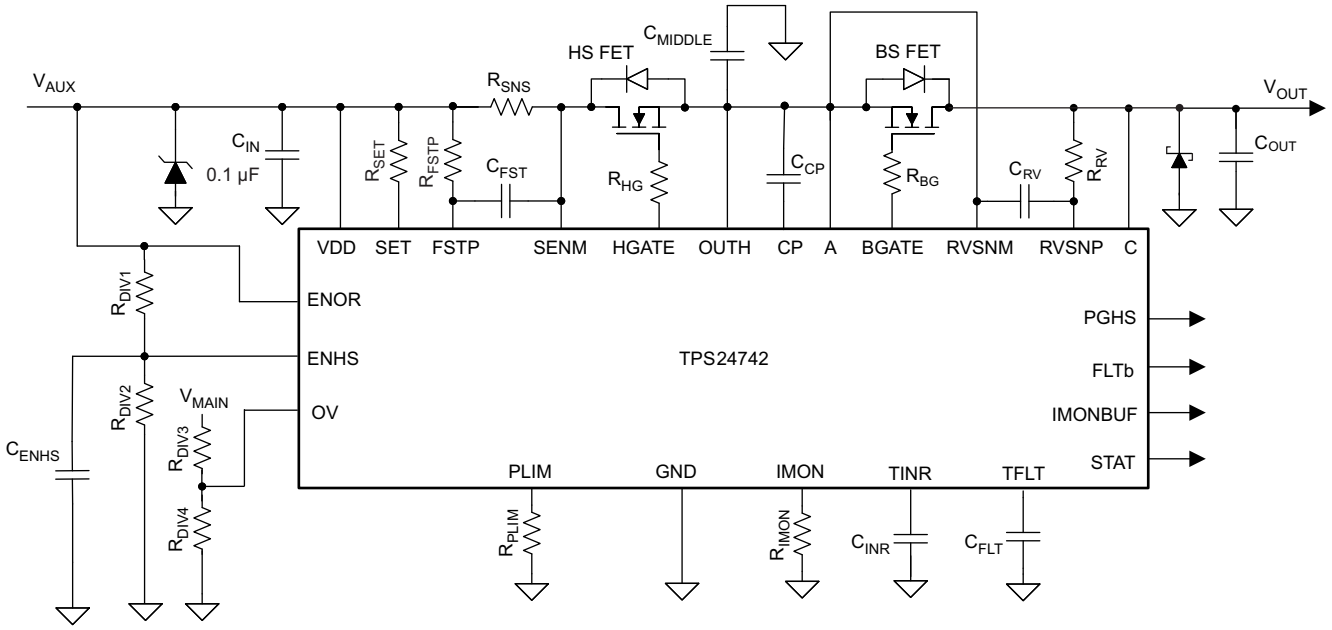


Figure 61. OV Pin Hook Up on the AUX Channel

The following waveforms show the performance of the priority mux using the settings from the Hot Swap then ORing design example. The OV pin on the AUX side was set to make it turn on once Main was below 11V. Note that for a 10A load the switch over occurs without any issues, but the system cannot handle it at 30A. This occurs due to VAUX being higher than VMAIN and VOUT drooping after the main channel shuts down and the AUX channel coming back up. As a result there is a voltage drop across the Hot Swap MOSFET (V_{AUX} – V_{OUT}) and the TPS24742 limits the input current to P_{LIM}/V_{DS}. If the supplied current is lower than the load current the output capacitor continues to discharge and the system shuts down. When the power limit was increased to 160W the switch over occurred without any issues, because sufficient current was supplied to power the load and charge the output capacitor.

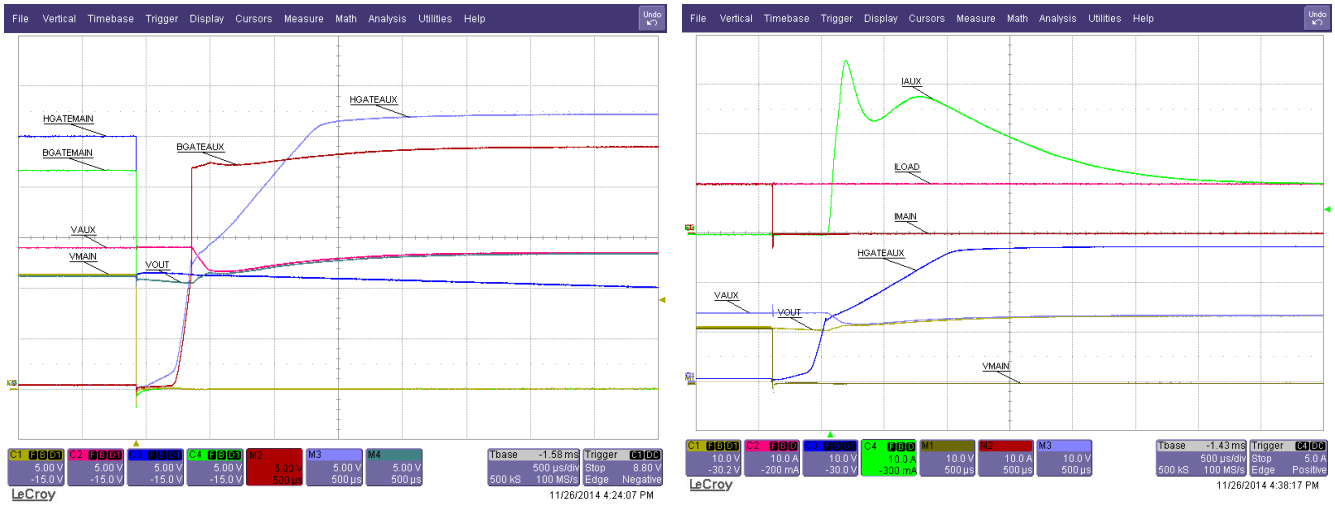
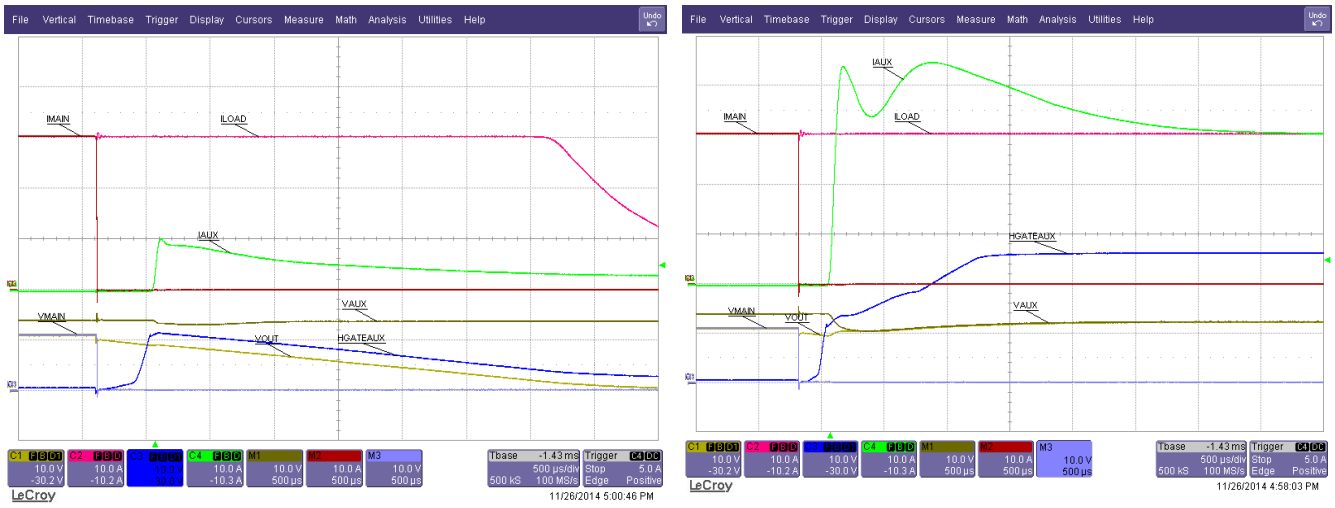


Figure 62. Switch from Main to Aux (V_{MAIN} = 12V, V_{AUX} = 14V, I_{LOAD} = 10A)

System Examples (continued)



P_{LIM} = 39W

P_{LIM} = 160W

Figure 63. Switch from Main to Aux with V_{MAIN} = 12V, V_{AUX} = 14V, I_{LOAD} = 30A (left: P_{LIM} = 39W, right; P_{LIM} = 160W)

10.3.3 TPS2474x with Multiple Loads and Multiple Supplies

Figure 64 applies to systems that have multiple supplies and multiple loads. The ORing after each supply ensures that the loads won't lose power if any of the supplies fail and the Hot Swap in front of each load ensures that a failure on one load doesn't affect the operation of the other loads. The node on the output of ORing and input of the Hot Swaps is referred to as V_{MIDDLE}.

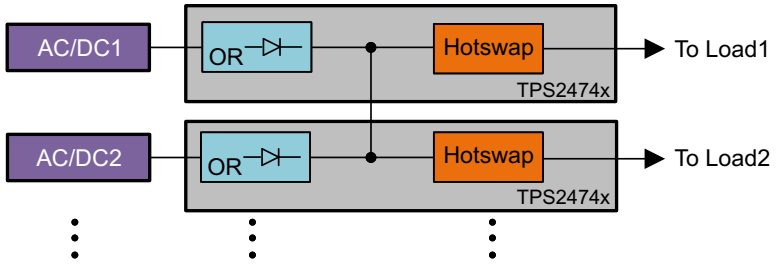


Figure 64. Block Diagram for Systems with Multiple Supplies and Loads

Figure 65 shows a hot-short on load 1, which results in a shutdown of the first Hot Swap gate. Note that the second load continues to be powered as both HGATE2 and VMIDDLE stay high.

System Examples (continued)

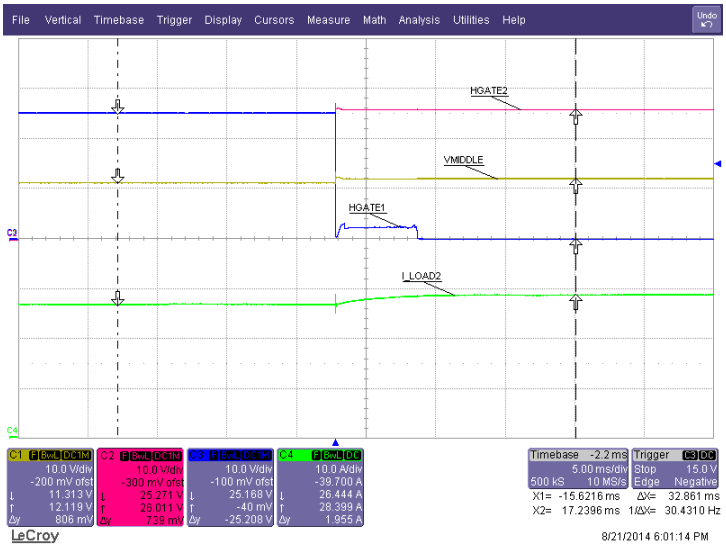
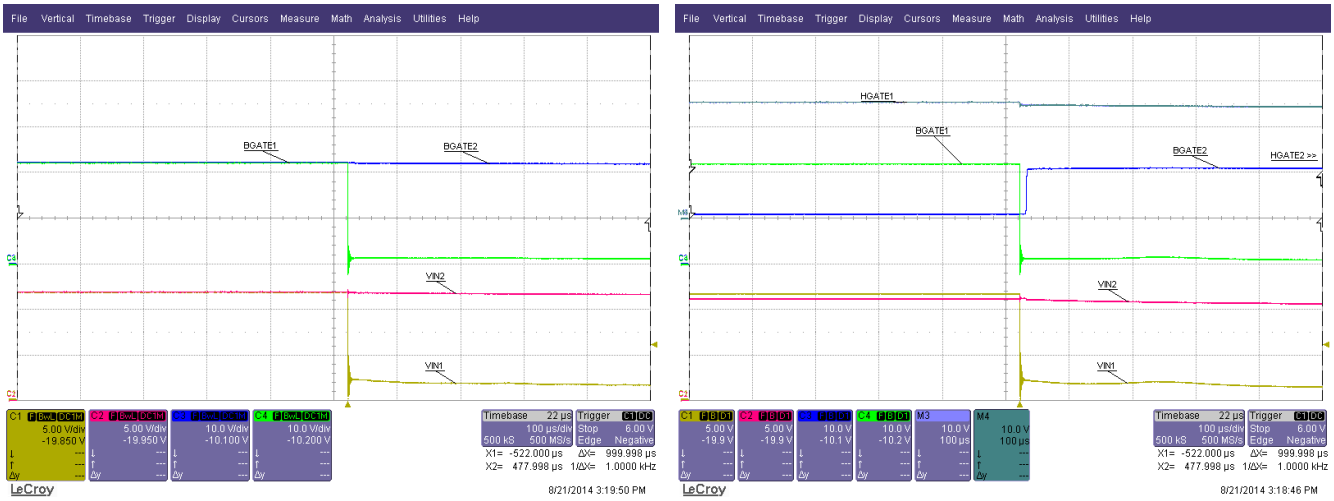


Figure 65. Hot Short on Load 1, Load 2 Not Interrupted

The main purpose of the ORing controller is to protect the loads when one of the input supplies has a failure. The two waveforms below show this scenario. The left waveform shows a condition where both of the power supplies are at the same voltage and both of the BGATEs are ON. When VIN1 goes to ground BGATE1 quickly turns OFF, while BGATE2 remains ON. In the waveform on the right VIN1 is above VIN2 so the system starts by with only BGATE1 being ON. When VIN1 goes to ground, BGATE1 quickly turns off and BGATE2 turns ON. There is a short delay between BGATE1 turning off and BGATE2 turning ON. This pause is due to V_{MIDDLE} discharging from 12.5V to 12V (BGATE2 will only turn on when VIN2 > VMIDDLE)



$V_{IN1} = V_{IN2} = 12V$ $V_{IN1} = 12.5V, V_{IN2} = 12V$

Figure 66. Hot Short on V_{IN1}
(left: $V_{IN1} = V_{IN2} = 12V$; right $V_{IN1} = 12.5V$, $V_{IN2} = 12V$, $I_{LOAD1} = I_{LOAD2} = 12A$)

System Examples (continued)

Figure 67 shows a system configuration where V_{IN1} equals V_{IN2} and V_{IN2} is hot plugged. Note that when BGATE2 comes up almost immediately and VIN1 raises as well. This is due to the fact that V_{IN1} had some voltage droop due to the IR drop of the input impedance. When a second supply was placed in parallel the load was shared reducing the droop. The quick input spike on V_{IN2} is due input inductance.

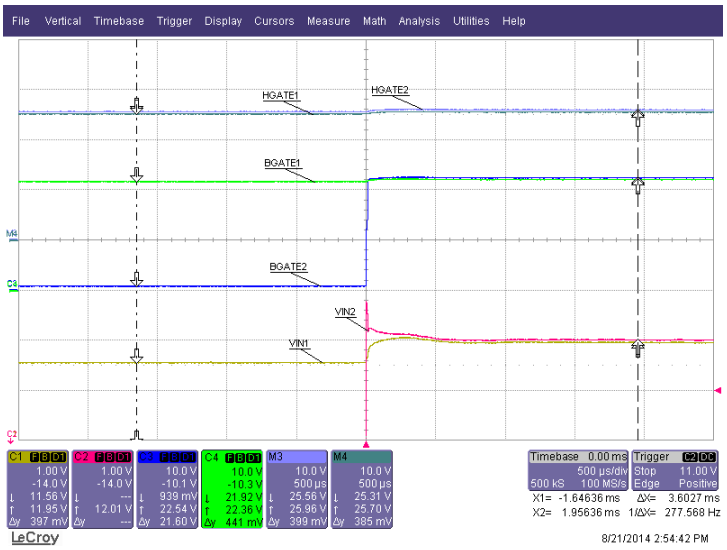


Figure 67. Hot Plug V_{IN2} (V_{IN1} = 12V; V_{IN2} = 12V; I_{LOAD1} = I_{LOAD2} = 12A)

10.3.4 Two Supplies Powering a Load

Figure 68 can be used when ORing two power supplies together to drive a single load. The ORing provide protection in case one of the AC/DC's fail and the Hot Swap provides protection if there is a failure at the load and if one of the AC/DC output voltages has an overvoltage condition.

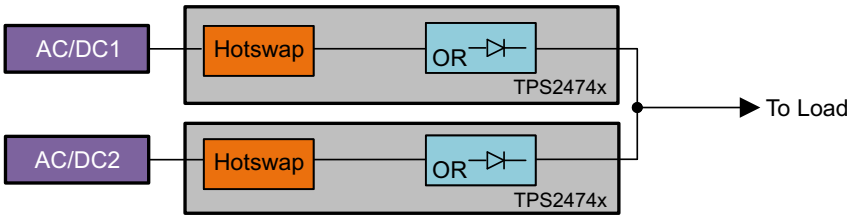


Figure 68. Block Diagram for ORing Two Power Supplies

Figure 69 and Figure 70 shows a hot plug event on power supply A, when power supply B is already up. If V_{INA} is above V_{INB}, the blocking gate of channel B turns off and the load is powered from channel A. If V_{INA} is below V_{INB}, BGATEA doesn't enhance and the power continues to be supplied from channel B.

System Examples (continued)

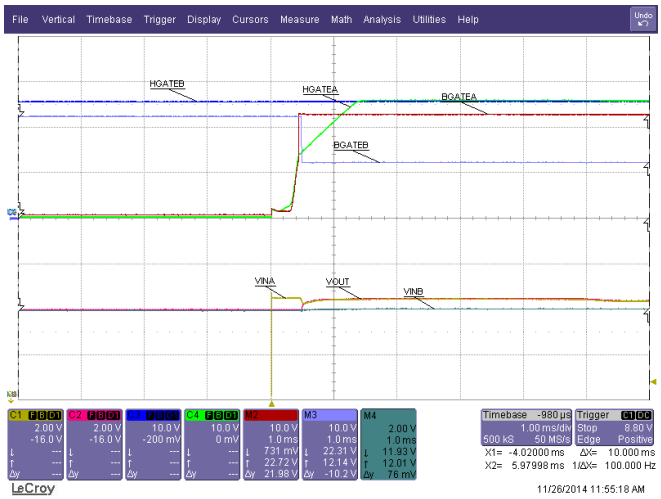


Figure 69. Hot Plug V_{INA} (V_{INA} =12.5, V_{INB} = 12V, R_{LOAD} = 10Ω)

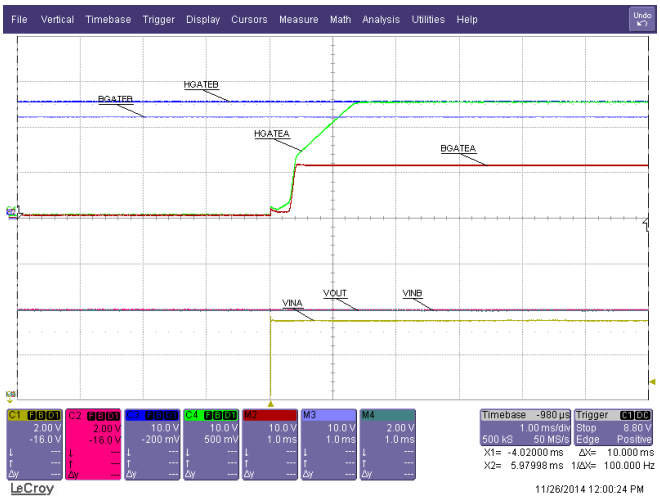


Figure 70. Hot Plug V_{INA} (V_{INA} =11.5V, V_{IN2} = 12V, R_{LOAD} = 10Ω)

Figure 71 shows power switching from V_{INA} to V_{INB} after V_{INA} shorts to ground. Note that V_{OUT} droops until it is at the same level as V_{INB} when BGATEB turns on.

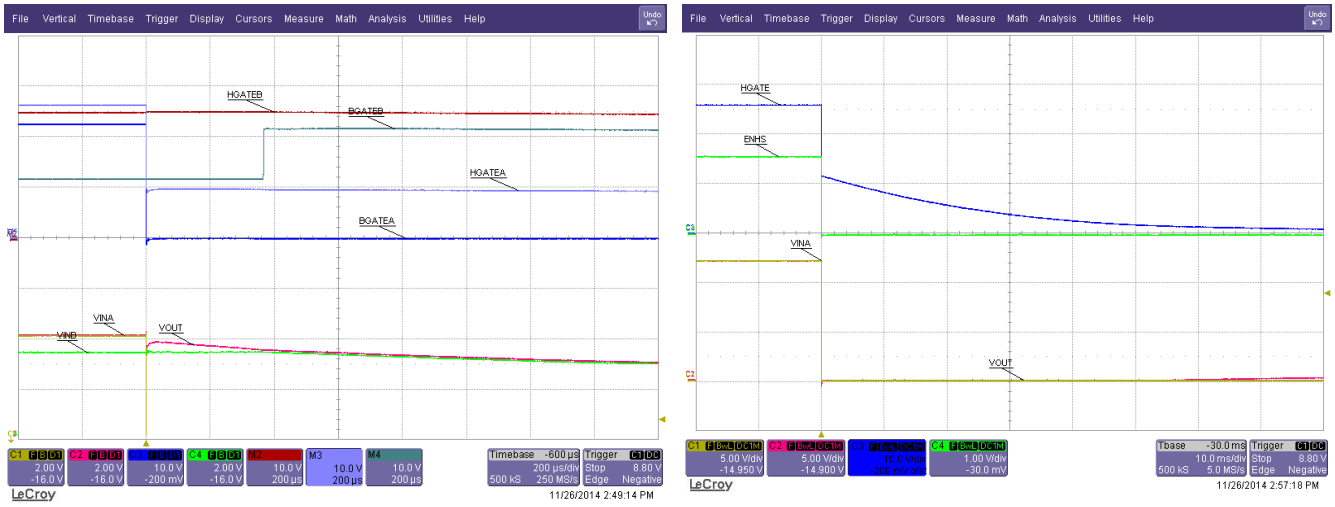


Figure 71. Short on V_{INA} Zoomed In and Zoomed Out View (I_{LOAD}=10A, V_{INA} = 12V, V_{INB} = 11.5V)

Figure 72 shows the same event when V_{INA} and V_{INB} are equal and both channels are on before VINA shorts to ground. Note channel B stays on and channel A shuts down.

System Examples (continued)

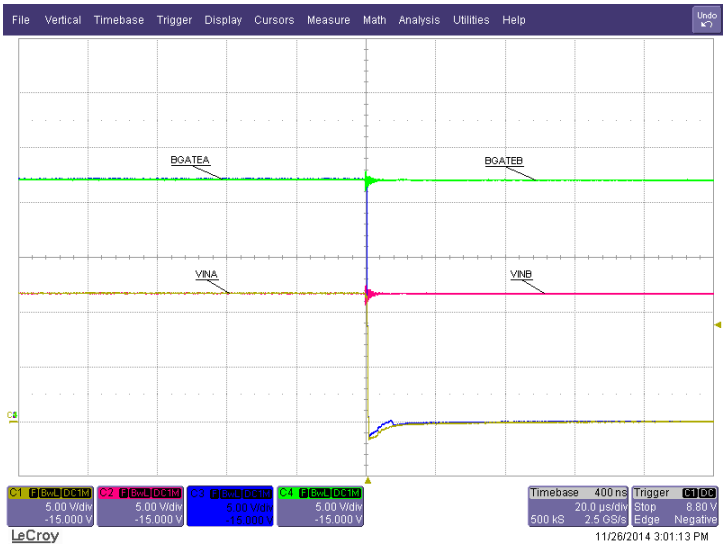


Figure 72. Short on V_{INA} (I_{LOAD}=10A, V_{INA} = 12V, V_{INB} = 12V)

10.3.5 TPS2474x in Redundant DC/DC Applications

In systems that require zero down time, redundant DC/DCs may be used. The goal is to maintain the output voltage bus even if one of the DC/DCs fail. Consider a case when there is a short on the high-side MOSFET. This would effectively short the input bus to the output bus through an inductor resulting in a system failure. Adding Hot Swap before the DC/DC will protect both the input bus and the output bus by disconnecting power to the faulty DC/DC module. Next consider a case when the low side MOSFET is shorted. This would pull down the output bus causing system failure as well. To prevent this and ORing controller should be added on the output of the DC/DC controller.

TPS2474x is ideal for this application because it can provide both the hot swap and ORing functionality. Note that the combination of the DC/DC and TPS2474x can be made into hot-swappable modules. That way these can be replaced without turning OFF the system.

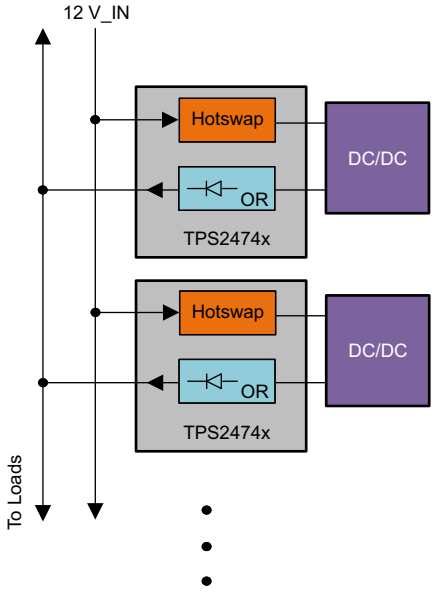


Figure 73. Block Diagram for Systems With Redundant DC/DC

System Examples (continued)

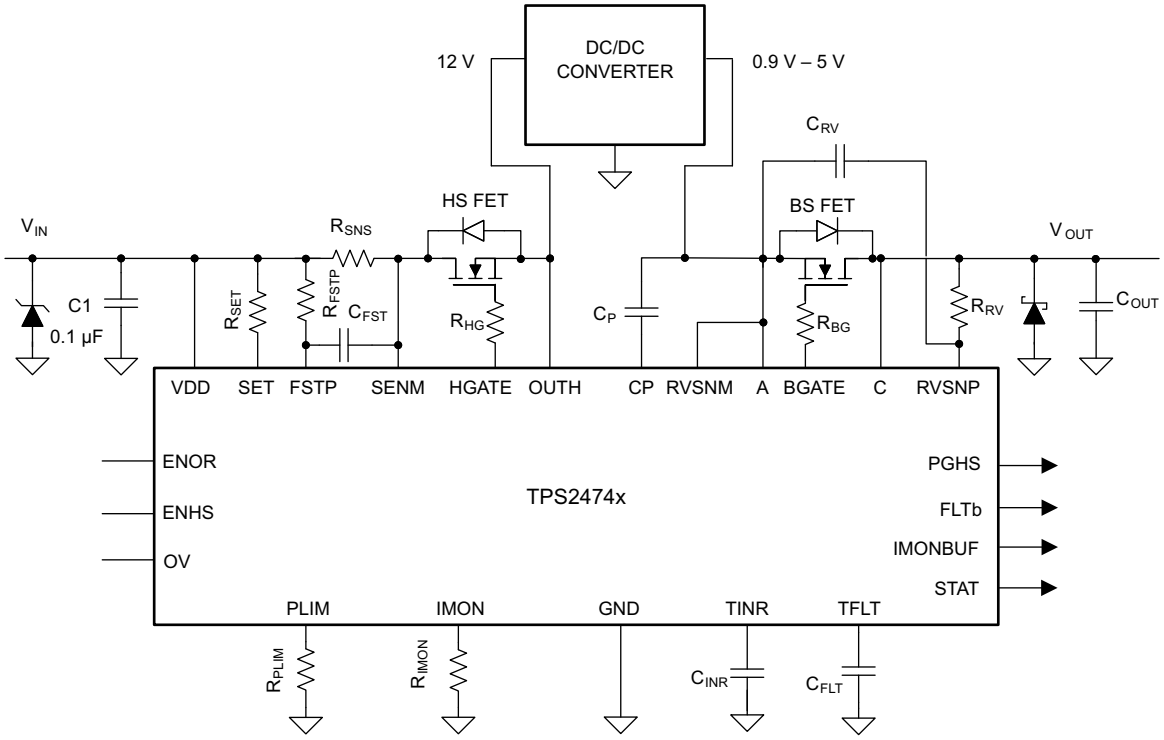


Figure 74. Application Schematic for Hot Swap, DC/DC, ORing Configuration

11 Power Supply Recommendations

In general, operation is best when the input supply isn't noisy and doesn't have significant transients. For noisier environments filtering on input, output, fast trip, and reverse trip should be adjusted to avoid nuisance trips.

12 Layout

12.1 Layout Guidelines

When doing the layout of the TPS2474x in the ORing then hot swap configuration the following are considered best practice.

- Ensure proper Kelvin Sense of R_{SNS}
- Keep the filtering capacitors C_{FSTP} and C_{RV} as close to the IC as possible.
- Keep the traces from C_{CP} to CP and A as short as possible.
- Run a separate trace from A and RVSNM to ORing FET source. This will prevent the charge pump noise along with a DC bias (due to supply current draw) from interfering with the reverse current threshold.
- Run a separate trace from C and from R_{RV} to ORing FET drain.
- Place a Schottky diode and a ceramic bypass capacitor close to the source of the Hot Swap MOSFET.
- Place a TVS and a ceramic bypass capacitor between V_{IN} and ground close to the source of the ORing MOSFET.
- Use a separate trace to connect to VDD and SENM.
- Note that special care must be taken when placing the bypass capacitor for the VDD pin. During Hot Shorts, there is a very large dv/dt on input voltage during the MOSFET turn off. If the bypass capacitor is placed right next to the pin and the trace from R_{SNS} to the pin is long, an LC filter is formed. As a result a large differential voltage can develop between VDD and SENM if there is a large transient on Vin. This could result in a violation of the abs max rating from VDD to SENM. To avoid this, place the bypass capacitor close to R_{SNS} instead of the VDD pin.

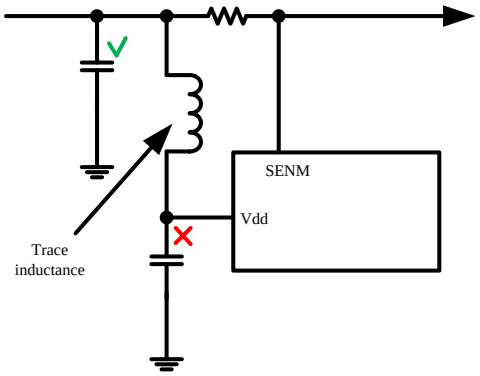


Figure 75. Layout Don'ts

12.2 Layout Example

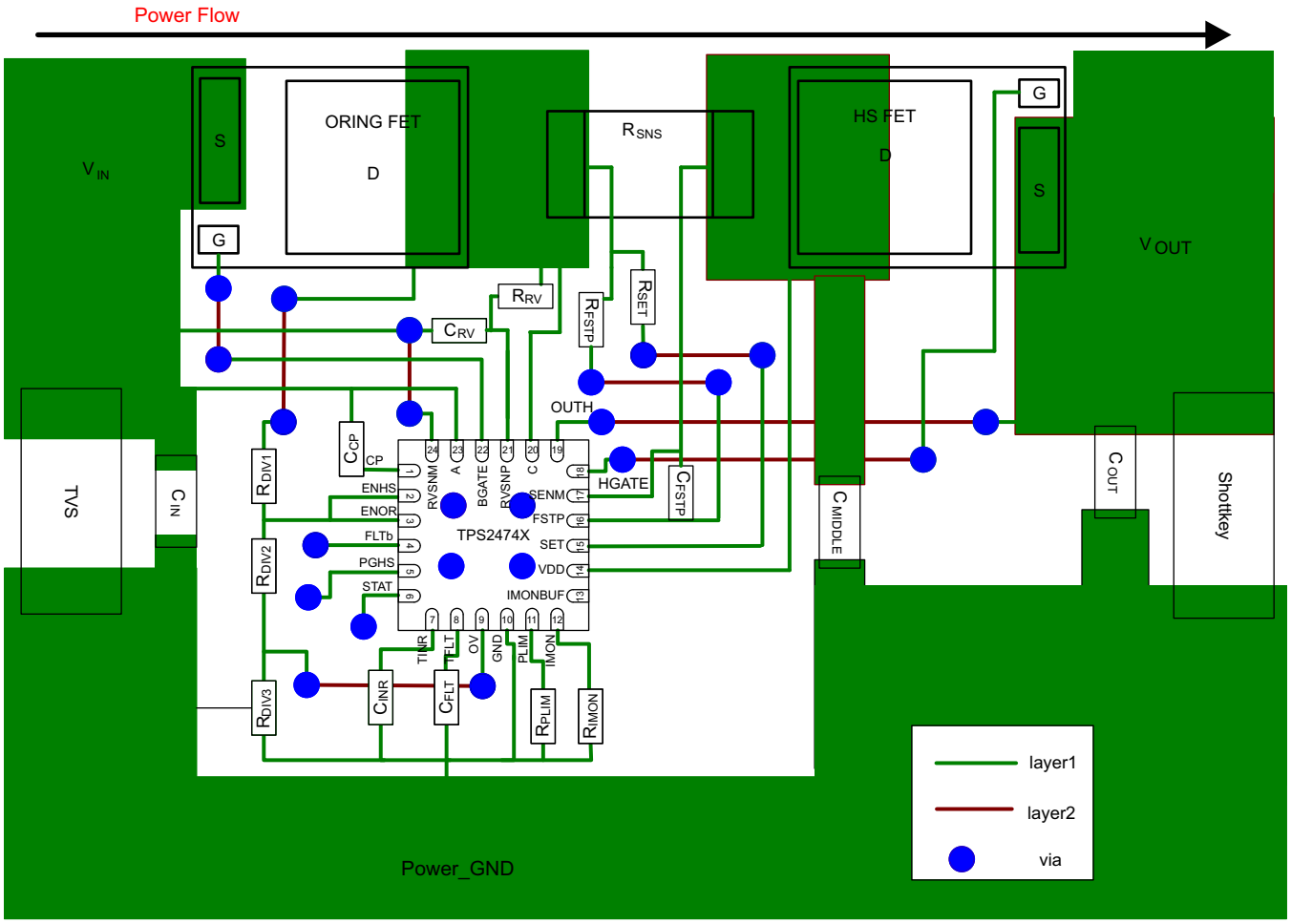


Figure 76. Layout Example for ORing then Hot Swap Configuration

13 Device and Documentation Support

13.1 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

Table 6. Related Links

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
TPS24740	Click here	Click here	Click here	Click here	Click here
TPS24741	Click here	Click here	Click here	Click here	Click here
TPS24742	Click here	Click here	Click here	Click here	Click here

13.2 Trademarks

All trademarks are the property of their respective owners.

13.3 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

13.4 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

14 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS24740RGER	ACTIVE	VQFN	RGE	24	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	TPS 24740	Samples
TPS24740RGET	ACTIVE	VQFN	RGE	24	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	TPS 24740	Samples
TPS24741RGER	ACTIVE	VQFN	RGE	24	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	TPS 24741	Samples
TPS24741RGET	ACTIVE	VQFN	RGE	24	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	TPS 24741	Samples
TPS24742RGER	ACTIVE	VQFN	RGE	24	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	TPS 24742	Samples
TPS24742RGET	ACTIVE	VQFN	RGE	24	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	TPS 24742	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

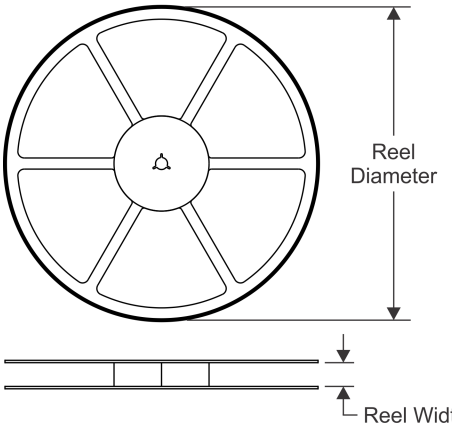
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

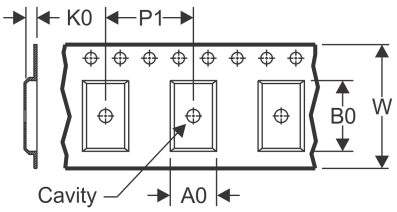
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

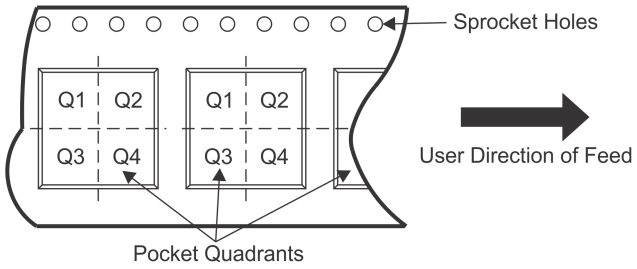


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

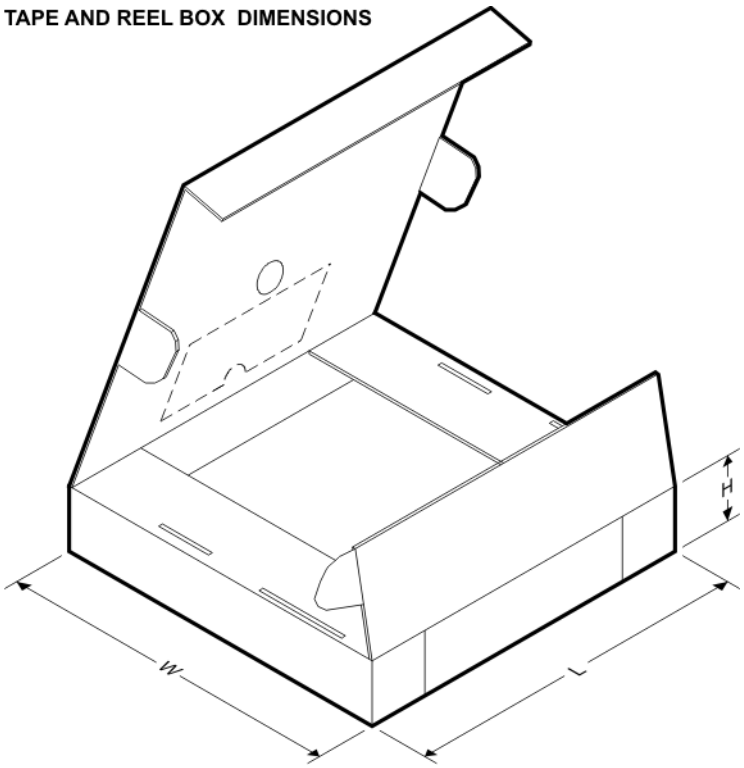
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS24740RGER	VQFN	RGE	24	3000	330.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2
TPS24740RGET	VQFN	RGE	24	250	180.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2
TPS24741RGER	VQFN	RGE	24	3000	330.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2
TPS24741RGET	VQFN	RGE	24	250	180.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2
TPS24742RGER	VQFN	RGE	24	3000	330.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2
TPS24742RGET	VQFN	RGE	24	250	180.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2

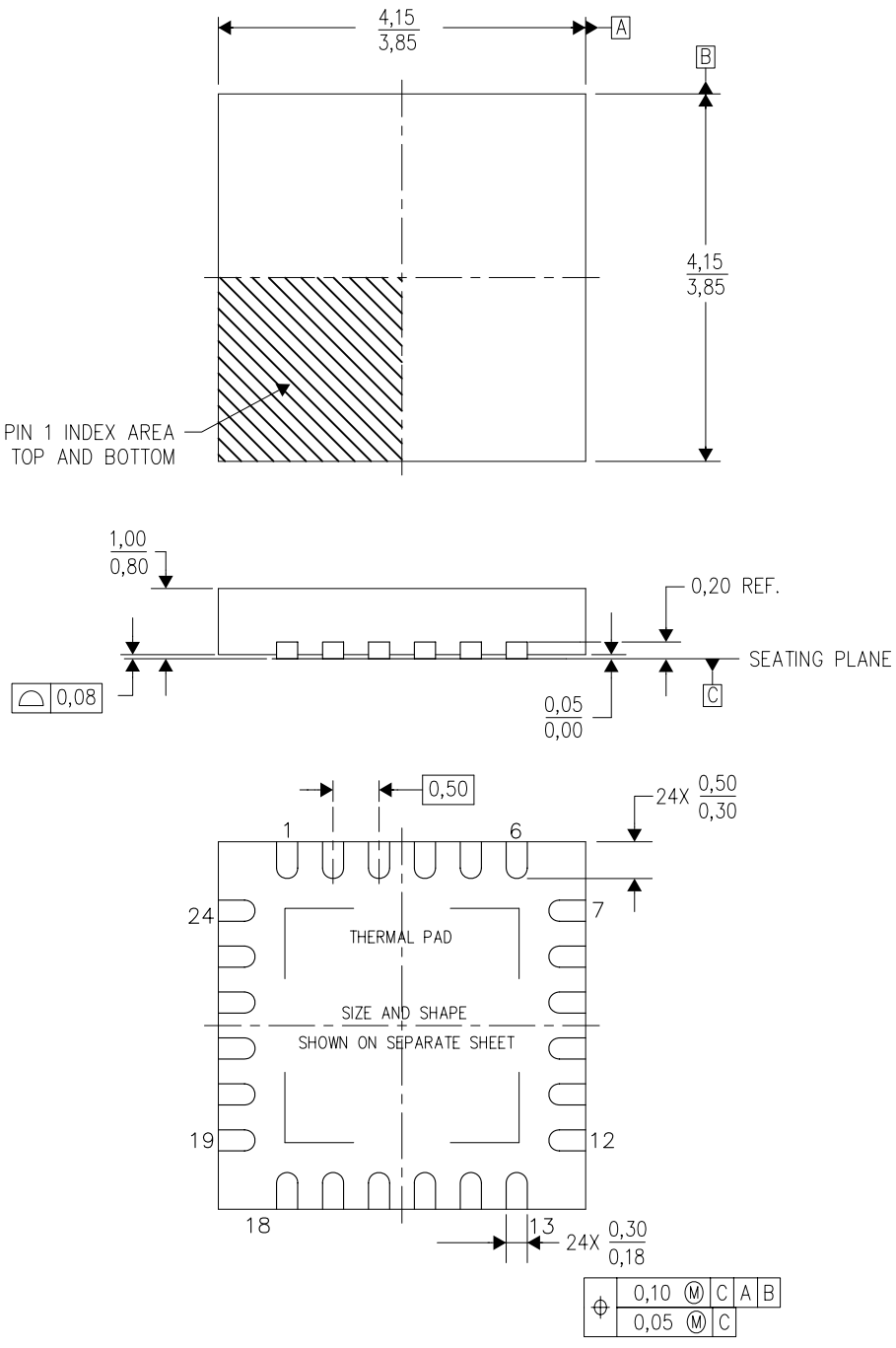
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS24740RGER	VQFN	RGE	24	3000	367.0	367.0	35.0
TPS24740RGET	VQFN	RGE	24	250	210.0	185.0	35.0
TPS24741RGER	VQFN	RGE	24	3000	367.0	367.0	35.0
TPS24741RGET	VQFN	RGE	24	250	210.0	185.0	35.0
TPS24742RGER	VQFN	RGE	24	3000	367.0	367.0	35.0
TPS24742RGET	VQFN	RGE	24	250	210.0	185.0	35.0

RGE (S–PVQFN–N24) PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Quad Flatpack, No–Leads (QFN) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
F. Falls within JEDEC MO–220.

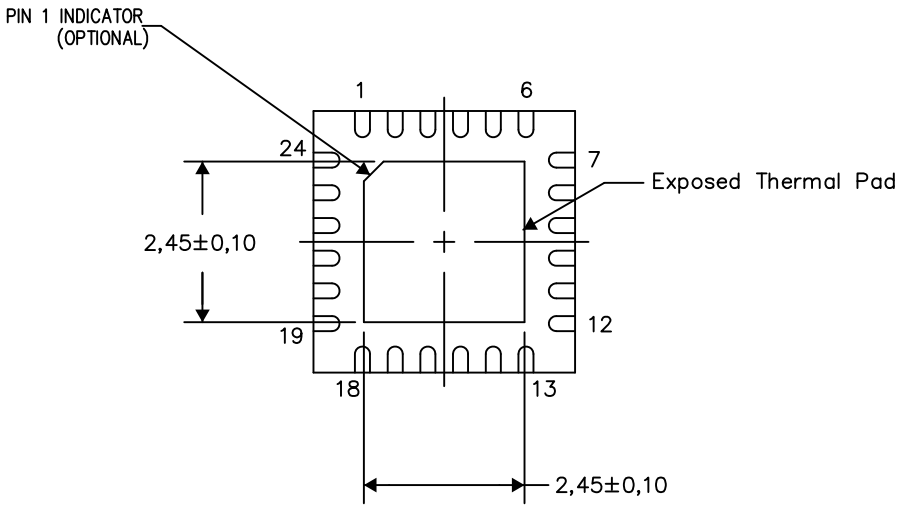
RGE (S–PVQFN–N24) PLASTIC QUAD FLATPACK NO–LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



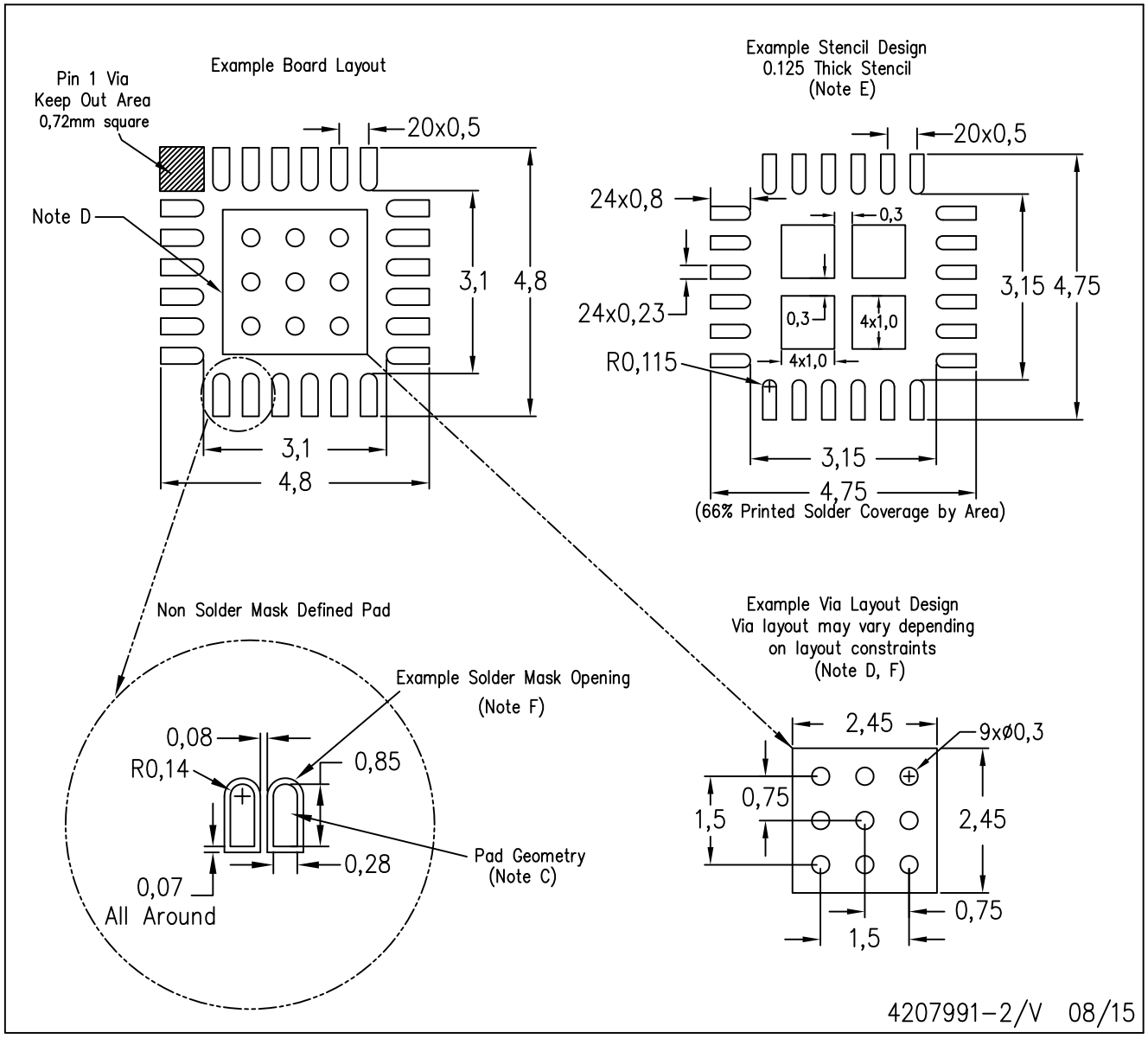
Bottom View

Exposed Thermal Pad Dimensions

4206344–3/AK 08/15

NOTES: A. All linear dimensions are in millimeters

RGE (S–PVQFN–N24) PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat–Pack Packages, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
F. Customers should contact their board fabrication site for recommended solder mask tolerances and via tenting recommendations for vias placed in the thermal pad.

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