TPS786 Ultralow-Noise, High-PSRR, Fast, RF, 1.5-A Low-Dropout Linear Regulators

1 Features

- 1.5-A Low-Dropout Regulator With Enable
- Available in Fixed and Adjustable (1.2 V to 5.5 V) Output Versions
- High PSRR (49 dB at 10 kHz)
- Ultralow Noise (48 μV_{RMS}, TPS78630)
- Fast Start-Up Time (50 μs)
- Stable With a 1-μF Ceramic Capacitor
- Excellent Load and Line Transient Response
- Very Low Dropout Voltage (390 mV at Full Load, TPS78630)
- 3 × 3 SON PowerPAD™, 6-Pin SOT223 and 5-Pin DDPAK Package

2 Applications

- RF: VCOs, Receivers, ADCs
- Audio
- Bluetooth®, Wireless LAN
- Cellular and Cordless Telephones
- Handheld Organizers, PDAs

3 Description

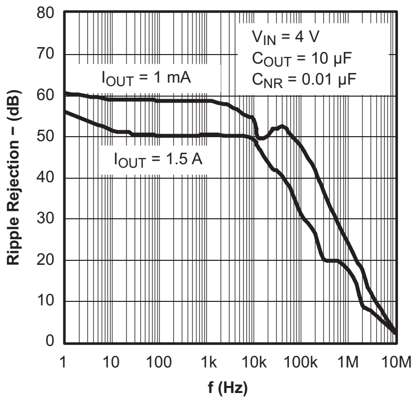
The TPS786 family of low-dropout (LDO) low-power linear voltage regulators features high power-supply rejection ratio (PSRR), ultralow noise, fast start-up, and excellent line and load transient responses in small outline, SOT223-6 and DDPAK-5 packages. Each device in the family is stable, with a small 1-μF ceramic capacitor on the output. The family uses an advanced, proprietary BiCMOS fabrication process to yield extremely low dropout voltages (for example, 390 mV at 1.5 A). Each device achieves fast start-up times (approximately 50 μs with a 0.001-μF bypass capacitor) while consuming very low quiescent current (265 μA, typical). Moreover, when the device is placed in standby mode, the supply current is reduced to less than 1 μA. The TPS78630 exhibits approximately 48 μV_{RMS} of output voltage at 3-V output noise with a 0.1-μF bypass capacitor. Applications with analog components that are noise sensitive, such as portable RF electronics, benefit from the high PSRR, low noise features, and the fast response time.

Device Information(1)

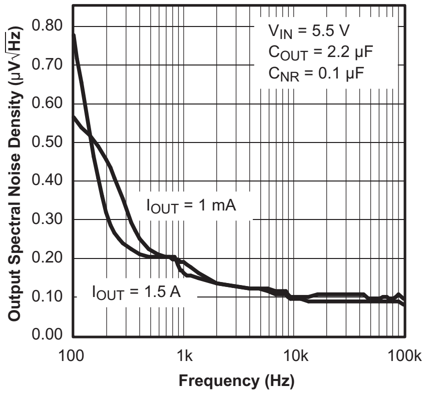
PART NUMBER	PACKAGE	BODY SIZE (NOM)
TPS786	TO-263 (5)	10.16 mm × 8.42 mm
	SOT-223 (6)	6.50 mm × 3.50 mm
	SON (8)	3.00 mm × 3.00 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Ripple Rejection vs Frequency



Output Spectral Noise Density vs Frequency



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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

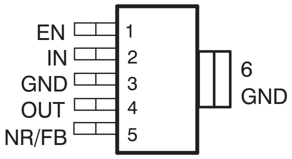
Changes from Revision L (October 2010) to Revision M	Page
• Added *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section	1
• Updated *Thermal Information*	5

Changes from Revision K (August, 2010) to Revision L	Page
• Corrected typo in Figure 34	20

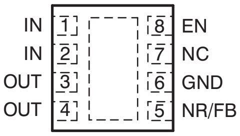
Changes from Revision J (May, 2009) to Revision K	Page
• Replaced the *Dissipation Ratings* table with the *Thermal Information* Table	5
• Revised section	17

5 Pin Configuration and Functions

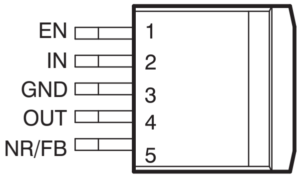
DCQ Package
6-Pin SOT-223
Top View



DRB Package
8-SON
Top View



KTT Package
5-Pin TO-263
Top View



Pin Functions

PIN				I/O	DESCRIPTION
NAME	SOT-223	TO-263	SON		
NR	5	5	5	—	Noise-reduction pin for fixed versions only. An external bypass capacitor, connected to this terminal, in conjunction with an internal resistor, creates a low-pass filter to further reduce regulator noise.
EN	1	1	8	I	The EN terminal is an input that enables or shuts down the device. When EN is a logic high, the device is enabled. When the device is a logic low, the device is in shutdown mode.
FB	5	5	5	I	Feedback input voltage for the adjustable device.
GND	3, 6	3, TAB	6	—	Regulator ground
IN	2	2	1, 2	I	Input supply
OUT	4	4	3, 4	O	Regulator output

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

	MIN	MAX	UNIT
V_{IN}	–0.3	6	V
V_{EN}	–0.3	V_{IN} + 0.3	V
V_{OUT}		6	V
Peak output current	Internally limited		
Continuous total power dissipation	See *Thermal Information*		
Junction temperature, T_J	–40	150	°C
Storage temperature, T_{stg}	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1)	±2000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins(2)	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating junction temperature range (unless otherwise noted)

	MIN	NOM	MAX	UNIT
V_{IN} Input supply voltage	2.7		5.5	V
I_{OUT} Output current	0		1.5	A
T_J Operating junction temperature	–40		125	°C

6.4 Thermal Information

THERMAL METRIC(1)(2)		TPS786(3)			UNIT
		DRB (SON)	DCQ (S0T-223)	KTT (TO-263)	
		8 PINS	6 PINS	5 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	41.1	54.2	40.7	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	49.1	33.3	43.1	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	16.6	8.9	21.5	°C/W
ψ_{JT}	Junction-to-top characterization parameter	0.7	2.6	9.4	°C/W
ψ_{JB}	Junction-to-board characterization parameter	16.8	8.8	20	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	5.2	N/A	2.1	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

(2) For thermal estimates of this device based on PCB copper area, see the TI PCB Thermal Calculator.

(3) Thermal data for the DRB, DCQ, and DRV packages are derived by thermal simulations based on JEDEC-standard methodology as specified in the JESD51 series. The following assumptions are used in the simulations:

- (a) i. DRB: The exposed pad is connected to the PCB ground layer through a 2×2 thermal via array.
  - ii. DCQ: The exposed pad is connected to the PCB ground layer through a 3×2 thermal via array.
  - iii. KTT: The exposed pad is connected to the PCB ground layer through a 5×4 thermal via array.
- (b) i. DRB: The top and bottom copper layers are assumed to have a 20% thermal conductivity of copper representing a 20% copper coverage.
  - ii. DCQ: Each of top and bottom copper layers has a dedicated pattern for 20% copper coverage.
  - iii. KTT: The top and bottom copper layers are assumed to have a 20% thermal conductivity of copper representing a 20% copper coverage.
- (c) These data were generated with only a single device at the center of a JEDEC high-K (2s2p) board with 3 inches × 3 inches copper area. To understand the effects of the copper area on thermal performance, see the *Power Dissipation* and *Estimating Junction Temperature* sections of this data sheet.

6.5 Electrical Characteristics

Over recommended operating temperature range (T_J = –40°C to 125°C), $V_{EN} = V_{IN}$, $V_{IN} = V_{OUT(nom)}$ + 1 V(1), I_{OUT} = 1 mA, C_{OUT} = 10 μF, and C_{NR} = 0.01 μF, unless otherwise noted. Typical values are at 25°C.

PARAMETER			TEST CONDITIONS		MIN	TYP	MAX	UNIT
Input voltage, V_{IN}(1)					2.7		5.5	V
Internal reference, V_{FB} (TPS78601)					1.200	1.225	1.250	V
Continuous output current I_{OUT}					0		1.5	A
Output voltage	Output voltage range	TPS78601			1.225		5.5 – V_{DO}	V
	Accuracy	TPS78601(2)	0 μA ≤ I_{OUT} ≤ 1.5 A, V_{OUT} + 1 V ≤ V_{IN} ≤ 5.5 V(1)		(0.98)V_{OUT}	V_{OUT}	(1.02)V_{OUT}	V
		Fixed V_{OUT} < 5 V	0 μA ≤ I_{OUT} ≤ 1.5 A, V_{OUT} + 1 V ≤ V_{IN} ≤ 5.5 V(1)		–2%		2%	
		Fixed V_{OUT} = 5 V	0 μA ≤ I_{OUT} ≤ 1.5 A, V_{OUT} + 1 V ≤ V_{IN} ≤ 5.5 V(1)		–3%		3%	
Output voltage line regulation ($\Delta V_{OUT}\%/V_{IN}$)(1)			V_{OUT} + 1 V ≤ V_{IN} ≤ 5.5 V			5	12	%/V
Load regulation ($\Delta V_{OUT}\%/V_{OUT}$)			0 μA ≤ I_{OUT} ≤ 1.5 A			7		mV
Dropout voltage(3) $V_{IN} = V_{OUT(nom)}$ – 0.1 V		TPS78628	I_{OUT} = 1.5 A			410	580	mV
		TPS78630	I_{OUT} = 1.5 A			390	550	
		TPS78633	I_{OUT} = 1.5 A			340	510	
		TPS78650	I_{OUT} = 1.5 A			310	470	
Output current limit			V_{OUT} = 0 V		2.4		4.2	A
Ground pin current			0 μA ≤ I_{OUT} ≤ 1.5 A			260	385	μA
Shutdown current(4)			V_{EN} = 0 V, 2.7 V ≤ V_{IN} ≤ 5.5 V			0.07	1	μA
FB pin current			V_{FB} = 1.225 V				1	μA
Power-supply ripple rejection		TPS78630	f = 100 Hz, I_{OUT} = 10 mA			59		dB
			f = 100 Hz, I_{OUT} = 1.5 A			52		
			f = 10 kHz, I_{OUT} = 1.5 A			49		
			f = 100 kHz, I_{OUT} = 1.5 A			32		
Output noise voltage (TPS78630)			BW = 100 Hz to 100 kHz, I_{OUT} = 1.5 A	C_{NR} = 0.001 μF		66		μV_{RMS}
				C_{NR} = 0.0047 μF		51		
				C_{NR} = 0.01 μF		49		
				C_{NR} = 0.1 μF		48		
Time, start-up (TPS78630)			R_L = 2 Ω, C_{OUT} = 1 μF	C_{NR} = 0.001 μF		50		μs
				C_{NR} = 0.0047 μF		75		
				C_{NR} = 0.01 μF		110		
High-level enable input voltage			2.7 V ≤ V_{IN} ≤ 5.5 V		1.7		V_{IN}	V
Low-level enable input voltage			2.7 V ≤ V_{IN} ≤ 5.5 V		0		0.7	V
EN pin current			V_{EN} = 0		–1		1	μA
UVLO threshold			V_{CC} rising		2.25		2.65	V
UVLO hysteresis						100		mV

(1) Minimum $V_{IN} = V_{OUT} + V_{DO}$ or 2.7 V, whichever is greater. The TPS78650 is tested at V_{IN} = 5.5 V.
(2) Tolerance of external resistors not included in this specification.
(3) Dropout is not measured for TPS78618 or TPS78625 because minimum V_{IN} = 2.7 V.
(4) For adjustable version, this applies only after V_{IN} is applied; then V_{EN} transitions high to low.

6.6 Typical Characteristics

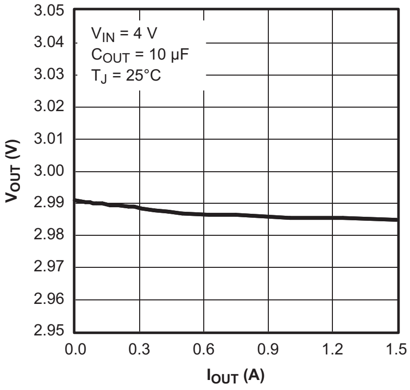


Figure 1. TPS78630 Output Voltage vs Output Current

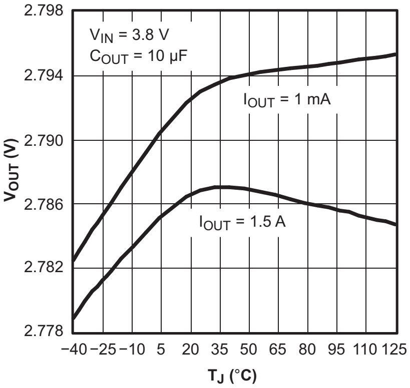


Figure 2. TPS78628 Output Voltage vs Junction Temperature

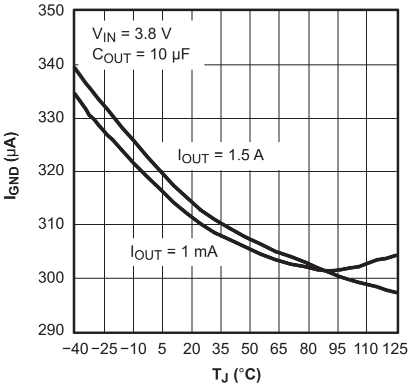


Figure 3. TPS78628 Ground Current vs Junction Temperature

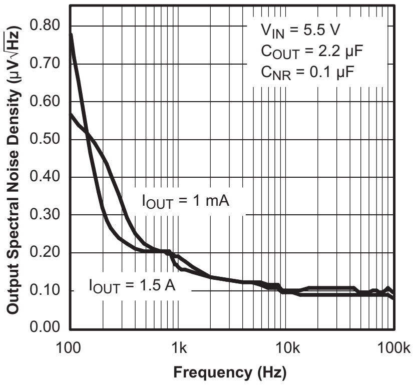


Figure 4. TPS78630 Output Spectral Noise Density vs Frequency

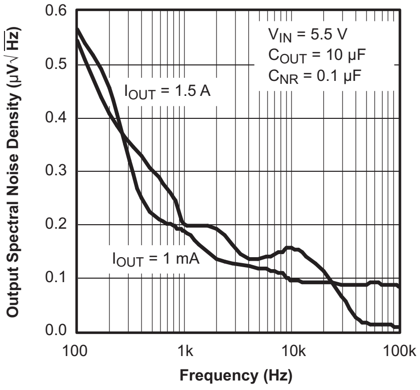


Figure 5. TPS78630 Output Spectral Noise Density vs Frequency

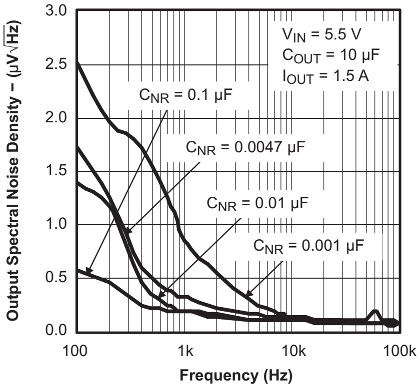


Figure 6. TPS78630 Output Spectral Noise Density vs Frequency

Typical Characteristics (continued)

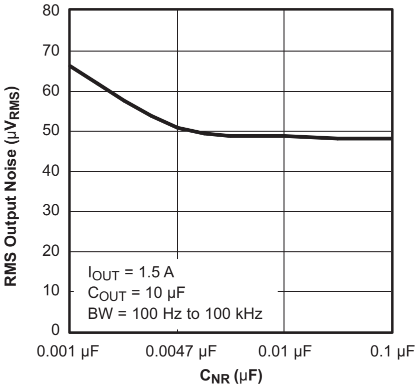


Figure 7. TPS78630 Root Mean Squared Output Noise vs Bypass Capacitance

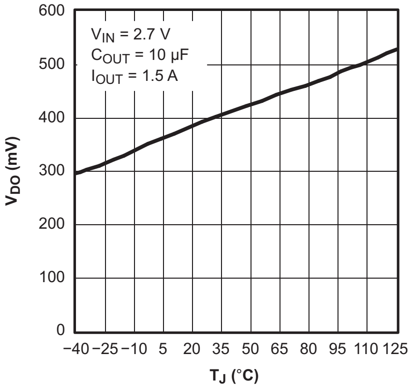


Figure 8. TPS78628 Dropout Voltage vs Junction Temperature

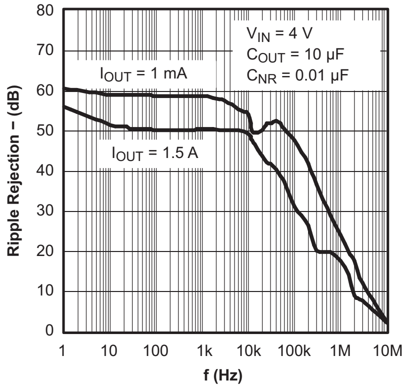


Figure 9. TPS78630 Ripple Rejection vs Frequency

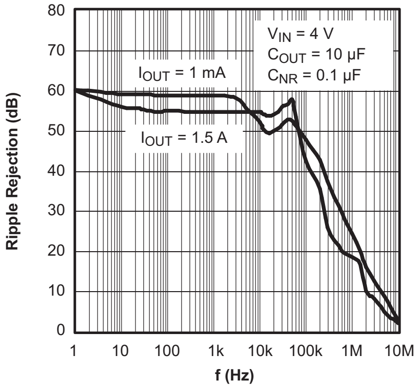


Figure 10. TPS78630 Ripple Rejection vs Frequency

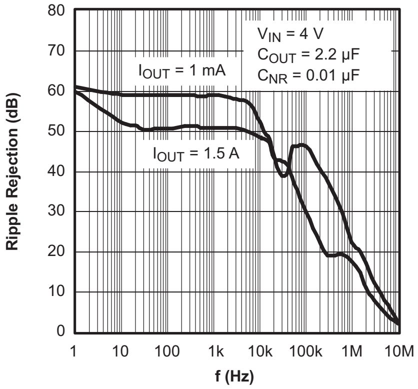


Figure 11. TPS78630 Ripple Rejection vs Frequency

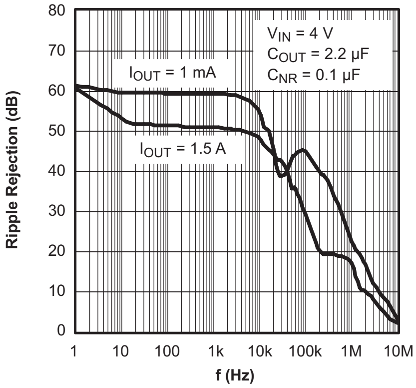


Figure 12. TPS78630 Ripple Rejection vs Frequency

Typical Characteristics (continued)

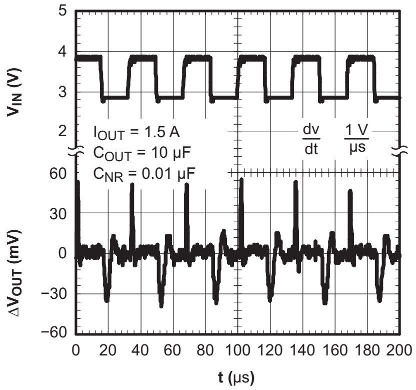


Figure 13. TPS78618 Line Transient Response

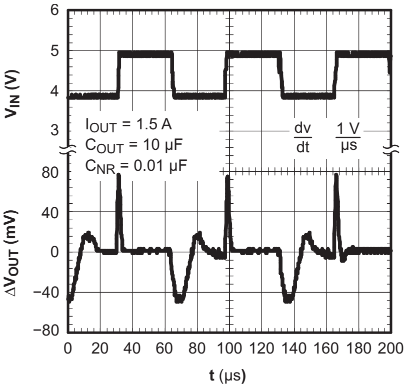


Figure 14. TPS78630 Line Transient Response

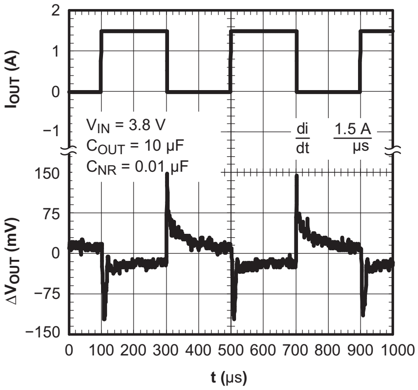


Figure 15. TPS78628 Load Transient Response

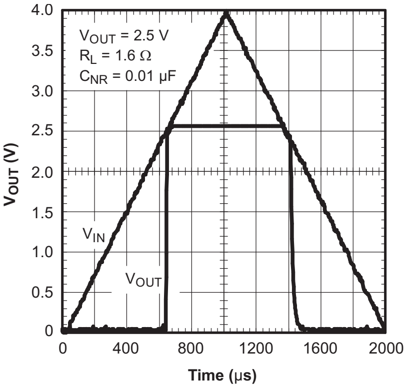


Figure 16. TPS78625 Power Up and Power Down

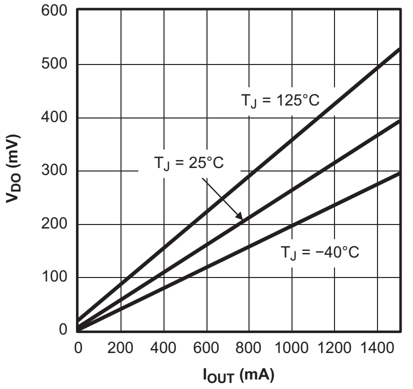


Figure 17. TPS78630 Dropout Voltage vs Output Current

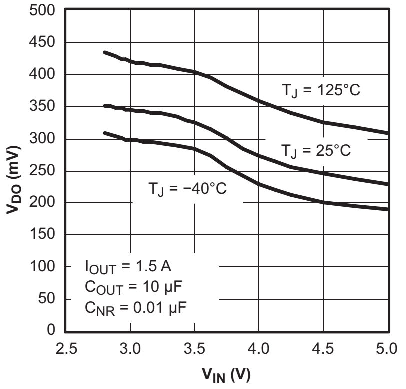


Figure 18. TPS78601 Dropout Voltage vs Input Voltage

Typical Characteristics (continued)

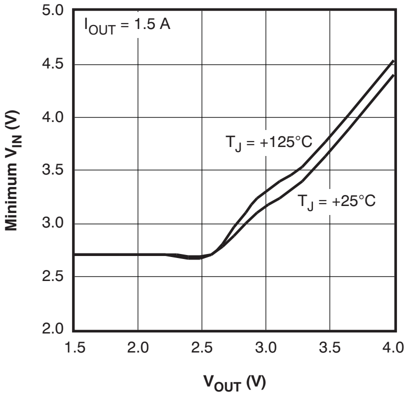


Figure 19. Minimum Required Input Voltage vs Output Voltage

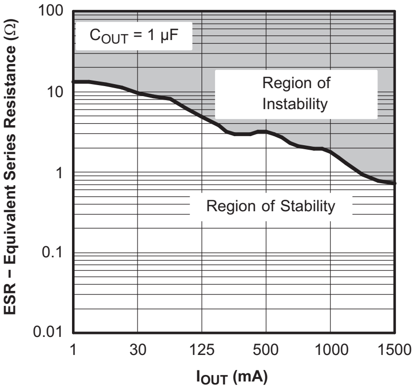


Figure 20. TPS78630 Typical Regions of Stability Equivalent Series Resistance (ESR) vs Output Current

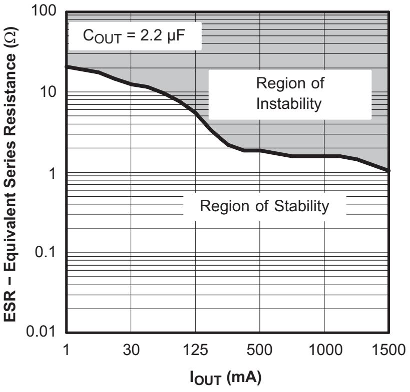


Figure 21. TPS78630 Typical Regions of Stability Equivalent Series Resistance (ESR) vs Output Current

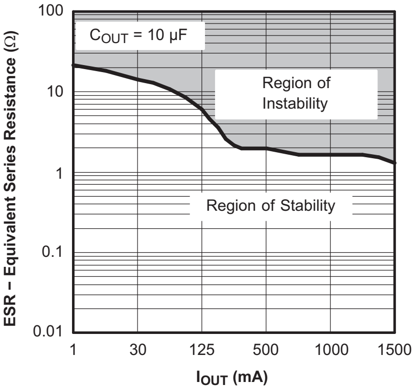


Figure 22. TPS78630 Typical Regions of Stability Equivalent Series Resistance (ESR) vs Output Current

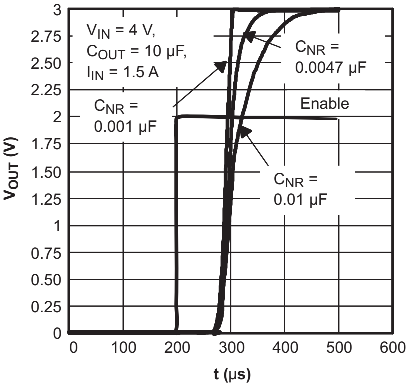


Figure 23. Start-Up

7 Detailed Description

7.1 Overview

The TPS786 family of low-dropout regulators offers low dropout voltages, high PSRR, and low-output noise.

7.2 Functional Block Diagrams

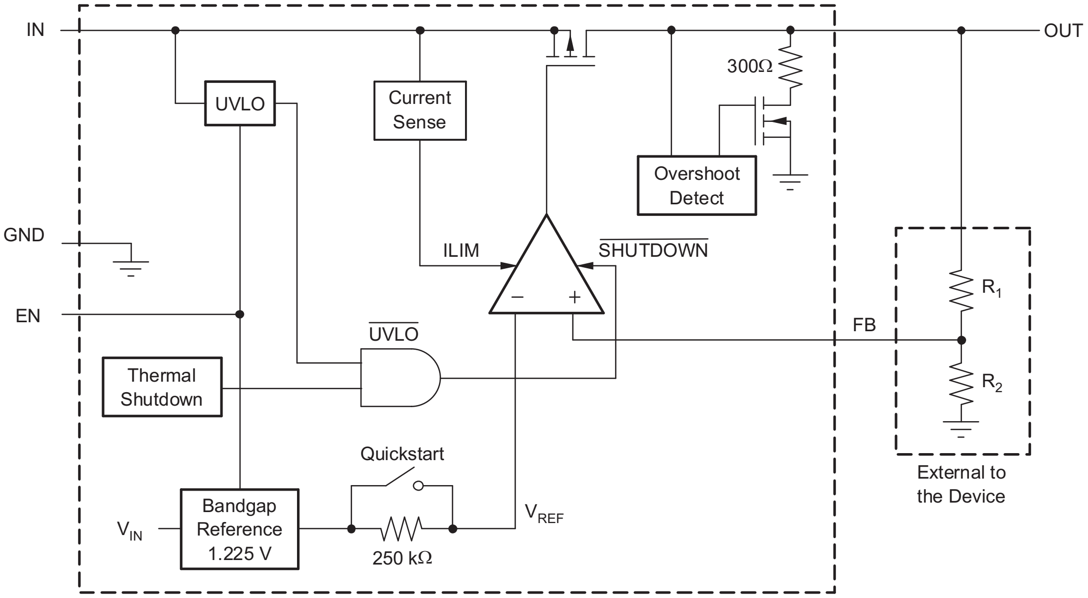


Figure 24. Functional Block Diagram—Adjustable Version

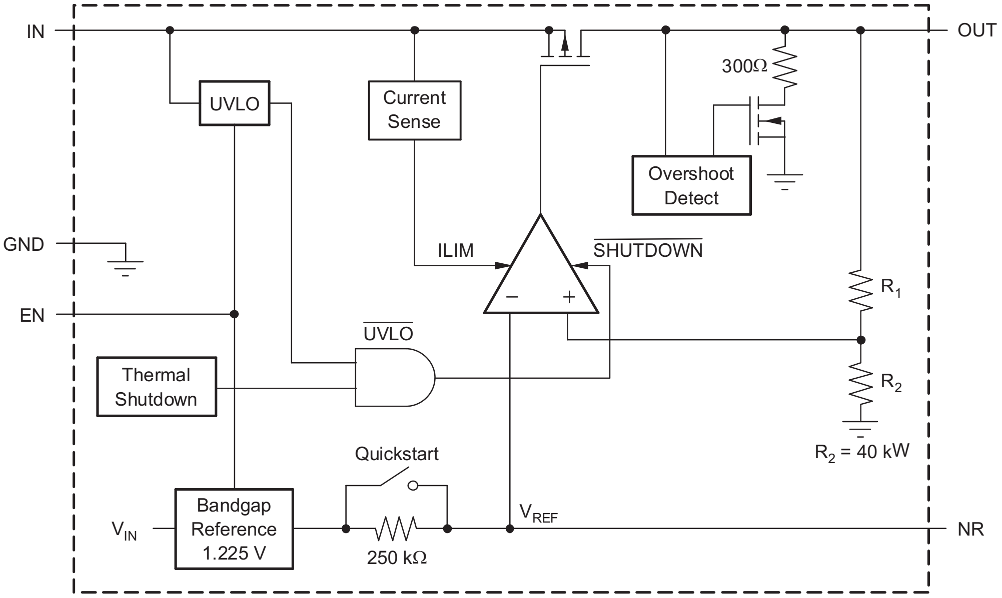


Figure 25. Functional Block Diagram—Fixed Version

7.3 Feature Description

7.3.1 Regulator Protection

The TPS786 PMOS-pass transistor has a built-in back diode that conducts reverse current when the input voltage drops below the output voltage (for example, during power down). Current is conducted from the output to the input and is not internally limited. If extended reverse voltage operation is anticipated, external limiting might be appropriate.

The TPS786 features internal current limiting and thermal protection. During normal operation, the TPS786 limits output current to approximately 2.8 A. When current limiting engages, the output voltage scales back linearly until the overcurrent condition ends. While current limiting is designed to prevent gross device failure, take care not to exceed the power dissipation ratings of the package. If the temperature of the device exceeds approximately 165°C, thermal-protection circuitry shuts it down. Once the device has cooled down to below approximately 140°C, regulator operation resumes.

7.4 Device Functional Modes

Driving EN over 1.7 V turns on the regulator. Driving EN below 0.7 V puts the regulator into shutdown mode, thus reducing the operating current to 70 nA, nominal.

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The TPS786 family of low-dropout (LDO) regulators has been optimized for use in noise-sensitive equipment. The device features extremely low dropout voltages, high PSRR, ultralow-output noise, low quiescent current (265 μA, typically), and enable input to reduce supply currents to less than 1 μA when the regulator is turned off.

8.1.1 Programming the TPS78601 Adjustable LDO Regulator

The output voltage of the TPS78601 adjustable regulator is programmed using an external resistor divider as shown in Figure 26. The output voltage is calculated using Equation 1:

$$V_{OUT} = V_{REF} \times \left(1 + \frac{R_1}{R_2}\right)$$

where

- V_{REF} = 1.2246 V typical (the internal reference voltage) (1)

Resistors R_1 and R_2 should be chosen for approximately 40-μA divider current. Lower value resistors can be used for improved noise performance, but the device wastes more power. Higher values should be avoided, as leakage current at FB increases the output voltage error.

The recommended design procedure is to choose R_2 = 30.1 kΩ to set the divider current at 40 μA, C_1 = 15 pF for stability, and then calculate R_1 using Equation 2.

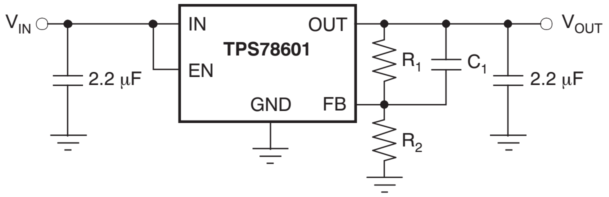
$$R_1 = \left(\frac{V_{OUT}}{V_{REF}} - 1\right) \times R_2 \qquad (2)$$

To improve the stability of the adjustable version, TI suggests placing a small compensation capacitor between OUT and FB.

The approximate value of this capacitor can be calculated using Equation 3:

$$C_1 = \frac{(3 \times 10^{-7}) \times (R_1 + R_2)}{(R_1 \times R_2)} \qquad (3)$$

The suggested value of this capacitor for several resistor ratios is shown in Figure 26. If this capacitor is not used (such as in a unity-gain configuration), then the minimum recommended output capacitor is 2.2 μF instead of 1 μF.



OUTPUT VOLTAGE PROGRAMMING GUIDE

OUTPUT VOLTAGE	R_1	R_2	C_1
1.8 V	14.0 kΩ	30.1 kΩ	33 pF
3.6 V	57.9 kΩ	30.1 kΩ	15 pF

Figure 26. TPS78601 Adjustable LDO Regulator Programming

8.2 Typical Application

A typical application circuit is shown in Figure 27.

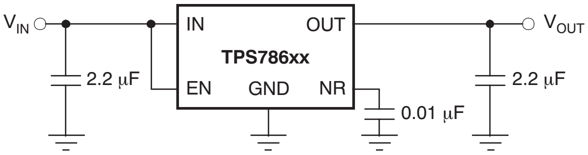


Figure 27. Typical Application Circuit

8.2.1 Design Requirements

Table 1 shows the design parameters for this application.

Table 1. Design Parameters

DESIGN PARAMETERS	EXAMPLE VALUE
V_{IN} (from DCDC)	Minimum = 4 V Maximum = 5.5 V
V_{OUT}	3 V ± –1%
I_{OUT}	Minimum = 1 mA Maximum = 1.5 A
PSRR at 1K	>50 db
Noise at 1K	<20 µV/√Hz

8.2.2 Detailed Design Procedure

Select TPS78630 to satisfy the V_{OUT} requirements. The fixed version of the device is chosen to save board space and reduce BOM cost.

Use a 2.2-uF capacitor on both the input and output to satisfy the capacitor requirements. Select a 0.1-uF NR capacitor to satisfy the noise requirement.

8.2.2.1 External Capacitor Requirements

A 2.2-µF or larger ceramic input bypass capacitor, connected between IN and GND and located close to the TPS786, is required for stability and improves transient response, noise rejection, and ripple rejection. A higher-value input capacitor may be necessary if large, fast-rise-time load transients are anticipated and the device is located several inches from the power source.

Like most low-dropout regulators, the TPS786 requires an output capacitor connected between OUT and GND to stabilize the internal control loop. The minimum recommended capacitor is 1 µF. Any 1-µF or larger ceramic capacitor is suitable.

The internal voltage reference is a key source of noise in an LDO regulator. The TPS786 has an NR pin that is connected to the voltage reference through a 250-kΩ internal resistor. The 250-kΩ internal resistor, in conjunction with an external bypass capacitor connected to the NR pin, creates a low pass filter to reduce the voltage reference noise and, therefore, the noise at the regulator output. For the regulator to operate properly, the current flow out of the NR pin must be at a minimum, because any leakage current creates an IR drop across the internal resistor, thus creating an output error. Therefore, the bypass capacitor must have minimal leakage current. The bypass capacitor should be no more than 0.1-µF to ensure that it is fully charged during the quickstart time provided by the internal switch shown in *Functional Block Diagrams*.

For example, the TPS78630 exhibits only 48 μV_{RMS} of output voltage noise using a 0.1-µF ceramic bypass capacitor and a 10-µF ceramic output capacitor. The output starts up slower as the bypass capacitance increases due to the RC time constant at the bypass pin that is created by the internal 250-kΩ resistor and external capacitor.

8.2.3 Application Curves

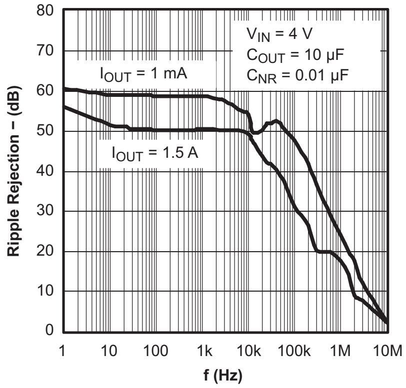


Figure 28. Ripple Rejection vs Frequency

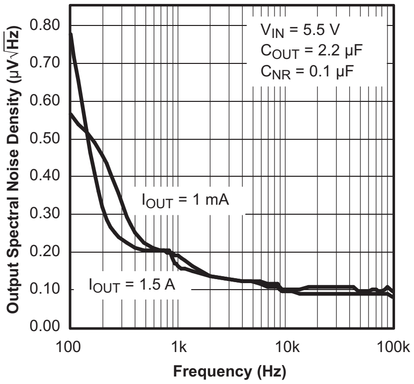


Figure 29. Output Spectral Noise Density vs Frequency

9 Power Supply Recommendations

These devices are designed to operate from an input voltage supply range from 2.7 V to 5.5 V. The input voltage range provides adequate headroom for the device to have a regulated output. This input supply is well-regulated and stable. If the input supply is noisy, additional input capacitors with low ESR can help improve the output noise performance.

10 Layout

10.1 Layout Guidelines

To improve AC measurements like PSRR, output noise, and transient response, TI recommends designing the board with separate ground planes for V_{IN} and V_{OUT}, with each ground plane connected only at the ground pin of the device. In addition, the ground connection for the bypass capacitor should connect directly to the ground pin of the device.

10.2 Layout Examples

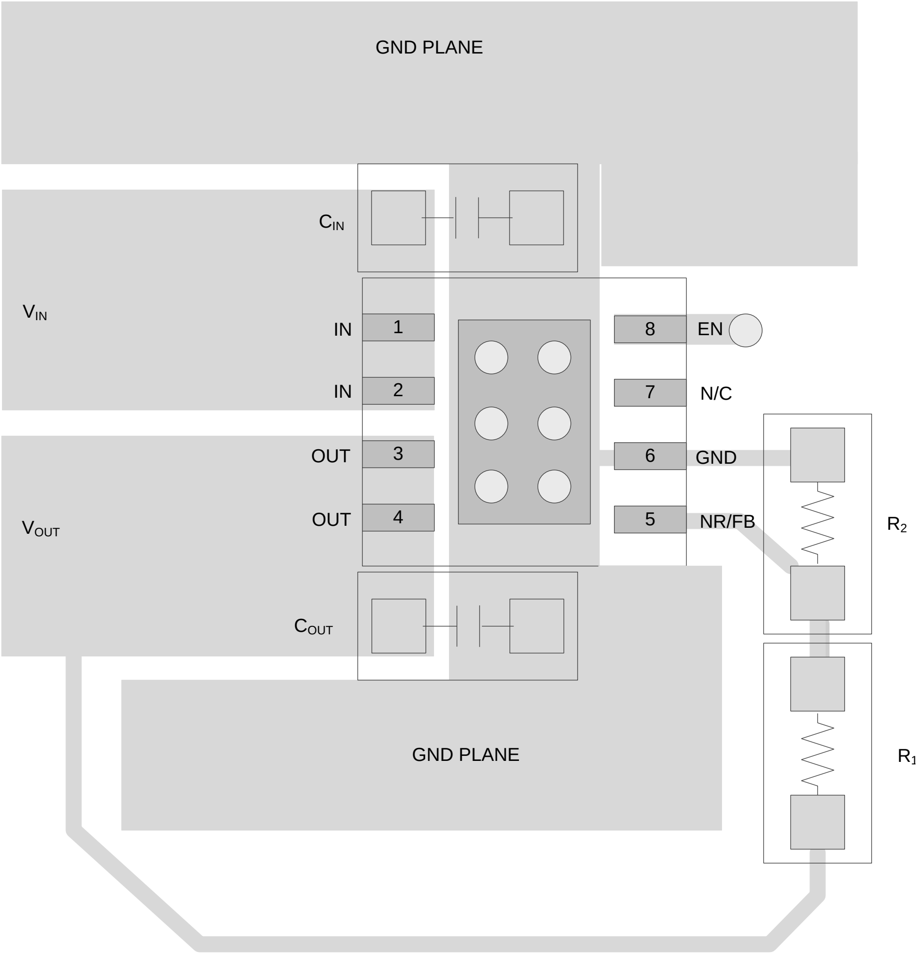


Figure 30. Recommended Layout – Adjustable-Voltage Version

Layout Examples (continued)

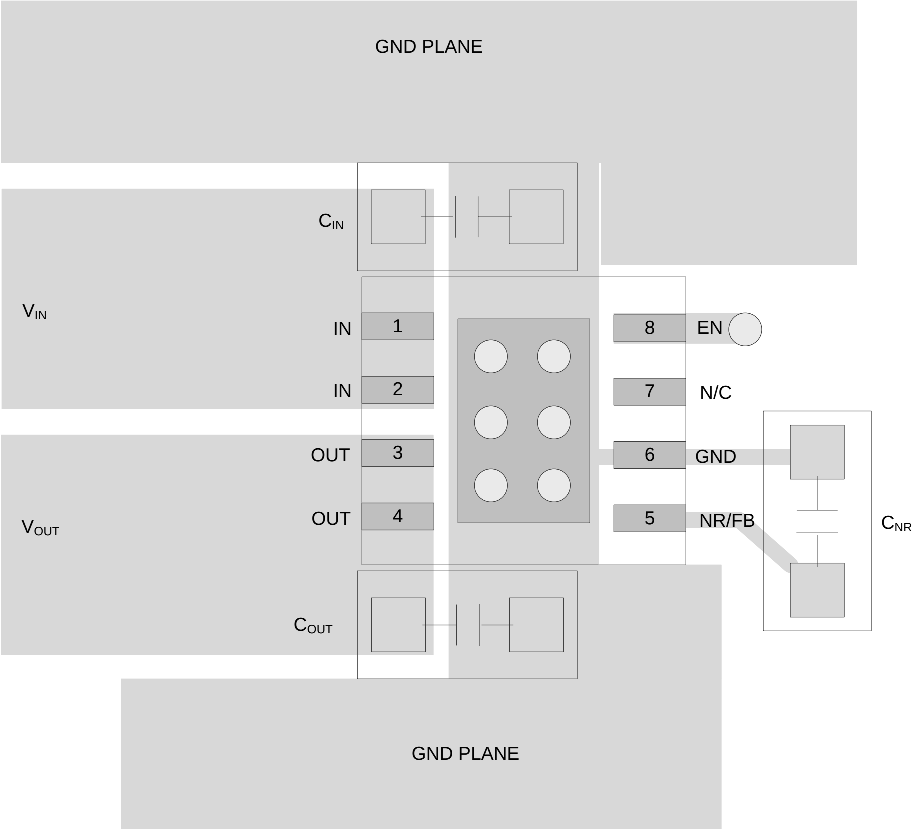


Figure 31. Recommended Layout – Fixed-Voltage Version

10.3 Regulator Mounting

The tab of the SOT223-6 package is electrically connected to ground. For best thermal performance, the tab of the surface-mount version should be soldered directly to a circuit-board copper area. Increasing the copper area improves heat dissipation.

Solder pad footprint recommendations for the devices are presented in Application Report SBFA015, *Solder Pad Recommendations for Surface-Mount Devices*, available from the TI website at www.ti.com.

10.4 Power Dissipation

Knowing the device power dissipation and proper sizing of the thermal plane that is connected to the tab or pad is critical to avoiding thermal shutdown and ensuring reliable operation.

Power dissipation of the device depends on input voltage and load conditions and can be calculated using Equation 4:

$$P_D = (V_{IN} - V_{OUT}) \times I_{OUT} \tag{4}$$

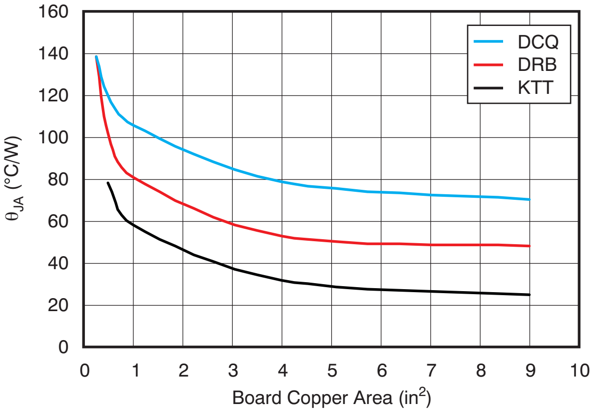
Power dissipation can be minimized and greater efficiency can be achieved by using the lowest possible input voltage necessary to achieve the required output voltage regulation.

Power Dissipation (continued)

On the SON (DRB) package, the primary conduction path for heat is through the exposed pad to the printed-circuit-board (PCB). The pad can be connected to ground or be left floating; however, it should be attached to an appropriate amount of copper PCB area to ensure the device does not overheat. On both SOT-223 (DCQ) and DDPAK (KTT) packages, the primary conduction path for heat is through the tab to the PCB. That tab should be connected to ground. The maximum junction-to-ambient thermal resistance depends on the maximum ambient temperature, maximum device junction temperature, and power dissipation of the device and can be calculated using Equation 5:

$$R_{\theta JA} = \frac{(+125°C - T_A)}{P_D} \tag{5}$$

Knowing the maximum $R_{\theta JA}$, the minimum amount of PCB copper area needed for appropriate heatsinking can be estimated using Figure 32.



Note: θ_{JA} value at board size of 9in^2 (that is, 3in × 3in) is a JEDEC standard.

Figure 32. θ_{JA} vs Board Size

Figure 32 shows the variation of θ_{JA} as a function of ground plane copper area in the board. It is intended only as a guideline to demonstrate the effects of heat spreading in the ground plane and should not be used to estimate actual thermal performance in real application environments.

NOTE

When the device is mounted on an application PCB, TI strongly recommends using Ψ_{JT} and Ψ_{JB}, as explained in the section.

10.4.1 Estimating Junction Temperature

Using the thermal metrics Ψ_{JT} and Ψ_{JB}, as shown in the *Thermal Information* table, the junction temperature can be estimated with corresponding formulas (given in Equation 6). For backwards compatibility, an older θ_{JC},*Top* parameter is listed as well.

Ψ_{JT}: $T_J = T_T + \Psi_{JT} \bullet P_D$

Ψ_{JB}: $T_J = T_B + \Psi_{JB} \bullet P_D$

where

- P_D is the power dissipation shown by Equation 5.
- T_T is the temperature at the center-top of the IC package.
- T_B is the PCB temperature measured 1mm away from the IC package *on the PCB surface* (as Figure 34 shows). (6)

Power Dissipation (continued)

NOTE

Both T_T and T_B can be measured on actual application boards using a thermo-gun (an infrared thermometer).

For more information about measuring T_T and T_B, see the application note SBVA025, *Using New Thermal Metrics*, available for download at www.ti.com.

By looking at Figure 33, the new thermal metrics (Ψ_{JT} and Ψ_{JB}) have very little dependency on board size. That is, using Ψ_{JT} or Ψ_{JB} with Equation 6 is a good way to estimate T_J by simply measuring T_T or T_B, regardless of the application board size.

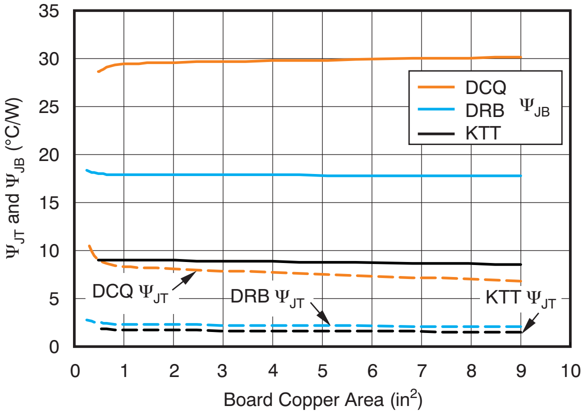
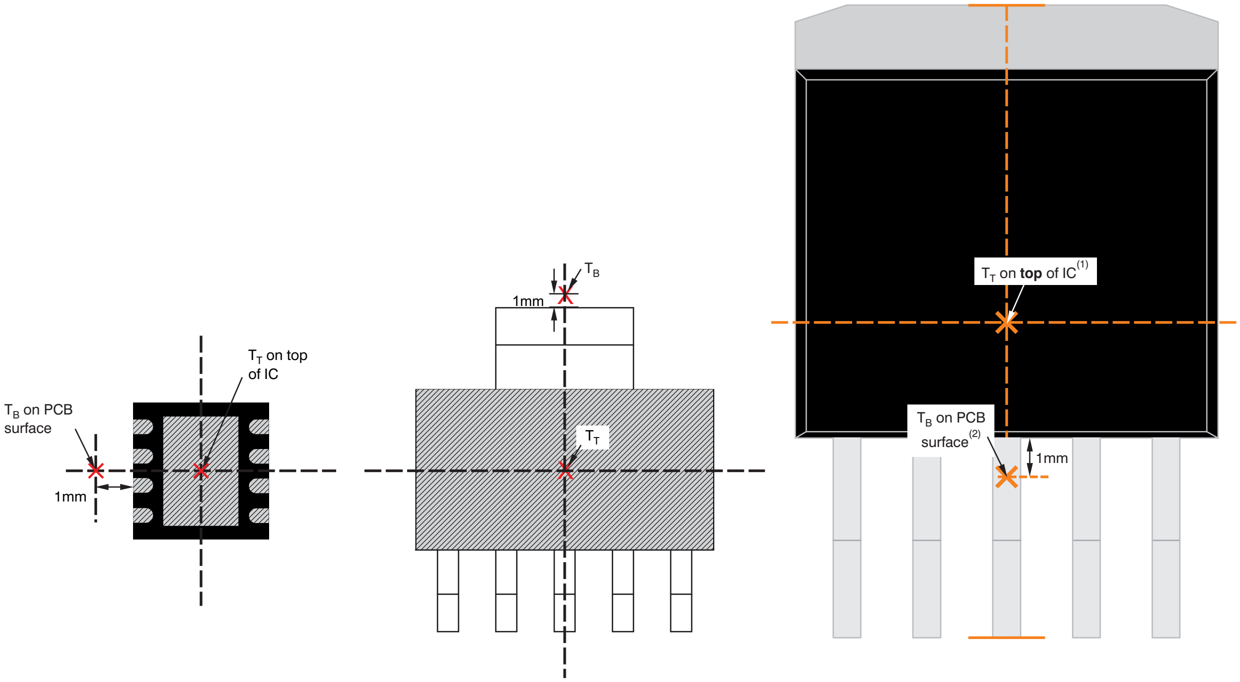


Figure 33. Ψ_{JT} and Ψ_{JB} vs Board Size

For a more detailed discussion of why TI does not recommend using $\theta_{JC(top)}$ to determine thermal characteristics, see application report *Using New Thermal Metrics*, SBVA025, available for download at www.ti.com. For further information, see application report *IC Package Thermal Metrics*, SPRA953, also available on the TI website.



(a) Example DRB (VSON) Package Measurement (b) Example DCQ (SOT-223) Package Measurement (c) Example KTT (TO-263) Package Measurement

(1) T_T is measured at the center of both the X- and Y-dimensional axes.

(2) T_B is measured ***below*** the package lead on the PCB surface.

Figure 34. Measuring Points for T_T and T_B

11 Device and Documentation Support

11.1 Device Support

11.1.1 Development Support

11.1.1.1 Evaluation Modules

An evaluation module (EVM) is available to assist in the initial circuit performance evaluation using the TPS786. This EVM, TPS78601DRBEVM Single Output LDO, can be requested at the Texas Instruments website through the product folders or purchased directly from the TI eStore.

11.1.1.2 Spice Models

Computer simulation of circuit performance using SPICE is often useful when analyzing the performance of analog circuits and systems. A SPICE model for the TPS786 devices are available through the product folders under simulation models.

11.1.2 Device Nomenclature

Table 2. Ordering Information

PRODUCT	V_{OUT} [1]
TPS786**xx*yyy***_z_	**XX** is nominal output voltage (for example, 28 = 2.8 V, 285 = 2.85 V, 01 = Adjustable). **YYY** is package designator. **Z** is package quantity.

[1] Output voltages from 1.3 V to 5.0 V in 100-mV increments are available; minimum order quantities may apply. Contact factory for details and availability.

11.2 Documentation Support

11.2.1 Related Documentation

For related documentation see the following:

- *Using New Thermal Metrics*, SBVA025.
- *Semiconductor and IC Package Thermal Metrics*, SPRA953.
- *Solder Pad Recommendations for Surface-Mount Devices*, SBFA015.

11.3 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

11.4 Trademarks

E2E is a trademark of Texas Instruments.
PowerPAD is a trademark of Texas Instruments Inc.
Bluetooth is a registered trademark of Bluetooth SIG, Inc.
All other trademarks are the property of their respective owners.

11.5 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

11.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS78601DCQ	ACTIVE	SOT-223	DCQ	6	78	Green (RoHS & no Sb/Br)	CU SN	Level-2-260C-1 YEAR	-40 to 125	PS78601	Samples
TPS78601DCQG4	ACTIVE	SOT-223	DCQ	6		TBD	Call TI	Call TI	-40 to 125		Samples
TPS78601DCQR	ACTIVE	SOT-223	DCQ	6	2500	Green (RoHS & no Sb/Br)	CU SN	Level-2-260C-1 YEAR	-40 to 125	PS78601	Samples
TPS78601DCQRG4	ACTIVE	SOT-223	DCQ	6	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	PS78601	Samples
TPS78601DRBR	ACTIVE	SON	DRB	8	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	OCI	Samples
TPS78601DRBT	ACTIVE	SON	DRB	8	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	OCI	Samples
TPS78601KTT	OBSOLETE	DDPAK/ TO-263	KTT	5		TBD	Call TI	Call TI	-40 to 125		
TPS78601KTTR	ACTIVE	DDPAK/ TO-263	KTT	5	500	Green (RoHS & no Sb/Br)	CU SN	Level-2-260C-1 YEAR		TPS 78601	Samples
TPS78601KTTRG3	ACTIVE	DDPAK/ TO-263	KTT	5	500	Green (RoHS & no Sb/Br)	CU SN	Level-2-260C-1 YEAR		TPS 78601	Samples
TPS78601KTTT	ACTIVE	DDPAK/ TO-263	KTT	5	50	Green (RoHS & no Sb/Br)	CU SN	Level-2-260C-1 YEAR	-40 to 125	TPS 78601	Samples
TPS78601KTTTG3	ACTIVE	DDPAK/ TO-263	KTT	5	50	Green (RoHS & no Sb/Br)	CU SN	Level-2-260C-1 YEAR	-40 to 125	TPS 78601	Samples
TPS78618DCQ	ACTIVE	SOT-223	DCQ	6	78	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	PS78618	Samples
TPS78618DCQR	ACTIVE	SOT-223	DCQ	6	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	PS78618	Samples
TPS78618DCQRG4	ACTIVE	SOT-223	DCQ	6	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	PS78618	Samples
TPS78618KTT	OBSOLETE	DDPAK/ TO-263	KTT	5		TBD	Call TI	Call TI	-40 to 125		
TPS78618KTTR	ACTIVE	DDPAK/ TO-263	KTT	5	500	Green (RoHS & no Sb/Br)	CU SN	Level-2-260C-1 YEAR		TPS 78618	Samples
TPS78618KTTRE3	ACTIVE	DDPAK/ TO-263	KTT	5	500	Green (RoHS & no Sb/Br)	CU SN	Level-2-260C-1 YEAR		TPS 78618	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS78618KTTRG3	ACTIVE	DDPAK/TO-263	KTT	5	500	Green (RoHS & no Sb/Br)	CU SN	Level-2-260C-1 YEAR		TPS 78618	Samples
TPS78618KTTT	ACTIVE	DDPAK/TO-263	KTT	5	50	Green (RoHS & no Sb/Br)	CU SN	Level-2-260C-1 YEAR	-40 to 125	TPS 78618	Samples
TPS78618KTTTG3	ACTIVE	DDPAK/TO-263	KTT	5	50	Green (RoHS & no Sb/Br)	CU SN	Level-2-260C-1 YEAR	-40 to 125	TPS 78618	Samples
TPS78625DCQ	ACTIVE	SOT-223	DCQ	6	78	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	PS78625	Samples
TPS78625DCQG4	ACTIVE	SOT-223	DCQ	6	78	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	PS78625	Samples
TPS78625DCQR	ACTIVE	SOT-223	DCQ	6	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	PS78625	Samples
TPS78625DCQRG4	ACTIVE	SOT-223	DCQ	6	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	PS78625	Samples
TPS78625KTT	OBSOLETE	DDPAK/TO-263	KTT	5		TBD	Call TI	Call TI	-40 to 125		
TPS78625KTTR	ACTIVE	DDPAK/TO-263	KTT	5	500	Green (RoHS & no Sb/Br)	CU SN	Level-2-260C-1 YEAR		TPS 78625	Samples
TPS78625KTTT	ACTIVE	DDPAK/TO-263	KTT	5	50	Green (RoHS & no Sb/Br)	CU SN	Level-2-260C-1 YEAR	-40 to 125	TPS 78625	Samples
TPS78625KTTTG3	ACTIVE	DDPAK/TO-263	KTT	5	50	Green (RoHS & no Sb/Br)	CU SN	Level-2-260C-1 YEAR	-40 to 125	TPS 78625	Samples
TPS78628DCQR	ACTIVE	SOT-223	DCQ	6	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	PS78628	Samples
TPS78628KTT	OBSOLETE	DDPAK/TO-263	KTT	5		TBD	Call TI	Call TI	-40 to 125		
TPS78628KTTT	ACTIVE	DDPAK/TO-263	KTT	5	50	Green (RoHS & no Sb/Br)	CU SN	Level-2-260C-1 YEAR	-40 to 125	TPS 78628	Samples
TPS78630DCQ	ACTIVE	SOT-223	DCQ	6	78	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	PS78630	Samples
TPS78630DCQR	ACTIVE	SOT-223	DCQ	6	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	PS78630	Samples
TPS78630KTT	OBSOLETE	DDPAK/TO-263	KTT	5		TBD	Call TI	Call TI	-40 to 125		
TPS78630KTTT	ACTIVE	DDPAK/TO-263	KTT	5	50	Green (RoHS & no Sb/Br)	CU SN	Level-2-260C-1 YEAR	-40 to 125	TPS 78630	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS78630KTTTG3	ACTIVE	DDPAK/ TO-263	KTT	5	50	Green (RoHS & no Sb/Br)	CU SN	Level-2-260C-1 YEAR	-40 to 125	TPS 78630	Samples
TPS78633DCQ	ACTIVE	SOT-223	DCQ	6	78	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	PS78633	Samples
TPS78633DCQG4	ACTIVE	SOT-223	DCQ	6	78	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	PS78633	Samples
TPS78633DCQR	ACTIVE	SOT-223	DCQ	6	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	PS78633	Samples
TPS78633DCQRG4	ACTIVE	SOT-223	DCQ	6	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	PS78633	Samples
TPS78633KTT	OBSOLETE	DDPAK/ TO-263	KTT	5		TBD	Call TI	Call TI	-40 to 125		
TPS78633KTTR	ACTIVE	DDPAK/ TO-263	KTT	5	500	Green (RoHS & no Sb/Br)	CU SN	Level-2-260C-1 YEAR		TPS 78633	Samples
TPS78633KTTRE3	ACTIVE	DDPAK/ TO-263	KTT	5	500	Green (RoHS & no Sb/Br)	CU SN	Level-2-260C-1 YEAR		TPS 78633	Samples
TPS78633KTTRG3	ACTIVE	DDPAK/ TO-263	KTT	5	500	Green (RoHS & no Sb/Br)	CU SN	Level-2-260C-1 YEAR		TPS 78633	Samples
TPS78633KTTT	ACTIVE	DDPAK/ TO-263	KTT	5	50	Green (RoHS & no Sb/Br)	CU SN	Level-2-260C-1 YEAR	-40 to 125	TPS 78633	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

[3] MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

[4] There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

[5] Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

[6] Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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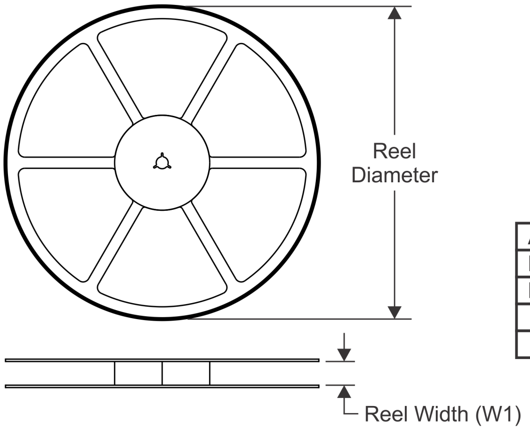
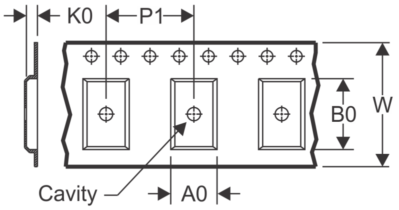
TAPE AND REEL INFORMATION

REEL DIMENSIONS

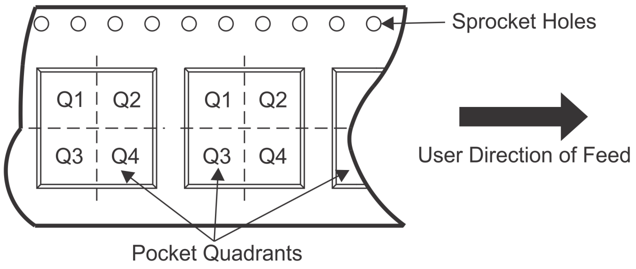


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

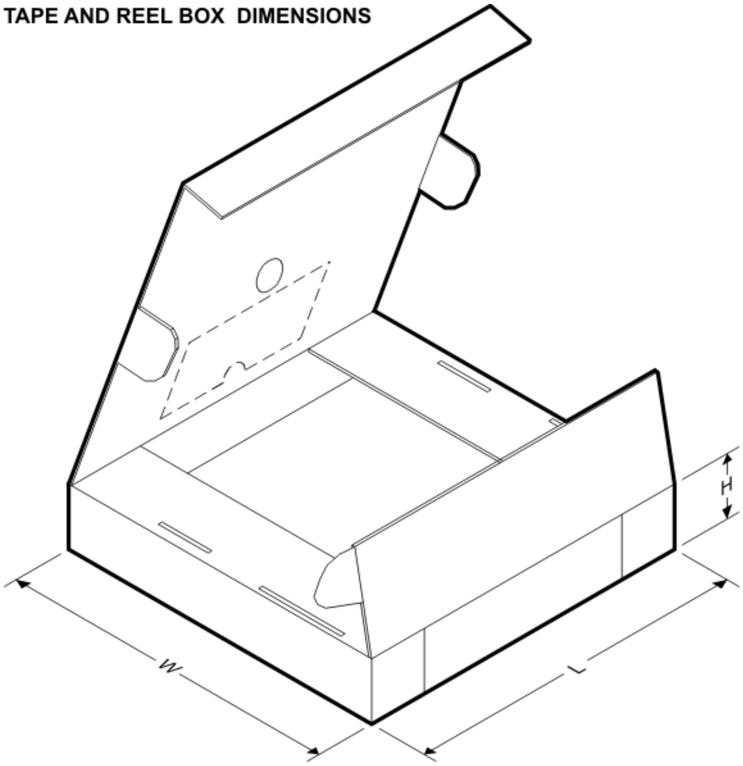


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS78601DCQR	SOT-223	DCQ	6	2500	330.0	12.4	7.1	7.45	1.88	8.0	12.0	Q3
TPS78601DCQRG4	SOT-223	DCQ	6	2500	330.0	12.4	7.1	7.45	1.88	8.0	12.0	Q3
TPS78601DRBR	SON	DRB	8	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TPS78601DRBT	SON	DRB	8	250	180.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TPS78601KTTR	DDPAK/ TO-263	KTT	5	500	330.0	24.4	10.6	15.6	4.9	16.0	24.0	Q2
TPS78601KTTT	DDPAK/ TO-263	KTT	5	50	330.0	24.4	10.6	15.6	4.9	16.0	24.0	Q2
TPS78618DCQR	SOT-223	DCQ	6	2500	330.0	12.4	7.1	7.45	1.88	8.0	12.0	Q3
TPS78618KTTR	DDPAK/ TO-263	KTT	5	500	330.0	24.4	10.6	15.6	4.9	16.0	24.0	Q2
TPS78618KTTRE3	DDPAK/ TO-263	KTT	5	500	330.0	24.4	10.6	15.6	4.9	16.0	24.0	Q2
TPS78618KTTT	DDPAK/ TO-263	KTT	5	50	330.0	24.4	10.6	15.6	4.9	16.0	24.0	Q2
TPS78625DCQR	SOT-223	DCQ	6	2500	330.0	12.4	7.1	7.45	1.88	8.0	12.0	Q3
TPS78625KTTR	DDPAK/ TO-263	KTT	5	500	330.0	24.4	10.6	15.6	4.9	16.0	24.0	Q2
TPS78625KTTT	DDPAK/ TO-263	KTT	5	50	330.0	24.4	10.6	15.6	4.9	16.0	24.0	Q2

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS78628DCQR	SOT-223	DCQ	6	2500	330.0	12.4	7.1	7.45	1.88	8.0	12.0	Q3
TPS78628KTTT	DDPAK/ TO-263	KTT	5	50	330.0	24.4	10.6	15.6	4.9	16.0	24.0	Q2
TPS78630DCQR	SOT-223	DCQ	6	2500	330.0	12.4	7.1	7.45	1.88	8.0	12.0	Q3
TPS78630KTTT	DDPAK/ TO-263	KTT	5	50	330.0	24.4	10.6	15.6	4.9	16.0	24.0	Q2
TPS78633DCQR	SOT-223	DCQ	6	2500	330.0	12.4	7.1	7.45	1.88	8.0	12.0	Q3
TPS78633KTTR	DDPAK/ TO-263	KTT	5	500	330.0	24.4	10.6	15.6	4.9	16.0	24.0	Q2
TPS78633KTTRE3	DDPAK/ TO-263	KTT	5	500	330.0	24.4	10.6	15.6	4.9	16.0	24.0	Q2
TPS78633KTTT	DDPAK/ TO-263	KTT	5	50	330.0	24.4	10.6	15.6	4.9	16.0	24.0	Q2

TAPE AND REEL BOX DIMENSIONS

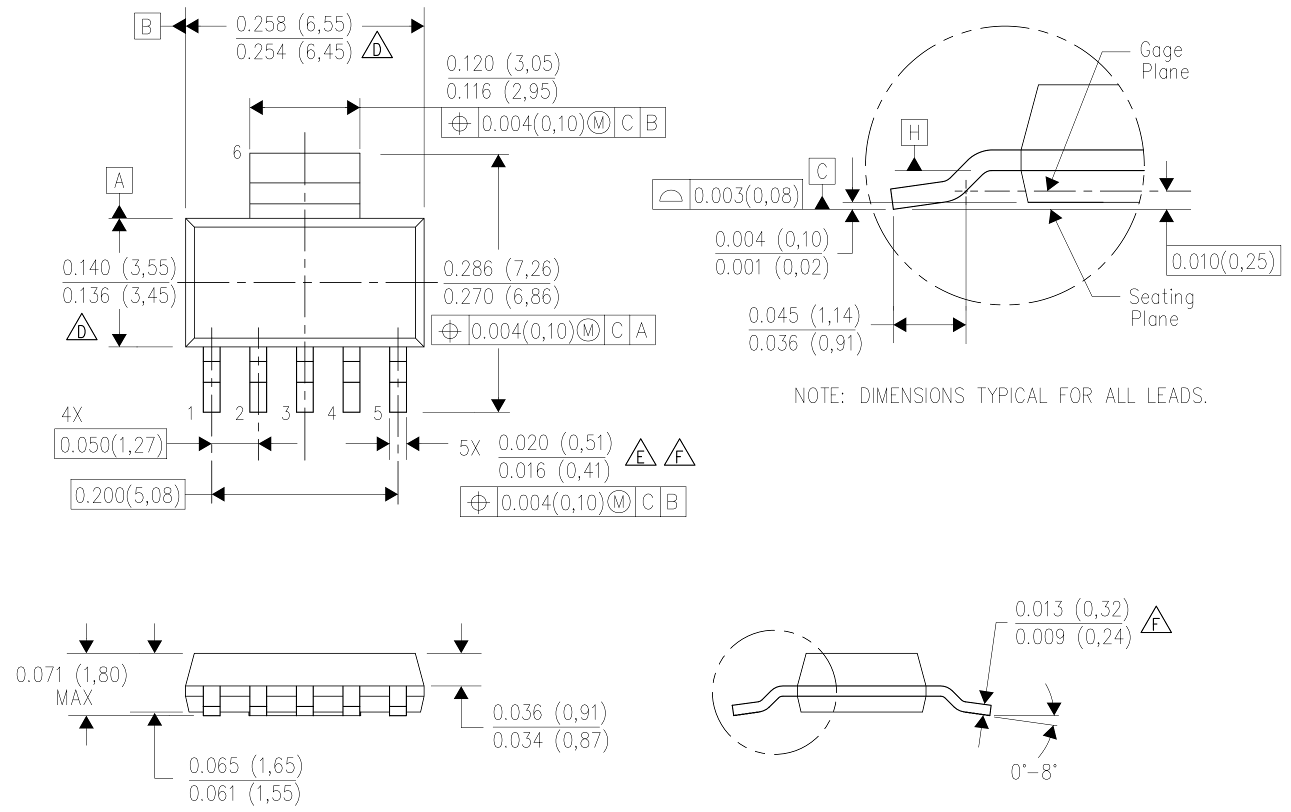


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS78601DCQR	SOT-223	DCQ	6	2500	367.0	367.0	35.0
TPS78601DCQRG4	SOT-223	DCQ	6	2500	358.0	335.0	35.0
TPS78601DRBR	SON	DRB	8	3000	367.0	367.0	35.0
TPS78601DRBT	SON	DRB	8	250	210.0	185.0	35.0
TPS78601KTTR	DDPAK/TO-263	KTT	5	500	367.0	367.0	45.0

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS78601KTTT	DDPAK/TO-263	KTT	5	50	367.0	367.0	45.0
TPS78618DCQR	SOT-223	DCQ	6	2500	358.0	335.0	35.0
TPS78618KTTR	DDPAK/TO-263	KTT	5	500	367.0	367.0	45.0
TPS78618KTTRE3	DDPAK/TO-263	KTT	5	500	367.0	367.0	45.0
TPS78618KTTT	DDPAK/TO-263	KTT	5	50	367.0	367.0	45.0
TPS78625DCQR	SOT-223	DCQ	6	2500	358.0	335.0	35.0
TPS78625KTTR	DDPAK/TO-263	KTT	5	500	367.0	367.0	45.0
TPS78625KTTT	DDPAK/TO-263	KTT	5	50	367.0	367.0	45.0
TPS78628DCQR	SOT-223	DCQ	6	2500	406.0	348.0	63.0
TPS78628KTTT	DDPAK/TO-263	KTT	5	50	367.0	367.0	45.0
TPS78630DCQR	SOT-223	DCQ	6	2500	406.0	348.0	63.0
TPS78630KTTT	DDPAK/TO-263	KTT	5	50	367.0	367.0	45.0
TPS78633DCQR	SOT-223	DCQ	6	2500	358.0	335.0	35.0
TPS78633KTTR	DDPAK/TO-263	KTT	5	500	367.0	367.0	45.0
TPS78633KTTRE3	DDPAK/TO-263	KTT	5	500	367.0	367.0	45.0
TPS78633KTTT	DDPAK/TO-263	KTT	5	50	367.0	367.0	45.0

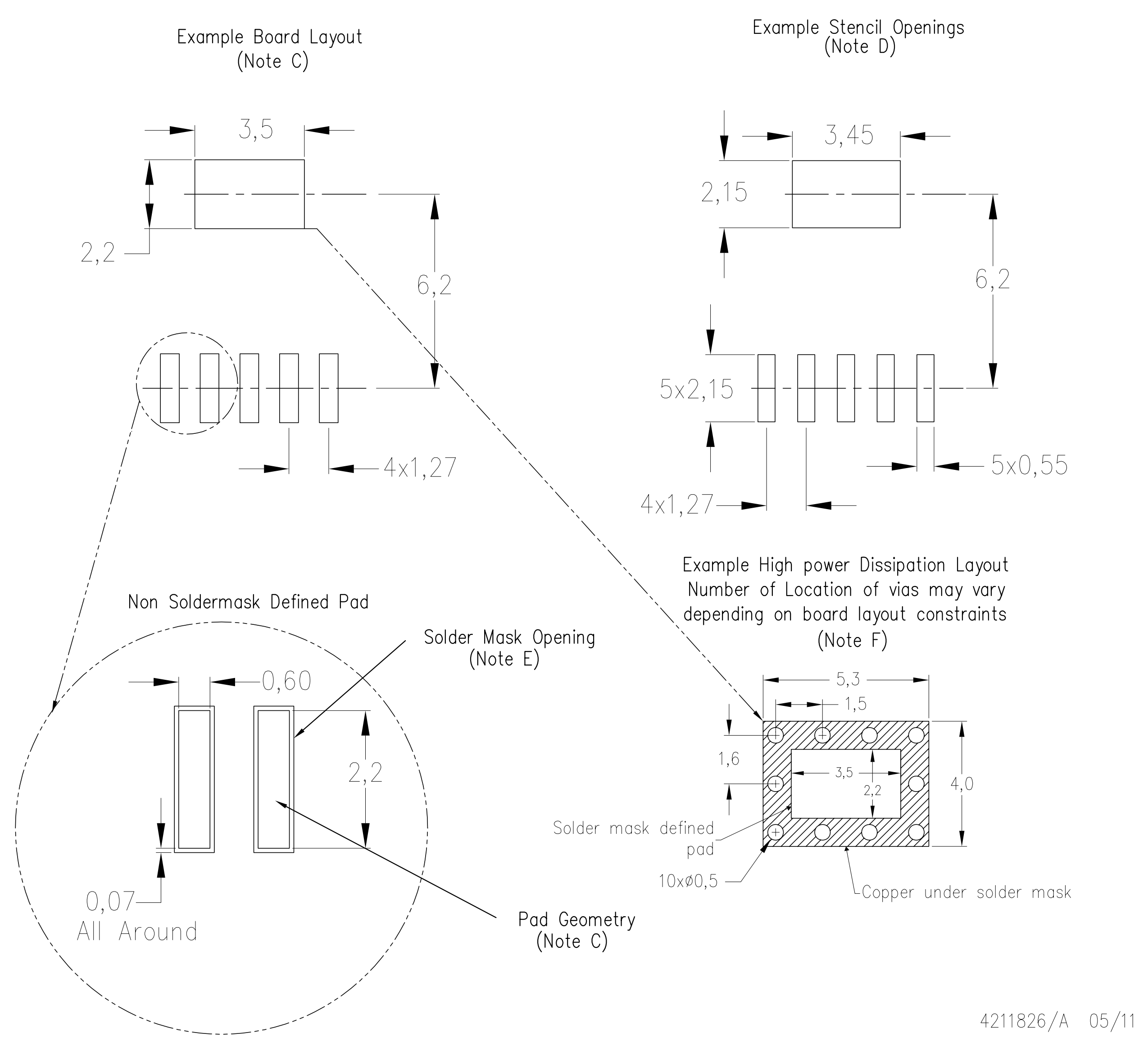
DCQ (R–PDSO–G6) PLASTIC SMALL–OUTLINE



4202109/D 06/09

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Controlling dimension in inches.
△D Body length and width dimensions are determined at the outermost extremes of the plastic body exclusive of mold flash, tie bar burrs, gate burrs, and interlead flash, but including any mismatch between the top and the bottom of the plastic body.
△E Lead width dimension does not include dambar protrusion.
△F Lead width and thickness dimensions apply to solder plated leads.
G. Interlead flash allow 0.008 inch max.
H. Gate burr/protrusion max. 0.006 inch.
I. Datums A and B are to be determined at Datum H.

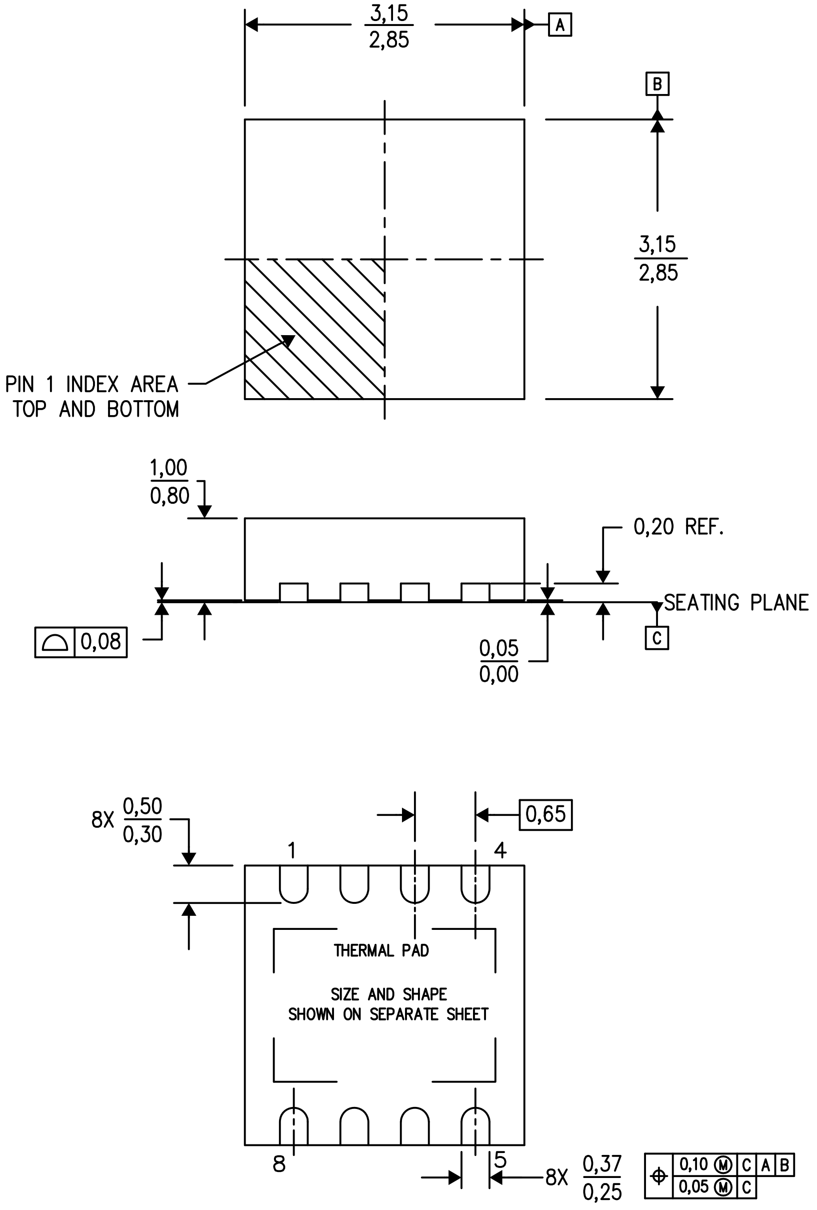
DCQ (R-PDSO-G6) PLASTIC SMALL OUTLINE



4211826/A 05/11

NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Publication IPC–SM–782 is recommended for alternate designs.
- D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations.
- E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.
- F. Please refer to the product data sheet for specific via and thermal dissipation requirements.

DRB (S–PVSON–N8) PLASTIC SMALL OUTLINE NO–LEAD



Bottom View

4203482–2/K 06/12

NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
- B. This drawing is subject to change without notice.
- C. Small Outline No–Lead (SON) package configuration.
- D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
- E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.

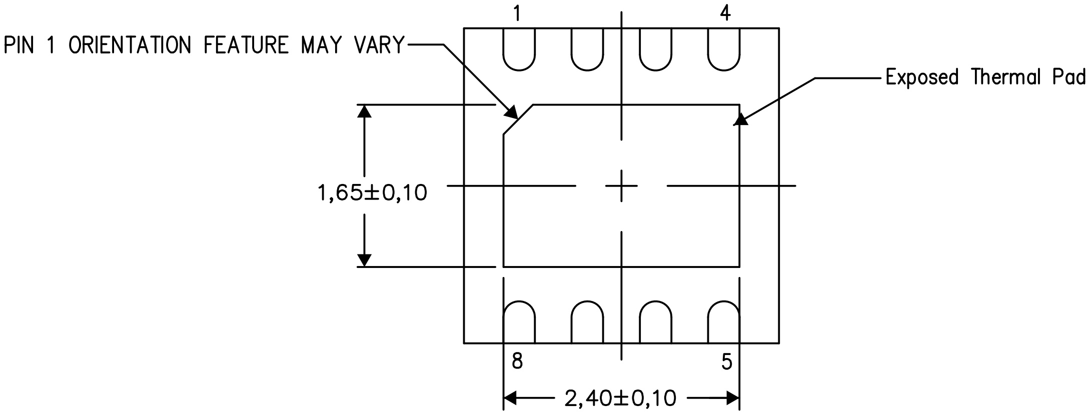
DRB (S–PVSON–N8) PLASTIC SMALL OUTLINE NO–LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



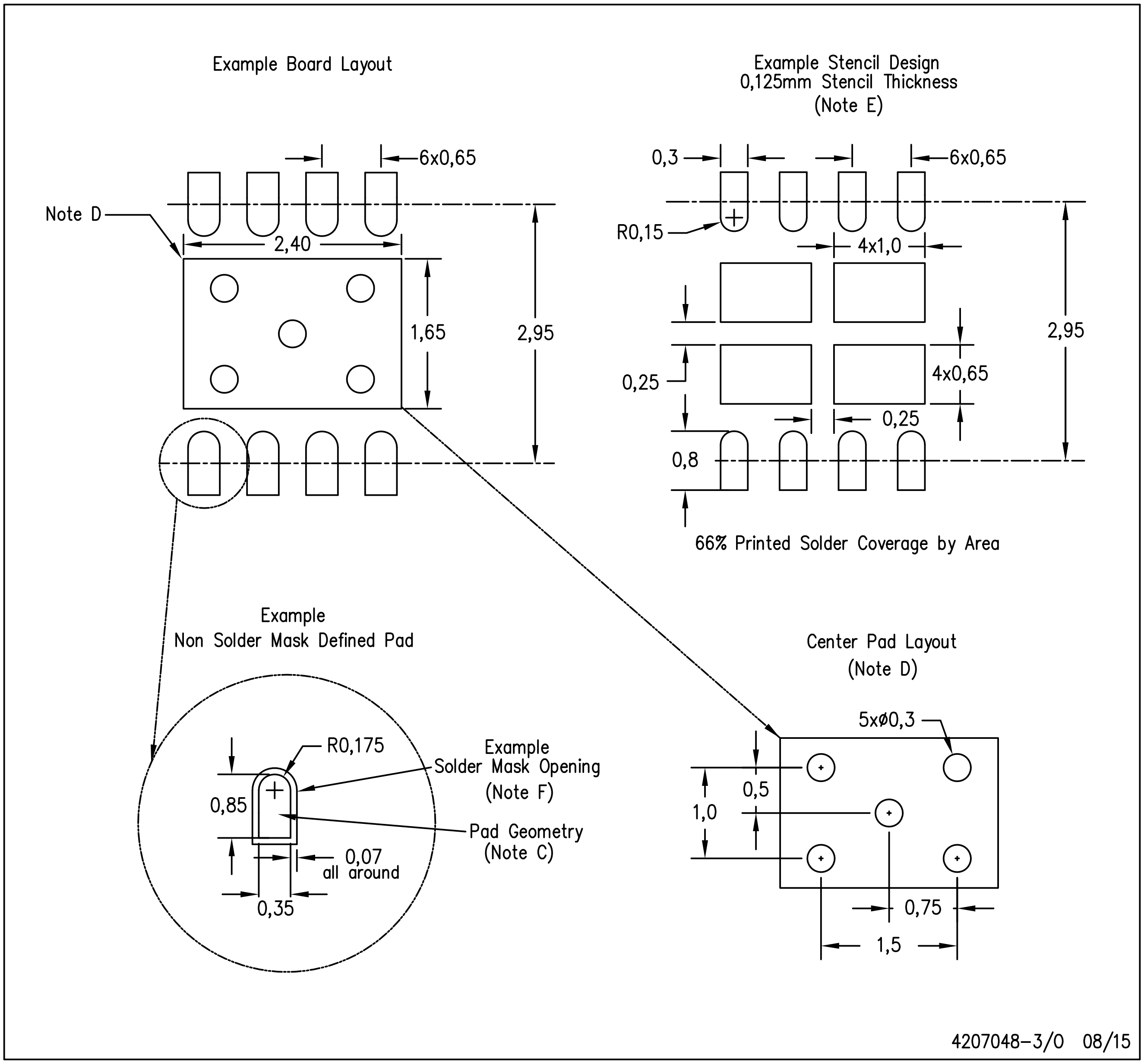
Bottom View

Exposed Thermal Pad Dimensions

4206340–3/T 08/15

NOTE: All linear dimensions are in millimeters

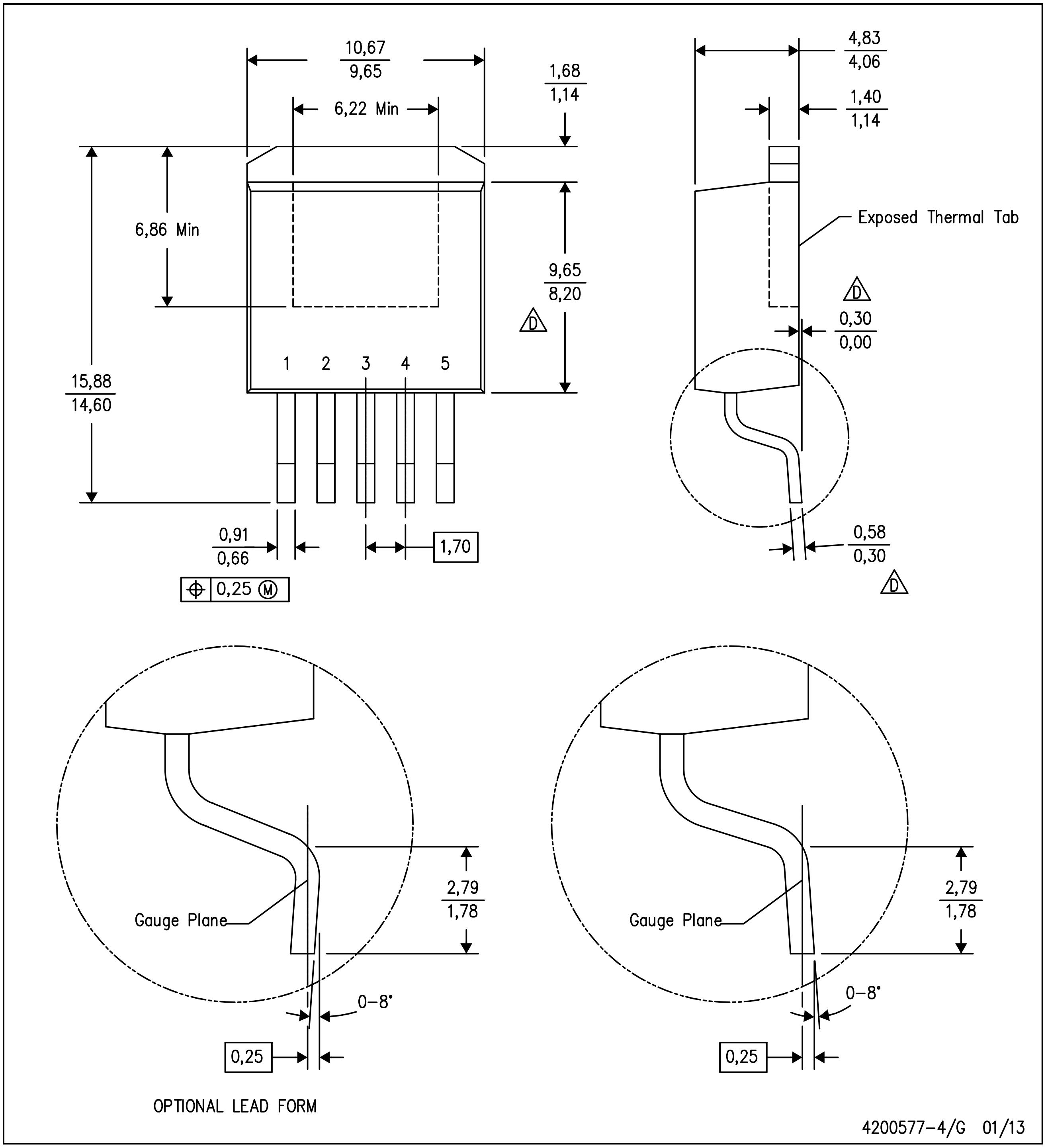
DRB (S–PVSON–N8) PLASTIC SMALL OUTLINE NO–LEAD



4207048–3/0 08/15

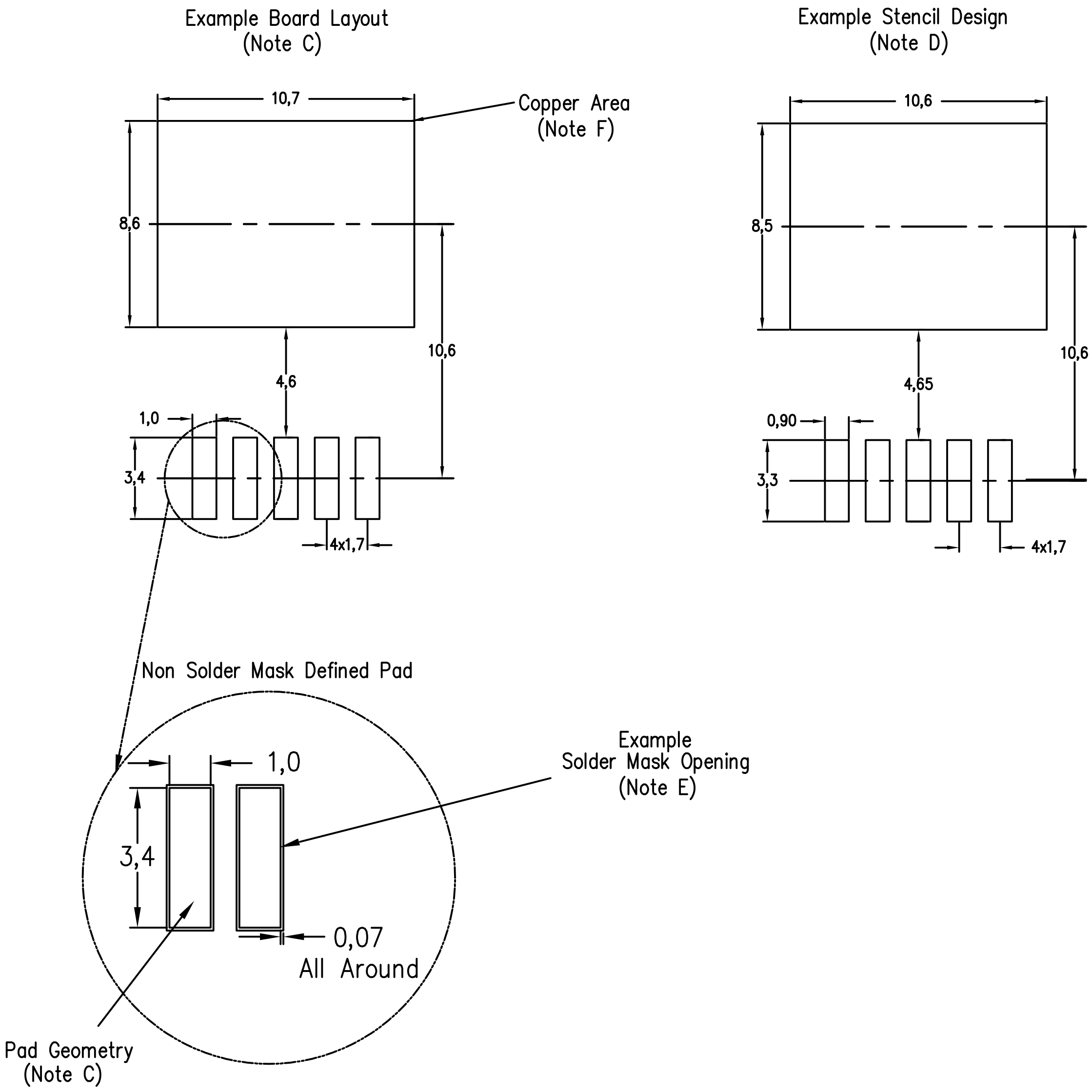
NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Publication IPC–7351 is recommended for alternate designs.
- D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, QFN Packages, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>.
- E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
- F. Customers should contact their board fabrication site for solder mask tolerances.

KTT (R–PSFM–G5) PLASTIC FLANGE–MOUNT PACKAGE



NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion. Mold flash or protrusion not to exceed 0.005 (0,13) per side.
- D. Falls within JEDEC TO–263 variation BA, except minimum lead thickness, maximum seating height, and minimum body length.

KTT (R-PSFM-G5) PLASTIC FLANGE-MOUNT PACKAGE



4208208-3/C 08/12

NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Publication IPC-SM-782 is recommended for alternate designs.
- D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525.
- E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.
- F. This package is designed to be soldered to a thermal pad on the board. Refer to the Product Datasheet for specific thermal information, via requirements, and recommended thermal pad size. For thermal pad sizes larger than shown a solder mask defined pad is recommended in order to maintain the solderable pad geometry while increasing copper area.

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