TEXAS INSTRUMENTS

UCC28910
UCC28911

SLUS769C – JULY 2013 – REVISED MARCH 2015

UCC28910, UCC28911 High-Voltage Flyback Switcher with Primary-Side Regulation and Output Current Control

1 Features

- Constant-Voltage (CV) and Constant-Current (CC) Output Regulation Without Optical-Coupler
- ±5% Output Voltage Regulation Accuracy
- ±5% Output Current Regulation With AC Line and Primary Inductance Tolerance Compensation
- 700-V Start-Up and Smart Power Management Enables <30-mW Standby Power
- 115-kHz Maximum Switching Frequency Design for High-Power Density
- Valley Switching and Frequency Dithering to Ease EMI Compliance
- Thermal Shut Down
- Low Line and Output Over-Voltage Protection

2 Applications

- Home and Building Automation
- Power Metering Bias
- Bias Power for Smoke Alarm, Fire Alarm and Thermostat
- Wall Adapters, Chargers for Mobile Phones
- Smart plug, IoT, MCU and WiFi Power
- Aux power for TV, Server, White Goods
- LED Lighting

3 Description

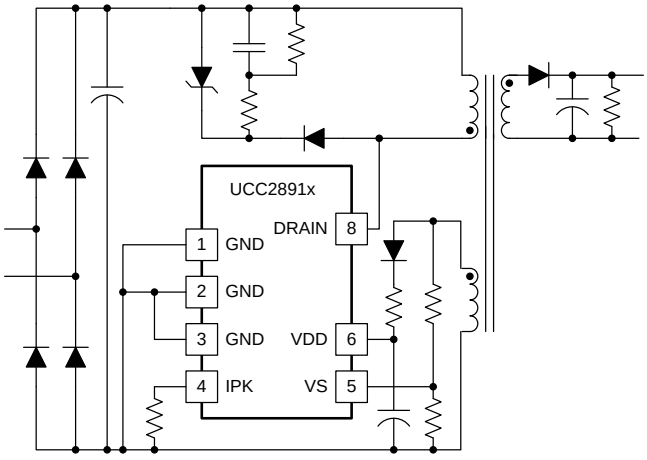
The UCC28910 and UCC28911 are high-voltage flyback switchers that provide output voltage and current regulation without the use of an optical coupler. Both devices incorporate a 700-V power FET and a controller that process operating information from the flyback auxiliary winding and power FET to provide a precise output voltage and current control. The integrated high-voltage current source for startup that is switched off during device operation, and the controller current consumption is dynamically adjusted with load. Both enable the very low stand-by power consumption.

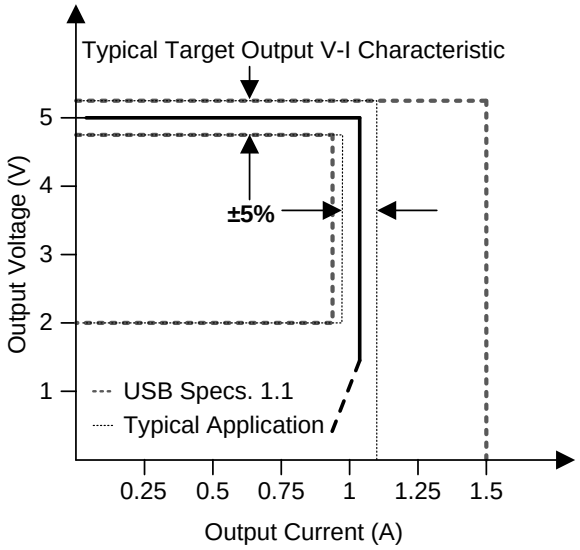
Control algorithms in the UCC28910 and UCC28911, combining switching frequency and peak primary current modulation, allow operating efficiencies to meet or exceed applicable standards. Discontinuous conduction mode (DCM) with valley switching is used to reduce switching losses. Built-in protection features help to keep secondary and primary component stress levels in check across the operating range. The frequency jitter helps to reduce EMI filter cost.

Device Information

PART NUMBER	PACKAGE	BODY SIZE (NOM)
UCC28910	SOIC-7 (7)	5.00 mm x 6.20 mm
UCC28911	SOIC-7 (7)	5.00 mm x 6.20 mm

4 Simplified Schematic





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• Changed marketing status from product preview to production data.	1

Changes from Revision A (July 2014) to Revision B	Page
• Changed Simplified Schematic diagram	1

Changes from Revision August 2014 (B) to Revision C	Page
• Added UCC28911 device.	1
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• Changed Applications and Implementation section to include the UCC28911 device	28

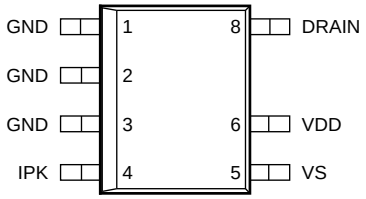
6 Device Comparison Table

PART NUMBER(1)	175 V_{AC} to 265 V_{AC}		90 V_{AC} to 265 V_{AC}		UNITS
	Adapter(2)	Open Frame(3)	Adapter(2)	Open Frame(3)	
UCC28910	6.5	9.5	6	7.5	W
UCC28911	8	12	7.5	10	W

(1) Obtained considering 125°C as maximum junction temperature. For lower operating maximum junction temperature maximum output power should be lower.
(2) Typical continuous power in enclosed adapter at 50°C ambient, with adequate copper area (> 560 mm^2) connected on GND pin to have 90°C/W as junction to ambient thermal resistance.
(3) Maximum continuous power with open frame design at 50°C ambient, with adequate copper area connected on GND pin and /or adequate air flow to have 50°C/W as junction to ambient thermal resistance.

7 Pin Configuration and Functions

D (SOIC) PACKAGE
7 PINS
(TOP VIEW)



Pin Functions

PIN		I/O(1)	DESCRIPTION
NAME	NO.		
DRAIN	8	P	DRAIN, the drain of the internal power FET, but also the input for the high-voltage current source used to start up the device.
GND	1, 2, 3	G	The ground pins (GND) are both the reference pins for the controller and the low-side return for the drive output. Special care should be taken to return all AC decoupling as close as possible to this pin and avoid any common trace length with analog signal return paths.
IPK	4	O	IPK is used to set the maximum peak current flowing in the power FET that is proportional to the maximum output current.
N/A	7	N/A	This pin is not present to provide enough distance between high voltage pin (DRAIN) and VDD pins.
VDD	6	P	VDD is the supply pin to the controller. A carefully placed bypass capacitor to GND is required on this pin.
VS	5	I	Voltage Sense (VS) is used to provide voltage and timing feedback to the controller. Normally this pin is connected to a voltage divider between an auxiliary winding and ground. The value of the upper resistor of this divider is used to program low line thresholds.

(1) P = Supply, G = Ground, I = Input, O = output

7.1 Detailed Pin Description

7.1.1 VDD (Device Voltage Supply)

The VDD pin is connected to a bypass capacitor to ground and typically to a rectifier diode connected to the auxiliary winding. The VDD turn on UVLO threshold is 9.5 V (VDD_{ON} typical) and turn off UVLO threshold is 6.5 V (VDD_{OFF} typical). The pin is provided with an internal clamp that prevents the voltage from exceeding the absolute maximum rating of the pin. The internal clamp cannot absorb currents higher than 10 mA (see $I_{VDD(clp)}$ in Absolute Maximum Ratings). To avoid damaging the device, when the clamp flowing current exceeds 6 mA (I_{DDCLP_OC} typical) the device stops switching. The VDD pin operating range is then from 7 V (VDD_{OFF} maximum) up to 26 V (VDD_{CLAMP} minimum). The USB charging specification requires that the output current operates in constant current mode from 5 V to a minimum of 2 V; this is easily achieved with a nominal VDD of approximately 17 V. Set N_{AS} (auxiliary-to-secondary windings turn ratio) to 17 V / (V_{OUT} + V_F) where V_F is the voltage drop on the output diode at low current. The additional VDD headroom up to the clamp allows for VDD to rise due to the leakage energy delivered to the VDD in high-load conditions.

The current consumption of the device depends upon the operating condition. The graph below shows the current consumption as a function of normalized converter output power.

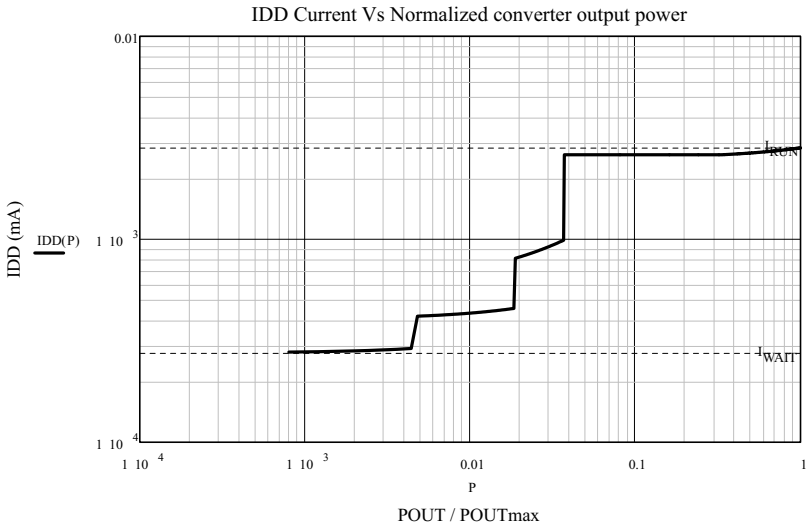


Figure 1. VDD Current Consumption

7.1.2 GND (Ground)

The device is provided with three pins, shorted together, that are used as external ground reference to the controller for analog signal reference. The three pins also function to pull out the heat caused by the power dissipation of the internal power FET. Place the VDD bypass capacitor close to GND and VDD with short traces to minimize noise on the VS and IPK signal pins.

Detailed Pin Description (continued)

7.1.3 VS (Voltage Sense)

The VS pin is connected to a resistor divider from the auxiliary winding to ground. The VS input provides three functions.

1. It provides output voltage information to the voltage control Loop. The output voltage feedback information is sampled at the end of the transformer secondary current demagnetization time to provide an accurate representation of the output voltage.
2. It also provides timing information to achieve valley switching and the duty cycle of the secondary transformer current is determined by the waveform on the VS pin.
3. It samples the bulk capacitor input voltage providing under-voltage shutdown.

The data provided in 1. and 2. are sensed during the MOSFET off-time; 3. is performed during the MOSFET on-time when the auxiliary-winding voltage is negative.

Connected between VS pin and the auxiliary winding there is the resistance R_{S1}. During MOSFET on-time the auxiliary voltage is negative and proportional to the converter input voltage. The voltage on VS pin is clamped to GND and through the resistance R_{S1}. During the on-time, the current sourced from the VS pin, proportional to converter input voltage and inversely proportional to resistance R_{S1}, is sensed by the device. For the under-voltage function, the enable threshold on VS current is 210 µA and the disable threshold is 75 µA.

The resistor values for R_{S1} and R_{S2} can be determined by the equations below.

$$R_{S1} = \frac{V_{RMS\_EN} \times \sqrt{2}}{N_{PA} \times I_{VSLRUN}} \quad (1)$$

where

- N_{PA} is the transformer primary to auxiliary turns ratio,
- V_{RMS_EN} is the AC RMS voltage to enable turn on of the controller,
- I_{VSLRUN} is the line sense current (210 µA typical).

$$R_{S2} = \frac{V_{VSR} \times R_{S1} \times N_{PA}}{(V_{OUT} + V_F) \times N_{PS} - (V_{VSR} \times N_{PA})} \quad (2)$$

where

- V_{OUT} is the converter output voltage in V,
- V_F is the output rectifier forward drop at low current in V,
- N_{PS} is the transformer primary to secondary turns ratio R_{S1} is the VS divider high side resistance in Ohms,
- V_{VSR} is the regulating level of VS pin.

Detailed Pin Description (continued)

7.1.4 IPK (Set the Maximum DRAIN Current Peak)

A resistance (R_{IPK}) connected between IPK pin and GND sets the maximum value of the power FET peak current, $I_{D\_PK(max)}$. A current, I_{SENSE}, proportional to the power FET current, comes out from the IPK pin during power FET on time. The voltage across R_{IPK} is fed to the PWM comparator and establish to switch off the power FET according to the following equation:

$$I_{D\_PK(max)} = \frac{V_{CSTE(max)}}{R_{IPK}} \quad (3)$$

where

- $V_{CSTE(max)}$ is the equivalent current sense threshold (see Electrical Characteristics table).

If the IPK pin is shorted to GND (RIPK = 0), the peak current is automatically set to $I_{D\_PEAK(max)}$, 600 mA for UCC28910, or 700 mA for UCC28911.

A test is performed at device start up to check whether the IPK pin is shorted to GND or the R_{IPK} is present. If R_{IPK} is less than R_{IPK_SHORT} (maximum), the device interprets it as a short (R_{IPK} = 0) and the DRAIN peak current is set to $I_{D\_PEAK(max)}$. Otherwise, if R_{IPK} is greater than $R_{IPK(min)}$ (minimum), the device sets the peak current DRAIN according to the previous equation. A value of R_{IPK} that is in between the before said values is not allowed since the value of the peak current may be selected using either of the two sense resistances: the internal sense resistance and R_{IPK}.

7.1.5 DRAIN

The DRAIN pin is connected to the DRAIN of the internal power FET. This pin also provides current to the high voltage current source at start up.

8 Specifications

8.1 Absolute Maximum Ratings

(unless otherwise noted) (1)(2)

		MIN	MAX	UNIT
V_{DRAIN}	DRAIN voltage	Internally limited(3)	700	V
I_{DRAIN}	Negative drain current	–100		mA
V_{DD}	Supply voltage		Internally limited(3)	V
$I_{VDD(clp)}$	Maximum VDD clamp current		10	mA
V_{VS}	Voltage range	Internally limited(3)	7	V
V_{IPK}	Voltage range	−0.5	5.0	V
I_{VS}	Peak VS pin current (current out of the pin)	−1.2		mA
I_{DRAIN}	Pulsed drain current(4), UCC28910		950	mA
	Pulsed drain current(4), UCC28911		1200	mA
T_{LEAD}	Lead temperature 1.6 mm (1/16 inch) from case for 10 seconds		260	°C
T_J	Operating junction temperature range	−55	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltages are with respect to GND. Currents are positive into, negative out of the specified pin. These ratings apply over the operating ambient temperature ranges unless otherwise noted.
(3) Do not drive with low impedance voltage source.
(4) Maximum pulse width = 100 µs.

8.2 Storage Conditions

		MIN	MAX	UNIT
T_{stg}	Storage temperature	−65	150	°C

8.3 ESD Ratings

		VALUE	UNIT
$V_{(ESD)}$ Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
	Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

8.4 Recommended Operating Conditions(1)(2)

			MIN	NOM	MAX	UNIT
V_{VDD}	Voltage on VDD terminal during operation		VDD_{OFF}		$V_{VDD(clp)}$	V
I_{VS}	Current out of the terminal				1	mA
$I_{D(peak\_max)}$	Maximum drain peak current	UCC28910		600		mA
		UCC28911		700		mA
T_J	Operating junction temperature		-40		125	°C

(1) Unless otherwise noted, all voltages are with respect to GND.
(2) In case of thermal shut down, if T_A > 100°C, the device does not restart because of the $T_{J(hys)}$ Electrical Characteristics.

8.5 Thermal Information

THERMAL METRIC(1)		UCC28910 D 7 PIN	UCC28911 D 7 PIN	UNITS
θ_{JA}	Junction-to-ambient thermal resistance	102.2	102.2	°C/W
θ_{JCtop}	Junction-to-case (top) thermal resistance	39.1	39.1	
θ_{JB}	Junction-to-board thermal resistance	54.7	54.7	
ψ_{JT}	Junction-to-top characterization parameter	5.4	5.4	
ψ_{JB}	Junction-to-board characterization parameter	54.7	54.7	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

8.6 Electrical Characteristics

over operating free-air temperature range (unless otherwise noted), V_{VDD} = 15 V, T_A = -40°C to 125°C, $T_A = T_J$

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
SUPPLY INPUT							
I_{RUN}	Supply current, run	V_{VS} = 3.9 V, $f_{SW} = f_{SW(max)}$	UCC28910	2.3	2.9	3.4	mA
		V_{VS} = 3.75 V, $f_{SW} = f_{SW(max)}$	UCC28911	2.3	2.9	3.4	mA
I_{RUNQ}	Quiescent supply current	V_{VS} = 3.9 V, f_{SW} = 0 Hz	UCC28910	1.90	2.35	2.80	mA
		V_{VS} = 3.75 V, $f_{SW} = f_{SW(max)}$	UCC28911	1.90	2.35	2.80	mA
I_{WAIT}	Wait supply current	V_{VS} = 4.1 V, $f_{SW} = f_{SW(min)}$	UCC28910	150	270	370	µA
		$f_{SW} = f_{SW(min)}$, T_J = 25°C	UCC28911		250	330	µA
I_{WAITQ}	Quiescent wait supply current	V_{VS} = 4.1 V, f_{SW} = 0 Hz	UCC28910	150	200	280	µA
		f_{SW} = 0, T_J = 25°C	UCC28911		190	240	µA
I_{START}	Supply current before start	V_{VDD} from 0 V to 5.6 V, V_{DRAIN} = 0 V	UCC28910		65	90	µA
		V_{VDD} from 0 V to 5.6 V, V_{DRAIN} = 0, T_J = 25°C	UCC28911		65	80	µA
I_{FAULT}	Supply current after fault	f_{SW} = 0 Hz	UCC28910		190	260	µA
		f_{SW} = 0, T_J = 25°C	UCC28911		190	240	µA
UNDER-VOLTAGE LOCKOUT							
VDD_{ON}	VDD turn-on threshold	V_{VDD} low to high		9.0	9.5	10.0	V
VDD_{OFF}	VDD turn-off threshold	V_{VDD} high to low		6.0	6.5	7.0	V
$VDD_{HV(on)}$	HV current source start	V_{VDD} high to low		4.8	5.2	5.6	V
ΔV_{UVLO}	UVLO hysteresis	$VDD_{ON} - VDD_{OFF}$		2.8	3.0	3.2	V
STARTUP CURRENT SOURCE							
I_{CH1}	Startup current with VDD shorted to GND	V_{VDD} < 250 mV, V_{DRAIN} = 100 V		–300		–100	µA
I_{CH2}	Sourced current for startup at high VDD	V_{VDD} = 8 V, V_{DRAIN} = 100 V		–9.75		–0.40	mA
I_{CH3}	Sourced current for startup at low VDD	V_{VDD} = 2 V, V_{DRAIN} = 100 V		–13.75		–1.30	mA

Electrical Characteristics (continued)

over operating free-air temperature range (unless otherwise noted), V_{VDD} = 15 V, T_A = -40°C to 125°C, $T_A = T_J$

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
VS INPUT							
V_{VSR}	Regulating level	Measured in no load condition, T_J = 25°C		4.01	4.05	4.09	V
V_{VSNC}	Negative clamp level	I_{VS} = –300 µA		–190	–250	–325	mV
I_{VS}	Input bias current	V_{VS} = 4 V		–0.25	0.00	0.25	µA
PROTECTION							
$I_{D(ocp)}$	DRAIN over current	I_{PK} pin shorted to GND	UCC28910	725	850	925	mA
			UCC28911	880	980	1090	mA
V_{CSTE_OCP}	Equivalent $V_{CST(OCP)}$, $I_{D(ocp)}$ x R_{IPK}	V_{VS} = 3.9 V	UCC28910	670	770	830	V
		V_{VS} = 3.75 V	UCC28911	800	885	975	V
V_{CSTE_OCP2}	Equivalent $V_{CST(OCP2)}$ $I_{D(ocp2)}$ x R_{IPK}	V_{VS} = 3.9 V	UCC28910		1200		V
		V_{VS} = 3.75 V	UCC28911		1400		V
$t_{ONMAX(max)}$	Maximum FET on time at high load	V_{VS} < 3.9 V, I_{PK} shorted to GND	UCC28910	13	18	24	µs
		V_{VS} = 3.75 V, I_{PK} shorted to GND	UCC28911	13	18	24	µs
$t_{ONMAX(min)}$	Maximum FET on time at low load	V_{VS} > 4.1 V, I_{PK} shorted to GND	UCC28910	4.3	6	10	µs
		V_{VS} = 4.35 V, I_{PK} shorted to GND	UCC28911	4.3	6	10	µs
V_{OVP}	Over-voltage threshold	At VS input, T_J = 25°C		4.45	4.60	4.75	V
$I_{VSL(run)}$	VS line sense run current	Current out of VS pin – increasing		175	215	260	µA
$I_{VSL(stop)}$	VS line sense stop current	Current out of VS pin – decreasing		60	75	100	µA
K_{VSL}	Line sense I_{VS} ratio	$I_{VSL(run)}$ / $I_{VSL(stop)}$		2.55	2.70	2.90	A/A
VDD_{CLP}	VDD voltage clamp	I_{VDDCLP} forced = 2 mA		26	28	30	V
I_{VDDCLP_OC}	VDD clamp over current	V_{VDD} > 25 V		4.65	6.00	7.65	mA
$T_{J(stop)}$	Thermal shutdown temperature	Internal junction temperature			150		°C
$T_{J(hys)}$	Thermal shutdown hysteresis	Internal junction temperature			50		°C
POWER FET							
BV_{DSS}	Break-down voltage	T_J = 25°C		700			V
$R_{DS(on)}$	Power FET on resistance	I_D = 150 mA, T_J = 25°C	UCC28910		10.5	12.0	Ω
			UCC28911		6.25	7.2	Ω
		I_D = 150 mA, T_J = 125°C	UCC28910		18.4	21.5	Ω
			UCC28911		11.4	13.4	Ω
$I_{LEAKAGE}$	DRAIN pin leakage current	V_{DS} = 400 V HV, VS = 4.2 V DC T_J = 25°C				10	µA
		V_{DS} = 400 V HV, VS = 4.2 V DC T_J = 125°C				20	µA
		V_{DS} = 700 V HV, VS = 4.2 V DC T_J = 25°C				10	µA

Electrical Characteristics (continued)

over operating free-air temperature range (unless otherwise noted), V_{VDD} = 15 V, T_A = -40°C to 125°C, T_A = T_J

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
CURRENTS							
$I_{D\_PEAK(max)}$	Maximum DRAIN peak current	IPK pin shorted to GND, T_J = 25°C	UCC28910	582	600	618	mA
			UCC28911	680	700	720	mA
R_{IPK_SHORT}	IPK to GND resistance Max to assume IPK shorted to GND					200	Ω
$R_{IPK(min)}$	IPK to GND minimum resistance			900			Ω
$V_{CSTE(max)}$	Equivalent current sense threshold, $I_{D\_PK(max)} \times R_{IPK}$	V_{VS} = 3.9 V, T_J = 25°C	UCC28910	532	540	548	V
		V_{VS} = 3.75 V	UCC28911	620	630	640	V
$V_{CSTE(min)}$	Equivalent current sense threshold, $I_{D\_PK(min)} \times R_{IPK}$	V_{VS} = 4.1 V	UCC28910	160	180	200	V
		V_{VS} = 4.35 V	UCC28911	170	216	265	V
K_{AM}	AM control ratio	$V_{CSE(max)}$ / $V_{CSE(min)}$		2.30	3.00	3.50	V/V
K_{CC}	CC regulation gain, $t_{DEMAG} \times f_{SW}$	V_{VS} < 3.9 V	UCC28910		0.413		
		V_{VS} = 3.75 V	UCC28911		0.413		
V_{CCR}	CC regulation constant, $V_{CSET(max)} \times K_{CC}$	V_{VS} < 3.9 V, T_J = 25°C	UCC28910	216	223	230	V
			UCC28911	250	260	270	V

8.7 Switching Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
TIMING							
$f_{SW(max)}$	Maximum switching frequency	V_{VS} < 3.9 V	UCC28910	105	115	125	kHz
		V_{VS} = 3.75 V	UCC28911	105	115	125	kHz
$f_{SW(min)}$	Minimum switching frequency	V_{VS} > 4.1 V	UCC28910	360	420	490	Hz
		V_{VS} = 4.35 V	UCC28911	360	420	500	Hz
t_{ZTO}	Zero crossing timeout delay	V_{VS} < 3.9 V	UCC28910	1.80	2.10	2.65	µs
		V_{VS} = 4.35 V	UCC28911	1.80	2.10	2.75	µs
$t_{ON(min)}$	Minimum on time	I_{PK} = 0.85 V	UCC28910		390		ns
			UCC28911		420		ns

8.8 Typical Characteristics

Unless otherwise specified, V_{VDD} = 15 V, T_A = –40°C to 125°C, T_A = T_J

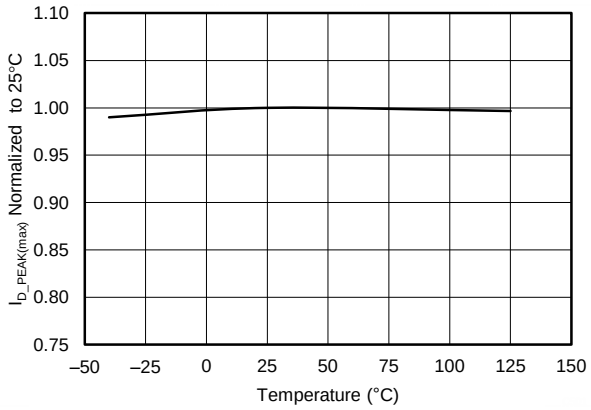


Figure 2. UCC28910 $I_{D\_PEAK(max)}$ vs Temperature

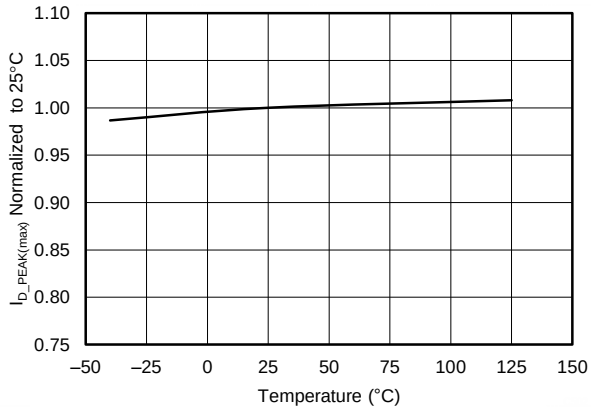


Figure 3. UCC28911 $I_{D\_PEAK(max)}$ vs Temperature

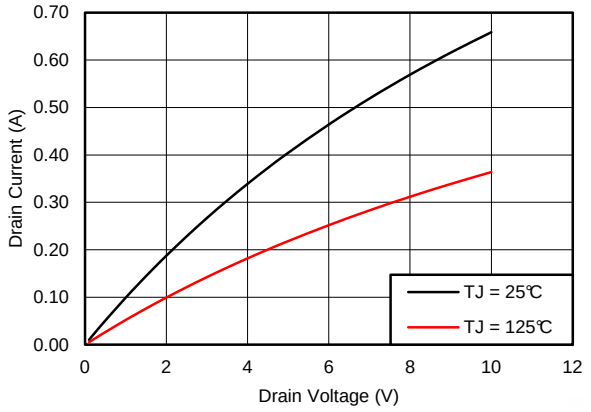


Figure 4. UCC28910 Drain Current vs Drain Voltage

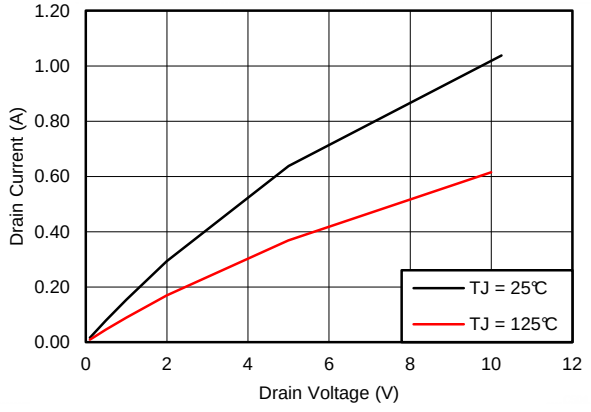


Figure 5. UCC28911 D_{RAIN} Current vs D_{RAIN} Voltage

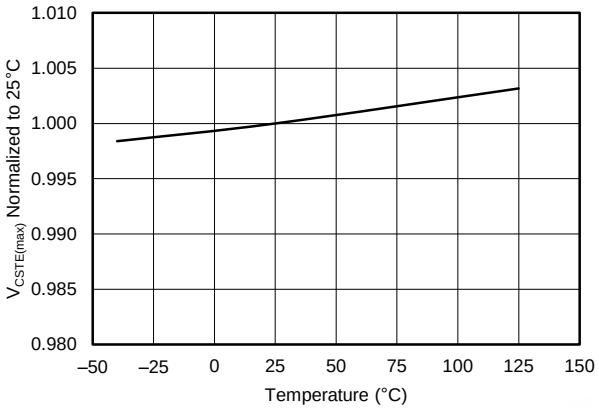


Figure 6. UCC28910 $V_{CSTE(max)}$ vs Temperature

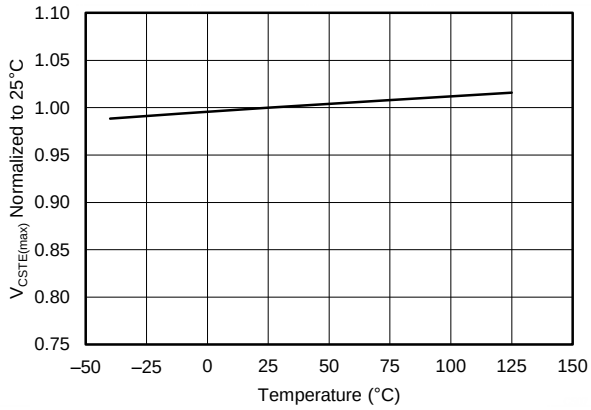


Figure 7. UCC28911 $V_{CSTE(max)}$ vs Temperature

Typical Characteristics (continued)

Unless otherwise specified, V_{VDD} = 15 V, T_A = –40°C to 125°C, T_A = T_J

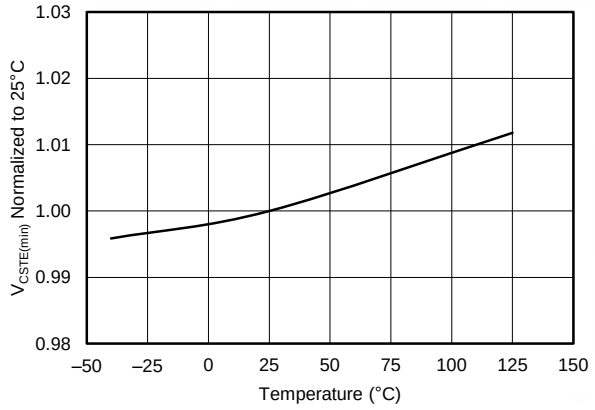


Figure 8. UCC28910 $V_{CSTE(min)}$ vs Temperature

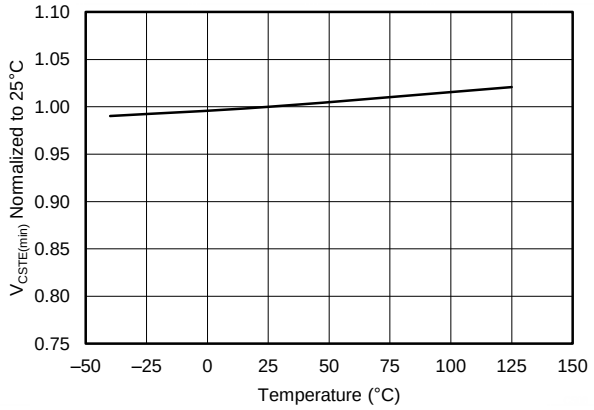


Figure 9. UCC28911 $V_{CSTE(min)}$ vs Temperature

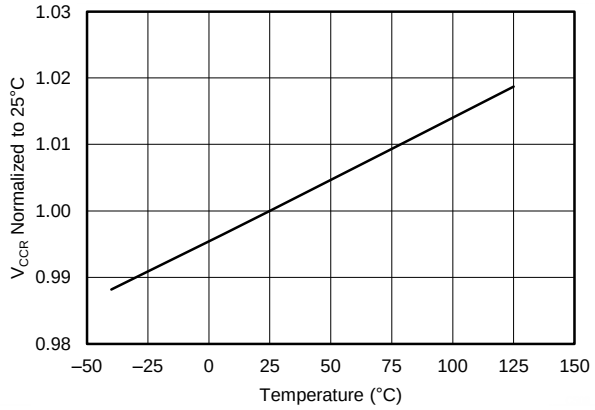


Figure 10. UCC28910 V_{CCR} vs Temperature

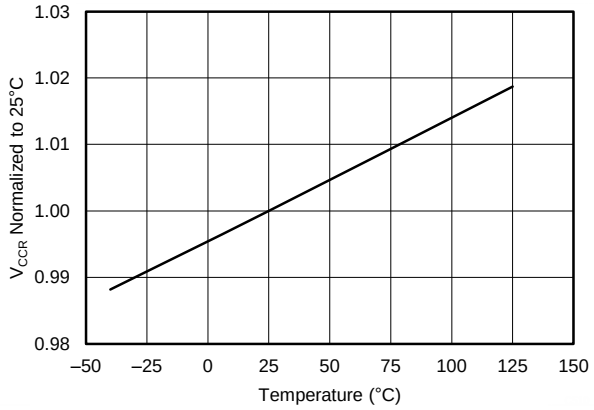


Figure 11. UCC28911 V_{CCR} vs Temperature

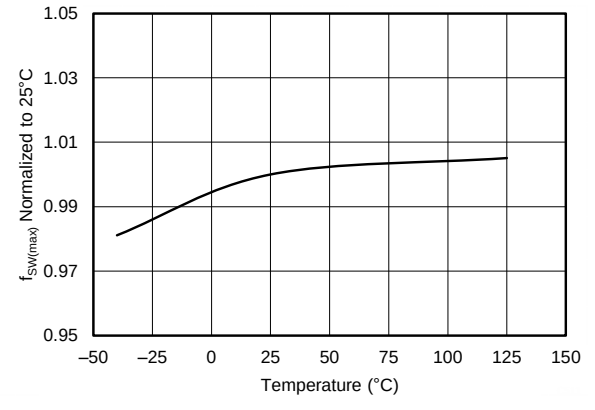


Figure 12. $f_{SW(max)}$ vs Temperature

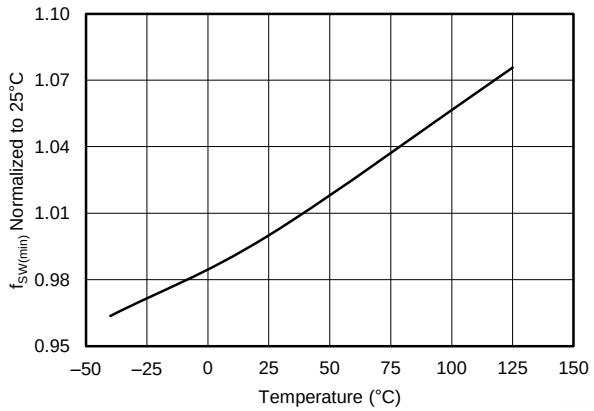


Figure 13. $f_{SW(min)}$ vs Temperature

Typical Characteristics (continued)

Unless otherwise specified, V_{VDD} = 15 V, T_A = –40°C to 125°C, T_A = T_J

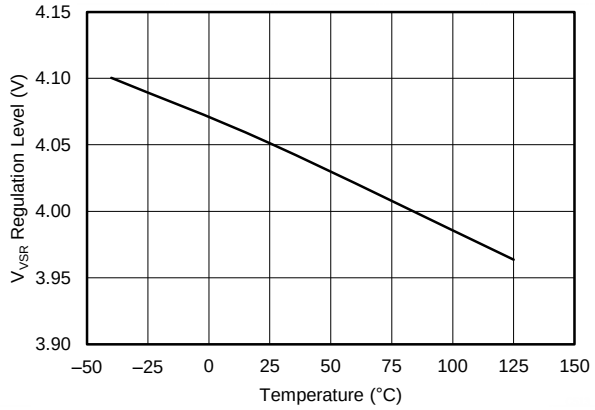


Figure 14. V_{VSR} vs Temperature

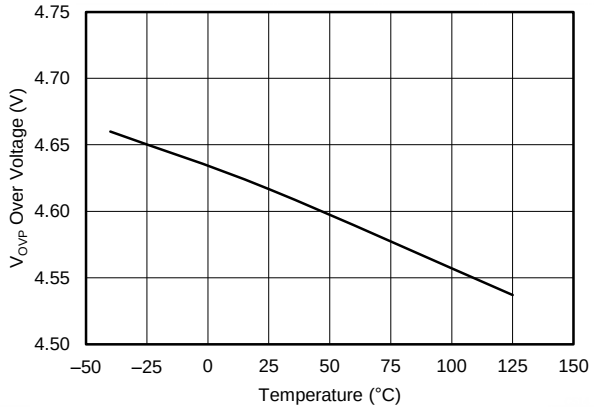


Figure 15. V_{OVP} vs Temperature

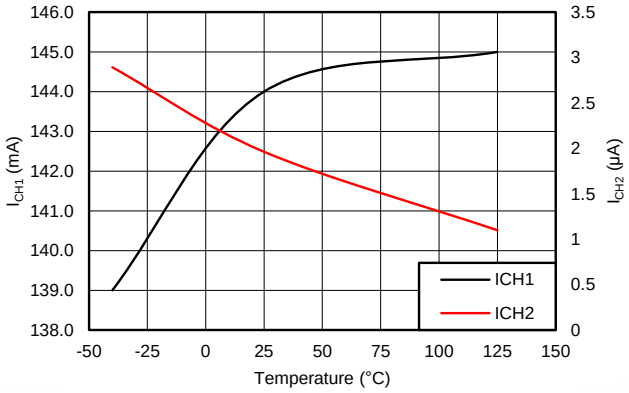


Figure 16. I_{CH1} and I_{CH2} vs Temperature

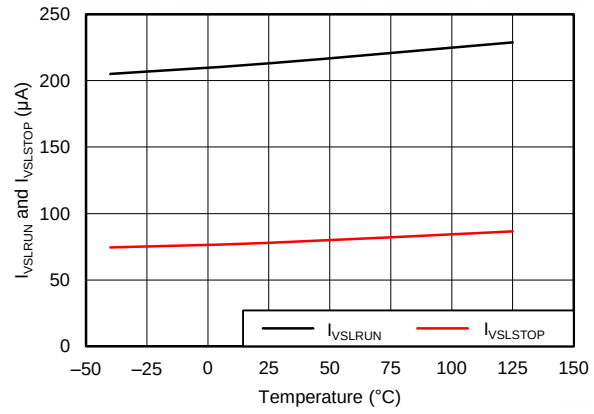


Figure 17. I_{VSLRUN} and $I_{VSLSTOP}$ vs Temperature

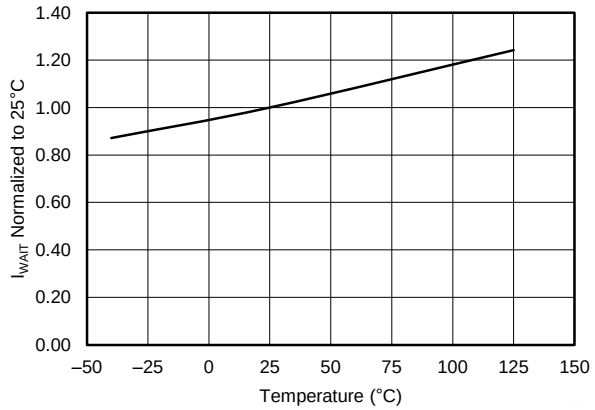


Figure 18. I_{WAIT} vs Temperature

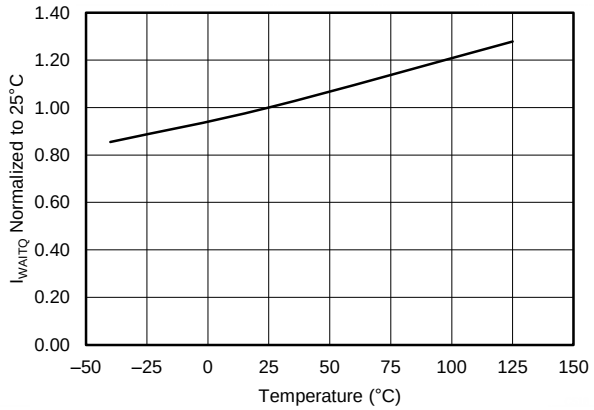


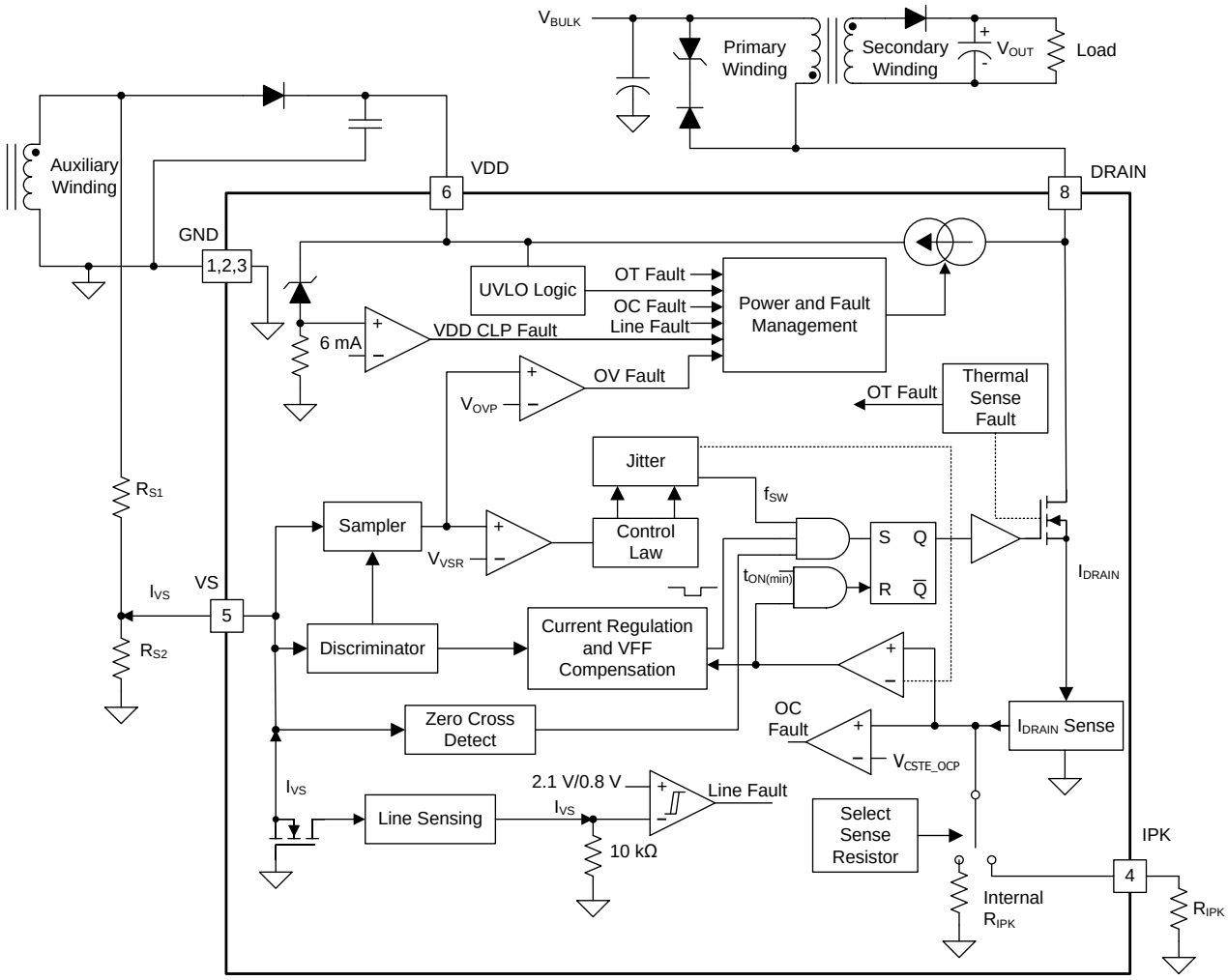
Figure 19. I_{WAITQ} vs Temperature

9 Detailed Description

9.1 Overview

UCC28910 and UCC28911 are HV switchers dedicated to an off-line power supply in an isolated flyback configuration. HV switcher means that each device integrates the power switch, a 700-V power FET, with the control logic. The two devices have the same control logic and they are different only for the Power FET $R_{DS(on)}$ and for the operating current levels. The control logic controls both the output voltage and the output current without the need of an optical coupler. This control method is known as Primary-Side Regulation (PSR) and it operates by analyzing the voltage waveform on the auxiliary winding of the transformer. This allows significant cost saving with respect to traditional control scheme that uses an optical coupler for feedback from a secondary-side shunt regulator. The transformer auxiliary winding is also used to provide housekeeping supply power to the control logic. The device operates in Constant Voltage mode (CV) when it is controlling the output voltage. The device operates in Constant Current mode (CC) when the output current is controlled. The device operates in CV mode or in CC mode according to the load condition. (See Figure 24). A control algorithm that implements both modulation of the switching frequency and the amplitude modulation of the primary current peak, allows the power supply to operate efficiently over the entire load range. The high-voltage current source used for startup is kept off during normal operation thereby minimizing standby power consumption. The device also incorporates a smart power management to minimize its current consumption from the VDD pin. This power consumption is reduced when the converter is lightly loaded or unloaded allowing for a total input power of less than 30 mW when converter input voltage is 265 V_{AC} and unloaded. A number of protection features inside the device allow for improved overall system reliability.

9.2 Functional Block Diagram



9.3 Feature Description

UCC28911 and UCC28910 are flyback power supply switchers which provide accurate output voltage and constant current regulation with primary-side feedback, eliminating the need for optical coupler feedback circuits. The device has an internal 700-V power FET plus a controller which forces the converter to operate in discontinuous conduction mode with valley switching to minimize switching losses. The modulation scheme is a combination of frequency and primary-peak current modulation to provide optimized conversion efficiency over the entire load range. The control law provides a wide dynamic operating range to achieve less than 30-mW standby power.

UCC28911 and UCC28910 include features in the modulator to reduce the EMI peak energy of the fundamental switching frequency and harmonics. Accurate voltage and constant current regulation, fast dynamic response, and fault protection are achieved with primary-side control.

A complete charger solution can be realized with a straightforward design process, low cost and low component count solution.

9.3.1 Primary-Side Voltage Regulation

Figure 20 illustrates a flyback converter. The voltage regulation blocks of the device are shown. The power train operation is the same as any DCM flyback circuit but accurate output voltage and current sensing is the key to primary side control.

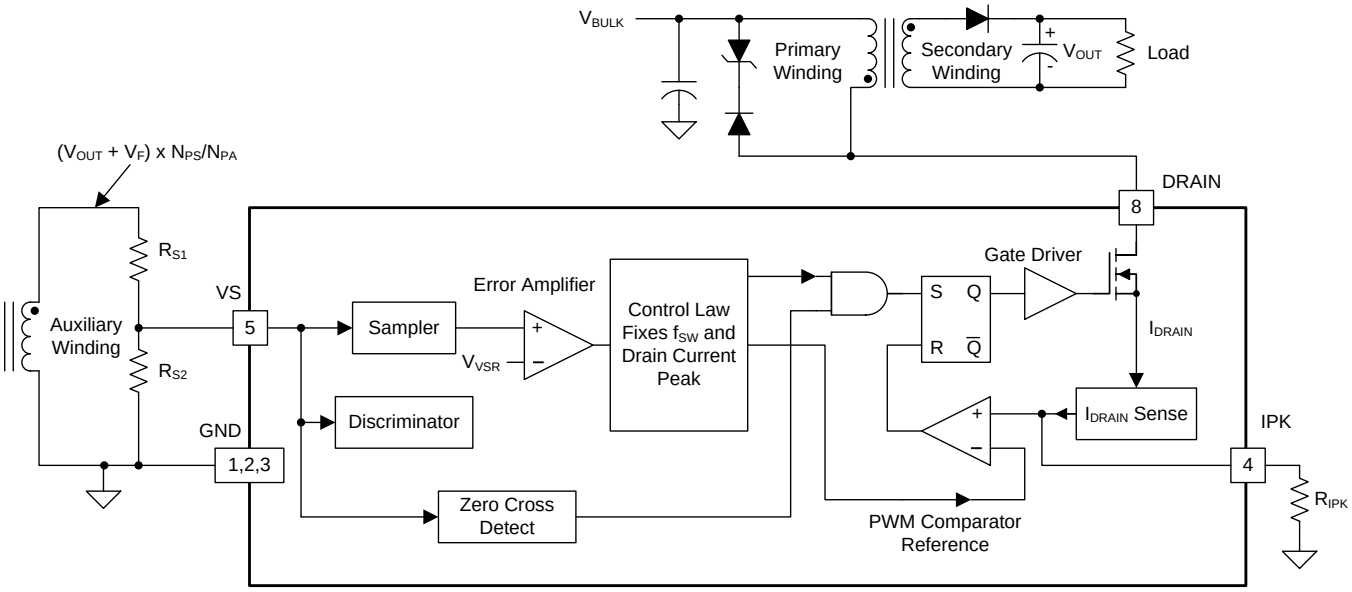


Figure 20. Voltage Loop Block Diagram

Feature Description (continued)

In primary-side control, the output voltage is sensed by the auxiliary winding during the transfer of transformer energy to the secondary. Figure 21 shows the down slope representing a decreasing total rectifier V_F and the secondary winding resistance voltage drop as the secondary current decreases to 0 A. To achieve an accurate representation of the secondary output voltage on the auxiliary winding, the *Discriminator Block* (Figure 20) reliably ignores the leakage inductance reset and ring, continuously samples the auxiliary voltage during the down slope after the ringing is diminished, and captures the error signal at the time the secondary winding reaches 0 current. The internal reference on VS is 4.05 V (V_{VSR} typical); the resistor divider is selected as outlined in the VS pin description.

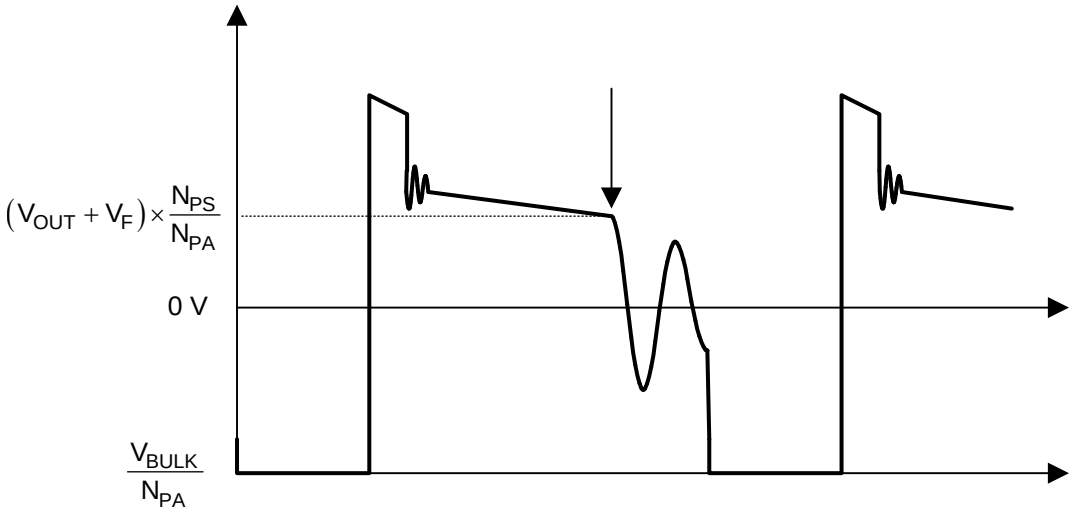


Figure 21. Auxiliary Winding Voltage

Feature Description (continued)

The UCC28910 VS signal *Discriminator Block* (Figure 20) ensures accurate sampling time for an accurate sample of the output voltage from the auxiliary winding. There are however some details of the auxiliary winding signal to ensure reliable operation, specifically the reset time of the leakage inductance and the duration of any subsequent leakage inductance ring. Refer to Figure 22 for a detailed illustration of waveform criteria to ensure a reliable sample on the VS pin. The first detail to examine is the duration of the leakage inductance reset pedestal, t_{LK_RESET}. Since this can mimic the waveform of the secondary current decay, followed by a sharp down-slope, it is important to keep the leakage reset time less than 500 ns for I_{DRAIN} minimum, and less than 1.5 µs for I_{DRAIN} maximum. The second detail is the amplitude of ringing on the auxiliary winding waveform (V_{AUX}) following t_{LK_RESET}. The peak-to-peak voltage at the VS pin should be less than approximately 100 mV_{p-p} at least 200 ns before the end of the demagnetization time, t_{DMAG}. If there is a concern with excessive ringing, it usually occurs during light or no-load conditions, when t_{DMAG} is at the minimum. The tolerable ripple on VS is scaled up to the auxiliary winding voltage by R_{S1} and R_{S2}, and is equal to 100 (R_{S1} + R_{S2}) / R_{S2} mV.

During voltage regulation, the controller operates in frequency modulation mode and amplitude modulation mode. The internal operating frequency limits of the controller are 115 kHz maximum and 420 Hz minimum. The transformer primary inductance and turns ratio sets the maximum operating frequency of the converter. The output preload resistor and efficiency at low power determines the converter minimum operating frequency. There is no external compensation required for the UCC2891x devices.

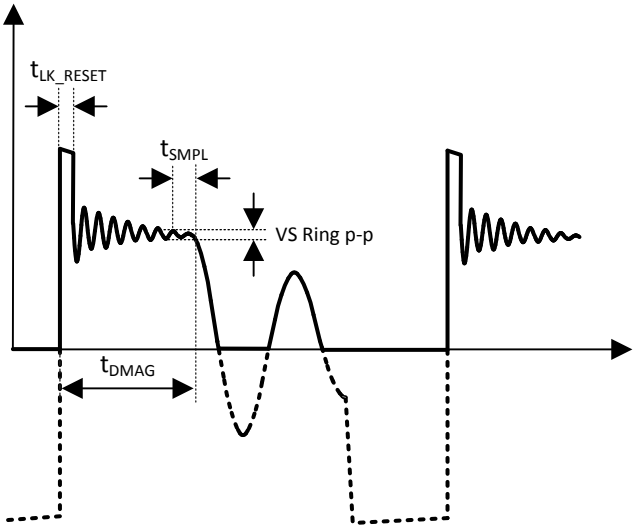
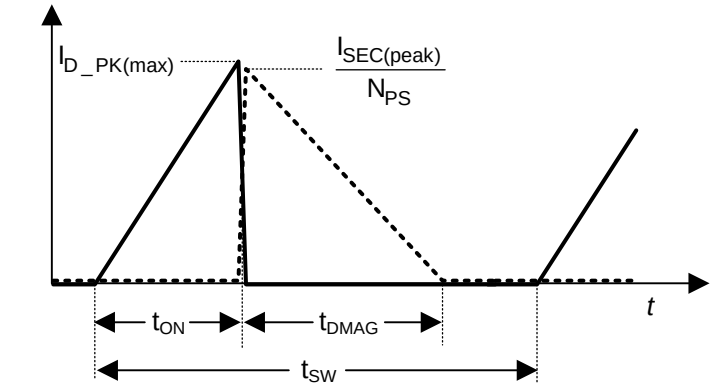


Figure 22. VS Voltage

Feature Description (continued)

9.3.2 Primary-Side Current Regulation

Timing information at the VS pin and the primary current information allow accurate regulation of the secondary average current. The control law dictates that as power is increased in CV regulation and approaching CC regulation the primary-peak current is at $I_{D\_PK(max)} = V_{CSTE(max)} / R_{IPK}$. Referring to Figure 23, the primary-peak current, turns ratio, secondary demagnetization time (t_{DMAG}), and switching period (t_{SW}) establish the secondary average output current. When the average output current reaches the regulation reference in the current control block, the controller operates in frequency modulation mode to control the output current at any output voltage at or below the voltage regulation target as long as the aux winding can keep VDD above the VDD UVLO threshold (VDD_{OFF}).



Primary Current

Secondary Current

$$I_{OUT} = \frac{1}{2} \times I_{S\_PK(max)} \times t_{DMAG} \times f_{SW} = \frac{N_{PS}}{2} \times I_{D\_PK(max)} \times D_{MAGCC}$$

where $D_{MAGCC} = t_{DMAG} \times f_{SW} = K_{CC}$

Figure 23. Output Current Estimation

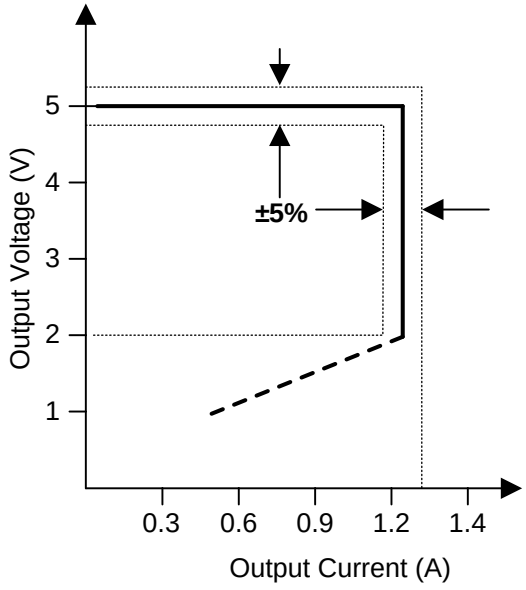


Figure 24. Target Output V-I Characteristic

Feature Description (continued)

K_{CC} is defined as the maximum value of the secondary-side conduction duty cycle (D_{MAGCC} in Figure 23). It is set internally by the UCC2891x and occurs during constant current control mode.

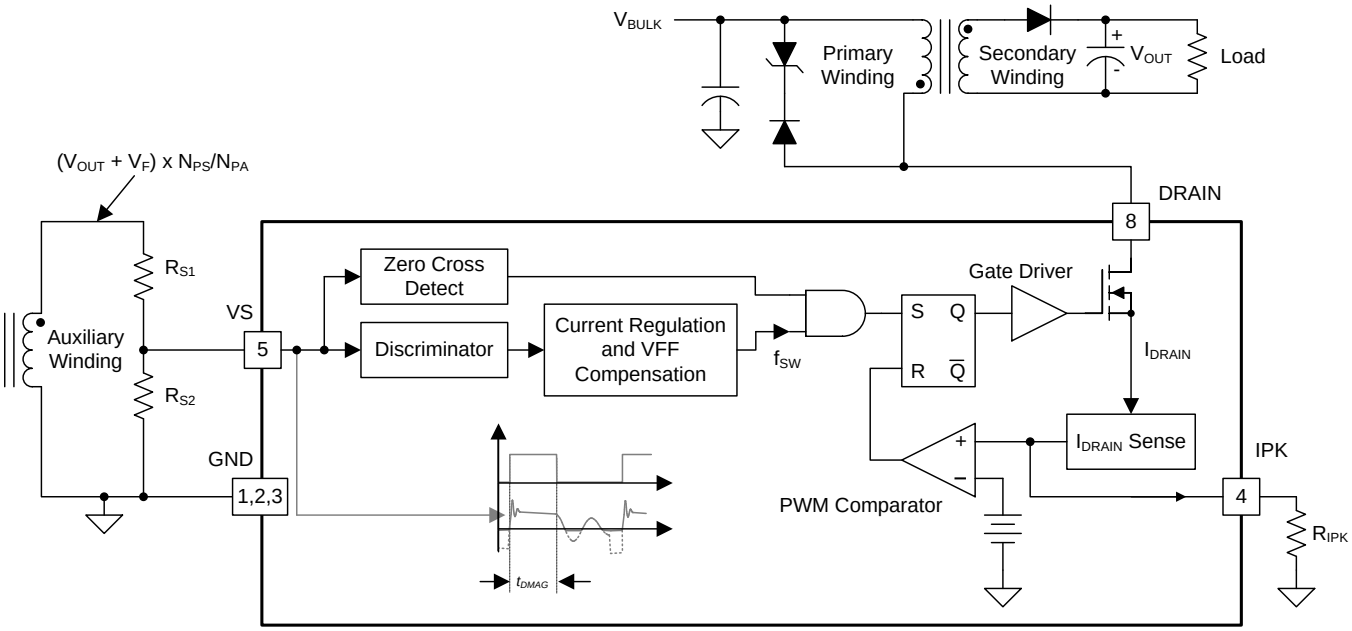


Figure 25. Output Current Control Loop Block Diagram

Feature Description (continued)

9.3.3 Voltage Feed Forward Compensation

During normal operation the on-time is determined by sensing the power FET current and switching off the power FET as this current reaches a threshold fixed by the feedback loop according to the load condition. The power FET is not immediately turned off and its current, that is also the primary winding current, continues to rise for some time during the propagation delay (t_{DELAY} in Figure 26). Keeping the reference for the PWM comparator constant, the value of the primary winding peak current depends on the slope of the primary winding current and t_{DELAY}. The slope of the primary current is proportional to the flyback stage input voltage (V_{BULK})

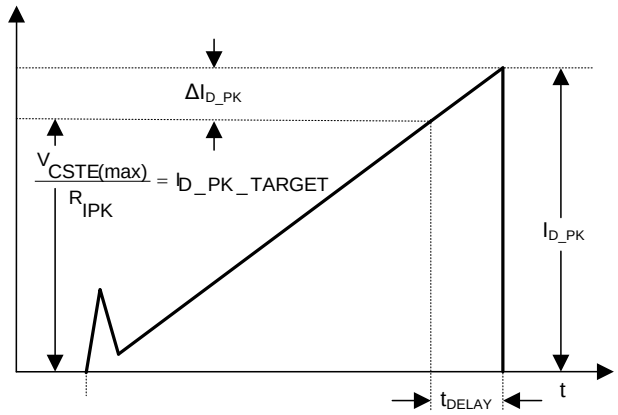


Figure 26. Propagation Delay Effect on the Primary Current Peak

$$\Delta I_{D\_PK} = \frac{V_{BULK}}{L_P} \times t_{delay} \tag{4}$$

$$I_{D\_PK} = I_{D\_PK\_TARGET} + \frac{V_{BULK}}{L_P} \times t_{delay} \tag{5}$$

The current loop estimates the output current assuming the primary winding peak current is equal to the I_{PK_TARGET} and compares this estimated current with a reference to obtain the current regulation. Considering, I_{D_PEAK} is different from $I_{D\_PEAK\_TARGET}$ (see Figure 26) we need to compensate the effect of the propagation delay. The UCC28910 and the UCC28911 incorporate fully-integrated propagation-delay compensation that modifies the switching frequency keeping the output current constant during (CC) Constant Current Mode operation. This function is integrated in the controller and requires no external components. This feature keeps the output current constant despite input voltage variations and primary inductance value spread.

Feature Description (continued)

9.3.4 Control Law

During voltage regulation, the device operates in switching frequency modulation mode and primary current peak amplitude modulation mode. The internal operating frequency limits of the device are $f_{SW(max)}$ and $f_{SW(min)}$. During constant current regulation the device operates only in frequency modulation mode reducing the switching frequency as the output voltage decreases. Figure 27 shows how the primary peak current and the switching frequency change with respect to changes in load. The solid lines are primary-side peak current and the output voltage, the dotted lines are the switching frequency and output current.

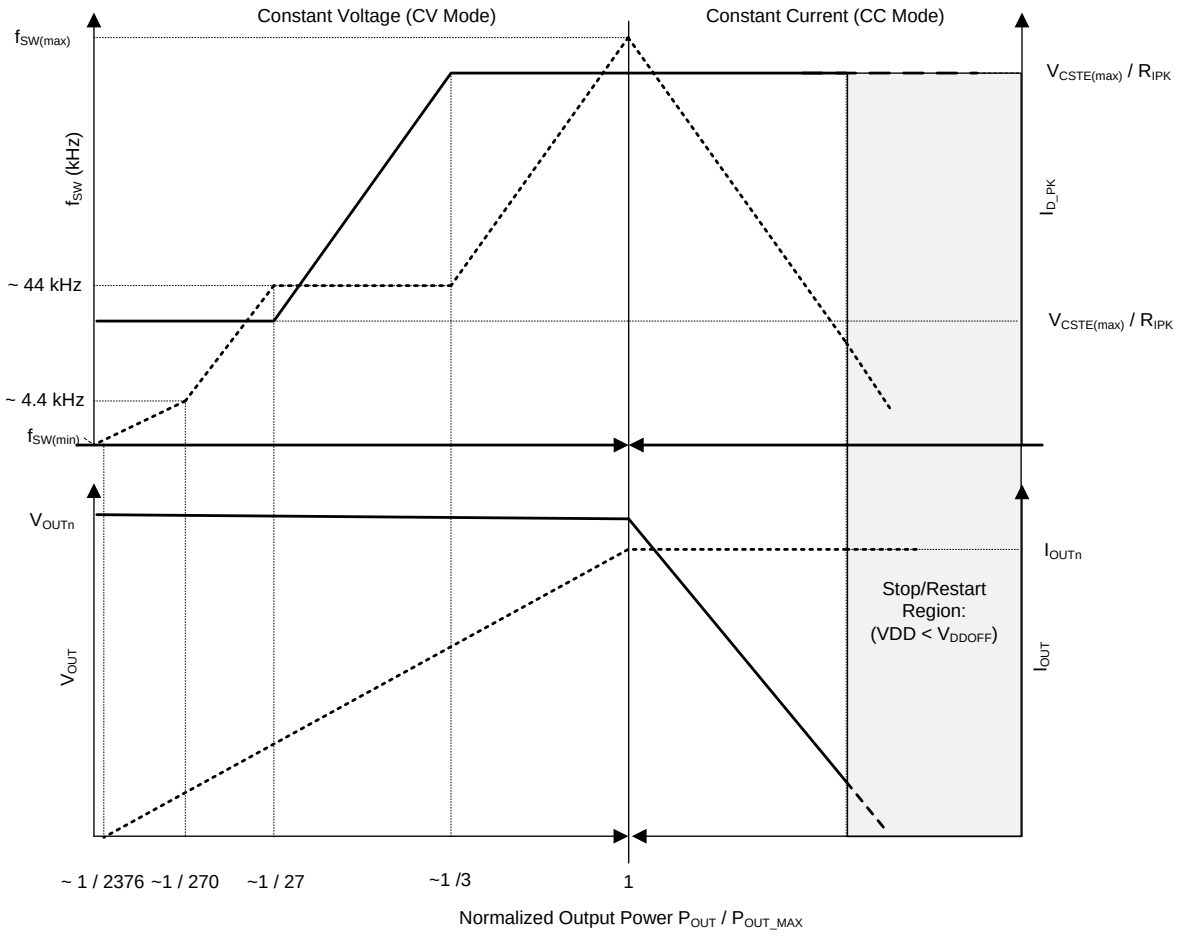


Figure 27. Control Law Profile

Feature Description (continued)

9.3.5 Valley Switching

The UCC28910 and the UCC28911 utilize valley switching to reduce switching losses in the MOSFET and minimize the current spike at the FET turn on. The UCC28910 operates in valley switching in almost all load conditions until the V_{DS} ringing is diminished. By switching at the lowest V_{DS} voltage the MOSFET turn on dV / dt is minimized which is a benefit to reduce EMI.

Referring to Figure 28, devices will operate in a valley switching mode in most load conditions to switch-on at the lowest available V_{DS} voltage. According to the load it is established a minimum switching period. The MOSFET is switched-on at the first valley that occurs after this minimum period is elapsed. With this control scheme the device can be turned-on at the first valley that occurs after transformer demagnetization or it can skip some valleys before turn-on operating in this case in the so called valley skipping mode. Valley switching is maintained during constant current regulation to provide improved efficiency and EMI benefits in constant current operation. If for some reason no valley is detected at the end of the t_{ZTO} time the MOSFET turns-on. In order to guarantee discontinuous mode operation at least the first valley needs to be detected or the Mosfet is not turned-on (see Figure 28).

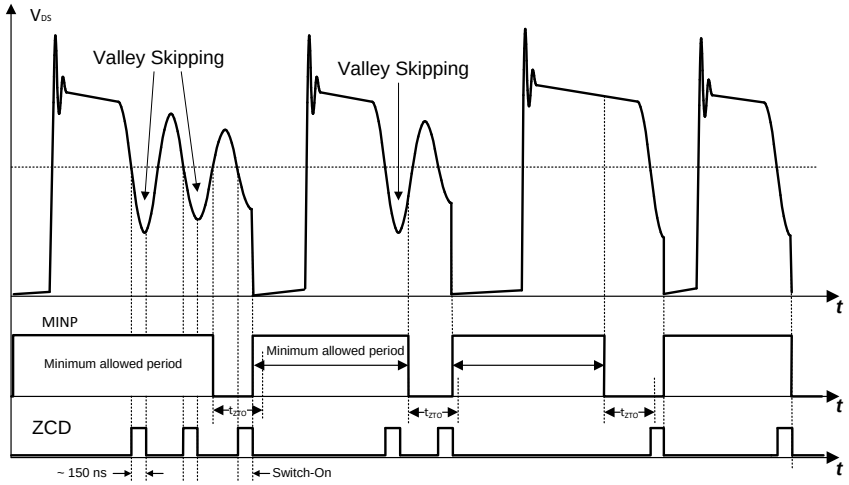


Figure 28. Valley Skipping

In very light-load or no-load condition the V_{DS} ringing amplitude is very low and not easy to detect, moreover with very low ringing amplitude there would be no benefit in valley switching so in this condition the valley switching is disabled (see Figure 29). The device switch on the MOSFET as soon the time t_{ZTO} is elapsed. The t_{ZTO} timer starts as soon as the minimum switching period is elapsed.

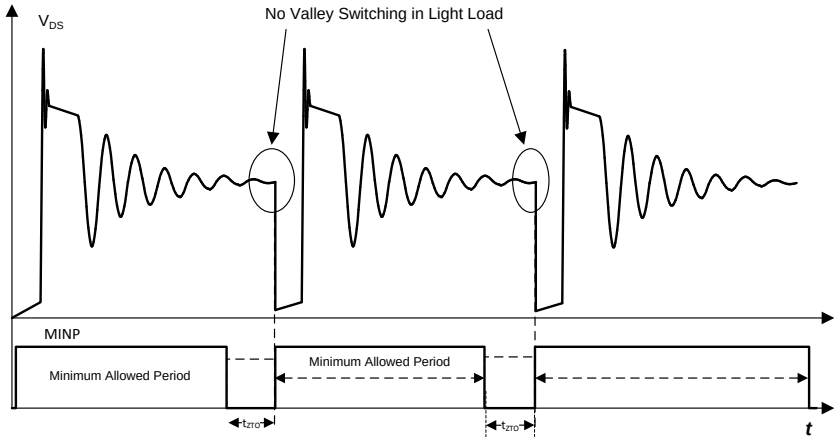


Figure 29. Valley Switching Disable at Light Load

Feature Description (continued)

9.3.6 Startup Operation

The UCC28910 and UCC28911 are provided with a high-voltage current source, connected between the DRAIN pin and the VDD pin; this current source is activated when a voltage is applied on DRAIN pin. The current source charges the capacitor connected between VDD and GND increasing the VDD voltage. As VDD exceeds VDD_{ON} the current source is turned off and the controller internal logic is activated and the device starts switching. If the VDD voltage falls below the VDD_{OFF} threshold, or a fault condition is detected, the controller stops operation and its current consumption is reduced to I_{START} or I_{FAULT}. The high-voltage current source is turned on again when VDD voltage goes below $VDD_{HV(on)}$ (see Figure 30 for reference).

The initial three cycles are limited to $I_{D\_PEAK(max)}$ / 3. This allows sensing any input or output faults with minimal power delivery. After the initial three cycles at $I_{D\_PEAK(max)}$ / 3, the controller responds to the condition dictated by the control law.

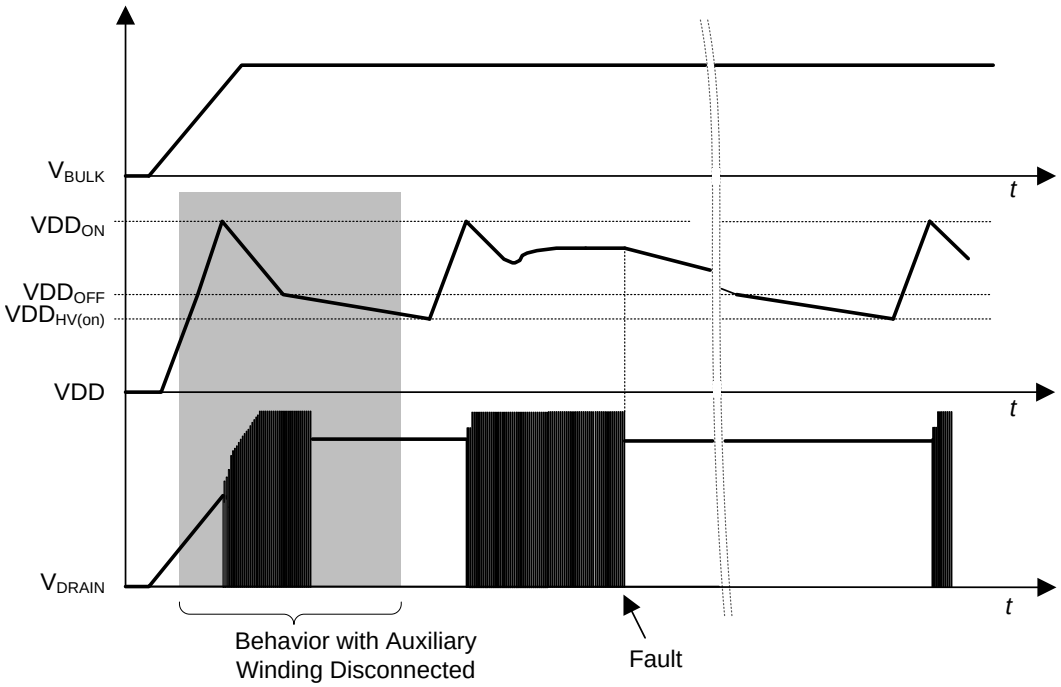


Figure 30. Start Up and Auto Re-Start Operation

The converter remains in DCM during charging of the output capacitor(s), and operates in constant current mode until the output voltage is in regulation.

To avoid high-power dissipation inside the device, such as in the event that VDD is accidentally shorted to GND, the current provided by the high-voltage current source is reduced (I_{CH1}) when VDD < 1 V (typical).

Feature Description (continued)

9.3.7 Fault Protection

There is comprehensive fault protection incorporated into the UCC2891x. Protection functions include:

- Output Over-Voltage Fault
- Input Under-Voltage Fault
- Primary Over-Current Fault
- VDD Clamp Over Current
- Thermal Shut Down

9.3.7.1 Output Over-Voltage

The output over-voltage function is determined by the voltage feedback on the VS pin. If the voltage sample on VS exceeds 4.6 V, which correlates to 113.5% of nominal V_{OUT}, the device stops switching and reduces its current consumption to I_{FAULT}, slowly discharging the VDD capacitor to the $VDD_{HV(on)}$ threshold. At this time the standard startup sequence begins. The initial three cycles of startup at low-peak DRAIN current is important to monitor V_{OUT} and deliver minimal power. The reset and restart, or hiccup, sequence applies for all fault protection. The slow VDD capacitor discharge after a fault allows the high voltage current source to have a low duty cycle to avoid over heating of the device if a fault condition is continuously present resulting in a repetitious start up sequence.

9.3.7.2 Input Under-Voltage

The input under voltage is determined by current information on the VS pin during the MOSFET on time. The VS pin is clamped close to GND during the MOSFET on time; at this time the current though R_{S1} is monitored to determine a sample of the bulk capacitor voltage. The under voltage shutdown current on VS is 75 µA; the enable current threshold is 210 µA. The device must sense the under-voltage condition for three consecutive switching cycles to recognize it as a fault condition. After an under-voltage fault, the same sequence described for output overvoltage occurs.

Feature Description (continued)

9.3.7.3 Primary Over-Current

The UCC28910 and the UCC28911 always operates with cycle-by-cycle primary current control. The normal operating range for the peak DRAIN current depends on the resistance (R_{IPK}) connected between the IPK pin and the GND pin. The peak DRAIN current should not exceed $I_{D\_PEAK(max)}$ even if the IPK pin is shorted to GND, or should not exceed V_{CSTE} / R_{IPK} if the IPK pin is tied to GND with the resistance R_{IPK}. There are different reasons the DRAIN current can go out of control, for example a secondary winding short or hard saturation of the transformer. To avoid over-stress of the power FET additional protections are added. If the DRAIN current exceeds I_{DOCP} (~33% higher than $I_{D\_PEAK(max)}$), such as when IPK pin is shorted to GND, or V_{CSTE_OCP} / R_{IPK}, (V_{CSTE_OCP} ~33% higher than $V_{CSTE(max)}$), and the condition is sensed for three consecutive switching cycles, a fault shutdown and retry sequence, detailed in the output overvoltage fault description, occurs. If the DRAIN current exceeds a second level of current (V_{CSTE_OCP2} / R_{IPK}) it is not necessary to detect the fault for three consecutive switching cycles, the device will stop switching immediately.

9.3.7.4 VDD Clamp Over-Current

The VDD pin is provided with an internal clamp to prevent the pin voltage from exceeding the absolute maximum rating. If the current in the clamp exceeds 6 mA (typical), in order to avoid any damage to the device and to the system, a fault condition is assumed and the device stops operation.

9.3.7.5 Thermal shutdown

The internal thermal shutdown threshold is 150°C (typical) with a hysteresis of 50°C (typical). If an over-temperature is detected the device stops switching and its current consumption is reduced to I_{FAULT}. The VDD voltage will decrease to $V_{DDHV(on)}$ where the high voltage current source is activated and the VDD voltage will rise again until $V_{DD(on)}$ where the internal logic is re-activated. If the temperature of the device is not dropped below approximately 100°C (150°C- 50°C) no switching cycles occurs and the fault condition is maintained and the current consumption is again I_{FAULT}. For diagnostic purpose, when a thermal shut down occurs a short voltage pulse, whose amplitude is around 2 V, is transmitted on the I_{PK} pin. Thermal shut down feature is not intended to protect the device itself but mainly to control the damage caused by the device thermally overstressed.

9.4 Device Functional Modes

According to the input voltage, the VDD voltage, and the load conditions, the device can operate in different modes:

1. At start-up with V_{DRAIN} > 20 V, VDD = 0 V, the HV voltage current source is ON and starts to charge the capacitor connected to the VDD pin. With VDD < 1 V the current provided is limited < 500 µA and VDD rises slowly.
2. When VDD exceeds 1 V (VDD < VDD_{ON}) the HV current source provides higher current and VDD rises faster.
3. When VDD exceeds VDD_{ON} the device starts switching and delivers power to its output. According to its load, the converter operates in CV mode or in CC mode.
   (a) CV mode means that the converter keeps the output voltage constant. This operating mode takes place when $R_{LOAD} > V_{OCV} / I_{OCC}$ where V_{OCV} is the target for output voltage and I_{OCC} is the maximum converter output current. In this condition the converter output voltage $V_{OUT} = V_{OCV}$ and the converter output current $I_{OUT} < I_{OCC}$.
   (b) CC mode means that the converter keeps the output current constant. This operating mode takes place when $R_{LOAD} < V_{OCV} / I_{OCC}$. In this condition the converter output voltage $V_{OUT} < V_{OCV}$ and the converter output current $I_{OUT} = I_{OCC}$.
4. Device operations can be stopped because of the events listed below:
   (a) If VDD drops below VDD_{OFF}, the device stops switching and its current consumption is lowered to I_{START}. Because the converter is not switching, no energy is delivered from the auxiliary winding, the HV current source is off, then the VDD capacitor is discharged with I_{START} current.
   (b) If a fault is detected device stops switching and its current consumption is lowered to I_{FAULT} that slowly discharges the VDD capacitor down to VDD_{OFF} where the current consumption is $I_{START} < I_{FAULT}$ and the VDD capacitor continues to discharge.
5. After the device stops switching, because of 4a or 4b, the VDD voltage drops, when it goes below $VDD_{HV(on)}$, the HV current source is turned on recharging the VDD capacitor up to VDD_{ON}.
6. When a fault condition is permanently present, the device operates in auto restart-mode. This means that a fault condition is detected, the device stops operation as described in 4b, then VDD drops down to $VDD_{HV(on)}$ when the device start-up sequence takes place. At device turn-on, the fault is again detected and the cycle repeats.

10 Applications and Implementation

10.1 Application Information

The UCC28910 and UCC28911 devices are HV switcher that integrates an HV power FET plus a controller that uses primary-side-regulated (PSR), supporting magnetically-sensed output voltage regulation via the transformer bias winding. This sensing eliminates the need for a secondary-side reference, error amplifier and optical-isolator for output voltage regulation. The devices deliver accurate output voltage static load and line regulation, and accurate control of the output current. The magnetic sampling scheme allows operation only in discontinuous conduction mode (DCM) so the device is not allowed to turn on the Power FET if it doesn't sense a ZCD event. A ZCD event is when auxiliary winding voltage crosses zero from high to low after transformer demagnetization is completed. The modulator adjusts both frequency and peak current in different load regions to maximize efficiency throughout the operating range. The smart management of the control logic power consumption and the HV current source, used for startup that is off during operation and have very low leakage current, allow designing converters with very low standby input power. The less than 30mW can be easily achieved with these devices.

10.2 Typical Application

10.2.1 Battery Charger, 5 V, 6 W

This design example describes the UCC28910FBEVM-526 design and outlines the design steps required to design a constant-voltage, constant-current flyback converter for a 5-V/6-W charger. Discontinuous conduction mode (DCM) with valley switching is used to reduce switching losses. A combination of switching frequency and peak primary current amplitude modulation is used to keep conversion efficiency high across the full load and input voltage range. Figure 31 below details the output V-I characteristic. Low system parts count and built in advanced protection features result in a cost-effective solution that meets stringent world-wide energy efficiency requirements.

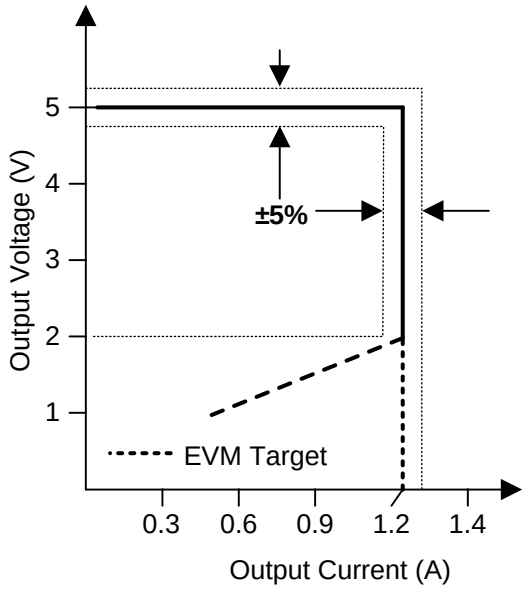


Figure 31. Target Output V-I Characteristic

Typical Application (continued)

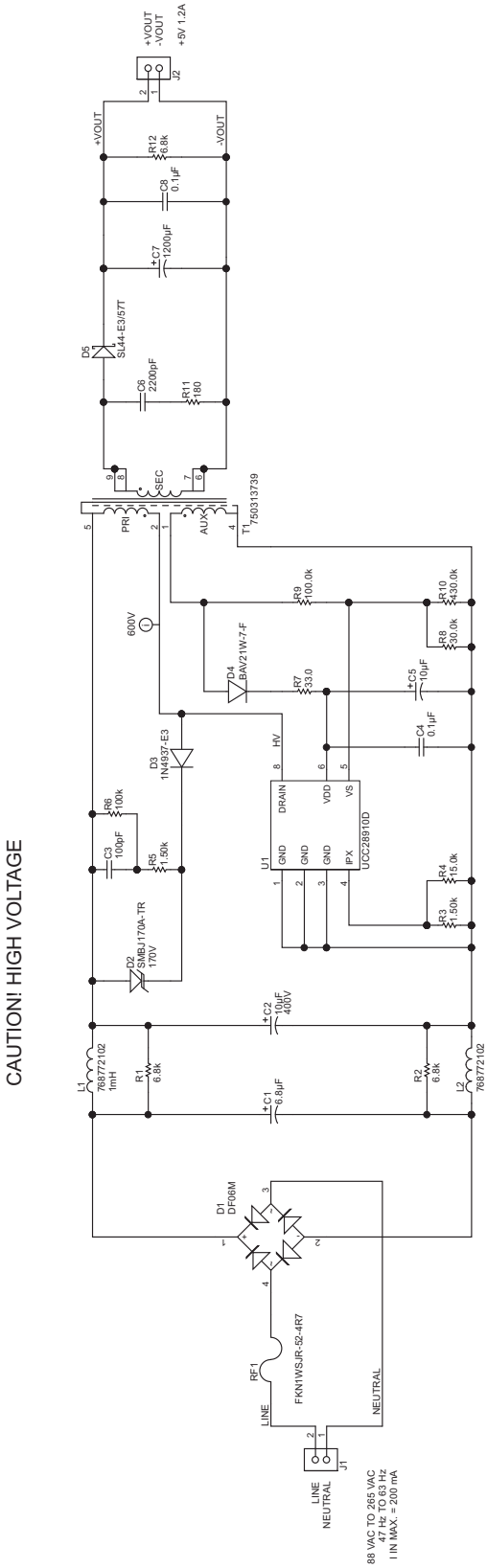


Figure 32. UCC28910FBEVM-526 Schematic

Typical Application (continued)

10.2.1.1 Design Requirements

For this design example, use the parameters listed in Table 1.

Table 1. Design Parameters

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
INPUT CHARACTERISTICS						
V_{IN}	Input voltage		90	115/230	265	V
f_{LINE}	Frequency		47	50/60	64	Hz
P_{NL}	No load power	$V_{IN} = V_{NOM}$ I_{OUT} = 0 A		15	20	mW
V_{INUVLO}	Brownout voltage	$I_{OUT} = I_{NOM}$		70		V
V_{INOV}	Brownout recovery voltage			80		V
I_{IN}	Input current	$V_{IN} = V_{MIN}$, I_{OUT} = max		0.2		A
OUTPUT CHARACTERISTICS						
V_{OUT}	Output voltage	$V_{IN} = V_{MIN}$ to V_{MAX}, I_{OUT} = 0 V to I_{NOM}	4.75	5.00	5.25	V
$I_{OUT(max)}$	Maximum output current	$V_{IN} = V_{MIN}$ to V_{MAX}	1.14	1.20	1.26	A
$I_{OUT(min)}$	Minimum output current	$V_{in} = V_{min}$ to V_{MAX}		0		A
ΔV_{OUT}	Output voltage ripple	$V_{IN} = V_{MIN}$ to V_{MAX}, I_{OUT} = 0 V to I_{NOM}		150		mV
P_{OUT}	Output power	$V_{IN} = V_{MIN}$ to V_{MAX}				
SYSTEM CHARACTERISTICS						
η	Average efficiency	25%, 50%, 75%, 100% of I_{OUT}		75%		
ENVIRONMENTAL						
	Conducted EMI		Meets CISPR22B/EN55022B			

10.2.1.2 Detailed Design Procedure

This procedure outlines the steps to design a constant-voltage, constant-current flyback converter based on UCC28910 switcher. Refer to the Figure 33 for component names and network locations. The design procedure equations use terms that are defined below.

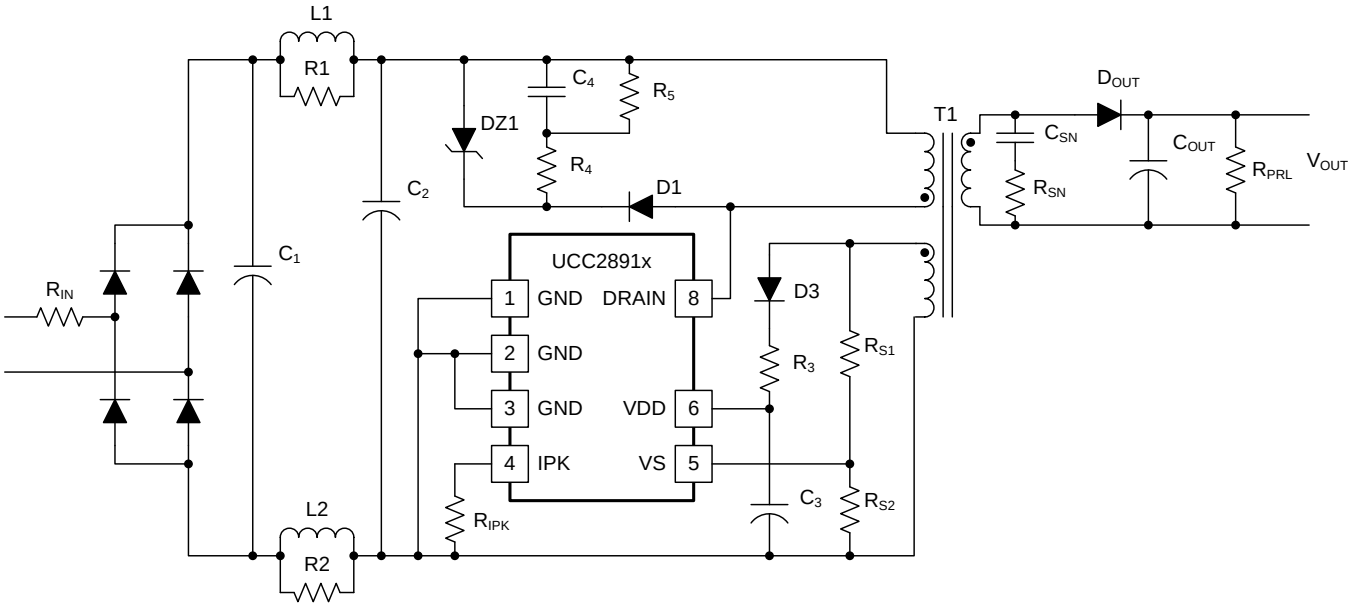


Figure 33. Standard Flyback Converter Based on UCC2891x

10.2.1.2.1 Power Handling Curves

The power handling curves give the maximum output power that can be handled by the devices versus the ambient temperature. These curves give the maximum output power achievable considering that the losses inside the device can cause rise of the junction temperature up to 125°C. The thermal resistance junction to ambient were provided with considerations to two different values. Thermal resistances values of 50°C /W and of 100°C / W were considered.

The device handling capability depends on the overall design and input and output voltage. Figure 34 and Figure 36 refer to a wide-range input voltage (90 V_{AC}; 264 V_{AC}) converter; Figure 35 and Figure 37 refer to a European range input voltage (180 V_{AC}; 265 V_{AC}). The dotted line curves refer to 12-V output voltage AC-to-DC converter, the continuous line curves refer to 5-V output voltage converter.

Figure 34 and Figure 35 show the power handling capabilities of UCC28910 and Figure 36 and Figure 37 show the power handling capabilities of UCC28911.

Table 2. Maximum Output Power(1)

PART NUMBER	180 V_{AC} to 265 V_{AC}		90 V_{AC} to 265 V_{AC}		UNITS
	Adapter (2)	Open Frame (3)	Adapter(2)	Open Frame (3)	
UCC28910	6.5	9.5	6	7.5	W
UCC28911	8	12	7.5	10	W

(1) Table 2 is obtained considering 125°C as maximum junction temperature. For lower operating maximum junction temperature, the maximum output power should be lower.
(2) Typical continuous power in enclosed adapter at 50°C ambient, with adequate (> 560 mm^2) copper area connected on GND pin to have 90°C/W as junction to ambient thermal resistance.
(3) Maximum continuous power with open frame design at 50°C ambient, with adequate copper area connected on GND pin and/or adequate air flow to have 50°C/W as junction to ambient thermal resistance.

The curves provided show the maximum power obtained through optimized designs.

A lower-efficiency design requires the converter to process more input power to deliver the same amount of power to the load. Therefore, less power handling capability is expected for lower-efficiency designs.

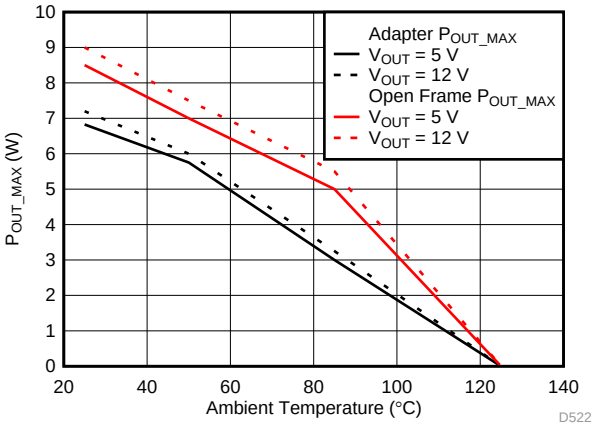


Figure 34. [90; 264] VRMS Input Voltage Range, (maximum input power vs ambient temperature of UCC28910)

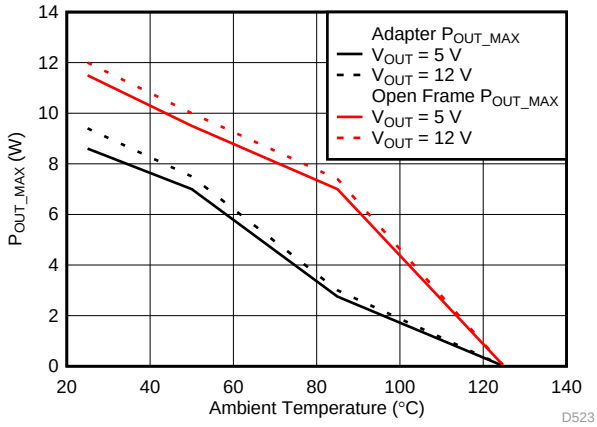


Figure 35. [180; 264] VRMS Input Voltage Range, (maximum input power vs ambient temperature of UCC28910)

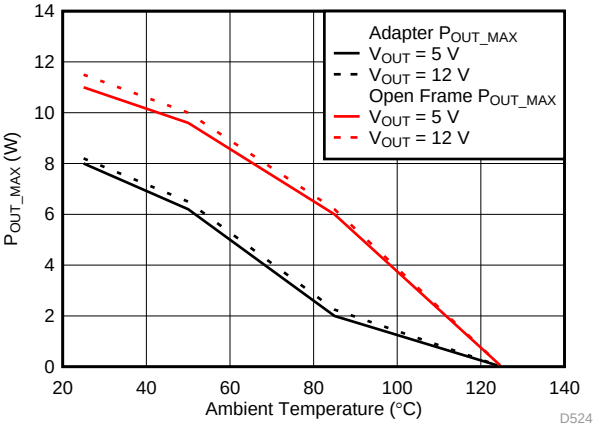


Figure 36. 90 V_{RMS}, 264 V_{RMS} Input Voltage Range, (maximum output power vs ambient temperature of UCC28911)

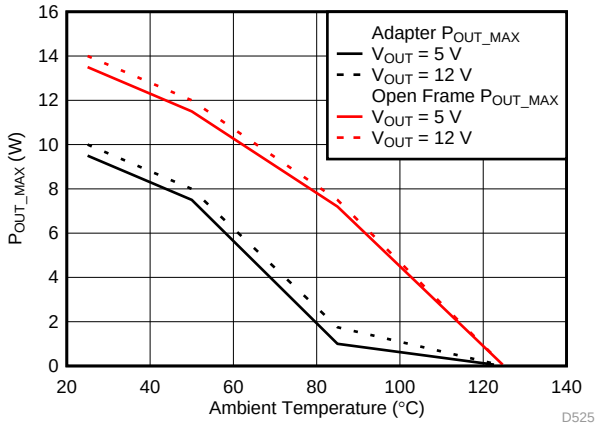


Figure 37. 180 V_{RMS}, 264 V_{RMS} Input Voltage Range, (maximum output power vs ambient temperature of UCC28911)

10.2.1.2.2 Input Stage Design and Bulk Capacitance

The input stage consists of:

1. Input fuse resistor (R_{IN}) is generally used to:
   (a) Limit the inrush current on the input capacitor when the line voltage is applied.
   (b) Disconnect the line in case of input over current.
2. A bridge diode or a single-wave rectifier diode used to rectify the main voltage.
3. A bulk capacitor (capacitors C1 and C2) that stores the energy and reduces input voltage ripple.
4. A line filter (L1, L2, R1, and R2) to reduce EMI generated by switching.

The minimum input capacitance voltage, the input power of the converter based on target full-load efficiency, minimum input RMS voltage, and minimum AC input frequency are used to determine the input capacitance requirement.

The maximum converter input power can be estimated from the output voltage in voltage constant mode, V_{OCV}, the converter's output current when operating in constant current more, I_{OCC}, and the full-load efficiency target, η.

$$P_{IN} = \frac{V_{OCV} \times I_{OCC}}{\eta} \tag{6}$$

The following equation provides an accurate solution for input capacitance based on a target minimum bulk capacitor voltage. To target a given input capacitance value, iterate the minimum capacitor voltage to achieve the target capacitance.

$$C_{BULK} = \frac{\frac{2 \times P_{IN}}{f_{LINE(min)}} \times \left(\frac{1}{RCT} - \frac{1}{2 \times \pi} \times \arccos\left(\frac{V_{BULK(min)}}{\sqrt{2} \times V_{IN(min)}} \right) \right)}{\sqrt{2} \times V_{IN(min)}^2 - V_{BULK(min)}^2} \tag{7}$$

In the case where the input rectifier is a single diode (half wave rectifier) , and for applications with bridge input rectifier (full wave rectifier), as in the schematic of Figure 31.

The voltage $V_{BULK(min)}$ is generally selected around 65% to 60% of $\sqrt{2}$ x $V_{IN(min)}$. $V_{BULK(min)}$ is determined by the selection of the high-voltage input capacitors.

For the considered example we have:

$$P_{IN} = \frac{V_{OCV} \times I_{OCC}}{\eta} = \frac{5V \times 1.2A}{0.72} = 8.33W \tag{8}$$

$$C_{BULK} = \frac{\frac{2 \times 8.33W}{57Hz} \times \left\{ \frac{1}{2} - \frac{1}{2 \times \pi} \times \arccos\left(\frac{80V}{124V} \right) \right\}}{2 \times (88V)^2 - (80V)^2} = 11.7\mu F \tag{9}$$

Taking into account that electrolytic capacitance, with 20% of tolerance, the values selected for C1 and C2 are: C1 = 6.8 µF and C2 = 10 µF.

10.2.1.2.3 Transformer Turns Ratio

The maximum primary-to-secondary turns ratio can be determined by the target maximum switching frequency at full load, the minimum input capacitor bulk voltage, and the estimated DCM quasi-resonant time. Initially determine the maximum available total duty cycle of the on-time and secondary conduction time based on target switching frequency and DCM resonant time. For DCM resonant time, assume t_R = 1 / 500 kHz if you do not have an estimate from previous designs. For the transition mode operation limit, the period required from the end of secondary current conduction to the first valley of the V_{DS} voltage is half of the DCM resonant period, or 1 µs assuming 500-kHz resonant frequency. D_{MAX} can be determined using the equation below.

$$D_{MAX} = 1 - \left(\frac{t_R}{2} \times f_{SW(max)} \right) - K_{CC} \tag{10}$$

Where K_{CC} is the regulation gain in constant current control mode and is equal to the secondary diode conduction duty cycle when the converter is operating at maximum output current.

Once D_{MAX} is known, the maximum turn ratio of the primary-to-secondary can be determined with the equation below.

$$N_{PS(max)} = \frac{D_{MAX} \times V_{BULK(min)}}{K_{CC} \times \left(V_{OCV} + V_F \right)} \tag{11}$$

The total voltage on the secondary winding needs to be determined; the sum of V_{OCV} and the secondary rectifier V_F. The voltage $V_{BULK(min)}$ is generally selected around 65% or 60% of the peak of low-line. $V_{BULK(min)}$ is determined by the selection of the high-voltage input capacitors.

For the 5-V USB charger applications N_{PS} values from 13 to 17 are typically used.

For our example the maximum value for primary to secondary turn ratio will be:

$$N_{PS(max)} = \frac{0.482 \times 80\,V}{0.413 \times \left(5V + 0.35\,V \right)} = 17.45 \tag{12}$$

In this example we fix N_{PS} = 16.5

In order to calculate the primary to auxiliary turn ratio (N_{PA}) we use the parameter $V_{OCC(min)}$ that is the minimum output voltage at which we want to guarantee the output current regulation.

$$N_{PA} = N_{PS} \times \frac{\left(V_{OCC(min)} + V_F \right)}{VDD_{OFF(max)} + V_{FAUX}} \tag{13}$$

In the example:

$$N_{PA} = 16.5 \times \frac{\left(2\,V + 0.35\,V \right)}{7\,V + 0.5\,V} = 5.17 \tag{14}$$

In Equation 13 V_{FAUX} is the D3 diode voltage drop when conducting. The value of N_{PA} is generally under-estimated and the number of auxiliary winding turns can be reduced with respect to the value provided by Equation 13. Optimization can be done directly on the circuit verifying the margin between the VDD's measured value and $VDD_{OFF(max)}$.

10.2.1.2.4 Output Capacitance

The output capacitance value is typically determined by the transient response requirement from no load. For example, in USB charger applications, it is often required to maintain a minimum output voltage of 4.1 V with a load-step transient from 0 mA to 500 mA (I_{TRAN}). The equation below assumes that the switching frequency is at the minimum of $f_{SW(min)}$.

$$C_{OUT} = \frac{I_{TRAN}}{V_{O\Delta} \times f_{SW(min)}} \tag{15}$$

$$C_{OUT} = \frac{500\,mA}{(5\,V - 4.1V) \times 420\,Hz} = 1.3\,mF \tag{16}$$

Another consideration on the output capacitor(s) is the ripple voltage requirement which is reviewed based on secondary-peak current and ESR. A margin of 20% is added to the capacitor ESR requirement in the equation below.

$$R_{ESR} < \frac{V_{RIPPLE}}{I_{D\_PK(max)} \times N_{PS}} \times 0.8 \tag{17}$$

V_{RIPPLE} is the maximum output-voltage ripple allowed for the design. The UCC2891x devices incorporates internal voltage-loop compensation circuits so that external compensation is not necessary, provided that the value of C_{OUT} is high enough. The following equation determines a minimum value of C_{OUT} necessary to maintain a phase margin >30 degrees over the full-load range.

$$C_{OUT} \geq \frac{400 \times I_{OCC}}{V_{OCV} \times f_{SW(max)}} \tag{18}$$

10.2.1.2.5 VDD Capacitance, C_{VDD}

The capacitance on VDD needs to supply the device operating current until the output of the converter reaches the target minimum operating voltage in constant-current regulation. At this time the auxiliary winding can sustain the supply voltage. The output current available to the load to charge the output capacitors is the constant-current regulation target. The equation below assumes the output current of the flyback is available to charge the output capacitance until the minimum output voltage is achieved. C_{VDD} capacitor is the C3 capacitor in the schematic of Figure 33.

$$C_{VDD} = \frac{C_{OUT} \times V_{OCC} \times I_{RUN(max)}}{I_{OCC} \times \Delta V_{UVLO}} \tag{19}$$

10.2.1.2.6 VS Resistor Divider

The VS divider resistors determine the output voltage regulation point of the flyback converter, also the high-side divider resistor (R_{S1}) determines the line voltage at which the controller enables continuous switching operation. R_{S1} is initially determined based on transformer auxiliary to primary turn ratio and desired input voltage operating threshold.

$$R_{S1} = \frac{V_{INAC(min)} \times \sqrt{2}}{N_{PA} \times I_{VSLRUN(max)}} = \frac{124\,V}{5.17 \times 215\,\mu A} = 112\,k\Omega \tag{20}$$

In our example the selected value of R_{S1} was 100 kΩ.

The low-side VS pin resistor is selected based on desired output voltage regulation.

$$R_{S2} = \frac{V_{VSR} \times R_{S1} \times N_{PA}}{(V_{OUT} + V_F) \times N_{PS} - (V_{VSR} \times N_{PA})} = \frac{4\,V \times 100\,k\Omega \times 5.17}{(5\,V + 0.35\,V) \times 16.5 - (4\,V \times 5.17)} = 30.5\,k\Omega \tag{21}$$

The value selected for R_{S2} resistance was 30 kΩ.

10.2.1.2.7 R_{VDD} Resistor and Turn Ratio

The value of R_{VDD} and the auxiliary-to-secondary turns ratio should be selected with care in order to be sure that the VDD is always higher than the VDD_{OFF} (7 V maximum) threshold under all operating conditions. The R_{VDD} resistor also limits the current that can go into the VDD pin preventing I_{VDDCLP_OC} clamp over-current protection from being erroneously activated.

10.2.1.2.8 Transformer Input Power

The power at the transformer input during full-load condition is given by the output power plus the power loss in the output diode plus the power consumption of the UCC2891x control logic (V_{VDD} × I_{RUN}) divided by the transformer efficiency that takes into account all the losses due to the transformer: copper losses, core losses, and energy loss in the leakage inductances.

$$P_{INTRX} = \frac{(V_{OCV} + V_F) \times I_{OCC} + V_{VDD} \times I_{RUN}}{\eta_{XFMR}} \tag{22}$$

10.2.1.2.9 R_{IPK} Value

The R_{IPK} value sets the value of the DRAIN current peak that equals the transformer primary winding current peak value. This value also sets the value of the output current when working in CC mode according to the following formula:

$$I_{OUT} = \left(\sqrt{\eta_{XFMR} - \frac{V_{VDD} \times I_{RUN}}{P_{INTRX}}} \right) \times N_{PS} \times \frac{1}{2} \times I_{D\_PK(max)} \times D_{MAGCC} = \left(\sqrt{\eta_{XFMR} - \frac{V_{VDD} \times I_{RUN}}{P_{INTRX}}} \right) \times N_{PS} \times \frac{1}{2} \times \frac{V_{CCR}}{R_{IPK}}$$

where

- K_{CC} is the secondary diode conduction duty cycle Electrical Characteristics
- N_{PS} is the primary-to-secondary transformer turns ratio
- V_{CCR} is the defined as $V_{CCR} = V_{CSTE(max)} \times K_{CC}$ and the value is specified in the Electrical Characteristics (23)

The term $\left(\sqrt{\eta_{XFMR} - \frac{V_{VDD} \times I_{RUN}}{P_{INTRX}}} \right)$ takes into account that not all the energy stored in the transformer goes to the secondary side but some of this energy, through the auxiliary winding, is used to supply the device control logic. The transfer of energy always happens with unavoidable losses. These losses are accounted for through the transformer efficiency term (η_{XFMR}). For a fixed target value for I_{OUT}, the value of R_{IPK} can be calculated using the following formula:

$$R_{IPK} = \left(\sqrt{\eta_{XFMR} - \frac{V_{VDD} \times I_{RUN}}{P_{INTRX}}} \right) \times N_{PS} \times \frac{1}{2} \times \frac{V_{CCR}}{I_{OUT}} \quad (24)$$

For the example:

$$P_{INTRX} = \frac{(5\,V + 0.35\,V) \times 1.2\,A + 28\,V \times 2.9\,mA}{0.9} = 7.25\,W \quad (25)$$

$$R_{IPK} = \left(0.9 - \frac{2 \times 28\,V \times 2.9\,mA}{7.25\,W} \right) \times 16.5 \times \frac{1}{2} \times \frac{223\,V}{1.2\,A} = 1.374\,k\Omega \quad (26)$$

10.2.1.2.10 Transformer Primary Inductance Value

After you have fixed the maximum switching frequency and the maximum value of the primary current peak for your application, the primary inductance value can be fixed by the following equation:

$$L_{P(min)} = \frac{2 \times P_{INTRX}}{(1 - L_P\_Tol) \times f_{TARGET(max)} \times I^2_{D\_PK(max)}} \quad (27)$$

L_P_Tol is the tolerance on the primary inductance value of the transformer. Typical values of L_P_Tol are between ±10% and ±15%)

$I_{D\_PK(max)}$ is given by:

$$I_{D\_PK(max)} = \frac{V_{CCR}}{R_{IPK}} \quad (28)$$

For the example:

$$L_P = \frac{2 \times 7.25\,W}{(1 - 0.1) \times 105\,kHz \times \left(\frac{540}{1.37}\right)^2} = \frac{14.5\,W}{0.9 \times 105\,kHz \times (395\,mA)^2} \cong 1mH \quad (29)$$

10.2.1.2.10.1 Secondary Diode Selection

The maximum reverse voltage that the secondary diode had to sustain can be calculated by the equation below where a margin of 30% is considered. Usually for this kind of application a Schottky diode is used to reduce the power losses due to the lower forward voltage drop. The maximum current rating of the diode is generally selected between two and five times the maximum output current (I_{OCC}).

$$V_{REV} = \left(V_{OCV} + \frac{V_{IN(max)} \times \sqrt{2}}{N_{PS}}\right) \times 1.3 \quad (30)$$

$$V_{REV} = \left(5\,V + \frac{265 \times \sqrt{2}}{16.5}\right) \times 1.3 = 36\,V \quad (31)$$

10.2.1.2.11 Pre-Load

When no load is applied on the converter output, the output voltage rises until the OVP (over voltage protection) of the device is tripped, because the device cannot operate at zero switching frequency. The device's minimum switching frequency of 420 Hz will always deliver some energy to the output, causing the voltage to rise at no load. To avoid this, an R_{PRL} (pre-load resistance) is used. The value of this pre-load can be selected using the following equation:

$$R_{PRL} = \frac{V^2_{OCV}}{\frac{\eta_{XFMR}}{2} \times L_P \times (1 + L_P\_Tol) \times f_{MAX} \times \left(\frac{I_{D\_PK(max)}}{K_{AM}}\right)^2 - VDD_{OFF(min)} \times I_{WAITQ(min)}} \quad (32)$$

$$R_{PRL} = \frac{(5\,V)^2}{\frac{0.9}{2} \times 1mH \times (1.1) \times f_{SW(min)} \times \left(\frac{395\,mA}{3}\right)^2 - 7\,V \times 200\,\mu A} \cong 6.8\,k\Omega \quad (33)$$

10.2.1.2.12 DRAIN Voltage Clamp Circuit

The main purpose of this circuit, as in most flyback converters, is to prevent the DRAIN voltage from rising up to the FET break-down voltage, at the FET turn-off, and destroying the FET itself. An additional task, required by the primary-side regulation mechanism, is to provide a clean input to the VS pin by damping the oscillation that is typically present on the DRAIN voltage due to the transformer primary leakage inductance.

To perform damping, the D2 diode (refer to Figure 38) selected should not be a fast recovery diode (0.3 µs < t_{rr} < 1 µs) so the reverse current can flow in the R_{LC} over damped circuit. This R_{LC} circuit is formed by the transformer primary-leakage inductance (L_{LKP}), the resistance R4, and the capacitance C4. To ensure proper damping the resistance R4 has to satisfy the following condition:

$$R_4 > 2 \times \sqrt{\frac{L_{LKP}}{C_4}} \tag{34}$$

The capacitance C_4 should not be too high so it does not require too much energy to be charged. Typical values for C_4 are between 100 pF and 1 nF.

The resistance, R5, has been added to discharge the C4 capacitance so at the next switching cycle diode D2 is activated providing enough current and storage to have a reverse-recovery current large enough for proper oscillation damping.

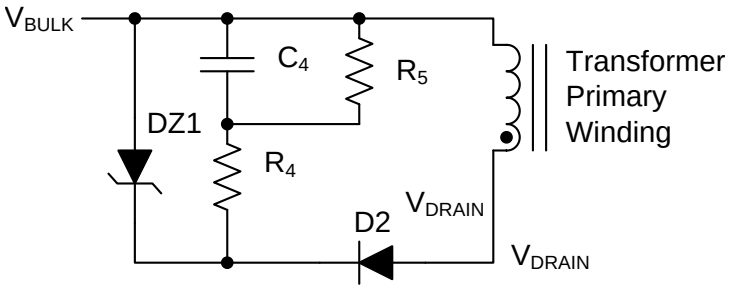


Figure 38. DRAIN Clamp Circuit Options

10.2.2 Application Curves

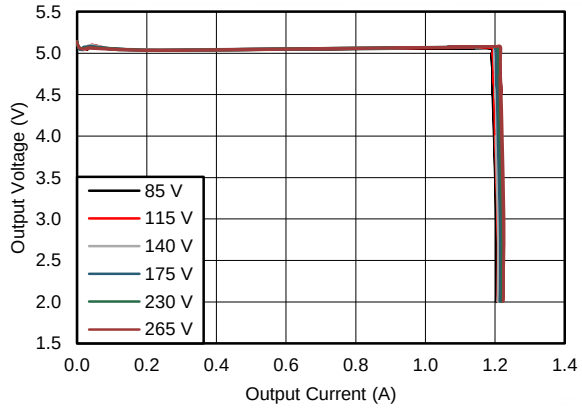


Figure 39. Output V-I Characteristic

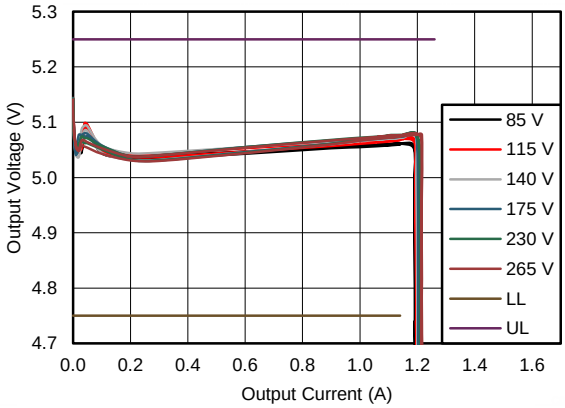


Figure 40. Output V-I Characteristic Output Current Regulation

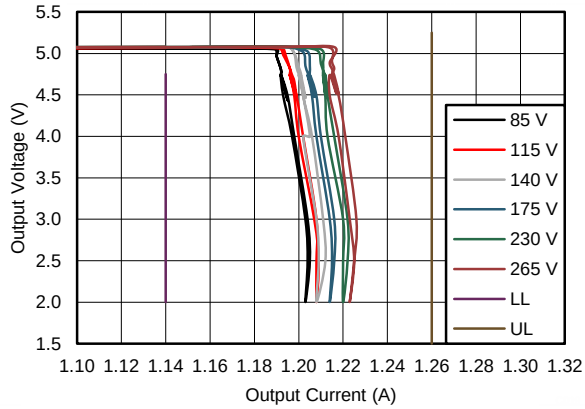


Figure 41. Output V-I Characteristic Output Voltage Regulation

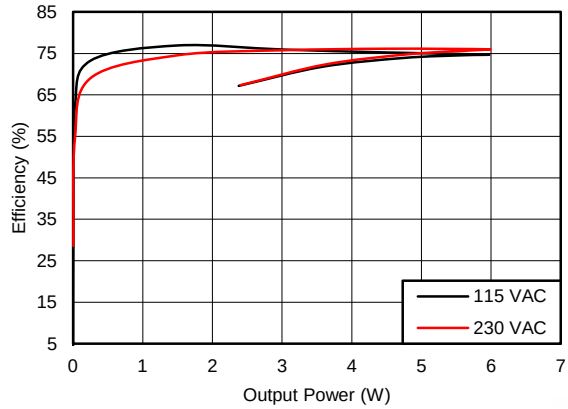


Figure 42. Efficiency vs P_{OUT} Diagram

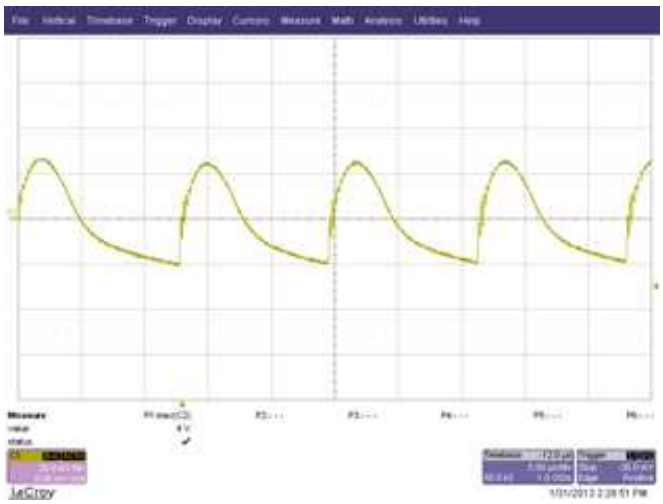


Figure 43. Ripple with 5-V, 1.2-A Output, 85 V_{AC} Input, 20 mV/div, 5 µs/div

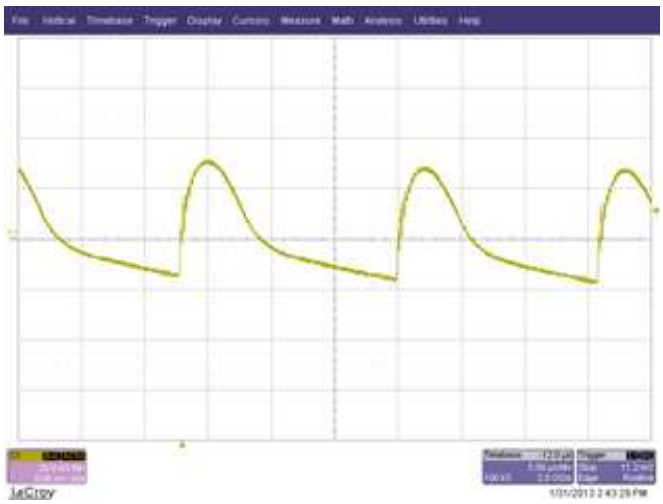


Figure 44. Ripple with 5-V,1.2-A Output, 265-V_{AC} Input, 20 mV/div 5 µs/div

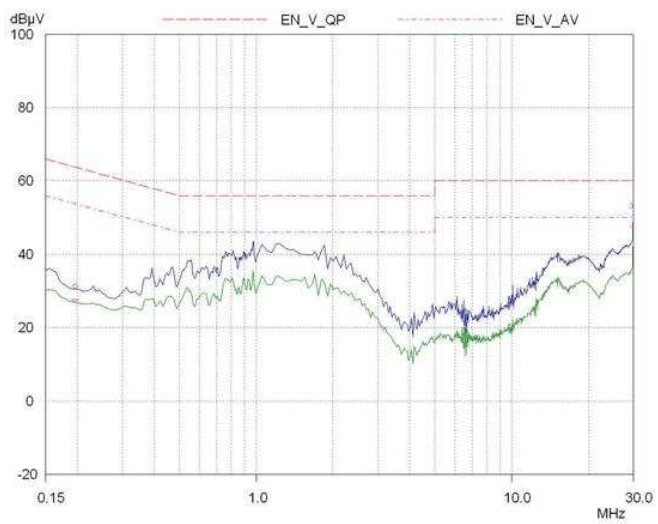


Figure 45. EMI Test Results per EN55022, Class B. 115 V_{AC} Input

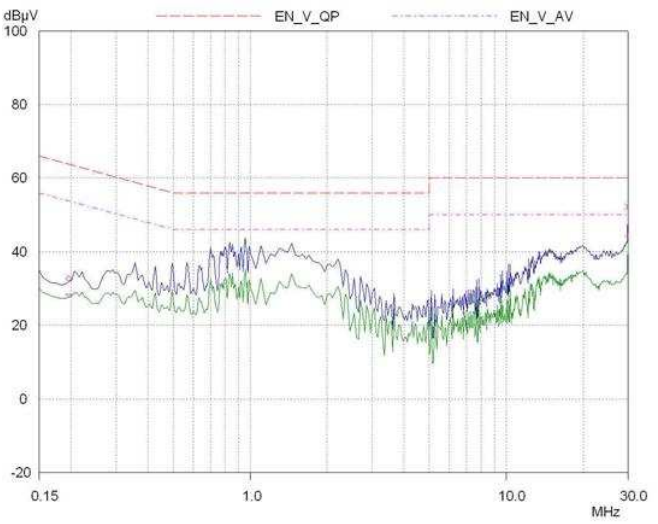


Figure 46. EMI Test Results per EN55022, Class B. 230-V_{AC} Input

10.2.2.1 Average Efficiency Performance and Standby Power of the UCC28910FBEVM-526

Table 3 summarizes the average efficiency performance of the UCC28910FBEVM-526 and Table 4 summarizes the standby power that is the no-load power consumption of the converter.

Table 3. Average Efficiency Performance of the UCC28910FBEVM-526

V_{IN} (V_{AC})	f (Hz)	P_{IN} (W)	I_{OUT} (A)	V_{OUT} (V)	P_{OUT} (W)	EFFICIENCY (%)	AVERAGE EFFICIENCY (%)
115	60	7.826	1.201	4.950	5.943	75.94	76.25
		5.845	0.901	4.942	4.451	76.15	
		3.889	0.601	4.934	2.964	76.19	
		1.930	0.301	4.927	1.481	76.73	
230	50	7.721	1.201	4.956	5.950	77.06	76.68
		5.783	0.901	4.948	4.457	77.07	
		3.853	0.601	4.938	2.966	76.97	
		1.960	0.301	4.930	1.482	75.60	

Table 4. Standby Power, No-Load Power Consumption of the Converter

V_{IN} (V_{AC})	f (Hz)	P_{IN} (mW)
88	60	10
115	60	10
230	50	10
265	50	12

10.2.3 Multi-Output Converter with UCC2891x Devices

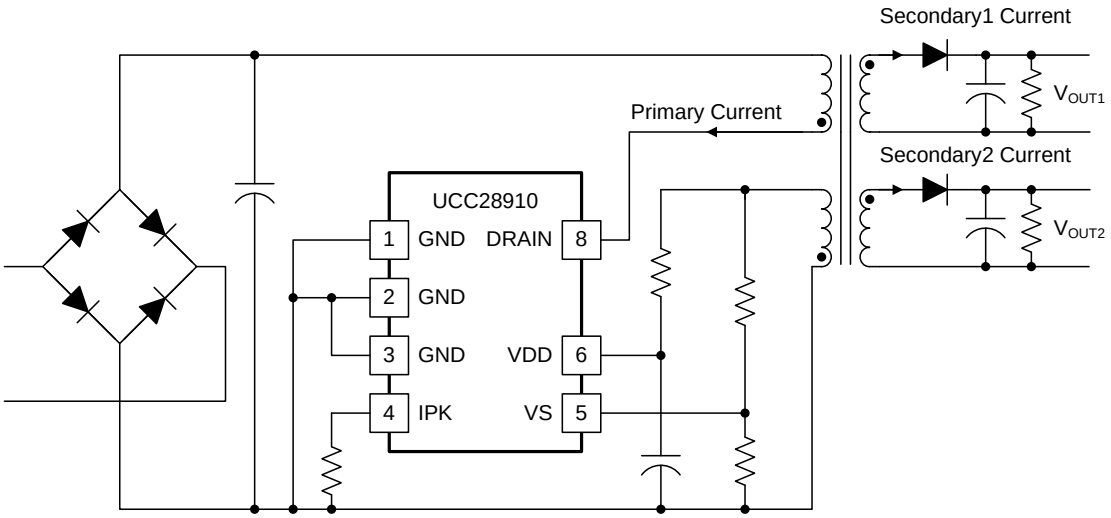


Figure 47. Multi-Output Flyback Converter

UCC2891x devices perform the output voltage regulation through PSR (Primary-Side Regulation). With PSR the output voltage is sensed sampling the auxiliary winding at the end of the transformer demagnetization. With multi-output flyback that implies multiple-secondary windings, the demagnetization time is not uniquely defined. We have multiple demagnetization time, one for each secondary winding. If secondary windings are well coupled together the UCC2891x samples the auxiliary winding at the end of the last demagnetization. (See Figure 48).

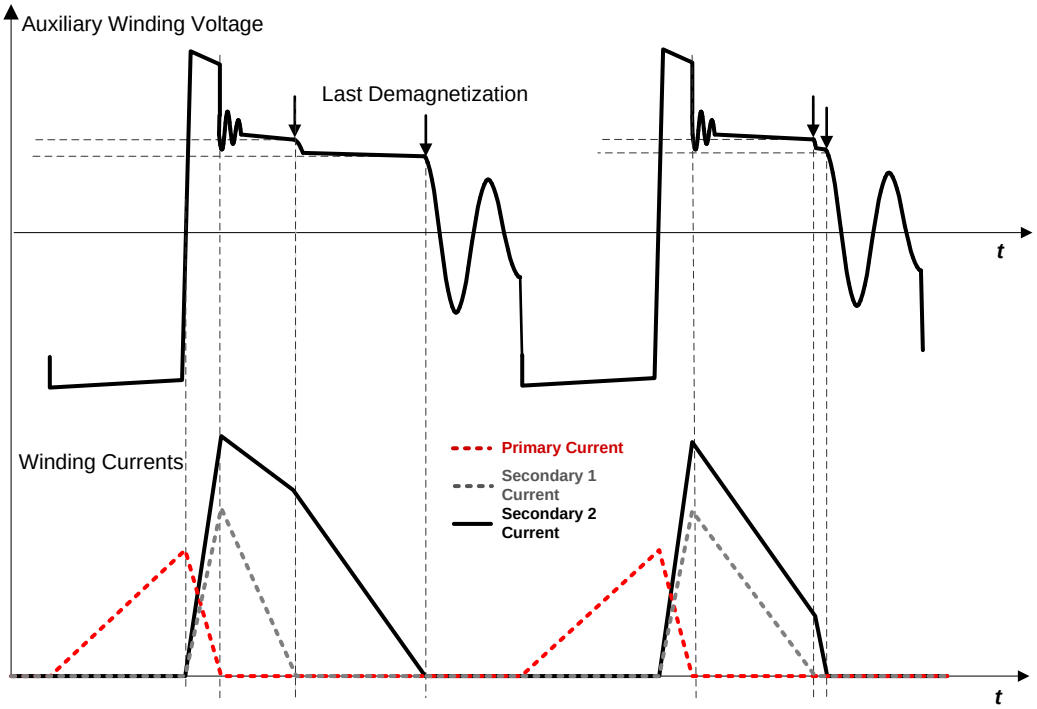


Figure 48. Winding Current Waveform in Multi-Output Flyback Converter

In multiple output flyback converter regardless if they use primary-side regulation or secondary-side regulation, the output voltages are not regulated at the target values in all the load ranges. This is called a cross-regulation problem. To minimize this problem, if the two outputs refer to the same ground voltage, the output stage can be configured as a DC stacked output, instead of staked windings (see Figure 49).

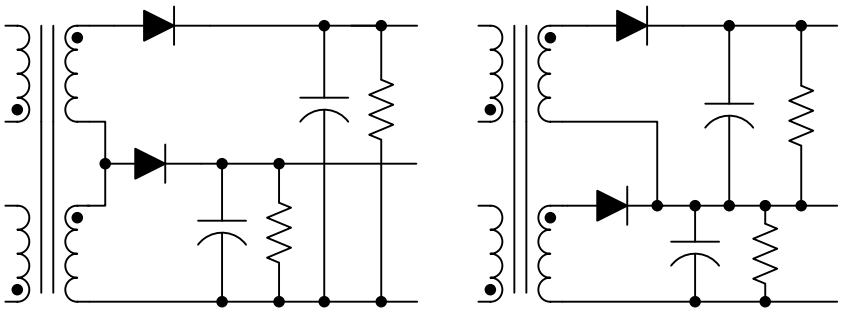


Figure 49. Stacked Windings and DC Stacked Outputs

10.2.4 Do's and Don'ts

Always design the converter to operate at maximum switching frequency (see $f_{SW(max)}$ in Electrical Characteristics).

Select the R_{IPK} to meet maximum output current requirement according to equation provided as first steps and fine tune the value on the real circuit according to design specification.

Provide enough copper area, connected to GND pins, to provide heat sinking capabilities.

Design the converter to keep junction temperature below 125°C in the worst case condition (maximum ambient temperature, minimum input voltage and maximum load). Estimate the junction temperature by measuring the GND pins temperature. The GND pins temperature are between 5°C to 15°C lower than the junction temperature.

11 Power Supply Recommendations

UCC28910 and UCC28911 are intended for AC-to-DC adapters and chargers with input voltage range of 85 $V_{AC(rms)}$ to 265 $V_{AC(rms)}$ using Flyback topology. It can be used in other applications and converter topologies with different input voltages. Be sure that all voltages and currents are within the recommended operating conditions and absolute maximum ratings of the device.

To maintain output current regulation over the entire input voltage range, design the converter to operate close to f_{MAX} when in full-load conditions.

To improve thermal performance increase the copper area connected to GND pins.

12 Layout

12.1 Layout Guidelines

In order to increase the reliability and feasibility of the project it is recommended to follow the here below guidelines.

1. Place the R_{IPK} resistance as close as possible to the device with the shortest available traces.
2. Try to minimize the area of DRAIN trace, this helps in keeping EMI disturbance low.
3. A copper area connected to the GND pins improves heat sinking thermal performance.
4. A copper area connected to anode and cathode secondary diode improves heat sinking with an emphasis on the quiet area of the diode, the diode connected to the output capacitor, this limits the EMI disturbance.
5. Place the auxiliary voltage sense resistor divider (R_{S1} and R_{S2} in Figure 50) directly on the VS pin keeping traces as short as possible.

12.2 Layout Example

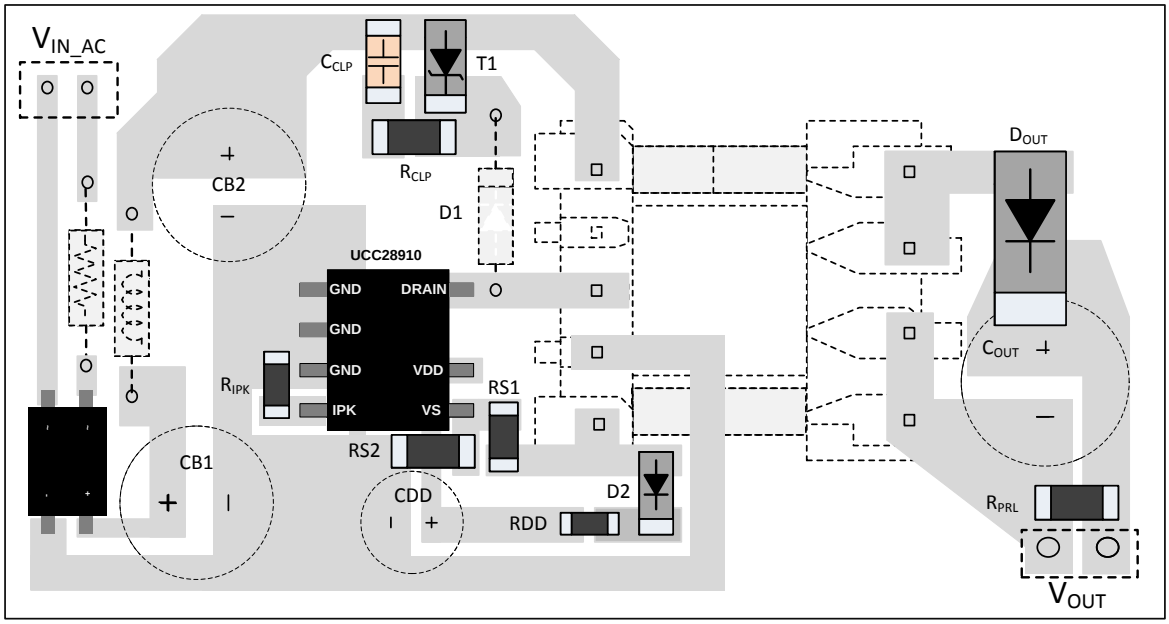


Figure 50. UCC28910 Layout Example

13 Device and Documentation Support

13.1 Documentation Support

13.1.1 Device Nomenclature

13.1.1.1 Definition of Terms

Capacitance Terms in Farads

- C_{BULK}: total input capacitance of C_{B1} and C_{B2}.
- C_{VDD}: capacitance on the VDD terminal.
- C_{OUT}: output capacitance.

Duty Cycle Terms

- K_{CC}: secondary diode conduction duty cycle in CC, (see Electrical Characteristics).
- D_{MAX}: MOSFET on-time maximum duty cycle.

Frequency Terms in Hertz

- f_{LINE}: minimum line frequency.
- $f_{TARGET(max)}$: target full-load maximum switching frequency of the converter.
- f_{MIN}: minimum switching frequency of the converter, add 15% margin over the $f_{SW(min)}$ limit of the device.
- $f_{SW(min)}$: minimum switching frequency (see Electrical Characteristics)

Current Terms in Amperes

- I_{OCC}: converter output current target when operating in constant current mode.
- $I_{D\_PK(max)}$: maximum transformer primary current peak.
- I_{TRAN}: required positive load-step current.
- I_{RUN}: maximum current consumption of the device (see Electrical Characteristics).
- I_{VSLRUN}: VS terminal run current (see Electrical Characteristics).

Current and Voltage Scaling Terms

- K_{AM}: maximum-to-minimum peak-primary current ratio (see Electrical Characteristics).

Documentation Support (continued)

Transformer Terms

- L_P: transformer primary inductance.
- N_{PA}: transformer primary-to-auxiliary turns ratio.
- N_{PS}: transformer primary-to-secondary turns ratio.

Power Terms in Watts

- P_{IN}: converter maximum input power.
- P_{INTRX}: transformer maximum input power.
- P_{OUT}: full-load output power of the converter.
- P_{SB}: total stand-by input power.

Resistance Terms in Ω

- R_{IPK}: primary current programming resistance.
- R_{ESR}: total ESR of the output capacitors.
- R_{PRL}: preload resistance on the output of the converter.
- R_{S1}: high-side VS terminal resistance.
- R_{S2}: low-side VS terminal resistance.

Timing Terms in Seconds

- $t_{DMAG(min)}$: minimum secondary rectifier conduction time.
- $t_{ON(min)}$: minimum MOSFET on time.
- t_R: resonant frequency during the DCM (discontinuous conduction mode) time.

Voltage Terms in Volts

- V_{BULK}: highest bulk capacitor voltage for stand-by power measurement.
- $V_{BULK(min)}$: minimum voltage on C_{B1} and C_{B2} at full power.
- V_{CCR}: constant-current regulating voltage (see Electrical Characteristics).
- $V_{O\Delta}$: output voltage drop allowed during the load-step transient.
- V_{DSPK}: peak MOSFET drain-to-source voltage at high line.
- V_F: secondary rectifier, D_{OUT}, forward voltage drop at near-zero current.
- V_{FA}: auxiliary rectifier, D2, forward voltage drop.
- V_{OCV}: regulated output voltage of the converter, V_{OUT} in CV mode.
- V_{VDD}: voltage value on VDD terminal.
- V_{OCC}: target lowest converter output voltage in constant-current regulation.
- V_{REV}: peak reverse voltage on the secondary rectifier, D_{OUT}.
- V_{RIPPLE}: output peak-to-peak ripple voltage at full-load.
- V_{VSR}: CV regulating level at the VS input (see Electrical Characteristics).
- ΔV_{UVLO}: $VDD_{ON} – VDD_{OFF}$ (see Electrical Characteristics).

AC Voltage Terms in V_{RMS}

- $V_{IN(max)}$: maximum AC input voltage to the converter.
- $V_{IN(min)}$: minimum AC input voltage to the converter.
- $V_{IN(run)}$: converter input start-up (run) AC voltage.

Efficiency Terms

- η: converter overall efficiency.
- η_{XFMR}: transformer primary-to-secondary power transfer efficiency.

Documentation Support (continued)

13.1.2 Related Documents

Using the UCC28910 EVM-526, Evaluation Module, Texas Instruments Literature Number SLUUAI4

13.2 Trademarks

All trademarks are the property of their respective owners.

13.3 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

13.4 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13.5 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

Table 5. Related Links

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
UCC28910, UCC28911	Click here	Click here	Click here	Click here	Click here

14 Mechanical, Packaging, and Orderable Information

The following pages include mechanical packaging and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
UCC28910D	ACTIVE	SOIC	D	7	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	U28910	Samples
UCC28910DR	ACTIVE	SOIC	D	7	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	U28910	Samples
UCC28911D	ACTIVE	SOIC	D	7	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	U28911	Samples
UCC28911DR	ACTIVE	SOIC	D	7	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	U28911	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

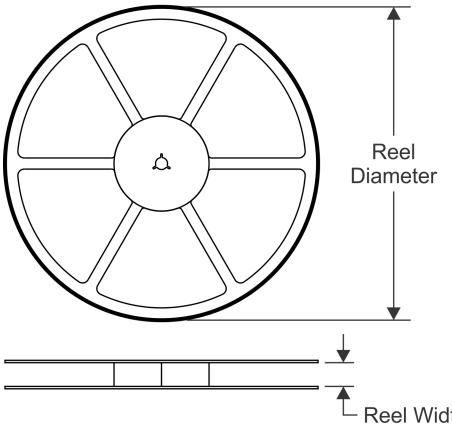
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

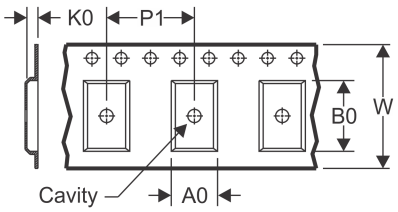
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

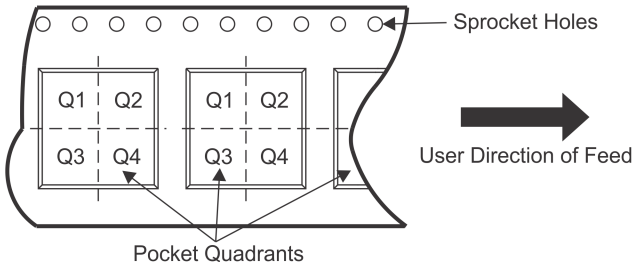


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

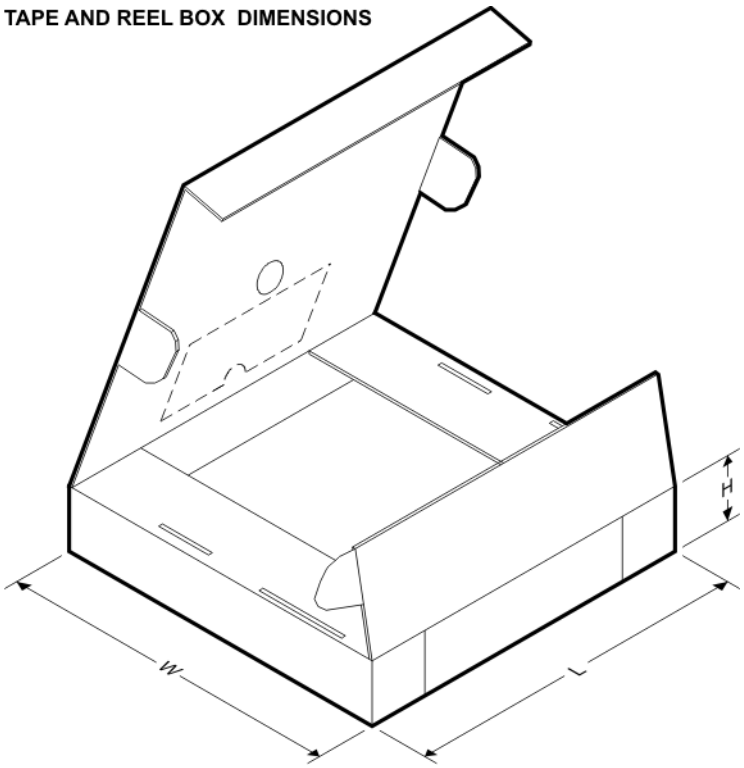
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
UCC28910DR	SOIC	D	7	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
UCC28911DR	SOIC	D	7	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

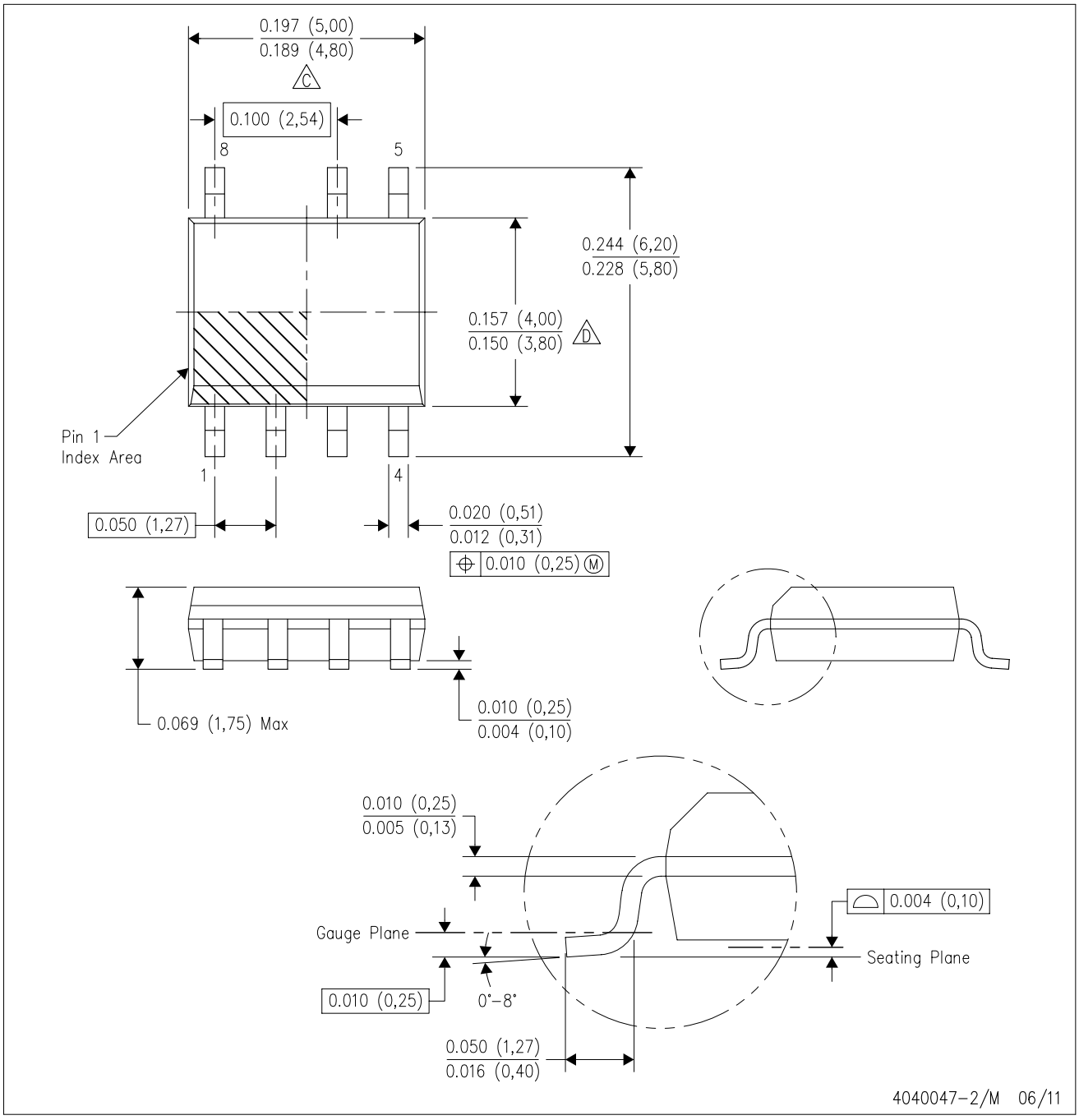
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
UCC28910DR	SOIC	D	7	2500	367.0	367.0	35.0
UCC28911DR	SOIC	D	7	2500	367.0	367.0	35.0

D (R–PDSO–G7) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AA.

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