

16-Bit, 4-Channel, CCD/CMOS Sensor Analog Front-End with LED Driver

Check for Samples: [VSP5620](#), [VSP5621](#), [VSP5622](#)

FEATURES

- Four-Channel CCD/CMOS Signal: 2-Channel, 3-Channel, and 4-Channel Selectable
- Power Supply: 3.3 V Only, Typ (Built-in LDO, 3.3 V to 1.8 V)
- Maximum Conversion Rate:
 - VSP5620: 35 MSPS
 - VSP5621: 50 MSPS
 - VSP5622: 70 MSPS
- 16-Bit Resolution
- CDS/SH Selectable
- Maximum Input Signal Range: 2.0 V
- Analog and Digital Hybrid Gain:
 - Analog Gain: 0.5 V/V to 3.5 V/V in 3/64-V/V Steps
 - Digital Gain: 1 V/V to 2 V/V in 1/256-V/V Steps
- Offset Correction DAC: ± 250 mV, 8-Bit
- Standard LVDS/CMOS Selectable Output:
 - LVDS:
 - Data Channel: 2-Channel
 - Clock Channel: 1-Channel
 - 8-Bit/7-Bit Serializer Selectable
 - CMOS: 4 Bits $\times$ 4
- Timing Generator
 - Fast Transfer Clock: One Signal
 - Slow Transfer Clock: One Signal
- LED Driver: Three Channels
 - Current: 60-mA/Channel Max, 16-Steps/Channel
- Timing Adjustment Resolution: $t_{MCLK}/48$
- Input Clamp/Input Reference Level Internal/External Selectable
- Reference DAC: 0.5 V, 1.1 V, 1.5 V, 2 V
- SPI™: Three-Wire Serial
- GPIO: Four-Port

- Power (at 4-channel, LVDS, 3.3 V, without LED Driver):
 - VSP5620: 320 mW at 35 MSPS
 - VSP5621: 406 mW at 50 MSPS
 - VSP5622: 523 mW at 70 MSPS

APPLICATIONS

- Copiers
- Facsimile Machines
- Scanners

DESCRIPTION

The VSP5620/21/22 are high-speed, high-performance, 16-bit analog-to-digital-converters (ADCs) that have four independent sampling circuit channels for multi-output charge-coupled device (CCD) and complementary metal oxide semiconductor (CMOS) line sensors. Pixel data from the sensor are sampled by the sample/hold (SH) or correlated double sampler (CDS) circuit, and are then converted to digital data by an ADC. Data output is selectable in low-voltage differential signaling (LVDS) or CMOS modes.

The VSP5620/21/22 include a programmable gain to support the pixel level inflection caused by luminance and a built-in light-emitting diode (LED) driver to adjust the brightness. The integrated digital-to-analog-converter (DAC) can be used to adjust the offset level for the analog input signal. Furthermore, the timing generator (TG) is integrated in these devices for the control of sensor operation.

The VSP5620/21/22 use 1.65 V to 1.95 V for the core voltage and 3.0 V to 3.6 V for I/Os. The core voltage is supplied by a built-in low-dropout regulator (LDO).



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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
VSP5621RSLR	NRND	VQFN	RSL	48	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	0 to 85	VSP 5621	

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

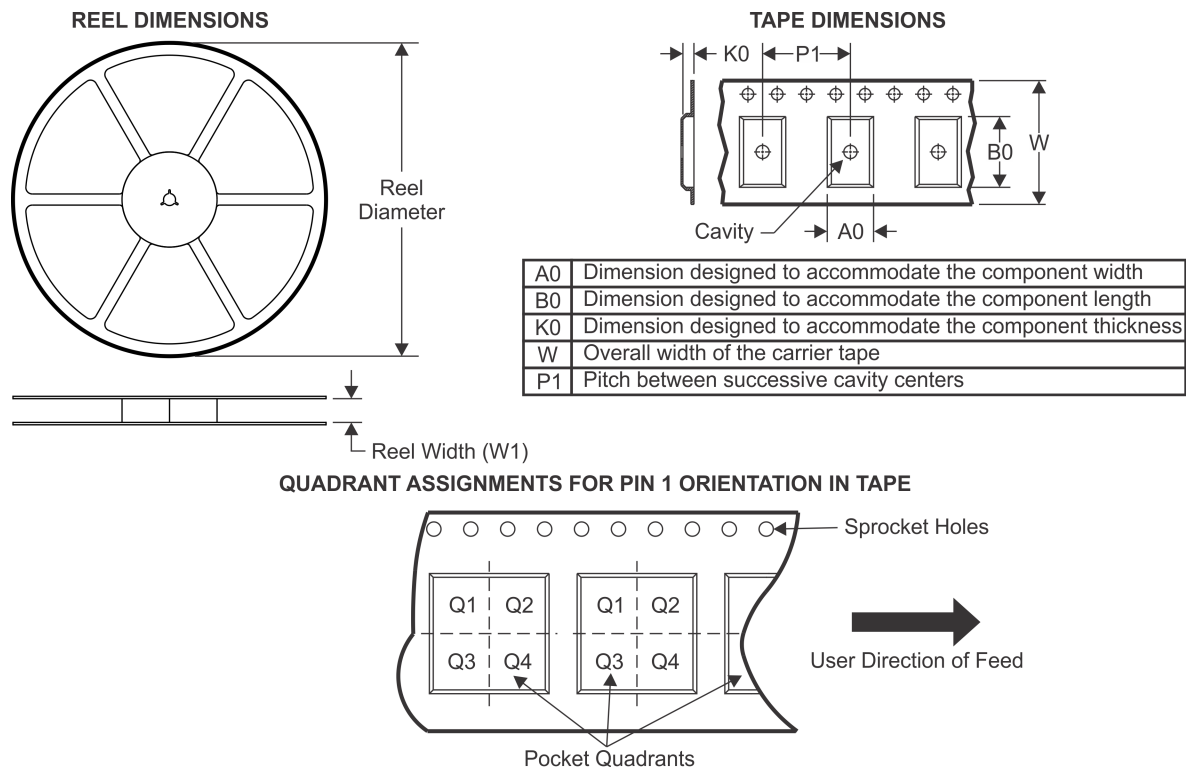
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "-" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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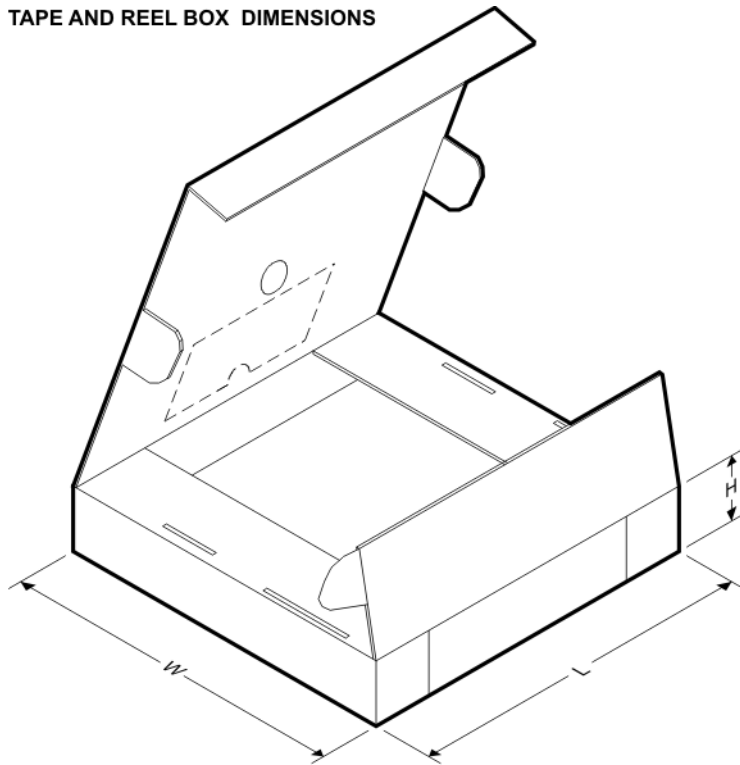
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TAPE AND REEL INFORMATION


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
VSP5621RSLR	VQFN	RSL	48	2500	330.0	16.4	6.3	6.3	1.1	12.0	16.0	Q2

TAPE AND REEL BOX DIMENSIONS

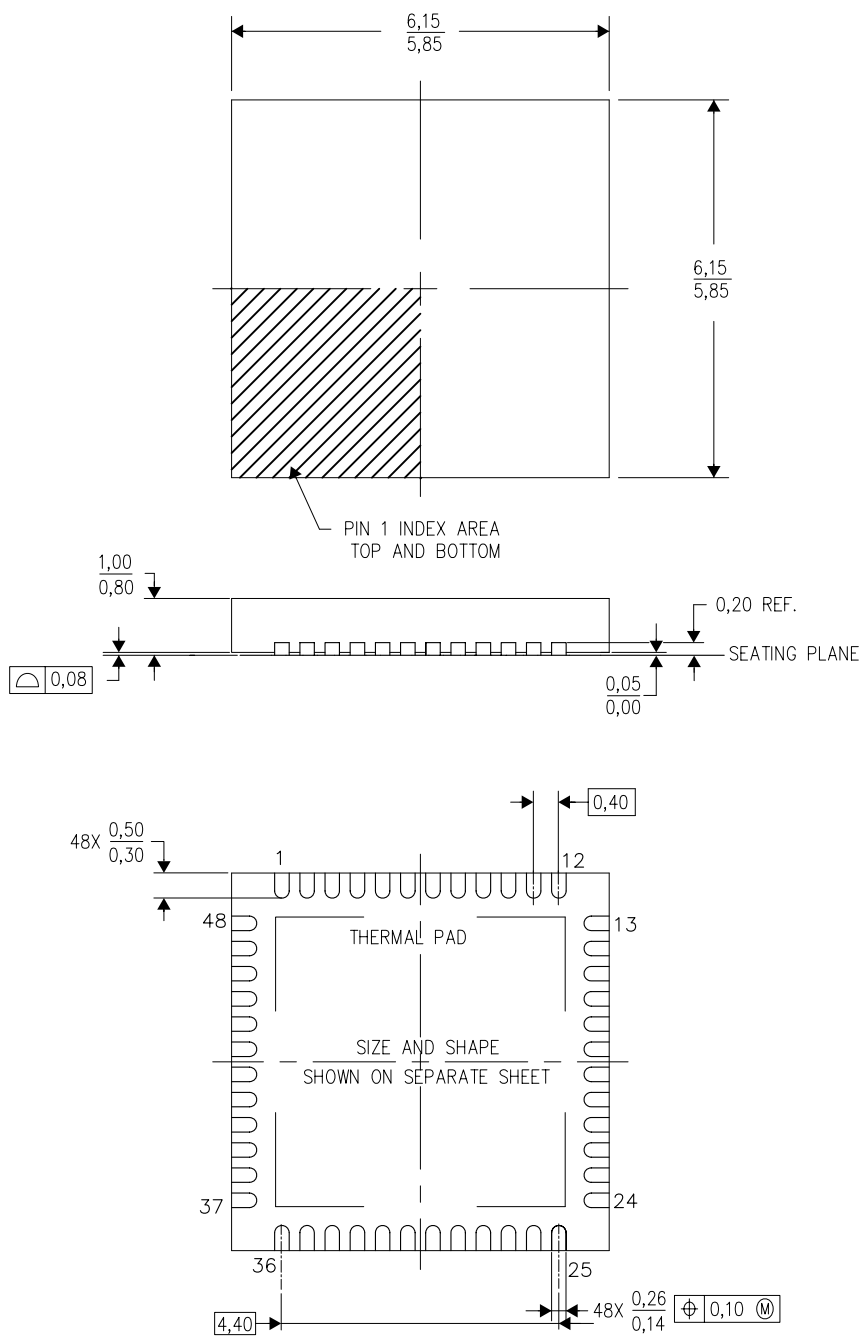


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
VSP5621RSLR	VQFN	RSL	48	2500	367.0	367.0	38.0

RSL (S-PVQFN-N48)

PLASTIC QUAD FLATPACK NO-LEAD



4207548/B 06/11

- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
 - B. This drawing is subject to change without notice.
 - C. Quad Flatpack, No-leads (QFN) package configuration.
 - D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
 - E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.

THERMAL PAD MECHANICAL DATA

RSL (S-PVQFN-N48)

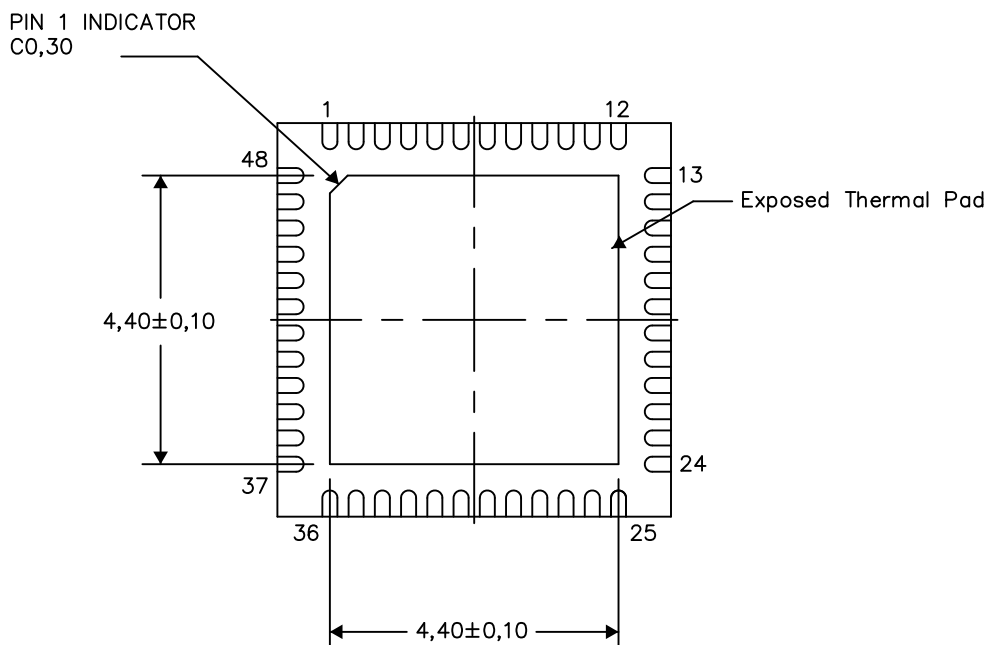
PLASTIC QUAD FLATPACK NO-LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No-Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



Bottom View

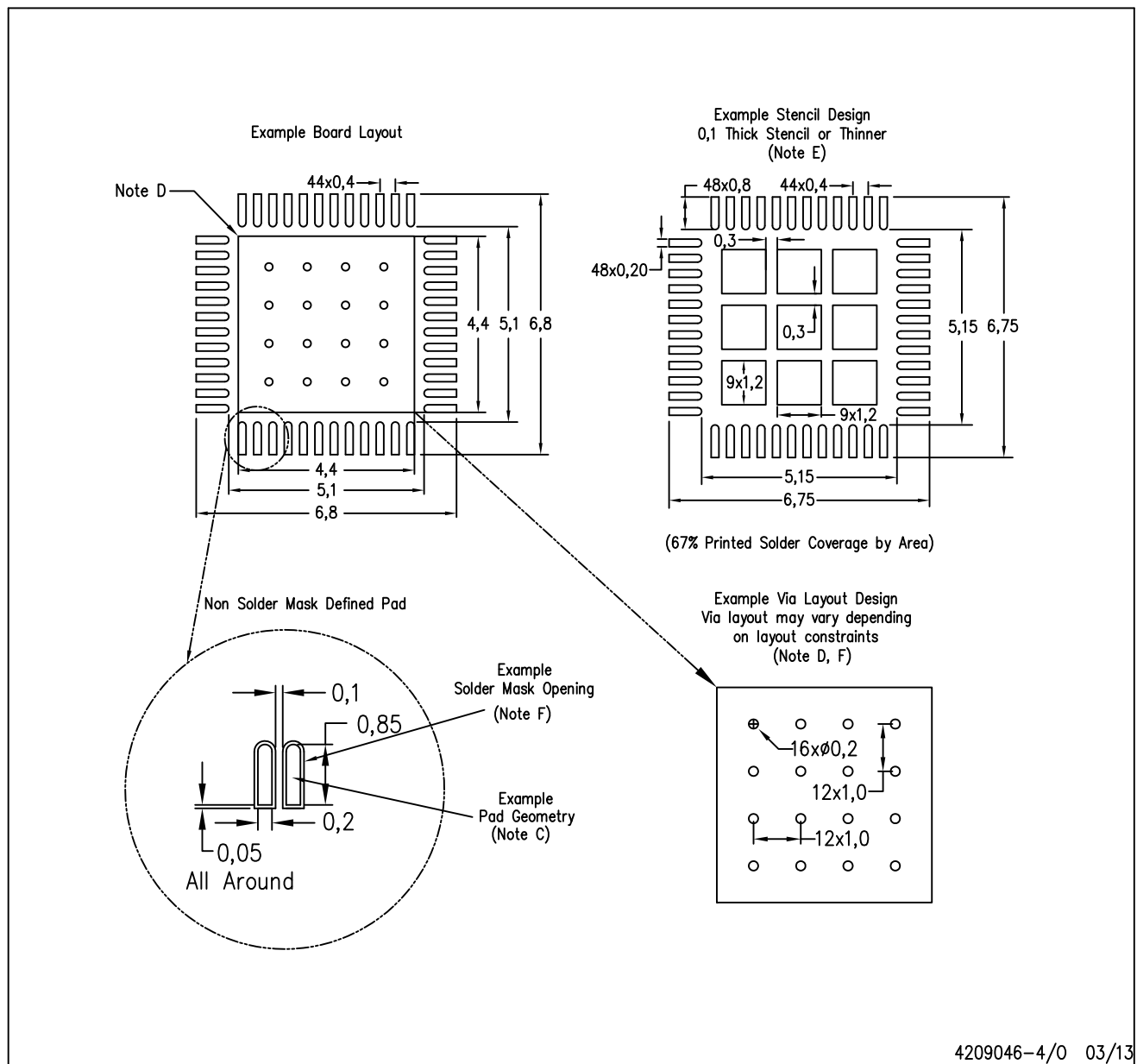
Exposed Thermal Pad Dimensions

4207841-2/P 03/13

NOTE: All linear dimensions are in millimeters

RSL (S-PVQFN-N48)

PLASTIC QUAD FLATPACK NO-LEAD



- NOTES:
- All linear dimensions are in millimeters.
 - This drawing is subject to change without notice.
 - Publication IPC-7351 is recommended for alternate designs.
 - This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <<http://www.ti.com>>.
 - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
 - Customers should contact their board fabrication site for recommended solder mask tolerances and via tenting recommendations for vias placed in the thermal pad.

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