ADC10065 10-Bit 65 MSPS 3V A/D Converter

Check for Samples: ADC10065

FEATURES

- **Single +3.0V Operation**
- **Selectable 2 V_{P-P}, 1.5 V_{P-P}, or 1 V_{P-P} Full-scale Input**
- **400 MHz −3 dB Input Bandwidth**
- **Low Power Consumption**
- **Standby Mode**
- **On-Chip Reference and Sample-and-Hold Amplifier**
- **Offset Binary or Two's Complement Data Format**
- **Separate Adjustable Output Driver Supply to Accommodate 2.5V and 3.3V Logic Families**
- **28-pin TSSOP Package**

APPLICATIONS

- **Ultrasound and Imaging**
- **Instrumentation**
- **Cellular Base Stations/Communications Receivers**
- **Sonar/Radar**
- **xDSL**
- **Wireless Local Loops**
- **Data Acquisition Systems**
- **DSP Front Ends**

KEY SPECIFICATIONS

- **Resolution 10 Bits**
- **Conversion Rate 65 MSPS**
- **Full Power Bandwidth 400 MHz**
- **DNL ±0.3 LSB (typ)**
- **SNR (f_{IN} = 11 MHz) 59.6 dB (typ)**
- **SFDR (f_{IN} = 11 MHz) −80 dB (typ)**
- **Power Consumption, 65 MHz 68.4 mW**

DESCRIPTION

The ADC10065 is a monolithic CMOS analog-to-digital converter capable of converting analog input signals into 10-bit digital words at 65 Megasamples per second (MSPS). This converter uses a differential, pipeline architecture with digital error correction and an on-chip sample-and-hold circuit to provide a complete conversion solution, and to minimize power consumption, while providing excellent dynamic performance. A unique sample-and-hold stage yields a full-power bandwidth of 400 MHz. Operating on a single 3.0V power supply, this device consumes just 68.4 mW at 65 MSPS, including the reference current. The Standby feature reduces power consumption to just 14.1 mW.

The differential inputs provide a full scale selectable input swing of 2.0 V_{P-P}, 1.5 V_{P-P}, 1.0 V_{P-P}, with the possibility of a single-ended input. Full use of the differential input is recommended for optimum performance. An internal +1.2V precision bandgap reference is used to set the ADC full-scale range, and also allows the user to supply a buffered referenced voltage for those applications requiring increased accuracy. The output data format is user choice of offset binary or two's complement.

This device is available in the 28-lead TSSOP package and will operate over the industrial temperature range of −40°C to +85°C.

Connection Diagram

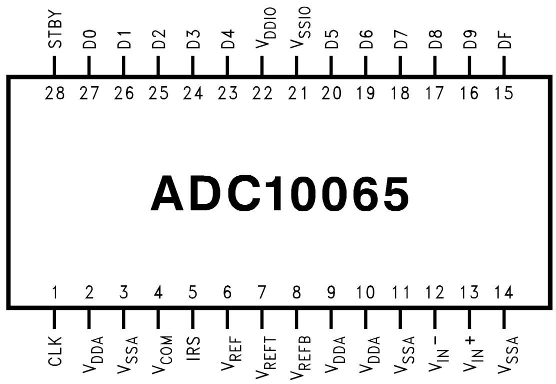
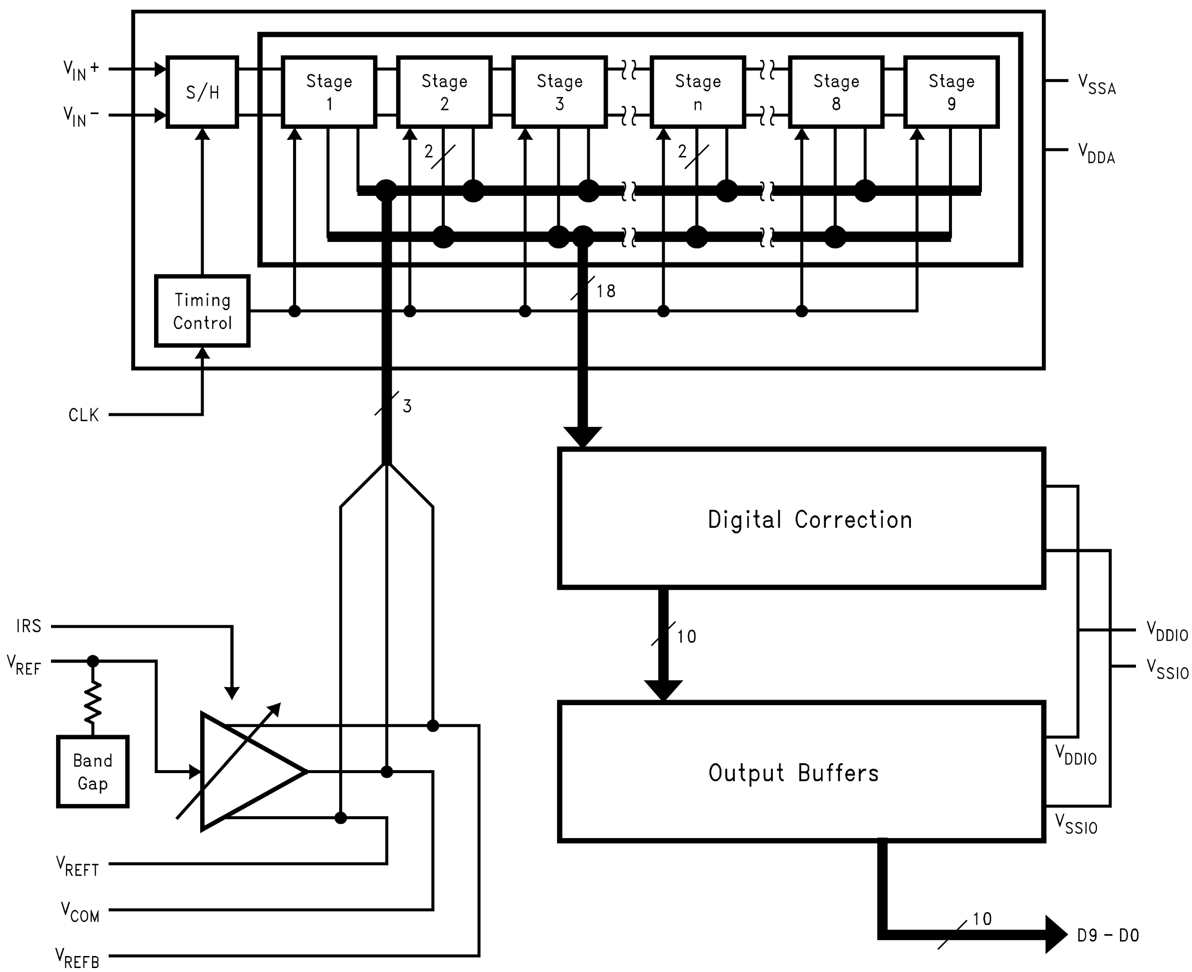
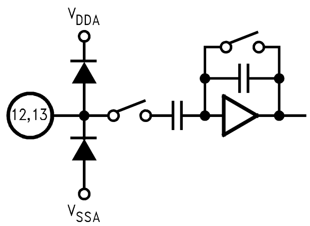
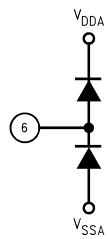
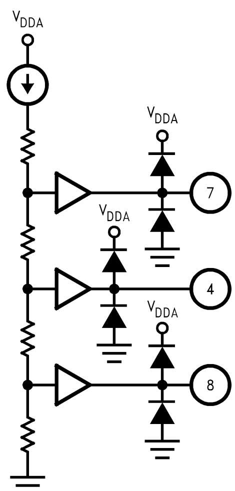
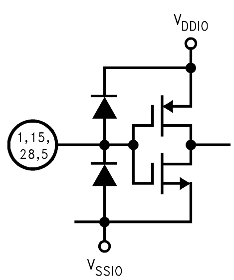


Figure 1. TSSOP Package
See Package Number PW0028A

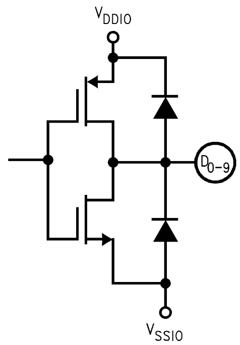
Block Diagram



Pin Descriptions and Equivalent Circuits

<table>
<tr><th>Pin No.</th><th>Pin Name</th><th>Equivalent Circuit</th><th>Description</th></tr>
<tr><td colspan="4">ANALOG I/O</td></tr>
<tr><td>12</td><td>V_{IN}^{-}</td><td rowspan="2">
</td><td>Inverting analog input signal. With a 1.2V reference the full-scale input signal level is a differential 1.0 V_{P-P}. This pin may be tied to V_{COM} (pin 4) for single-ended operation.</td></tr>
<tr><td>13</td><td>V_{IN}^{+}</td><td>Non-inverting analog input signal. With a 1.2V reference the full-scale input signal level is a differential 1.0 V_{P-P}.</td></tr>
<tr><td>6</td><td>V_{REF}</td><td>
</td><td>Reference input. This pin should be bypassed to V_{SSA} with a 0.1 µF monolithic capacitor. V_{REF} is 1.20V nominal. This pin may be driven by a 1.20V external reference if desired. Do not load this pin.</td></tr>
<tr><td>7</td><td>V_{REFT}</td><td rowspan="3">
</td><td rowspan="3">These pins are high impedance reference bypass pins only. Connect a 0.1 µF capacitor from each of these pins to V_{SSA}. These pins should not be loaded. V_{COM} may be used to set the input common mode voltage, V_{CM}.</td></tr>
<tr><td>4</td><td>V_{COM}</td></tr>
<tr><td>8</td><td>V_{REFB}</td></tr>
<tr><td colspan="4">DIGITAL I/O</td></tr>
<tr><td>1</td><td>CLK</td><td rowspan="4">
</td><td>Digital clock input. The range of frequencies for this input is 20 MHz to 65 MHz. The input is sampled on the rising edge of this input.</td></tr>
<tr><td>15</td><td>DF</td><td>DF = “1” Two’s Complement
DF = “0” Offset Binary</td></tr>
<tr><td>28</td><td>STBY</td><td>This is the standby pin. When high, this pin sets the converter into standby mode. When this pin is low, the converter is in active mode.</td></tr>
<tr><td>5</td><td>IRS (Input Range Select)</td><td>IRS = “V_{DDA}” 2.0 V_{P-P} differential input range
IRS = “V_{SSA}” 1.5 V_{P-P} differential input range
IRS = “Floating” 1.0 V_{P-P} differential input range
If using both V_{IN}+ and V_{IN}- pins, (or differential mode), then the peak-to-peak voltage refers to the differential voltage (V_{IN}+ - V_{IN}-).</td></tr>
</table>

Pin Descriptions and Equivalent Circuits (continued)

Pin No.	Pin Name	Equivalent Circuit	Description
16–20, 23–27	D0–D9		Digital output data. D0 is the LSB and D9 is the MSB of the binary output word.
ANALOG POWER			
2, 9, 10	V_{DDA}		Positive analog supply pins. These pins should be connected to a quiet 3.0V source and bypassed to analog ground with a 0.1 µF monolithic capacitor located within 1 cm of these pins. A 4.7 µF capacitor should also be used in parallel.
3, 11, 14	V_{SSA}		Ground return for the analog supply.
DIGITAL POWER			
22	V_{DDIO}		Positive digital supply pins for the ADC10065's output drivers. This pin should be bypassed to digital ground with a 0.1 µF monolithic capacitor located within 1 cm of this pin. A 4.7 µF capacitor should also be used in parallel. The voltage on this pin should never exceed the voltage on V_{DDA} by more than 300 mV.
21	V_{SSIO}		The ground return for the digital supply for the output drivers. This pin should be connected to the ground plane, but not near the analog circuitry.

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

Absolute Maximum Ratings [1][2][3]

V_{DDA}, V_{DDIO}		3.9V
Voltage on Any Pin to GND		−0.3V to V_{DDA} or V_{DDIO} +0.3V
Input Current on Any Pin		±25 mA
Package Input Current [4]		±50 mA
Package Dissipation at T = 25°C		See [5]
ESD Susceptibility	Human Body Model [6]	2500V
	Machine Model [6]	250V
Soldering Temperature Infrared, 10 sec. [7]		235°C
Storage Temperature		−65°C to +150°C

(1) All voltages are measured with respect to GND = V_{SSA} = V_{SSIO} = 0V, unless otherwise specified.
(2) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is functional, but do not ensure specific performance limits. For ensured specifications and test conditions, see the AC Electrical Characteristics. The ensured specifications apply only for the test conditions listed. Some performance characteristics may degrade when the device is not operated under the listed test conditions.
(3) If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/ Distributors for availability and specifications.
(4) When the voltage at any pin exceeds the power supplies (V_{IN} < V_{SSA} or V_{IN} > V_{DDA}), the current at that pin should be limited to 25 mA. The 50 mA maximum package input current rating limits the number of pins that can safely exceed the power supplies with an input current of 25 mA to two.
(5) The absolute maximum junction temperature ($T_J$max) for this device is 150°C. The maximum allowable power dissipation is dictated by $T_J$max, the junction-to-ambient thermal resistance (θ_{JA}), and the ambient temperature (T_A), and can be calculated using the formula P_DMAX = ($T_J$max − T_A)/θ_{JA}. In the 28-pin TSSOP, θ_{JA} is 96°C/W, so P_DMAX = 1,302 mW at 25°C and 677 mW at the maximum operating ambient temperature of 85°C. Note that the power dissipation of this device under normal operation will typically be about 68.6 mW. The values for maximum power dissipation listed above will be reached only when the ADC10065 is operated in a severe fault condition.
(6) Human body model is 100 pF capacitor discharged through a 1.5 kΩ resistor. Machine model is 220 pF discharged through 0Ω.
(7) The 235°C reflow temperature refers to infrared reflow. For Vapor Phase Reflow (VPR) the following conditions apply: Maintain the temperature at the top of the package body above 183°C for a minimum of 60 seconds. The temperature measured on the package body must not exceed 220°C. Only one excursion above 183°C is allowed per reflow cycle.

Operating Ratings [1][2]

Operating Temperature Range	−40°C ≤ T_A ≤ +85°C
V_{DDA} (Supply Voltage)	+2.7V to +3.6V
V_{DDIO} (Output Driver Supply Voltage)	+2.5V to V_{DDA}
V_{REF}	1.20V
$\lvert V_{SSA}–V_{SSIO}\rvert$	≤ 100 mV
Clock Duty Cycle	30 to 70 %

(1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is functional, but do not ensure specific performance limits. For ensured specifications and test conditions, see the AC Electrical Characteristics. The ensured specifications apply only for the test conditions listed. Some performance characteristics may degrade when the device is not operated under the listed test conditions.
(2) All voltages are measured with respect to GND = V_{SSA} = V_{SSIO} = 0V, unless otherwise specified.

Converter Electrical Characteristics

Unless otherwise specified, the following specifications apply for $V_{SSA} = V_{SSIO} = 0V$, $V_{DDA} = +3.0V$, $V_{DDIO} = +2.5V$, $V_{IN} = 2\ V_{P-P}$, STBY = 0V, $V_{REF} = 1.20V$ (External), $f_{CLK} = 65$ MHz, 50% Duty Cycle, $C_L = 10$ pF/pin. **Boldface limits apply for $T_A = T_{MIN}$ to T_{MAX}**: all other limits $T_A = 25°C$. [1][2][3][4].

Parameter		Test Conditions	Min	Typ	Max	Units
STATIC CONVERTER CHARACTERISTICS						
	No Missing Codes ensured		**10**			Bits
INL	Integral Non-Linearity	F_{IN} = 500 kHz, −0 dB Full Scale	**−1.0**	±0.3	**+1.1**	LSB
DNL	Differential Non-Linearity	F_{IN} = 500 kHz, −0 dB Full Scale	**−0.9**	±0.3	**+0.9**	LSB
GE	Gain Error	Positive Error	**−1.5**	+0.4	**+1.9**	% FS
		Negative Error	**−1.5**	+0.03	**+1.9**	% FS
OE	Offset Error ($V_{IN}+ = V_{IN}-$)		**−1.4**	0.2	**+1.7**	% FS
	Under Range Output Code			0		
	Over Range Output Code			1023		
FPBW	Full Power Bandwidth [5]			400		MHz
REFERENCE AND INPUT CHARACTERISTICS						
V_{CM}	Common Mode Input Voltage		0.5		1.5	V
V_{COM}	Output Voltage for use as an input common mode voltage [6]			1.45		V
V_{REF}	Reference Voltage			1.2		V
V_{REFTC}	Reference Voltage Temperature Coefficient			±80		ppm/°C
C_{IN}	V_{IN} Input Capacitance (each pin to V_{SSA})			4		pF
POWER SUPPLY CHARACTERISTICS						
I_{VDDA}	Analog Supply Current	STBY = 1		4.7	**6.0**	mA
		STBY = 0		22	**29**	mA
I_{VDDIO}	Digital Supply Current [7]	STBY = 1, f_{IN} = 0 Hz		0		mA
		STBY 0, f_{IN} = 0 Hz		0.97	**1.2**	mA
PWR	Power Consumption [8]	STBY = 1		14.1	**18.0**	mW
		STBY = 0		68.4	**90**	mW

(1) To ensure accuracy, it is required that $|V_{DDA}–V_{DDIO}| \le 100$ mV and separate bypass capacitors are used at each power supply pin.
(2) With the test condition for 2 V_{P-P} differential input, the 10-bit LSB is 1.95 mV.
(3) Typical figures are at $T_A = T_J = 25°C$ and represent most likely parametric norms. Test limits are specified to Texas Instrument's AOQL (Average Outgoing Quality Level).
(4) The analog inputs are protected as shown below. Input voltage magnitude up to 500 mV beyond the supply rails will not damage this device. However, input errors will be generated if the input goes above V_{DDA} or V_{DDIO} and below V_{SSA} or V_{SSIO}. See Figure 2
(5) The input bandwidth is limited using a capacitor between V_{IN}^- and V_{IN}^+.
(6) VCOM is a typical value, measured at room temperature. It is not specified by test. Do not load this pin.
(7) I_{DDIO} is the current consumed by the switching of the output drivers and is primarily determined by load capacitance on the output pins, the supply voltage, V_{DR}, and the rate at which the outputs are switching (which is signal dependent). $I_{DR} = V_{DR} \times (C_0 \times f_0 + C_1 \times f_1 + C_2 + f_2 + \ldots C_{11} \times f_{11})$ where V_{DR} is the output driver supply voltage, C_n is the total load capacitance on the output pin, and f_n is the average frequency at which the pin is toggling.
(8) Power consumption includes output driver power. (f_{IN} = 0 MHz).

DC and Logic Electrical Characteristics

Unless otherwise specified, the following specifications apply for $V_{SSA} = V_{SSIO}$ = 0V, V_{DDA} = +3.0V, V_{DDIO} = +2.5V, V_{IN} = 2 V_{P-P}, STBY = 0V, V_{REF} = 1.20V (External), f_{CLK} = 65 MHz, 50% Duty Cycle, C_L = 10 pF/pin. **Boldface limits apply for $T_A = T_{MIN}$ to T_{MAX}**: all other limits T_A = 25°C. (1)

Parameter		Test Conditions	Min	Typ	Max	Units
CLK, DF, STBY, SENSE						
	Logical "1" Input Voltage		**2**			V
	Logical "0" Input Voltage				**0.8**	V
	Logical "1" Input Current				**+10**	µA
	Logical "0" Input Current		**−10**			µA
D0–D9 OUTPUT CHARACTERISTICS						
	Logical "1" Output Voltage	I_{OUT} = −0.5 mA	**V_{DDIO}−0.2**			V
	Logical "0" Output Voltage	I_{OUT} = 1.6 mA			**0.4**	V
DYNAMIC CONVERTER CHARACTERISTICS (2)						
ENOB	Effective Number of Bits	f_{IN} = 11 MHz	9.4, **9.3**	9.6		Bits
		f_{IN} = 32 MHz	9.3, **9.2**	9.5		Bits
SNR	Signal-to-Noise Ratio	f_{IN} = 11 MHz	58.6, **58**	59.6		dB
		f_{IN} = 32 MHz	58.5, **57.9**	59.3		dB
SINAD	Signal-to-Noise Ratio + Distortion	f_{IN} = 11 MHz	58.3, **57.6**	59.4		dB
		f_{IN} = 32 MHz	58, **57.4**	59		dB
2nd HD	2nd Harmonic	f_{IN} = 11 MHz	−75.6, **−69.7**	−90		dBc
		f_{IN} = 32 MHz	−72.7, **−68.9**	−82		dBc
3rd HD	3rd Harmonic	f_{IN} = 11 MHz	−66.2, **−63**	−74		dBc
		f_{IN} = 32 MHz	−65.4, **−63.3**	−72		dBc
THD	Total Harmonic Distortion (First 6 Harmonics)	f_{IN} = 11 MHz	−66.2, **−63**	−74		dB
		f_{IN} = 32 MHz	−65.4, **−63.3**	−72		dB
SFDR	Spurious Free Dynamic Range (Excluding 2nd and 3rd Harmonic)	f_{IN} = 11 MHz	−75.8, **−74.5**	−80		dBc
		f_{IN} = 32 MHz	−74.4, **−73.3**	−80		dBc

(1) The analog inputs are protected as shown below. Input voltage magnitude up to 500 mV beyond the supply rails will not damage this device. However, input errors will be generated if the input goes above V_{DDA} or V_{DDIO} and below V_{SSA} or V_{SSIO}. See Figure 2
(2) Optimum dynamic performance will be obtained by keeping the reference input in the +1.2V.

AC Electrical Characteristics

Unless otherwise specified, the following specifications apply for $V_{SSA} = V_{SSIO}$ = 0V, V_{DDA} = +3.0V, V_{DDIO} = +2.5V, V_{IN} = 2 V_{P-P}, STBY = 0V, V_{REF} = 1.20V (External), f_{CLK} = 65 MHz, 50% Duty Cycle, C_L = 10 pF/pin. **Boldface limits apply for $T_A = T_{MIN}$ to T_{MAX}**: all other limits T_A = 25°C. (1)

Parameter		Test Conditions	Min (2)	Typ (2)	Max (2)	Units
CLK, DF, STBY, SENSE						
$f_{CLK}1$	Maximum Clock Frequency				65	MHz (min)
$f_{CLK}2$	Minimum Clock Frequency			20		MHz
t_{CH}	Clock High Time			7.69		ns
t_{CL}	Clock Low Time			7.69		ns
	Conversion Latency				**6**	Cycles

(1) The analog inputs are protected as shown below. Input voltage magnitude up to 500 mV beyond the supply rails will not damage this device. However, input errors will be generated if the input goes above V_{DDA} or V_{DDIO} and below V_{SSA} or V_{SSIO}. See Figure 2
(2) Timing specifications are tested at TTL logic levels, V_{IL} = 0.4V for a falling edge, and V_{IH} = 2.4V for a rising edge.

AC Electrical Characteristics (continued)

Unless otherwise specified, the following specifications apply for $V_{SSA} = V_{SSIO} = 0V$, $V_{DDA} = +3.0V$, $V_{DDIO} = +2.5V$, $V_{IN} = 2\ V_{P-P}$, STBY = 0V, $V_{REF} = 1.20V$ (External), $f_{CLK} = 65$ MHz, 50% Duty Cycle, $C_L = 10$ pF/pin. **Boldface limits apply for $T_A = T_{MIN}$ to T_{MAX}:** all other limits $T_A = 25°C$. (1)

Parameter		Test Conditions	Min (2)	Typ (2)	Max (2)	Units
t_{OD}	Data Output Delay after a Rising Clock Edge	T = 25°C	2	3.4	5	ns
			1		**6**	ns
t_{AD}	Aperture Delay			1		ns
t_{AJ}	Aperture Jitter			2		ps (RMS)
	Over Range Recovery Time	Differential V_{IN} step from ±3V to 0V to get accurate conversion		1		Clock Cycle
t_{STBY}	Standby Mode Exit Cycle			20		Cycles

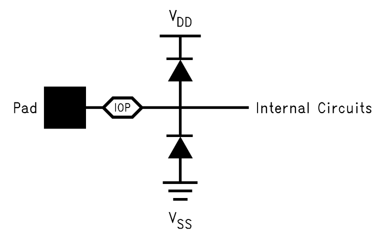


Figure 2.

Specification Definitions

APERTURE DELAY is the time after the rising edge of the clock to when the input signal is acquired or held for conversion.

APERTURE JITTER (APERTURE UNCERTAINTY) is the variation in aperture delay from sample to sample. Aperture jitter manifests itself as noise in the output.

COMMON MODE VOLTAGE (V_{CM}) is the d.c. potential present at both signal inputs to the ADC.

CONVERSION LATENCY See PIPELINE DELAY.

DIFFERENTIAL NON-LINEARITY (DNL) is the measure of the maximum deviation from the ideal step size of 1 LSB.

DUTY CYCLE is the ratio of the time that a repetitive digital waveform is high to the total time of one period. The specification here refers to the ADC clock input signal.

EFFECTIVE NUMBER OF BITS (ENOB, or EFFECTIVE BITS) is another method of specifying Signal-to-Noise and Distortion or SINAD. ENOB is defined as (SINAD - 1.76) / 6.02 and states that the converter is equivalent to a perfect ADC of this (ENOB) number of bits.

FULL POWER BANDWIDTH is a measure of the frequency at which the reconstructed output fundamental drops 3 dB below its low frequency value for a full scale input.

GAIN ERROR is the deviation from the ideal slope of the transfer function. It can be calculated as:

$$\text{Gain Error} = \text{Positive Full-Scale Error} - \text{Negative Full-Scale Error} \quad (1)$$

INTEGRAL NON LINEARITY (INL) is a measure of the deviation of each individual code from a line drawn from negative full scale through positive full scale. The deviation of any given code from this straight line is measured from the center of that code value.

MISSING CODES are those output codes that will never appear at the ADC outputs. The ADC10065 is specified not to have any missing codes.

NEGATIVE FULL SCALE ERROR is the difference between the input voltage ($V_{IN}^+ - V_{IN}^-$) just causing a transition from negative full scale to the first code and its ideal value of 0.5 LSB.

OFFSET ERROR is the input voltage that will cause a transition from a code of 01 1111 1111 to a code of 10 0000 0000.

OUTPUT DELAY is the time delay after the rising edge of the clock before the data update is presented at the output pins.

PIPELINE DELAY (LATENCY) is the number of clock cycles between initiation of conversion and when that data is presented to the output driver stage. Data for any given sample is available at the output pins the Pipeline Delay plus the Output Delay after the sample is taken. New data is available at every clock cycle, but the data lags the conversion by the pipeline delay.

POSITIVE FULL SCALE ERROR is the difference between the actual last code transition and its ideal value of 1½ LSB below positive full scale.

SIGNAL TO NOISE RATIO (SNR) is the ratio, expressed in dB, of the rms value of the input signal to the rms value of the sum of all other spectral components below one-half the sampling frequency, not including harmonics or DC.

SIGNAL TO NOISE PLUS DISTORTION (S/N+D or SINAD) is the ratio, expressed in dB, of the rms value of the input signal to the rms value of all of the other spectral components below half the clock frequency, including harmonics but excluding DC.

SPURIOUS FREE DYNAMIC RANGE (SFDR) is the difference, expressed in dB, between the rms values of the input signal and the peak spurious signal, where a spurious signal is any signal present in the output spectrum that is not present at the input.

TOTAL HARMONIC DISTORTION (THD) is the ratio, expressed in dBc, of the rms total of the first six harmonic levels at the output to the level of the fundamental at the output. THD is calculated as:

$$\mathrm{THD} = 20 \times \log \sqrt{\frac{f_2^2 + f_3^2 + \ldots + f_6^2}{f_1^2}}$$

where

- f_1 is the RMS power of the fundamental (output) frequency
- f_2 through f_6 are the RMS power in the first 6 harmonic frequencies. (2)

SECOND HARMONIC DISTORTION (2ND HARM) is the difference expressed in dB, between the RMS power in the input frequency at the output and the power in its 2nd harmonic level at the output.

THIRD HARMONIC DISTORTION (3RD HARM) is the difference, expressed in dB, between the RMS power in the input frequency at the output and the power in its 3rd harmonic level at the output.

Timing Diagram

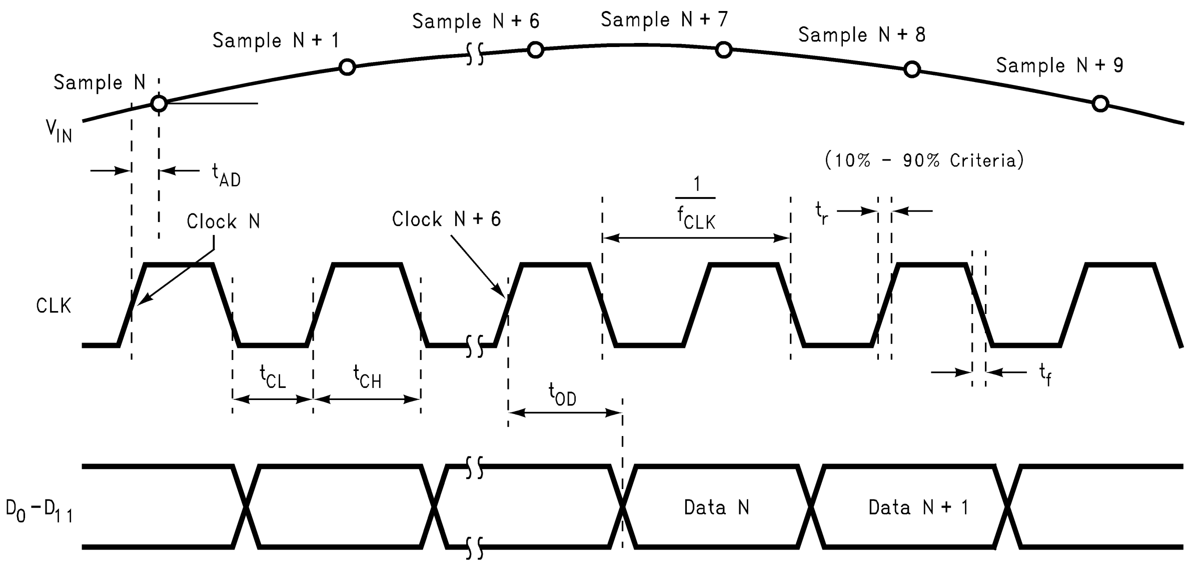


Figure 3. Clock and Data Timing Diagram

Transfer Characteristics

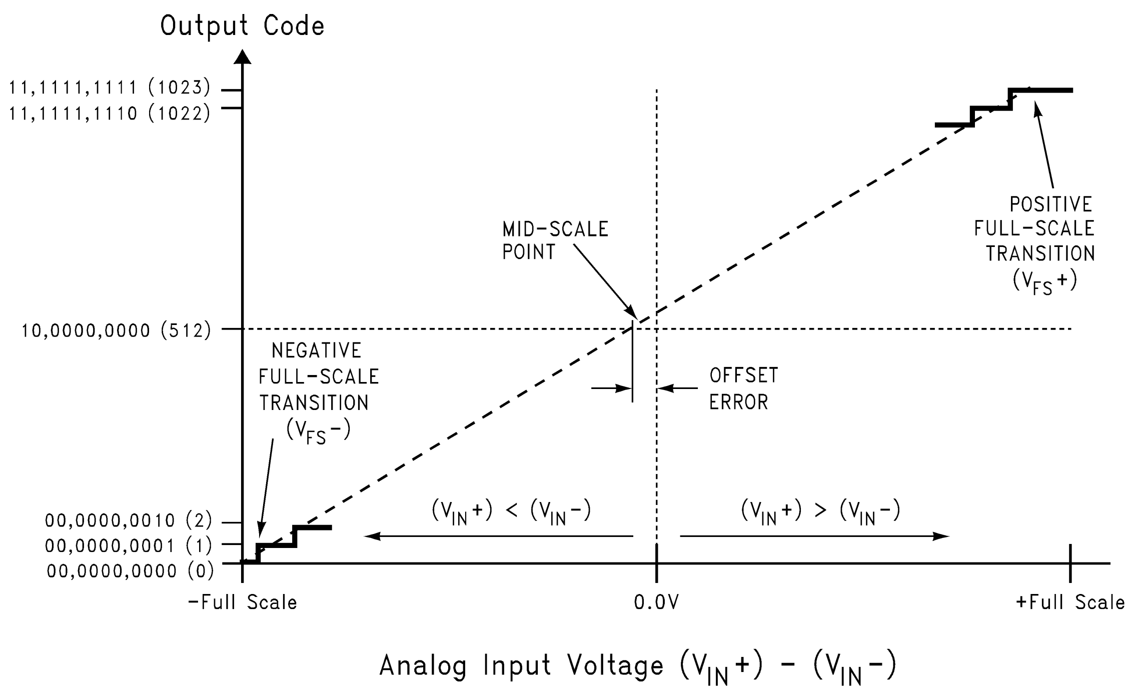


Figure 4. Input vs. Output Transfer Characteristic

Typical Performance Characteristics

Unless otherwise specified, the following specifications apply: $V_{SSA} = V_{SSIO} = 0V$, $V_{DDA} = +3.0V$, $V_{DDIO} = +2.5V$, $V_{IN} = 2\ V_{P-P}$, STBY = 0V, V_{REF} = External 1.2V, f_{CLK} = 65 MHz, f_{IN} = 11 MHz, 50% Duty Cycle.

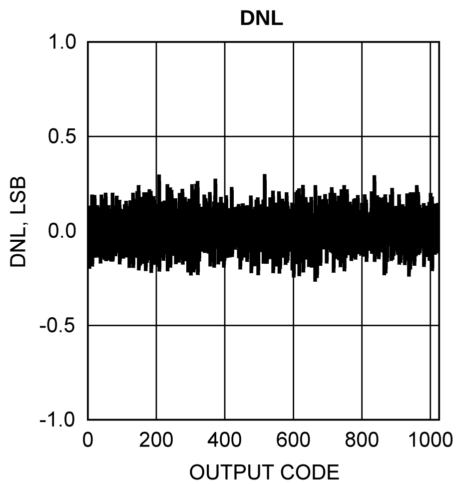


Figure 5.

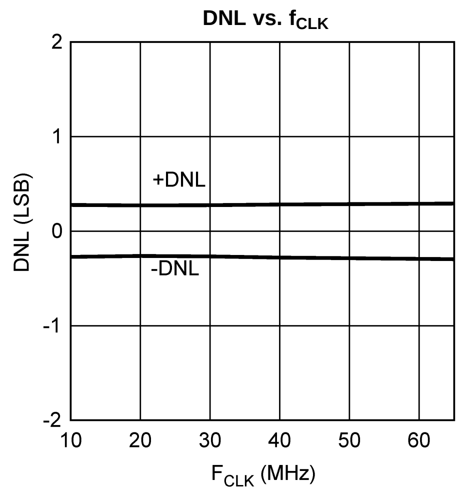


Figure 6.

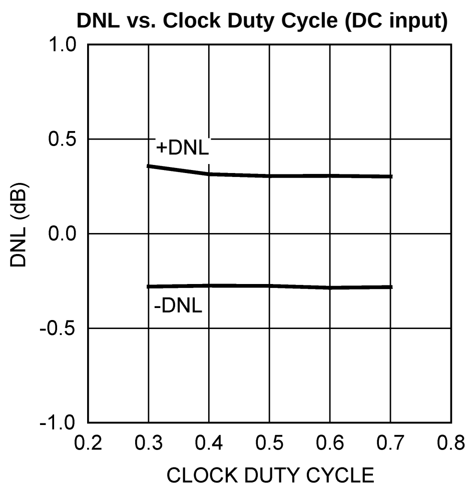


Figure 7.

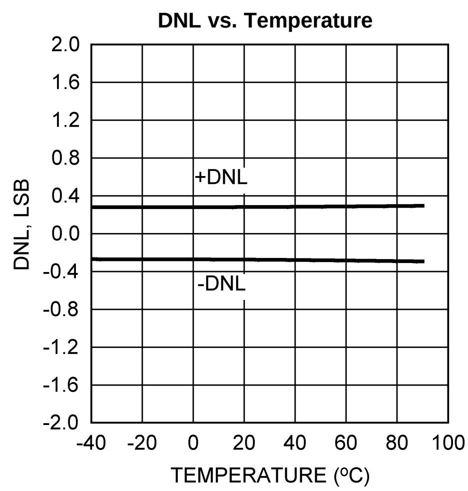


Figure 8.

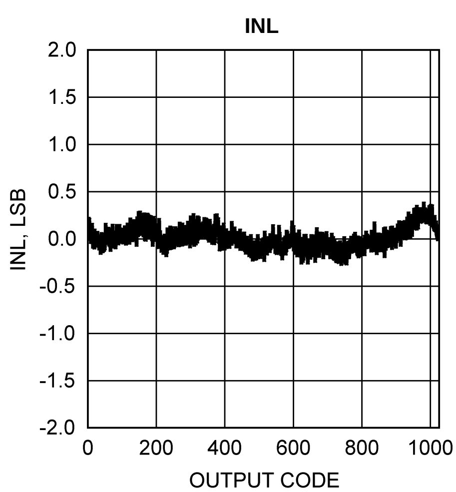


Figure 9.

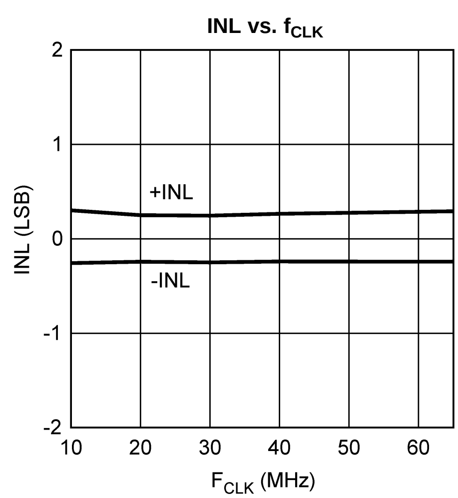


Figure 10.

Typical Performance Characteristics (continued)

Unless otherwise specified, the following specifications apply: $V_{SSA} = V_{SSIO} = 0V$, $V_{DDA} = +3.0V$, $V_{DDIO} = +2.5V$, $V_{IN} = 2\ V_{P-P}$, STBY = 0V, V_{REF} = External 1.2V, f_{CLK} = 65 MHz, f_{IN} = 11 MHz, 50% Duty Cycle.

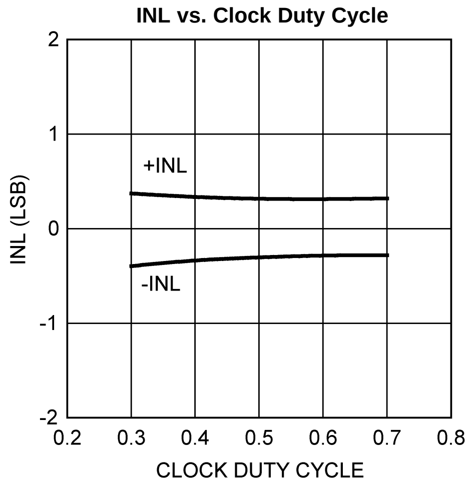


Figure 11.

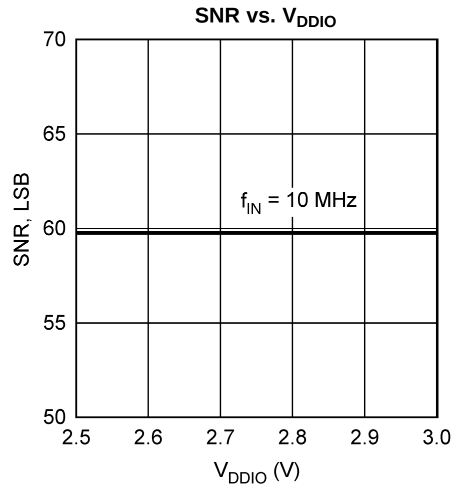


Figure 12.

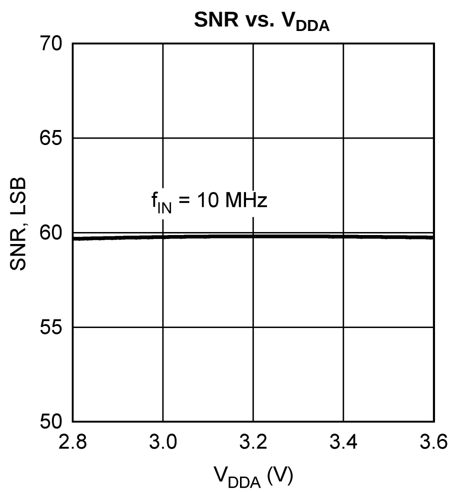


Figure 13.

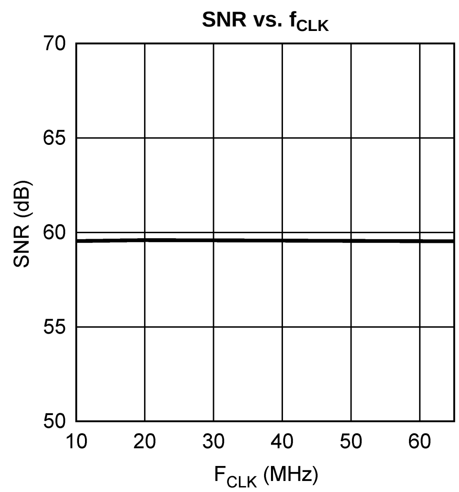


Figure 14.

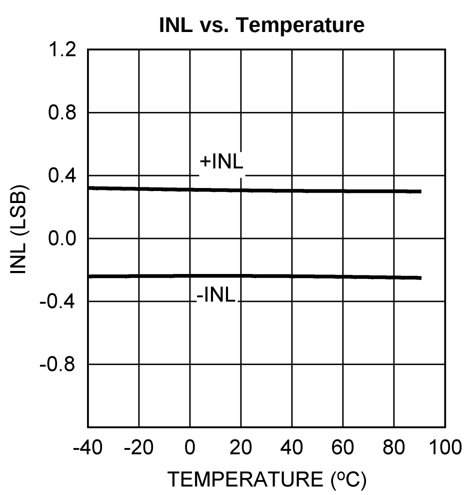


Figure 15.

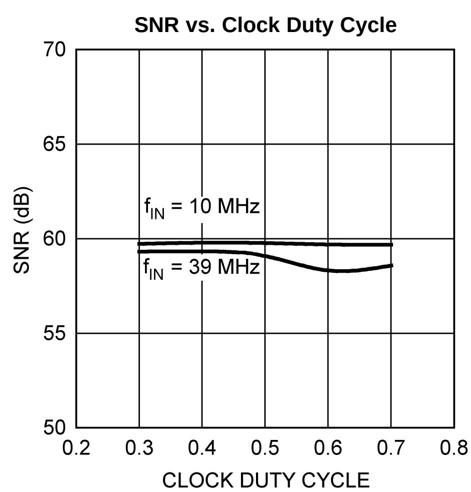


Figure 16.

Typical Performance Characteristics (continued)

Unless otherwise specified, the following specifications apply: $V_{SSA} = V_{SSIO} = 0V$, $V_{DDA} = +3.0V$, $V_{DDIO} = +2.5V$, $V_{IN} = 2\ V_{P-P}$, STBY = 0V, V_{REF} = External 1.2V, f_{CLK} = 65 MHz, f_{IN} = 11 MHz, 50% Duty Cycle.

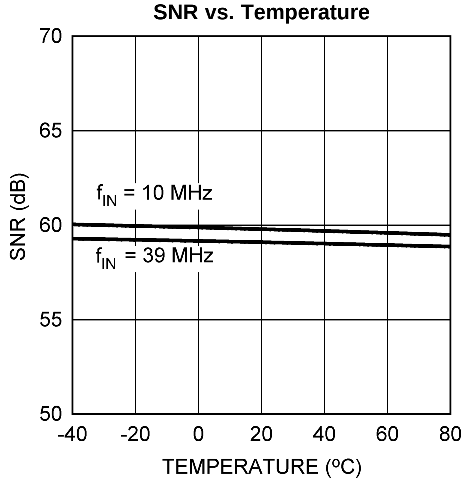


Figure 17.

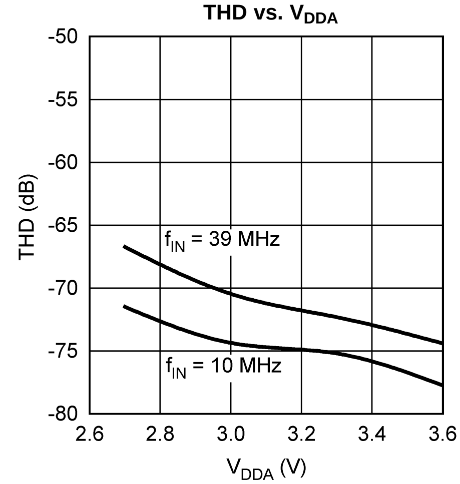


Figure 18.

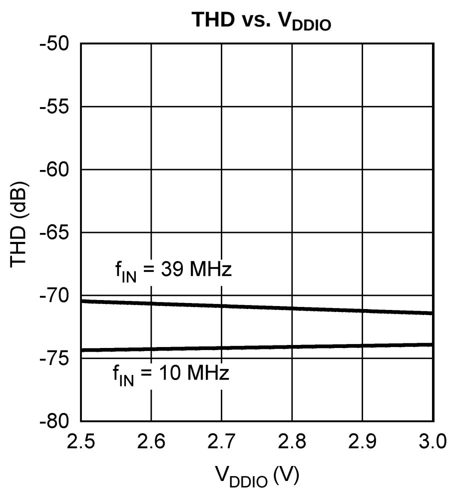


Figure 19.

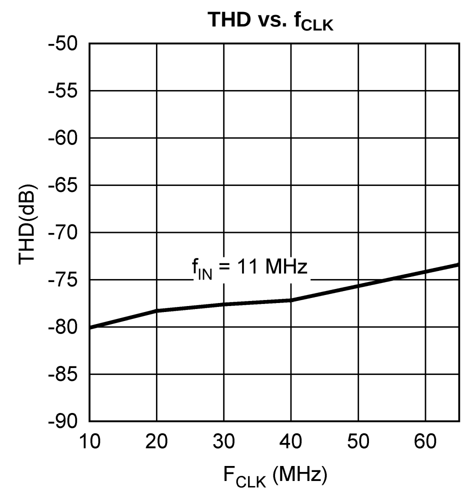


Figure 20.

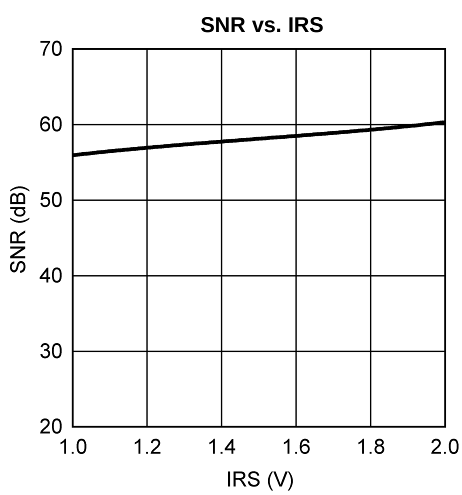


Figure 21.

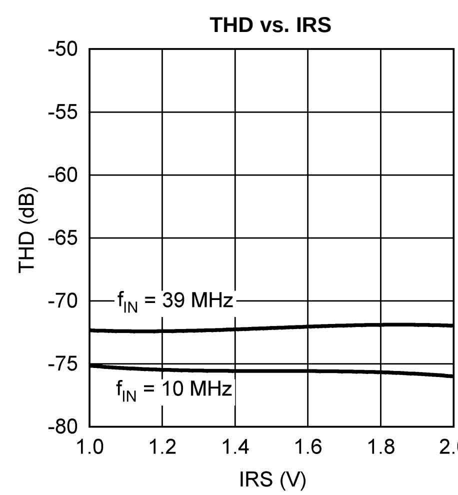


Figure 22.

Typical Performance Characteristics (continued)

Unless otherwise specified, the following specifications apply: $V_{SSA} = V_{SSIO} = 0V$, $V_{DDA} = +3.0V$, $V_{DDIO} = +2.5V$, $V_{IN} = 2\ V_{P-P}$, STBY = 0V, V_{REF} = External 1.2V, f_{CLK} = 65 MHz, f_{IN} = 11 MHz, 50% Duty Cycle.

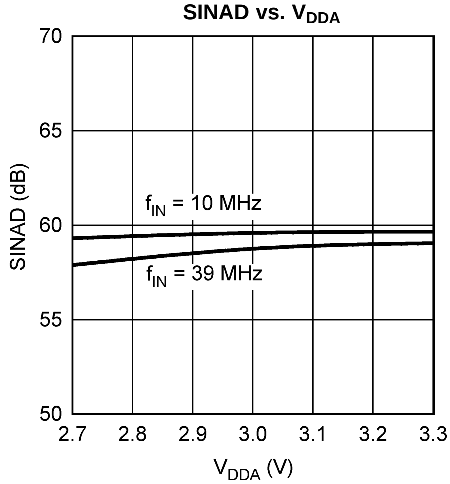


Figure 23.

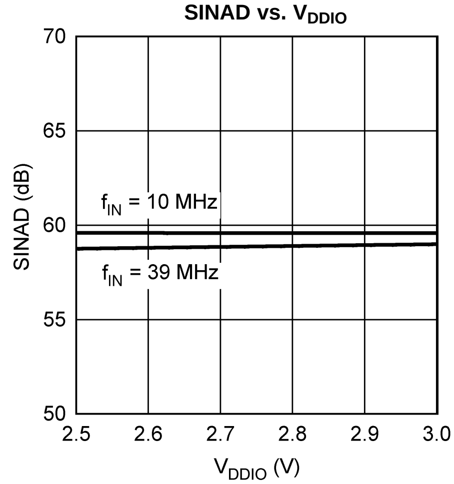


Figure 24.

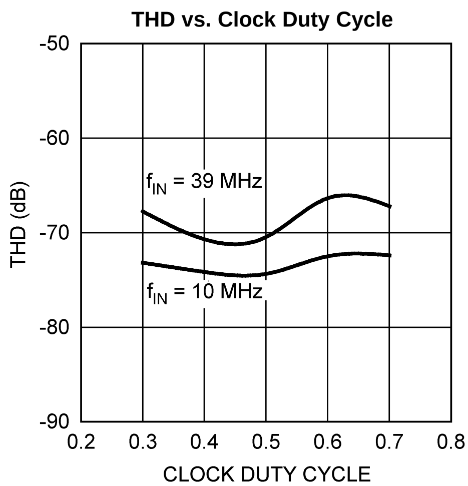


Figure 25.

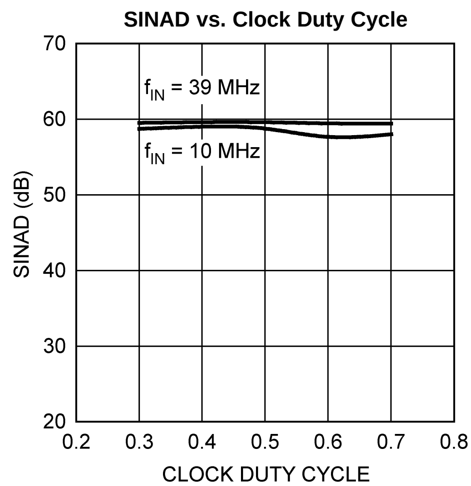


Figure 26.

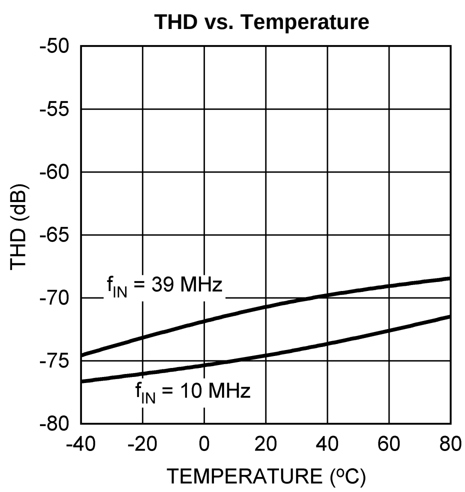


Figure 27.

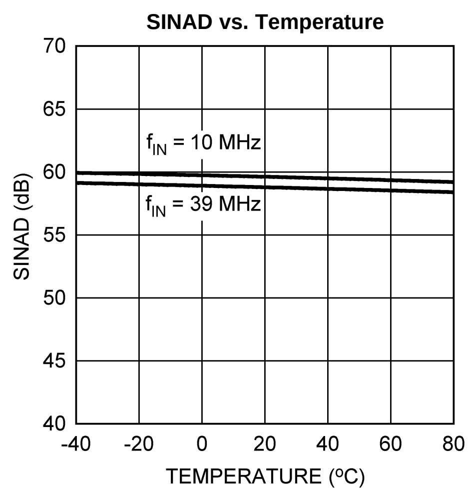


Figure 28.

Typical Performance Characteristics (continued)

Unless otherwise specified, the following specifications apply: $V_{SSA} = V_{SSIO} = 0V$, $V_{DDA} = +3.0V$, $V_{DDIO} = +2.5V$, $V_{IN} = 2\ V_{P-P}$, STBY = 0V, V_{REF} = External 1.2V, f_{CLK} = 65 MHz, f_{IN} = 11 MHz, 50% Duty Cycle.

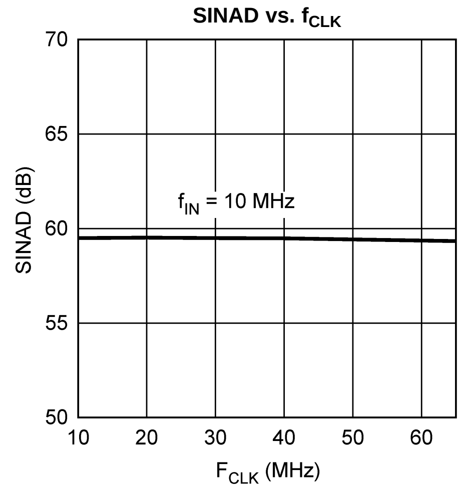


Figure 29.

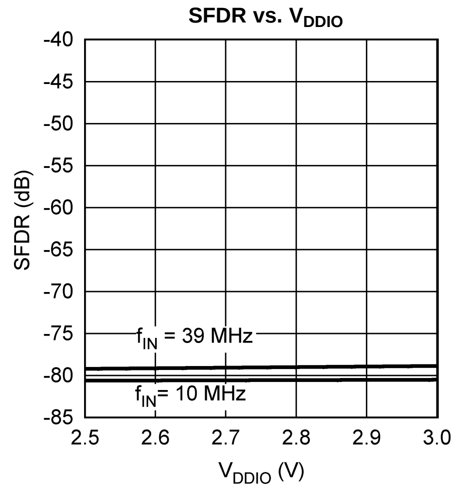


Figure 30.

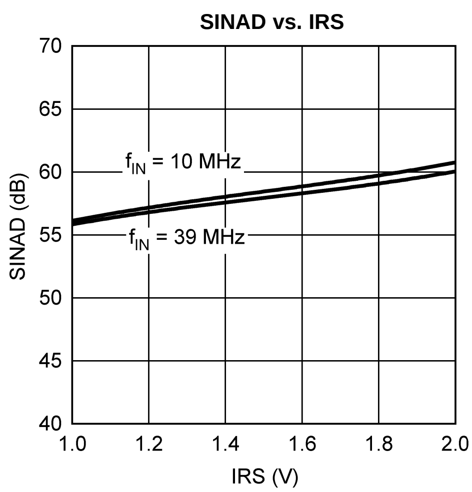


Figure 31.

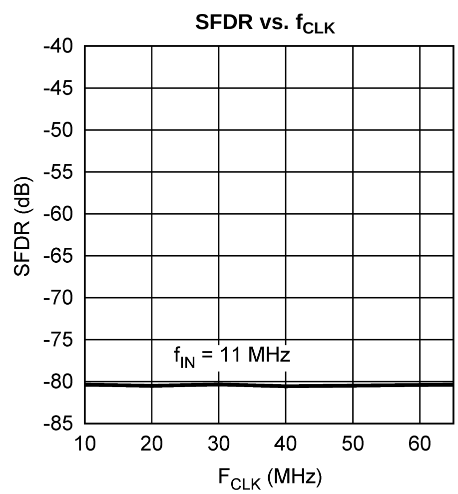


Figure 32.

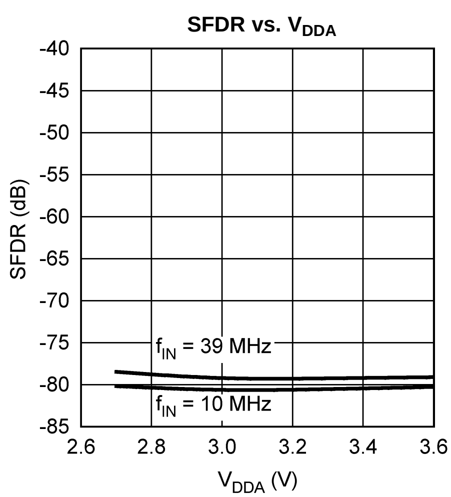


Figure 33.

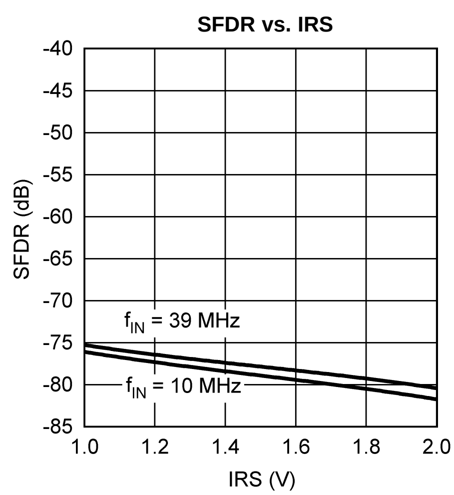


Figure 34.

Typical Performance Characteristics (continued)

Unless otherwise specified, the following specifications apply: $V_{SSA} = V_{SSIO} = 0V$, $V_{DDA} = +3.0V$, $V_{DDIO} = +2.5V$, $V_{IN} = 2\ V_{P-P}$, STBY = 0V, V_{REF} = External 1.2V, f_{CLK} = 65 MHz, f_{IN} = 11 MHz, 50% Duty Cycle.

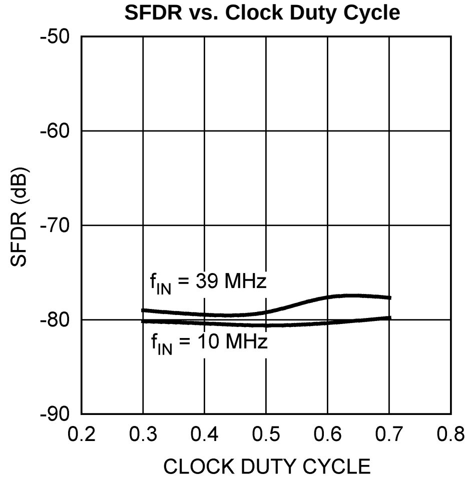


Figure 35.

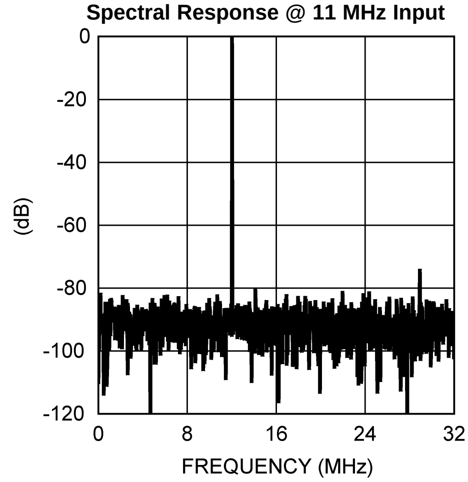


Figure 36.

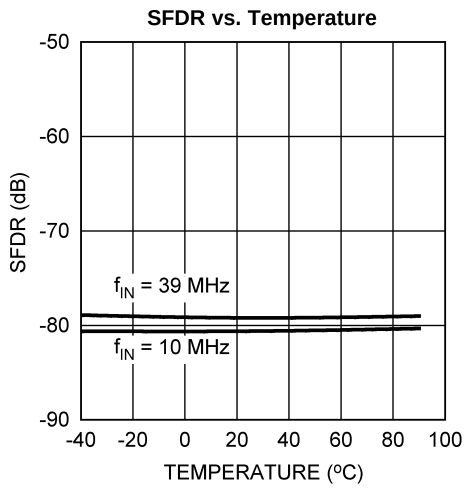


Figure 37.

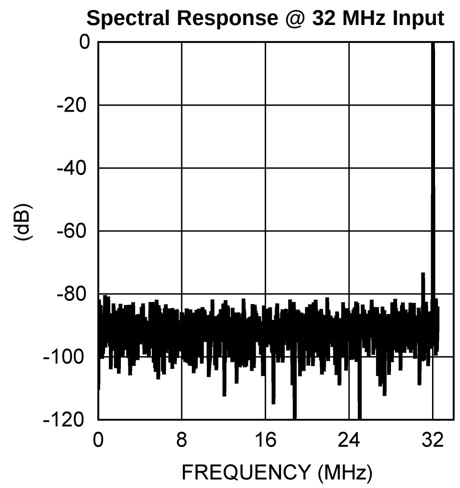


Figure 38.

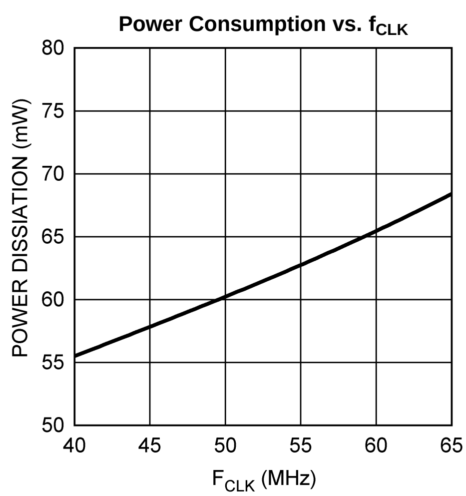


Figure 39.

FUNCTIONAL DESCRIPTION

The ADC10065 uses a pipeline architecture and has error correction circuitry to help ensure maximum performance. Differential analog input signals are digitized to 10 bits. In differential mode, each analog input signal should have a peak-to-peak voltage equal to 1.0V, 0.75V or 0.5V, depending on the state of the IRS pin (pin 5), and be centered around V_{CM} and be 180° out of phase with each other. If single ended operation is desired, V_{IN}- may be tied to the V_{COM} pin (pin 4). A single ended input signal may then be applied to V_{IN}+, and should have an average value in the range of V_{CM}. The signal amplitude should be 2.0V, 1.5V or 1.0V peak-to-peak, depending on the state or the IRS pin (pin 5).

Applications Information

ANALOG INPUTS

The ADC10065 has two analog signal inputs, V_{IN}+ and V_{IN}−. These two pins form a differential input pair. There is one common mode pin V_{COM} that may be used to set the common mode input voltage.

REFERENCE PINS

The ADC10065 is designed to operate with a 1.2V reference. The voltages at V_{COM}, V_{REFT}, and V_{REFB} are derived from the reference voltage. It is very important that all grounds associated with the reference voltage and the input signal make connection to the analog ground plane at a single point to minimize the effects of noise currents in the ground path. The three Reference Bypass Pins V_{REF}, V_{REFT} and V_{REFB}, are made available for bypass purposes only. These pins should each be bypassed to ground with a 0.1 µF capacitor. DO NOT LOAD these pins.

V_{COM} PIN

This pin supplies a voltage for possible use to set the common mode input voltage. This pin may also be connected to V_{IN}-, so that V_{IN}+ may be used as a single ended input. This pin should be bypassed with at least a 0.1 µF capacitor. Do not load this pin.

SIGNAL INPUTS

The signal inputs are V_{IN}+ and V_{IN}−. The input signal amplitude is defined as $V_{IN}+ - V_{IN}-$ and is represented schematically in Figure 40*:*

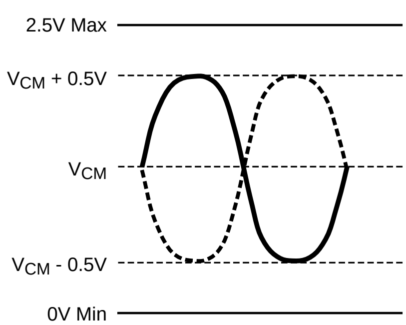


Figure 40. Input Voltage Waveforms for a $2V_{P-P}$ differential Input

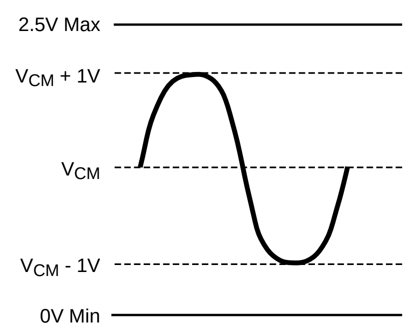


Figure 41. Input Voltage Waveform for a $2V_{P-P}$ Single Ended Input

A single ended input signal is shown in Figure 41.

The internal switching action at the analog inputs causes energy to be output from the input pins. As the driving source tries to compensate for this, it adds noise to the signal. To prevent this, use 18Ω series resistors at each of the signal input pins with a 25 pF capacitor across the inputs, as shown in Figure 42. These components should be placed close to the ADC because the input pins of the ADC is the most sensitive part of the system and this is the last opportunity to filter the input. The two 18Ω resistors and the 25 pF capacitor form a low-pass filter with a -3 dB frequency of 177 MHz.

CLK PIN

The CLK signal controls the timing of the sampling process. Drive the clock input with a stable, low jitter clock signal in the frequency range indicated in AC Electrical Characteristics with rise and fall times of less than 2 ns. The trace carrying the clock signal should be as short as possible and should not cross any other signal line, analog or digital, not even at 90°. The CLK signal also drives an internal state machine. If the CLK is interrupted, or its frequency is too low, the charge on internal capacitors can dissipate to the point where the accuracy of the output data will degrade. This is what limits the lowest sample rate. The duty cycle of the clock signal can affect the performance of any A/D Converter. Because achieving a precise duty cycle is difficult, the ADC10065 is designed to maintain performance over a range of duty cycles. While it is specified and performance is ensured with a 50% clock duty cycle, performance is typically maintained with minimum clock low and high times indicated in AC Electrical Characteristics. Both minimum high and low times may not be held simultaneously

STBY PIN

The STBY pin, when high, holds the ADC10065 in a power-down mode to conserve power when the converter is not being used. The power consumption in this state is 15 mW. The output data pins are undefined in this mode. Power consumption during power-down is not affected by the clock frequency, or by whether there is a clock signal present. The data in the pipeline is corrupted while in power down.

DF PIN

The DF (Data Format) pin, when high, forces the ADC10065 to output the 2's complement data format. When DF is tied low, the output format is offset binary.

IRS PIN

The IRS (Input Range Select) pin defines the input signal amplitude that will produce a full scale output. Table 1 describes the function of the IRS pin.

Table 1. IRS Pin Functions

IRS Pin	Full-Scale Input
V_{DDA}	$2.0V_{P-P}$
V_{SSA}	$1.5V_{P-P}$
Floating	$1.0V_{P-P}$

OUTPUT PINS

The ADC10065 has 10 TTL/CMOS compatible Data Output pins. The offset binary data is present at these outputs while the DF and STBY pins are low. Be very careful when driving a high capacitance bus. The more capacitance the output drivers must charge for each conversion, the more instantaneous digital current flows through V_{DDIO} and V_{SSIO}. These large charging current spikes can cause on-chip noise and couple into the analog circuitry, degrading dynamic performance. Adequate bypassing, limiting output capacitance and careful attention to the ground plane will reduce this problem. Additionally, bus capacitance beyond the specified 10 pF/pin will cause t_{OD} to increase, making it difficult to properly latch the ADC output data. The result could be an apparent reduction in dynamic performance. To minimize noise due to output switching, minimize the load currents at the digital outputs. This can be done by minimizing load capacitance and by connecting buffers between the ADC outputs and any other circuitry, which will isolate the outputs from trace and other circuit capacitances and limit the output currents, which could otherwise result in performance degradation. Only one driven input should be connected to the ADC output pins.

While the t_{OD} time provides information about output timing, a simple way to capture a valid output is to latch the data on the rising edge of the conversion clock.

APPLICATION SCHEMATICS

The following figures show simple examples of using the ADC10065. Figure 42 shows a typical differentially driven input. Figure 43 shows a single ended application circuit.

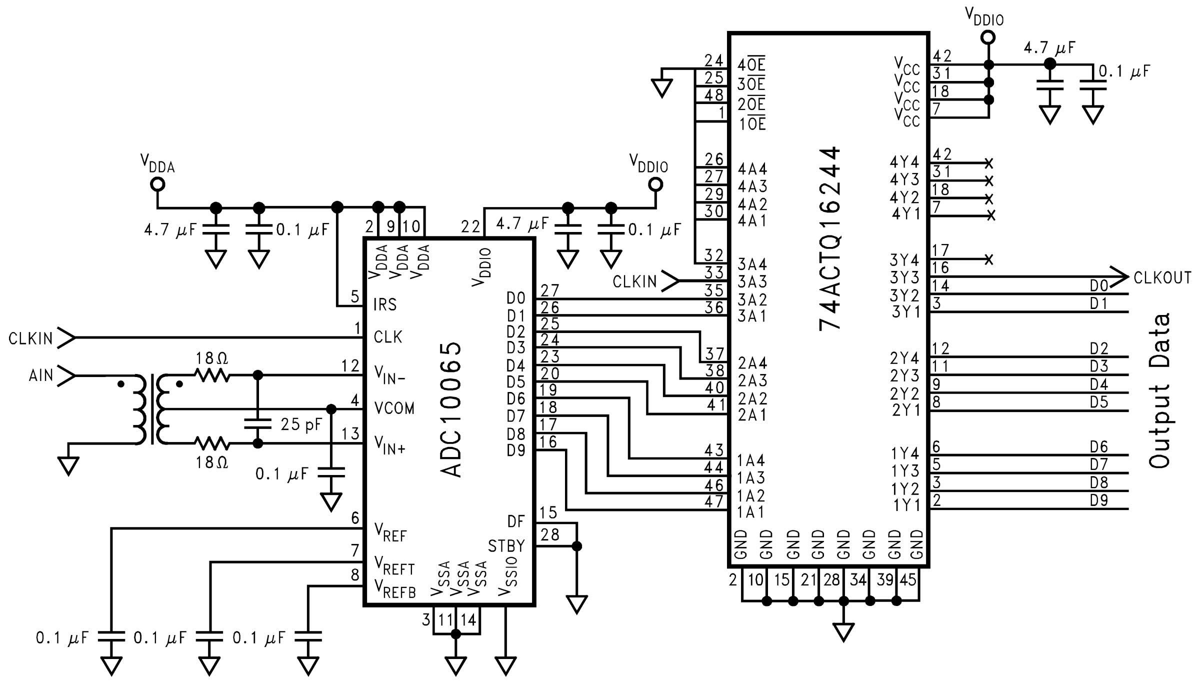


Figure 42. A Simple Application Using a Differential Driving Source

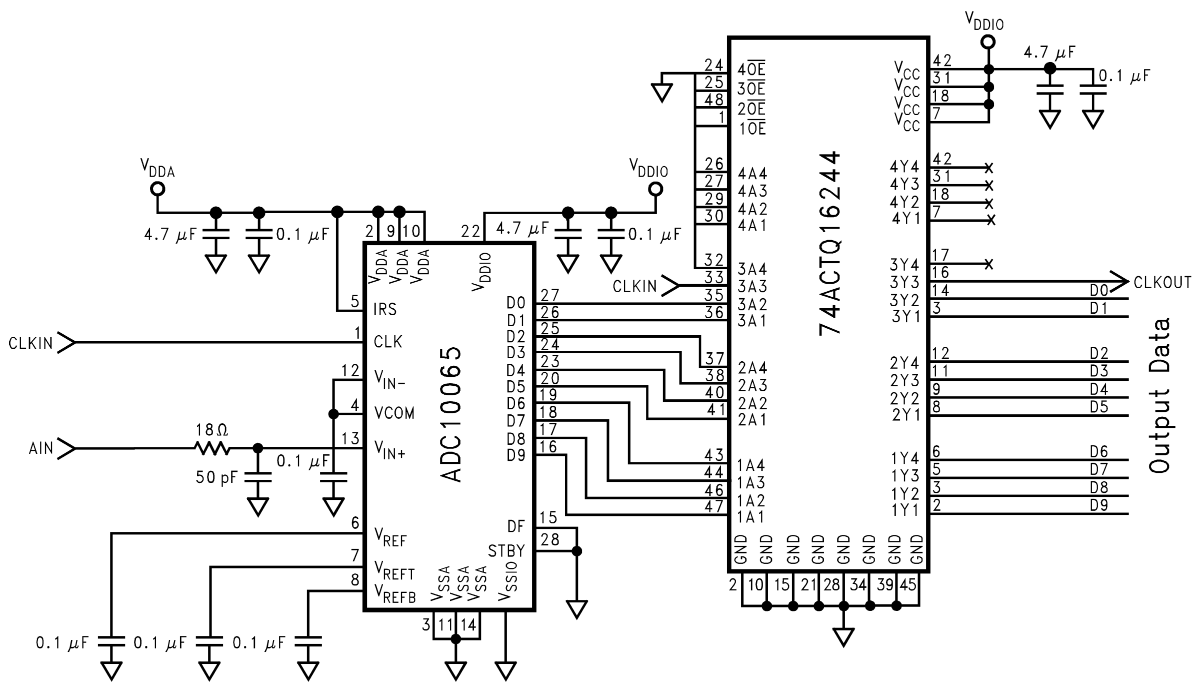


Figure 43. A Simple Application Using a Single Ended Driving Source

REVISION HISTORY

Changes from Revision G (April 2013) to Revision H	Page
• Changed layout of National Data Sheet to TI format	19

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
ADC10065CIMT/NOPB	ACTIVE	TSSOP	PW	28	48	Green (RoHS & no Sb/Br)	CU SN	Level-3-260C-168 HR	-40 to 85	ADC10065 CIMT	Samples
ADC10065CIMTX/NOPB	ACTIVE	TSSOP	PW	28	2500	Green (RoHS & no Sb/Br)	CU SN	Level-3-260C-168 HR	-40 to 85	ADC10065 CIMT	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

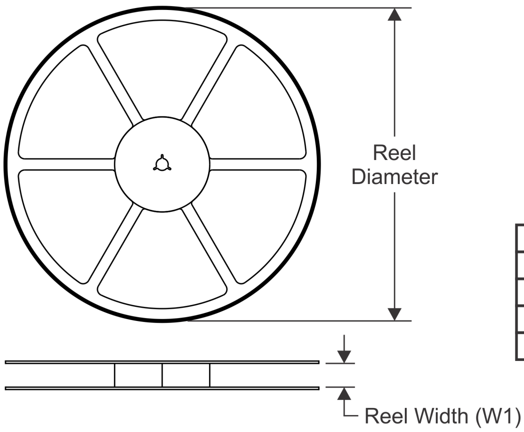
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

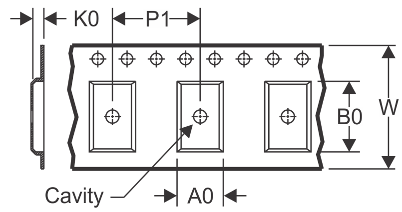
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

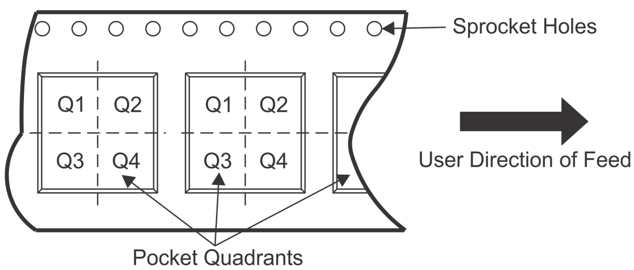


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

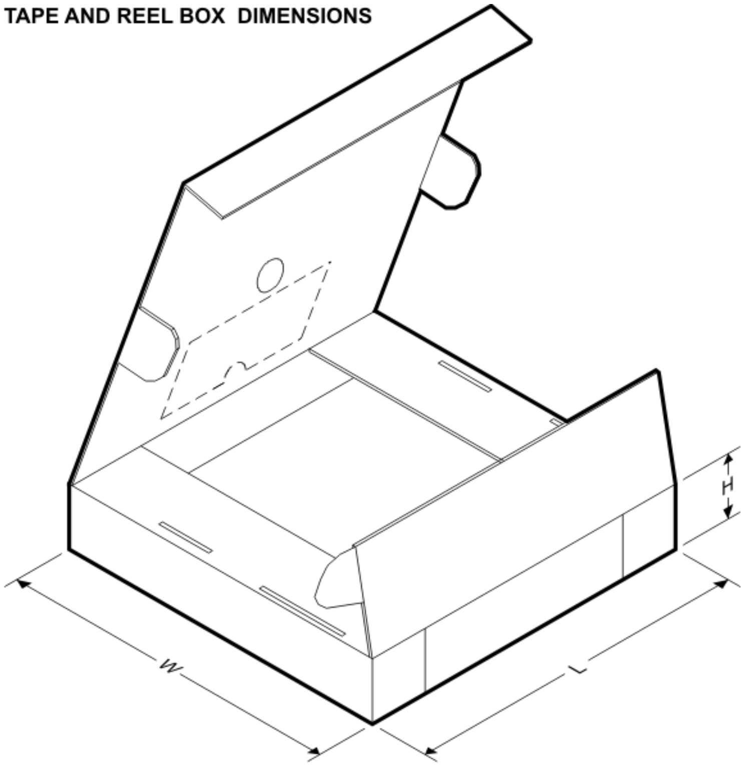
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
ADC10065CIMTX/NOPB	TSSOP	PW	28	2500	330.0	16.4	6.8	10.2	1.6	8.0	16.0	Q1

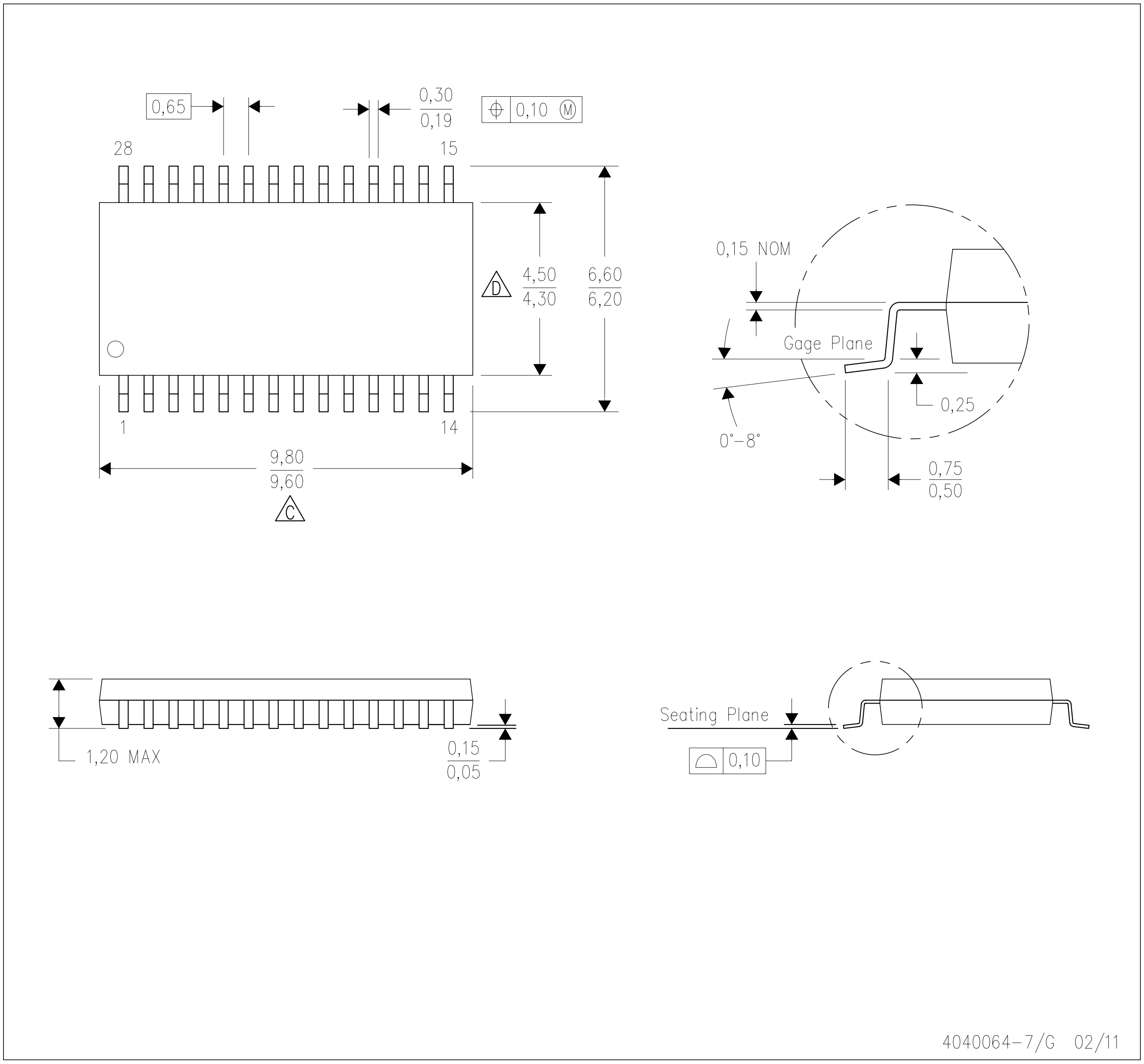
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
ADC10065CIMTX/NOPB	TSSOP	PW	28	2500	367.0	367.0	38.0

PW (R–PDSO–G28) PLASTIC SMALL OUTLINE



NOTES: A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
E. Falls within JEDEC MO–153