DS250DF410 25 Gbps Multi-Rate 4-Channel Retimer

1 Features

- Quad-Channel Multi-Rate Retimer with Integrated Signal Conditioning
- All Channels Lock Independently from 20.6 to 25.8 Gbps (Including Sub-Rates Like 10.3125 Gbps, 12.5 Gbps, and More)
- Ultra-Low Latency: <500 ps Typical for 25.78125-Gbps Data Rate
- Single Power Supply, No Low-Jitter Reference Clock Required, and Minimal Supply Decoupling to Reduce Board Routing Complexity and BOM Cost
- Integrated 2×2 Cross Point
- Adaptive Continuous Time Linear Equalizer (CTLE)
- Adaptive Decision Feedback Equalizer (DFE)
- Low-Jitter Transmitter With 3-Tap FIR Filter
- Combined Equalization Supporting 35+ dB Channel Loss at 12.9 GHz
- Adjustable Transmit Amplitude: 205 mVppd to 1225 mVppd (Typical)
- On-Chip Eye Opening Monitor (EOM), PRBS Pattern Checker/Generator
- Supports JTAG/AC-JTAG Boundary Scan
- Small 6-mm × 6-mm BGA Package with Easy Flow-Through Routing

2 Applications

- Jitter Cleaning for Front-Port Optical
- Active Cable Assemblies
- Backplane/Mid-Plane Reach Extension
- IEEE802.3bj 100GbE, Infiniband EDR, and OIF-CEI-25G-LR/MR/SR/VSR Electrical Interfaces
- SFP28, QSFP28, CFP2/CFP4, CDFP

3 Description

The DS250DF410 is a four-channel multi-rate retimer with integrated signal conditioning. It is used to extend the reach and robustness of long, lossy, crosstalk-impaired high-speed serial links while achieving a bit error rate (BER) of 10^{-15} or less.

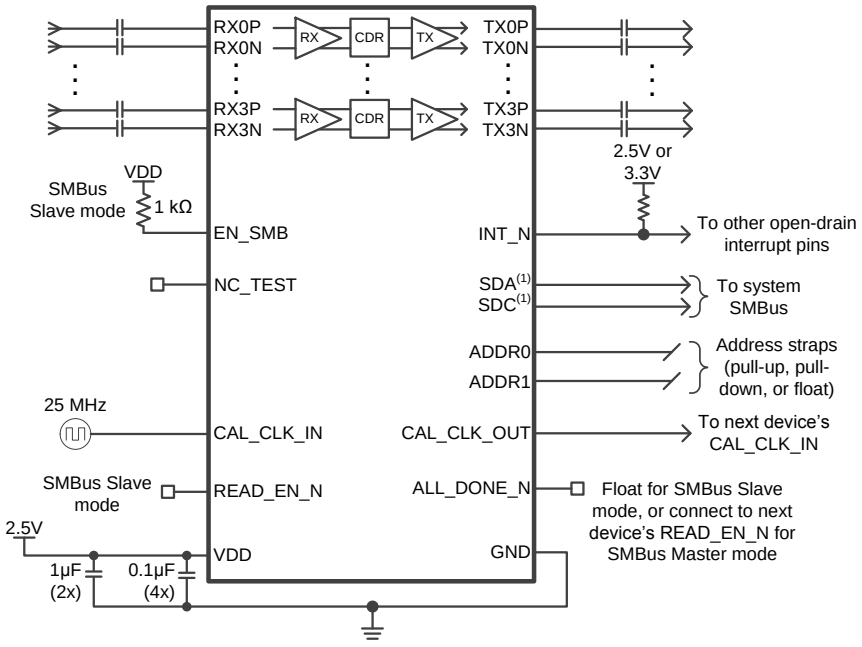
Each channel of the DS250DF410 independently locks to serial data rates in a continuous range from 20.6 Gbps to 25.8 Gbps or to any supported sub-rate (÷2 and ÷4), including key data rates such as 10.3125 Gbps and 12.5 Gbps, which allows the DS250DF410 to support individual lane Forward Error Correction (FEC) pass-through.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
DS250DF410	ABM (101)	6.0 mm × 6.0 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Simplified Schematic



(1) SMBus signals need to be pulled up elsewhere in the system.

4 Description (continued)

The DS250DF410 has a single power supply and minimal need for external components. These features reduce PCB routing complexity and BOM cost.

The advanced equalization features of the DS250DF410 include a low-jitter 3-tap transmit finite impulse response (FIR) filter, an adaptive continuous-time linear equalizer (CTLE), and an adaptive decision feedback equalizer (DFE). This enables reach extension for lossy interconnect and backplanes with multiple connectors and crosstalk. The integrated CDR function is ideal for front-port optical module applications to reset the jitter budget and retime the high-speed serial data. The DS250DF410 implements 2x2 cross-point on each channel pair, providing the host with lane crossing, fanout, and multiplexing options.

The DS250DF410 can be configured either through the SMBus or through an external EEPROM. Up to 16 devices can share a single EEPROM using Common Channel format. A non-disruptive on-chip eye monitor and a PRBS generator/checker allow for in-system diagnostics.

Table of Contents

5 Revision History

DATE	REVISION	NOTES
February 2016	*	Initial release.

6 Device and Documentation Support

6.1 Device Support

6.1.1 Development Support

For additional information, see TI's Surface Mount Technology (SMT) References at:

http://focus.ti.com/quality/docs under the *Quality & Lead (Pb)-Free Data* menu.

6.2 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

6.3 Trademarks

E2E is a trademark of Texas Instruments.

6.4 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

6.5 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

7 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
DS250DF410ABMR	ACTIVE	FC/CSP	ABM	101	1000	Green (RoHS & no Sb/Br)	SNAGCU	Level-3-260C-168 HR	-40 to 85	DS250DF4	Samples
DS250DF410ABMT	ACTIVE	FC/CSP	ABM	101	250	Green (RoHS & no Sb/Br)	SNAGCU	Level-3-260C-168 HR	-40 to 85	DS250DF4	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

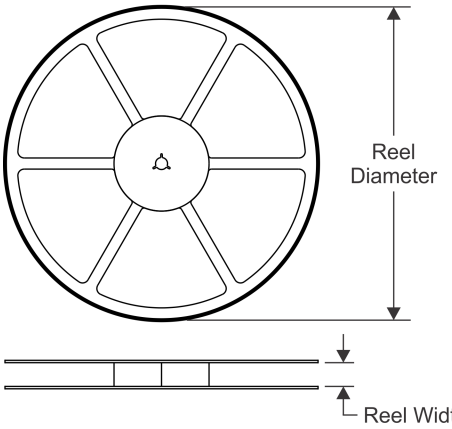
(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

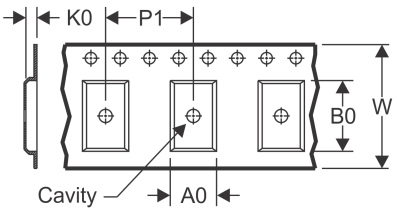
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

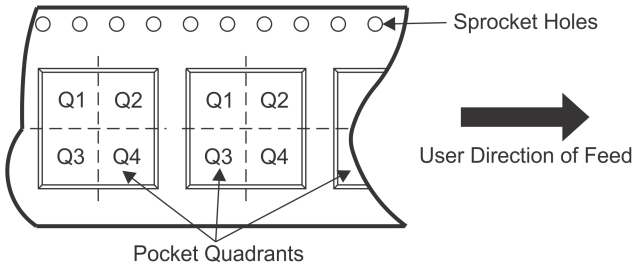


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

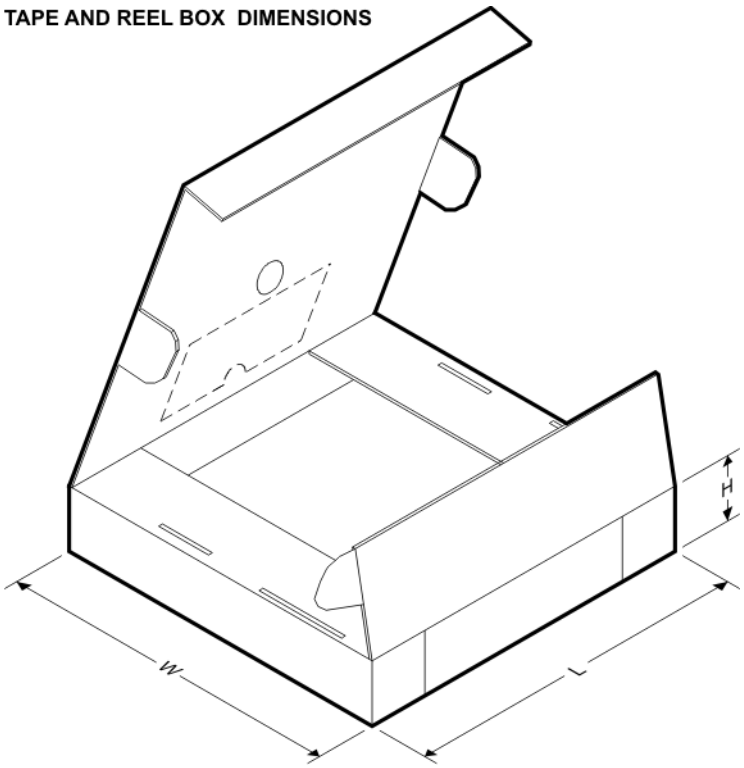
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
DS250DF410ABMR	FC/CSP	ABM	101	1000	330.0	16.4	6.3	6.3	1.5	12.0	16.0	Q1
DS250DF410ABMT	FC/CSP	ABM	101	250	178.0	16.4	6.3	6.3	1.5	12.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

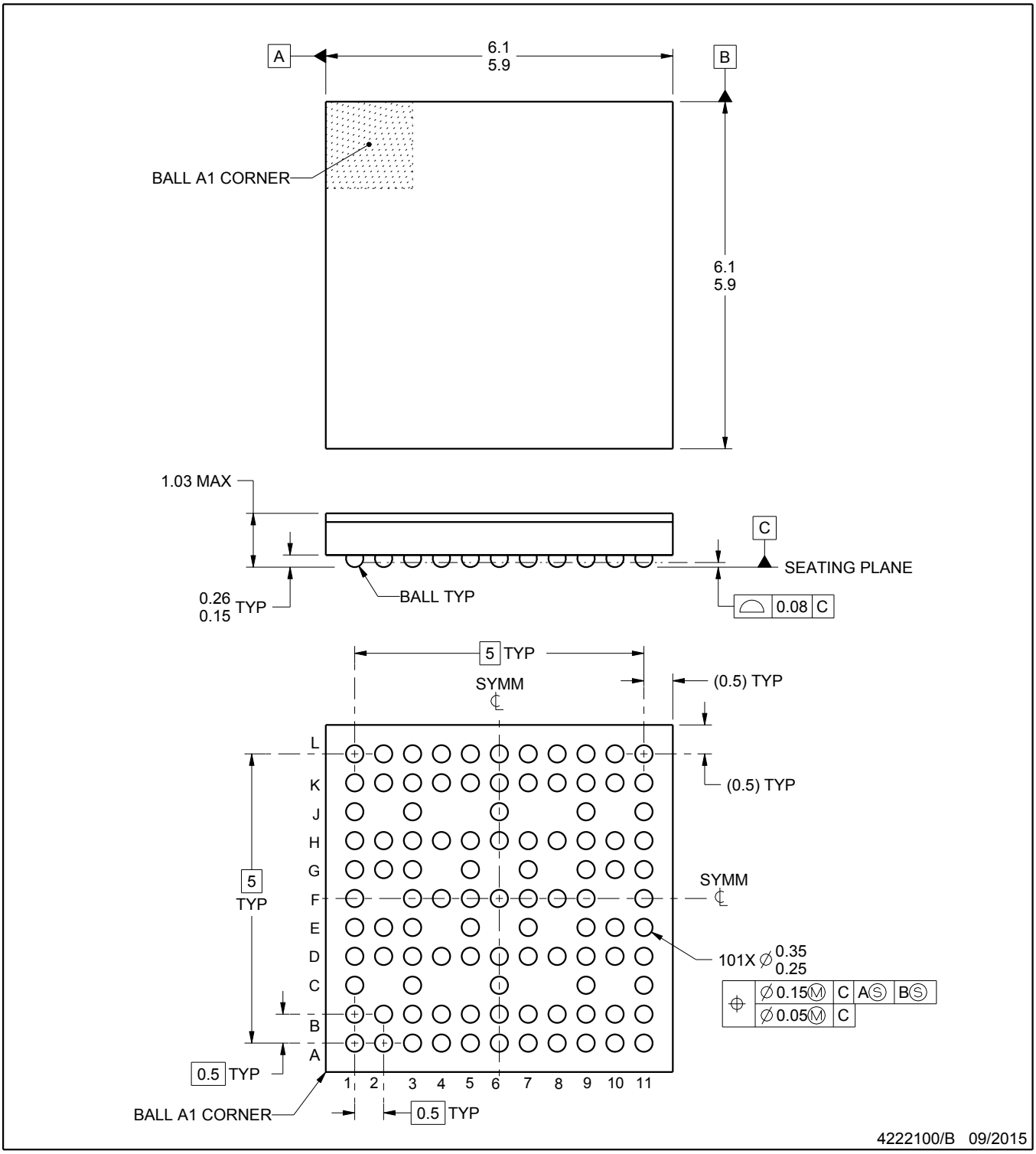
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
DS250DF410ABMR	FC/CSP	ABM	101	1000	367.0	367.0	38.0
DS250DF410ABMT	FC/CSP	ABM	101	250	210.0	185.0	35.0

PACKAGE OUTLINE

ABM0101A

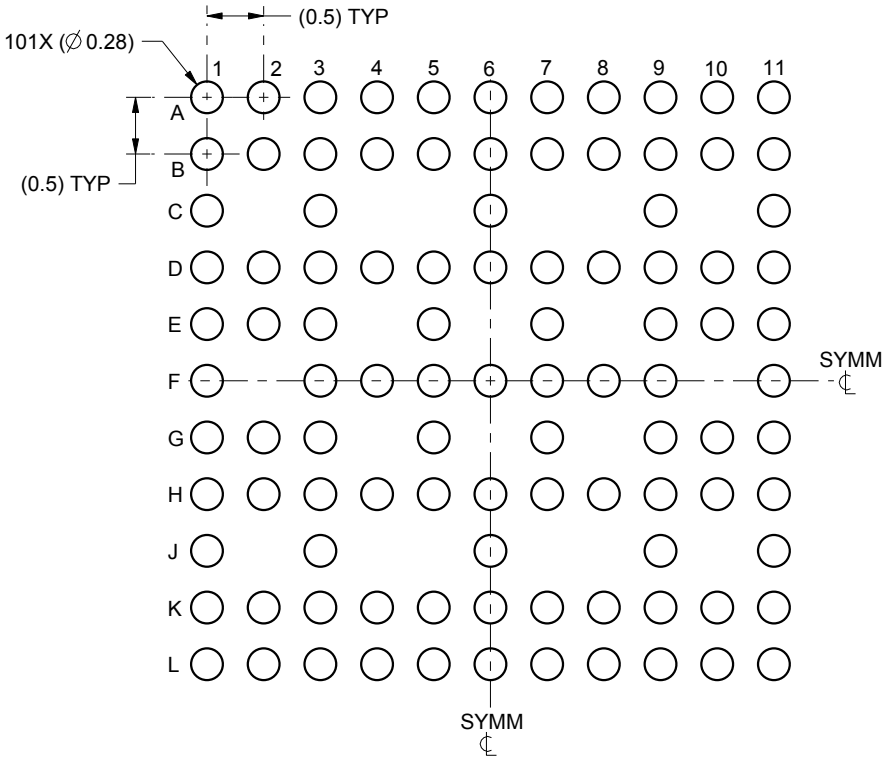
FCBGA - 1.03 mm max height

PLASTIC BALL GRID ARRAY

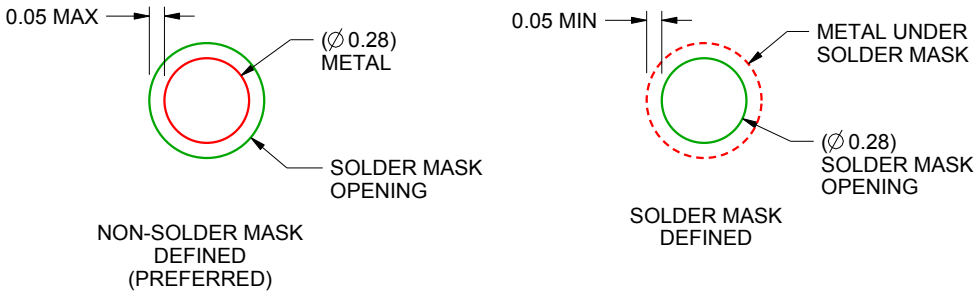


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.



LAND PATTERN EXAMPLE
SCALE:15X



SOLDER MASK DETAILS
NOT TO SCALE

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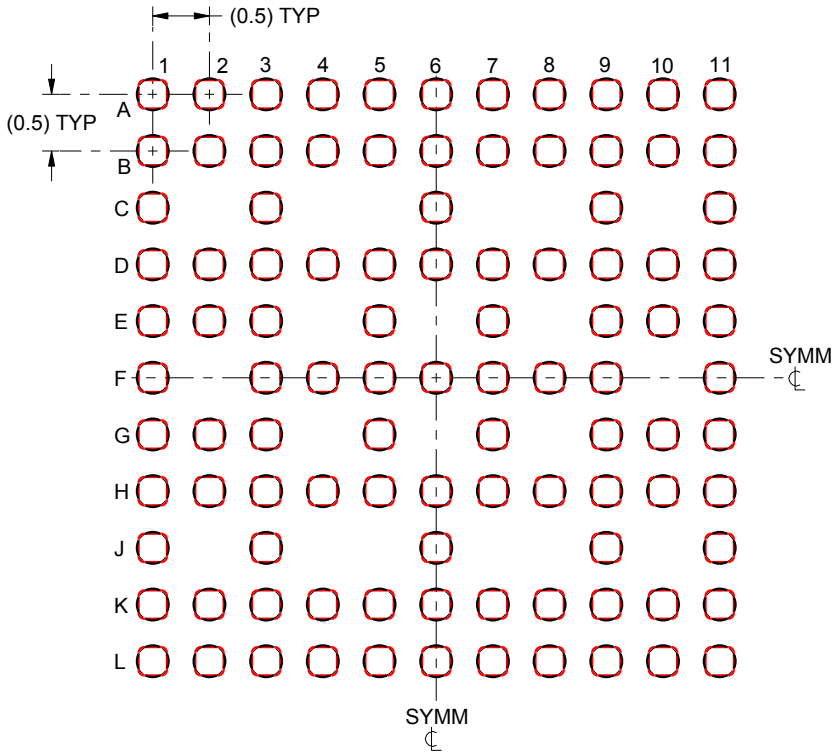
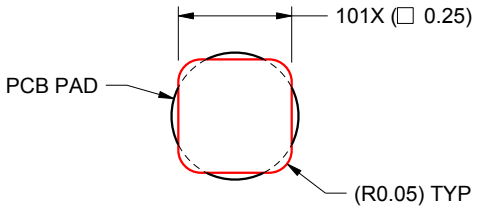
NOTES: (continued)

3. Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints.
   For information, see Texas Instruments literature number SPRAA99 (www.ti.com/lit/spraa99).



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL
SCALE:15X



STENCIL DETAIL
NTS

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NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.

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