TLC5957 48-Channel, 16-Bit ES-PWM LED Driver with Pre-Charge FET, LED OPEN Detection and Caterpillar Cancelling

1 Features

- 48 Constant-Current Sink Output Channels
- Sink Current Capability with Max BC/CC data
  - 1~20mA (VCC = 3.3V)
  - 1~25mA (VCC = 5V)
- Global Brightness Control (BC): 3-Bit (8 Step)
- Global Brightness Control (CC) for Each Color Group: 9-Bit (512 Step), Three Groups
- LED Power Supply Voltage up to 10V
- VCC = 3.0 to 5.5V
- Knee Voltage Vout = 0.24V at 10mA
- Constant Current Accuracy
  - Channel to Channel = ±1%(Typ), ±3%(Max)
  - Device to Device = ±1%(Typ), ±2%(Max)
- Data Transfer Rate : 33MHz
- Grayscale Control Clock : 33MHz
- Pre-charge FET for Ghost Cancelling
- Enhanced Circuit for Caterpillar Cancelling
- Selectable Data Transfer Bit and PWM Bit (9 bit to 16 bit)
- Selectable Traditional PWM and ES-PWM
- LED Open Detection (LOD)
- Thermal Shut Down (TSD)
- Auto Display Repeat/Auto Data Refresh
- Delay Switching to Prevent Inrush Current
- Operating Temperature : –40°C to +85°C

2 Applications

- LED Video Displays
- LED Signboards

3 Description

The TLC5957 is a 48-channel constant current sink driver. Each channel has an individually-adjustable, 65536-step, pulse width modulation (PWM) grayscale (GS) brightness control.

The output channels are divided into three groups, each group has a 512 step color brightness control (CC), CC adjusts brightness between colors. The maximum current value of all 48 channels can be set by 8-step global brightness control (BC). BC adjusts brightness deviation between LED drivers. GS, CC and BC data are accessible via a serial interface port.

TLC5957 has one error flag: LED open detection (LOD), which can be read via a serial interface port. Each constant-current has a pre-charge field- effect transistor (FET), which can remove ghosting and improve display performance on the multiplexing LED display. Besides, TLC5957 has an enhanced circuit, it can cancel the caterpillar effect caused by LED open.

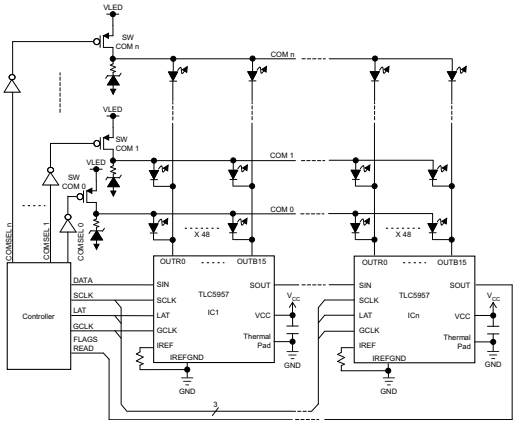
TLC5957 has a poker data transmission mode; GS data length can be configured from 9 bit to 16 bit according to PWM bits in each sub-segment. Poker Mode can significantly increase visual refresh rate in multiplexing applications.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
TLC5957	QFN (56)	8.0 mm × 8.0 mm

(1) For all available packages, see the orderable addendum at the end of the datasheet.

4 Typical Application Circuit (Multiple Daisy Chained TLC5957s)



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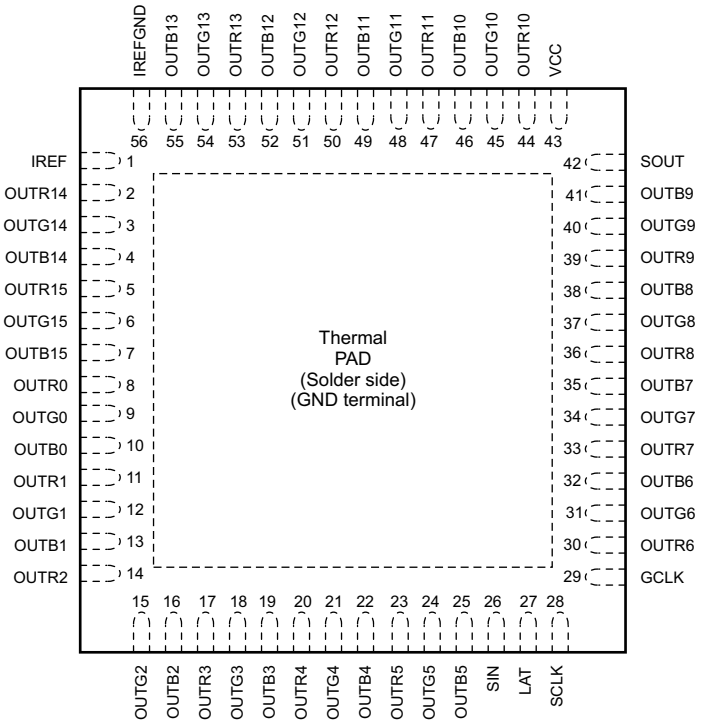
5 Revision History

DATE	REVISION	NOTES
October 2014	*	Initial release.

6 Pin Configuration and Functions

RTQ
56 PINS
Top View



Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
GCLK	29	I	Grayscale(GS) pulse width modulation (PWM) reference clock control for OUTXn.
			Each GCLK rising edge increase the GS counter by1 for PWM control.
GND	ThermalPad	—	Power ground. The thermal pad must be soldered to GND on PCB.
IREF	1	—	Maximum constant-current value setting. The OUTR0 to OUTB15 maximum constant output current are set to the desired values by connecting an external resistor between IREF and IREFGND. See Equation 1 for more detail. The external resistor should be placed close to the device.
IREFGND	56	—	Analog ground. Dedicated ground pin for the external IREF resistor. This pin should be connected to analog ground trace which is connected to power ground near the common GND point of board.
LAT	27	I	The LAT falling edge latches the data from the common shift register into the GS data latch or FC data latch.
OUTR0-R15	8, 11, 14, 17, 20, 23, 30, 33, 36, 39, 44, 47, 50, 53, 2, 5	O	Constant current output for RED LED. Multiple outputs can be tied together to increase the constant current capability. Different voltages can be applied to each output. These outputs are turned on-off by GCLK signal and the data in GS data memory.
OUTG0-G15	9, 12, 15, 18, 21, 24, 31, 34, 37, 40, 45, 48, 51, 54, 3, 6	O	Constant current output for GREEN LED. Multiple outputs can be tied together to increase the constant current capability. Different voltages can be applied to each output. These outputs are turned on-off by GCLK signal and the data in GS data memory.
OUTB0-B15	10, 13, 16, 19, 22, 25, 32, 35, 38, 41, 46, 49, 52, 55, 4, 7	O	Constant current output for BLUE LED. Multiple outputs can be tied together to increase the constant current capability. Different voltages can be applied to each output. These outputs are turned on-off by GCLK signal and the data in GS data memory.

Pin Functions (continued)

PIN		I/O	DESCRIPTION
NAME	NO.		
SCLK	28	I	Serial data shift clock. Data present on SIN are shifted to the 48-bit common shift register LSB with the SCLK rising edge. Data in the shift register are shifted towards the MSB at each SCLK rising edge. The common shift register MSB appears on SOUT.
SIN	26	I	Serial data input of the 48-bit common shift register. When SIN is high level, the LSB is set to '1' for only one SCLK input rising edge. If two SCLK rising edges are input while SIN is high, then the 48-bit shift register LSB and LSB+1 are set to '1'. When SIN is low, the LSB is set to '0' at the SCLK input rising edge.
SOUT	42	O	Serial data output of the 48-bit common shift register. SOUT is connected to the MSB of the register.
VCC	43	—	Power-supply voltage.

7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) (1)

			MIN	MAX	UNIT
V_{CC} (2)	Supply voltage	VCC	–0.3	6.0	V
I_{OUT}	Output current (dc)	OUTx0 to OUTx15, x = R, G, B	30	30	mA
V_{IN} (2)	Input voltage range	SIN, SCLK, LAT, GCLK, IREF	–0.3	V_{CC} + 0.3	V
V_{OUT} (2)	Output voltage range	SOUT	–0.3	V_{CC} + 0.3	V
		OUTx0 to OUTx15, x = R, G, B	–0.3	11	V
$T_{J(MAX)}$	Operation junction temperature		–40	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to device ground terminal.

7.2 Handling Ratings

			MIN	MAX	UNIT
T_{stg}	Storage temperature range		–55	150	°C
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins (1)	–3	3	kV
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins (2)	–1	1	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

At T_A = –40°C to 85°C, unless otherwise noted.

			MIN	NOM	MAX	UNIT
DC CHARACTERISTICS V_{CC} = 3 V to 5.5 V						
V_{CC}	Supply voltage		3		5.5	V
V_O	Voltage applied to output	OUTx0 to OUTx15, x = R, G, B			10	V
V_{IH}	High level input voltage	SIN, SCLK, LAT, GCLK	0.7×V_{CC}		V_{CC}	V
V_{IL}	Low level input voltage	SIN, SCLK, LAT, GCLK	GND		0.3×V_{CC}	V
I_{OH}	High level output current	SOUT			–2	mA
I_{OL}	Low level output current	SOUT			2	mA
I_{OLC}	Constant output sink current	OUTx0 to OUTx15, x = R, G, B, 3V ≤ V_{CC} ≤ 4V			20	mA
		OUTx0 to OUTx15, x = R, G, B, 4V < V_{CC} ≤ 5.5V			25	
T_A	Operating free air temperature		–40		85	°C
T_J	Operation junction temperature		–40		125	°C
AC CHARACTERISTICS, V_{CC} = 3 V to 5.5 V						
$F_{CLK(SCLK)}$	Data shift clock frequency	SCLK			33	MHz
$F_{CLK(GCLK)}$	Grayscale control clock frequency	GCLK			33	MHz

7.4 Thermal Information

THERMAL METRIC[1]		TLC5957 RTQ (56 PINS)	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	27.4	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	13.6	
$R_{\theta JB}$	Junction-to-board thermal resistance	5.5	
ψ_{JT}	Junction-to-top characterization parameter	0.2	
ψ_{JB}	Junction-to-board characterization parameter	5.5	
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	0.8	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

7.5 Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OH}	Output voltage	High	I_{OH} = –2mA at SOUT	V_{CC}-0.4		V_{CC}	V
V_{OL}		Low	I_{OL} = 2mA at SOUT			0.4	V
V_{LOD0}	LED open detection threshold		LODVTH = 00b	0.05	0.09	0.15	V
V_{LOD1}			LODVTH = 01b	0.15	0.19	0.25	V
V_{LOD2}			LODVTH = 10b	0.3	0.35	0.4	V
V_{LOD3}			LODVTH = 11b	0.45	0.49	0.55	V
V_{IREF}	Reference voltage output		R_{IREF} = 5.97kΩ (1mA target), BC = 0h, CCR/G/B = 80h	1.184	1.209	1.234	V
I_{IN}	Input current (SIN, SCLK, LAT, GCLK)		V_{IN} = V_{CC} or GND	–1		1	µA
I_{CC0}	Supply current (V_{CC})		SIN/SCLK/LAT/GSCLK = GND, GSn = 0000h, BC = 4h, CCR/G/B = 120h, VOUTn = 0.6V, RIREF = OPEN, V_{CC} = 4V		8	10	mA
I_{CC1}			SIN/SCLK/LAT/GSCK = GND, GSn = 0000h, BC = 4h, CCR/G/B = 120h, VOUTn = 0.6V, RIREF = 7.5kΩ (Io = 10mA target) , V_{CC} = 4V		11	13	
I_{CC2}			SIN/SCLK/LAT = GND, GCLK = 33MHz, T_{SU3} = 200ns, XREFRESH = 0, GSn = FFFFh, BC = 4h, CCR/G/B = 120h, VOUTn = 0.6V, RIREF = 7.5kΩ (Io = 10mA target) , V_{CC} = 4V		20	26	
I_{CC3}			SIN/SCLK/LAT = GND, GCLK = 33MHz, T_{SU3} = 200ns, XREFRESH = 0, GSn = FFFFh, BC = 7h, CCR/G/B = 1D2h, VOUTn = 0.6V, RIREF = 7.5kΩ (Io = 25mA target) , V_{CC} = 4V		22	28	
I_{CC4}			In power save mode		0.9	1.5	

Electrical Characteristics (continued)

over operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
ΔI_{OLC0}	Constant current error (OUTx0-15, x = R/G/B)	Channel-to-channel(1)	All OUTn = on, BC = 0h, CCR/G/B = 08Fh, VOUTn = VOUTfix = 0.6V, RIREF = 7.5kΩ(1mA target), T_A = +25C, at same color grouped output of OUTR0-15, OUTG0-15 and OUTB0-15		±1%	±3%	
ΔI_{OLC1}	Constant current error (OUTx0-15, x = R/G/B)	Device-to-device(2)	All OUTn = on, BC = 0h, CCR/G/B = 08Fh, VOUTn = VOUTfix = 0.6V, RIREF = 7.5kΩ(1mA target), T_A = +25C, at same color grouped output of OUTR0-15, OUTG0-15 and OUTB0-15		±1%	±2%	
ΔI_{OLC2}	Line regulation(3)		VCC = 3.0 to 5.5V, All OUTn = on, BC = 0h, CCR/G/B = 08Fh, VOUTn = VOUTfix = 0.6V, RIREF = 7.5kΩ (1mA target)		±1	±3	%/V
ΔI_{OLC3}	Load regulation(4)		VCC = 4V, All OUTn = on, BC = 0h, CCR/G/B = 08Fh, VOUTn = 0.6 to 3V, VOUTfix = 1V, RIREF = 7.5kΩ (1mA target)		±1	±3	%/V
ΔI_{OLC4}	Constant current error (OUTx0-15, x = R/G/B)	Channel-to-channel(1)	All OUTn = on, BC = 7h, CCR/G/B - 1CCh, VOUTn = VOUTfix = 0.6V, RIREF = 7.5kΩ(25mA target), T_A = +25C, at same color grouped output of OUTR0-15, OUTG0-15 and OUTB0-15		±1%	±3%	
ΔI_{OLC5}	Constant current error (OUTx0-15, x = R/G/B)	Device-to-device(2)	All OUTn = on, BC = 7h, CCR/G/B - 1CCh, VOUTn = VOUTfix = 0.6V, RIREF = 7.5kΩ(25mA target), T_A = +25C, at same color grouped output of OUTR0-15, OUTG0-15 and OUTB0-15		±1%	±3%	
ΔI_{OLC6}	Line regulation(3)		VCC = 3.0 to 5.5V, All OUTn = on, BC = 7h, CCR/G/B - 1CCh, VOUTn = VOUTfix = 0.6V, RIREF = 7.5kΩ (25mA target)		±1	±3	%/V
ΔI_{OLC7}	Load regulation(4)		All OUTn = on, BC = 7h, CCR/G/B - 1CCh, VOUTn = 0.6 to 3V, VOUTfix = 0.6V, RIREF = 7.5kΩ (25mA target)		±1	±3	%/V
T_{TSD}	Thermal shutdown threshold			160	170	180	°C
T_{HYS}	Thermal shutdown hysterisis				10		°C
$V_{ISP(in)}$	I_{REF} resistor short protection threshold				0.190		V
$V_{ISP(out)}$	I_{REF} resistor short-protection release threshold				0.330		V

(1) The deviation of each outputs in same color group (OUTR0~15 or OUTG0~15 or OUTB0~15) from the average of same color group constant current. The deviation is calculated by the formula. (X = R or G or B, n = 0~15

$$\Delta(\%) = \left(\frac{IOUTXn}{\frac{(IOUTX0 + IOUTX1 + ... + IOUTX14 + IOUTX15)}{16}} - 1 \right) \times 100$$

(2) The deviation of the average of constant-current in each color group from the ideal constant-current value. (X = R or G or B) :

$$\Delta(\%) = \left(\frac{\frac{(IOUTX0 + IOUTX1 + ... + IOUTX15)}{16} - (\text{Ideal Output Current})}{\text{Ideal Output Current}} \right) \times 100$$

Ideal current is calculated by the following equation:

$$\text{Ideal Output (mA)} = \text{Gain} \times \left(\frac{V_{IREF}}{R_{IREF}(\Omega)} \right) \times \text{CCR(or CCG, CCB) / 511d, VIREF = 1.209V(Typ), refer to Table 1 for the Gain at chosen BC.}$$

(3) Line regulation is calculated by the following equation. (X = R or G or B, n = 0~15):

$$\Delta(\% / V) = \left(\frac{(IOUTXn \text{ at } VCC = 5.5V) - (IOUTXn \text{ at } VCC = 3.0V)}{(IOUTXn \text{ at } VCC = 3.0V} \right) \times \frac{100}{5.5V - 3V}$$

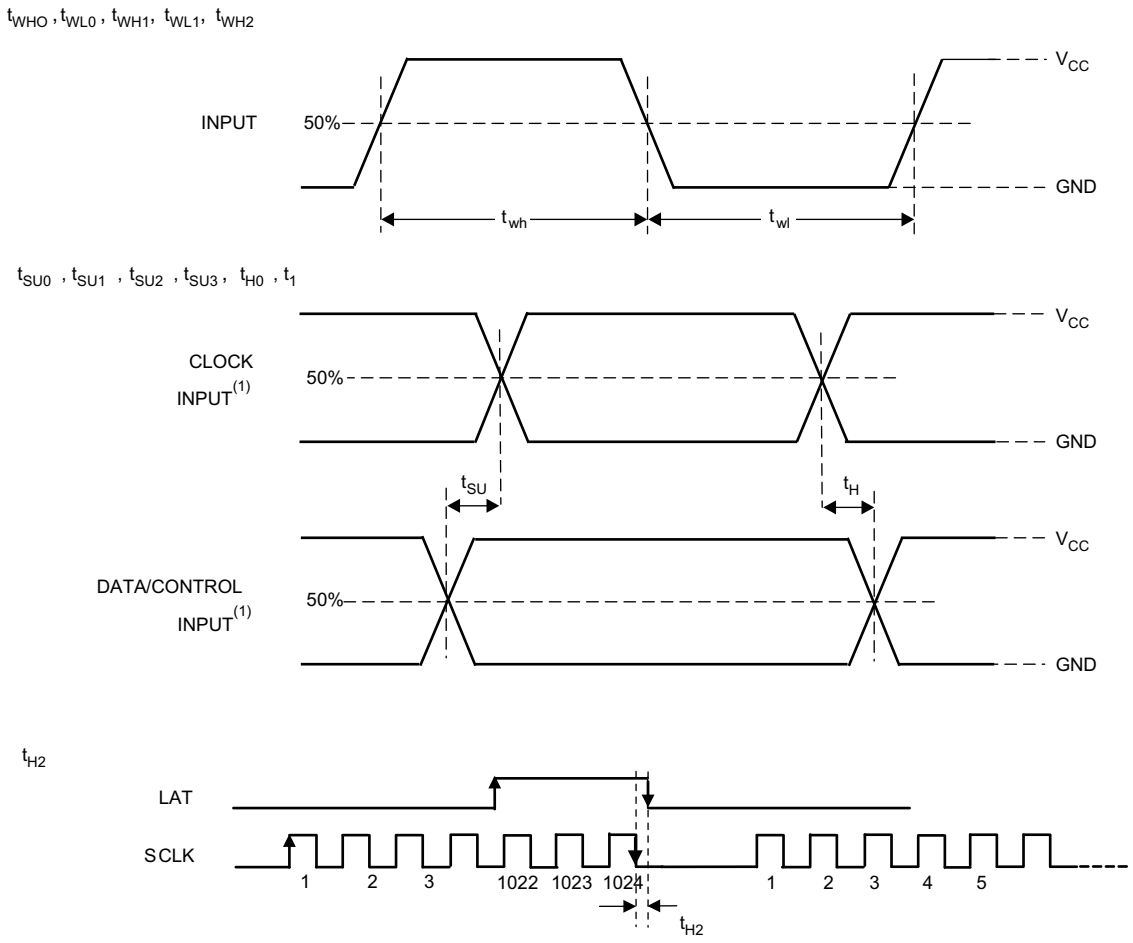
(4) Load regulation is calculated by the following equation. (X = R or G or B, n = 0~15):

$$\Delta(\% / V) = \left(\frac{(IOUTXn \text{ at } VOUTXn = 3V) - (IOUTXn \text{ at } VOUTXn = 1V)}{(IOUTXn \text{ at } VOUTXn = 1V} \right) \times \frac{100}{3V - 1V}$$

7.6 Timing Requirements

At T_A = –40°C to 85°C, unless otherwise noted.

			MIN	TYP	MAX	UNIT
AC CHARACTERISTICS, V_{CC} = 3 V to 5.5 V						
t_{WH0}	Pulse duration	SCLK	10			ns
t_{WL0}		SCLK	10			ns
t_{WH1}		GCLK	10			ns
t_{WL1}		GCLK	10			ns
t_{WH2}		LAT	10			ns
t_{SU0}	Setup time	SIN – SCLK↑	2			ns
t_{SU1}		LAT↑ – SCLK↑	3			ns
t_{SU2}		LAT↓ – SCLK↑ , for WRTGS, WRTFC, and TMGST Command	20			ns
		LAT↓ – SCLK↑ , for LATGS, READFC, and LINERESET Command	80			ns
t_{SU3}		LAT↓ – GCLK↑ , for LATGS AND LINERESET Command	30			ns
t_{H0}		SCLK↑ – SIN	2			ns
t_{H1}		SCLK↑ – LAT↑	2			ns
t_{H2}		SCLK↓ – LAT↓	2			ns



LAT Signal needs to include falling edge of SCLK

Figure 1. Input Timing

7.7 Typical Characteristics

At VCC= 4V and T_A = 25°C, unless otherwise noted.

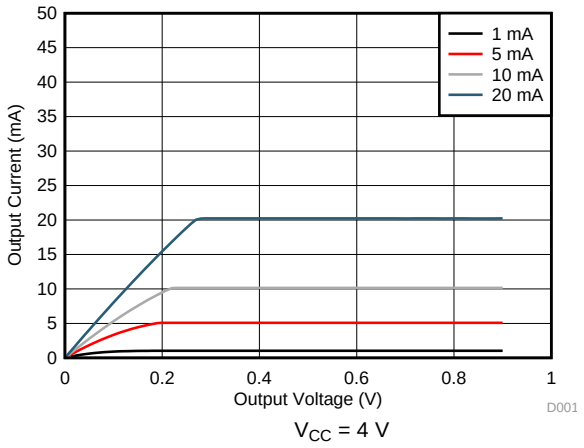


Figure 2. Output Current vs Output Voltage

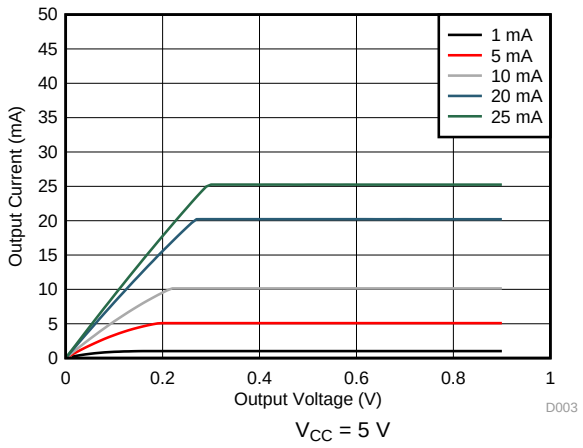


Figure 3. Output Current vs Output Voltage

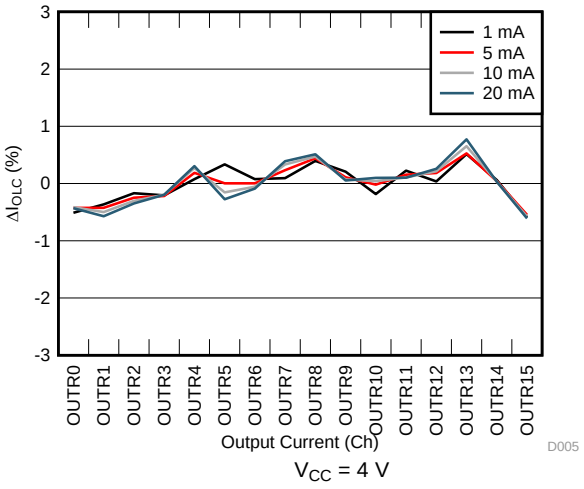


Figure 4. Constant-Current Error vs Output Current (Channel-to-Channel in RED color group)

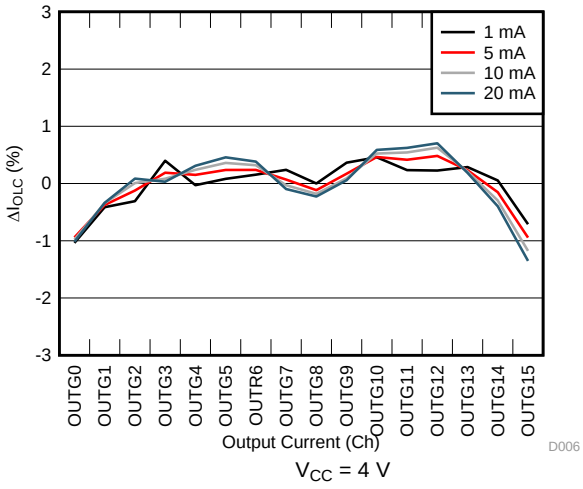


Figure 5. Constant-Current Error vs Output Current (Channel-to-Channel in GREEN color group)

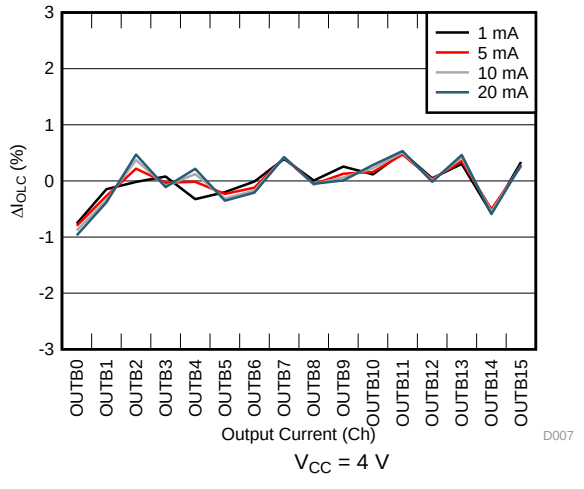


Figure 6. Constant-Current Error vs Output Current (Channel-to-Channel in BLUE color group)

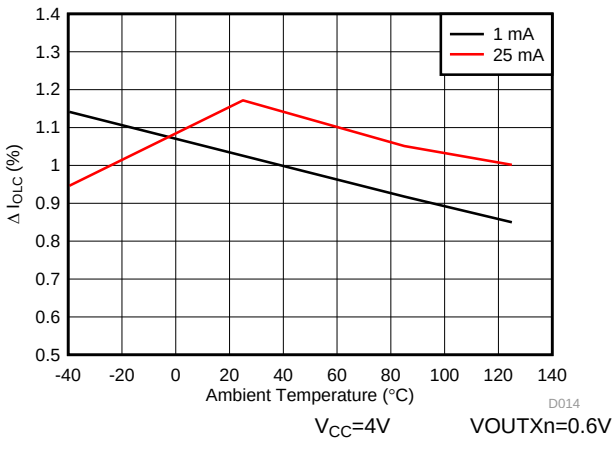
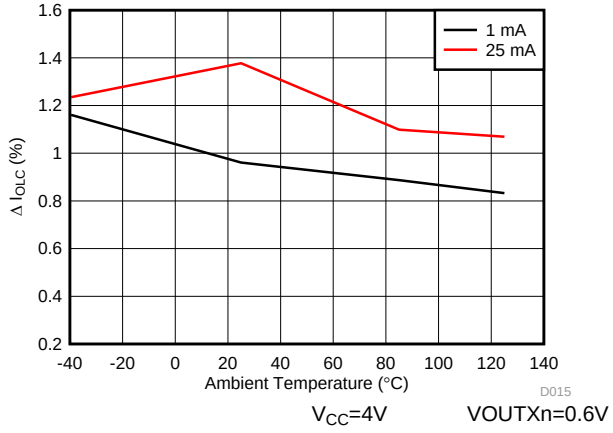


Figure 7. Maximum Constant-Current Error vs Ambient Temperature (Channel-to-Channel in RED color group)

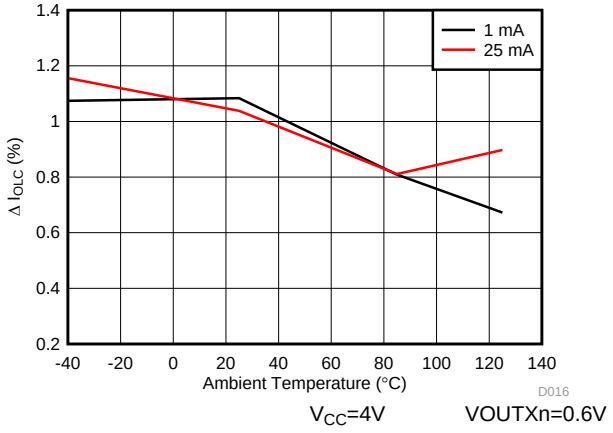
Typical Characteristics (continued)

At VCC= 4V and T_A = 25°C, unless otherwise noted.



V_{CC}=4V VOUTXn=0.6V

Figure 8. Maximum Constant-Current Error vs Ambient Temperature (Channel-to-Channel in GREEN color group)



V_{CC}=4V VOUTXn=0.6V

Figure 9. Maximum Constant-Current Error vs Ambient Temperature (Channel-to-Channel in BLUE color group)

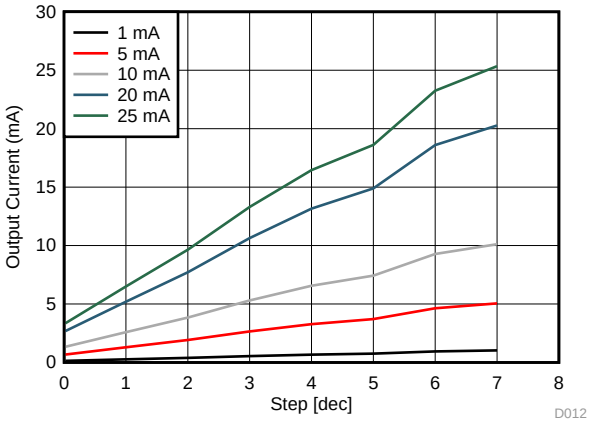
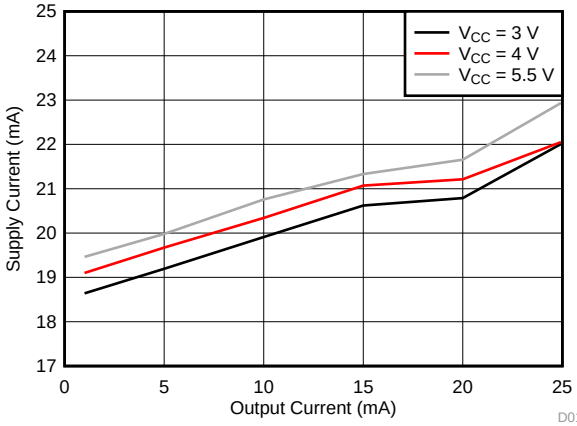
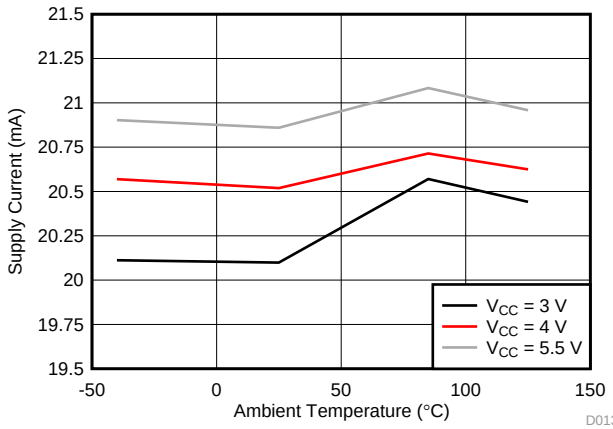


Figure 10. Global Brightness Control Linearity



VOUTXn=0.6V, GCLK=33MHz, GSXn=FFFFh,

Figure 11. Supply Current (I_{CC}) vs Output Current



GCLK=33MHz VOUTXn=0.6V, Output Current=10mA, GSXn=FFFFh,

Figure 12. Supply Current vs Ambient Temperature

8 Parameter Measurement Information

8.1 Pin Equivalent Input and Output Schematic Diagrams

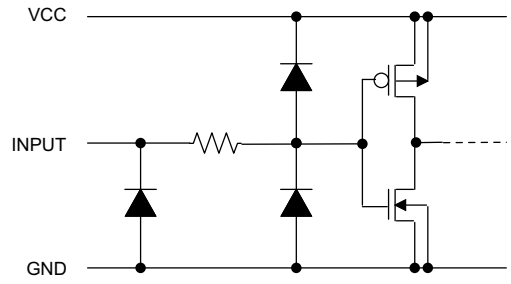


Figure 13. SIN, SCLK

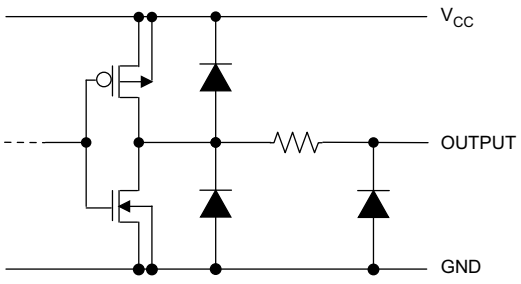


Figure 14. SOUT

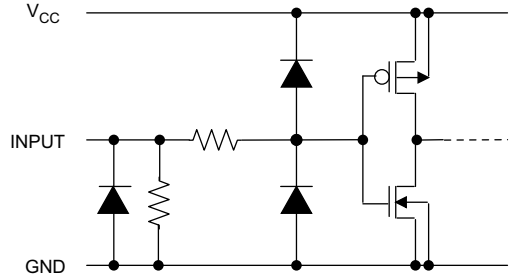


Figure 15. LAT, GCLK

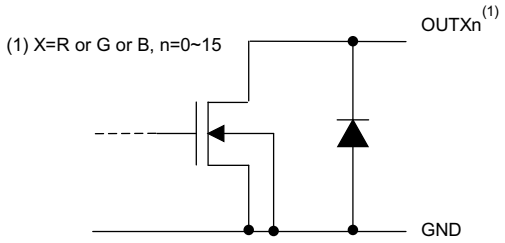


Figure 16. OUTR0/G0/B0 through OUTR15/G15/B15

8.2 Test Circuit

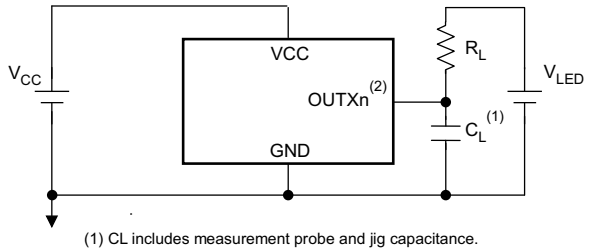


Figure 17. Rise Time and Fall Time Test Circuit for OUTXn

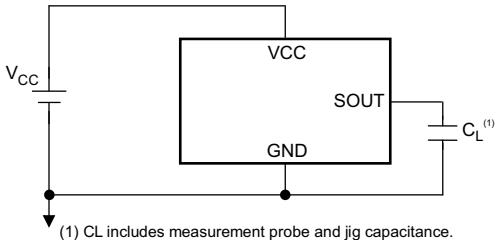


Figure 18. Rise Time and Fall Time Test Circuit for SOUT

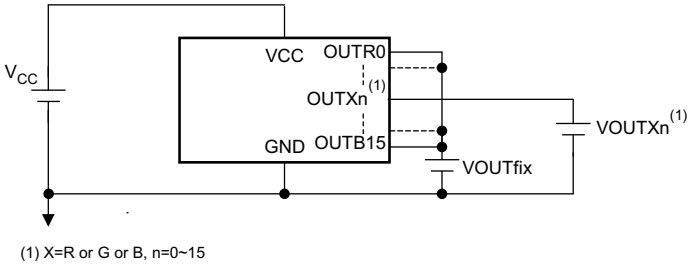


Figure 19. Constant Current Test Circuit for OUTXn

9 Detailed Description

9.1 Overview

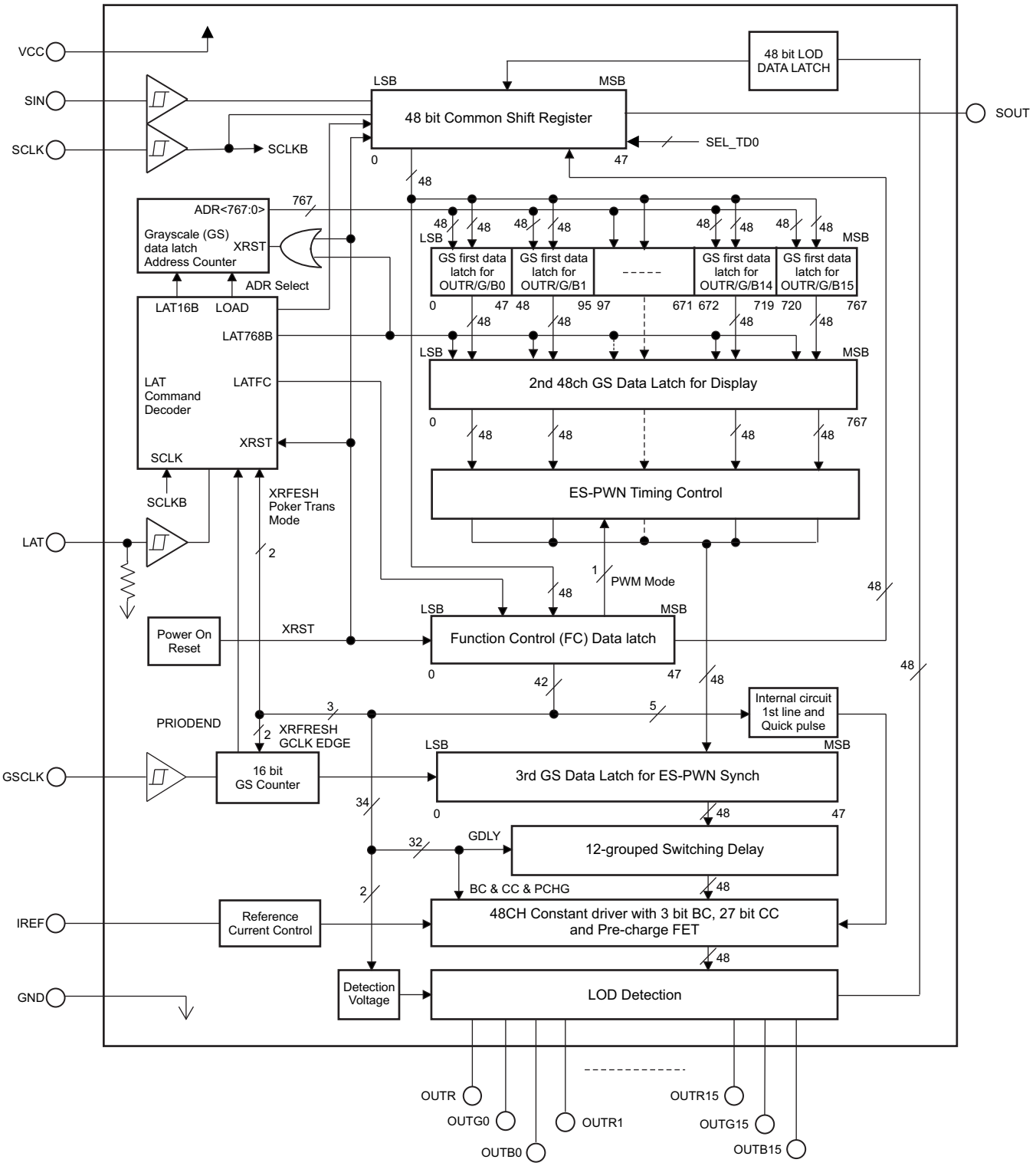
The TLC5957 is a 48-channel constant-current sink driver for multiplexing an LED display system. Each channel has an individually-adjustable, 65536-step, pulse width modulation (PWM) grayscale control.

The TLC5957 supports output current range from 1 mA to 25 mA. Channel-to-channel accuracy is 3% max, device-to-device accuracy is 2% max in all current ranges. Also, the TLC5957 implements Low Grayscale Enhancement (LGSE) technology to improve the display quality at low grayscale conditions. These features improve the performance of the TLC5957-multiplexed display system.

The output channels are grouped in three groups, each group has 16 channels for one color. Each group has a 512-step color brightness control (CC) function. The maximum current value of all 48 channels can be set by 8-step global brightness control (BC) function. GS, CC and BC data are accessible via a serial interface port.

The TLC5957 has one error flag: LED open detection (LOD), that can be read via a serial interface port. The TLC5957 also has an enhanced circuit to solve the caterpillar issue caused by open LEDs. Thermal shutdown (TSD) and Iref resistor short protection (ISP) assure TLC5957 of a higher system reliability.

9.2 Functional Block Diagram



9.3 Device Functional Modes

After power on, all OUTXn of TLC5957 are turned off. All the internal counters and function control registers are initialized. Below is a brief summary of the sequence to operate TLC5957, just give users a general idea how this part works. After that, the function block related to each step will be detailed in following sections.

1. According to required LED current, choose BC and CC code, select the current programming resistor R_{IREF}.
2. Send WRTFC command to set FC register value if the default value need be changed.
3. Write GS data of line 1 into GS data latch. Using LATGS command for the last group of 48bit GS data loading, the GS data written just now will be displayed.
4. Input GCLK continuously, 2^N GCLK (N>=9) as a segment. Between the interval of two segments, supply voltage should be switched from one line to next line accordingly.
5. During the same period of step4, GS data for next line should be written into GS data latch. Using LATGS command for the last group of 48bit GS data loading.
6. Repeat step 4-5 until it comes to the last line for a multiplexing panel. Input 2^N GCLK (N>=9) as a segment, at the same time, GS data for 1^{st} line should be written into GS data latch. Using LINERESET command for the last group of 48bit GS data loading.

Repeat step 4 through 6.

9.3.1 Brightness Control (BC) Function

The TLC5957 is able to adjust the output current of all constant-current outputs simultaneously. This function is called *global brightness control* (BC). The global BC for all outputs is programmed with a 3-bit word, thus all output currents can be adjusted in 8 steps from 12.9% to 100% (See Table 2) for a given current programming resistor(R_{IREF})

BC data can be set via the serial interface. When the BC data change, the output current also changes immediately. When the device is powered on, the BC data in the function control (FC) register is set to 4h as the initial value.

9.3.2 Color Control (CC) Function

The TLC5957 is able to adjust the output current of each of the three color groups OUTR0-OUTR15, OUTG0-OUTG15, and OUTB0-OUTB15 separately. This function is called *color brightness control* (CC). For each color, it has 9-bit data latch CCR, CCG, or CCB in FC register. Thus, all color group output currents can be adjusted in 512 steps from 0% to 100% of the maximum output current, I_{OLCMax}. (See next section for more details about I_{OLCMax}). The CC data are entered via the serial interface. When the CC data change, the output current also changes immediately.

When the IC is powered on, the CC data are set to ‘100h’.

Equation 1 calculates the actual output current.

$$Iout(mA) = I_{OLCMax}(mA) \times (CCR/511d \text{ or } CCB/511d) \quad (1)$$

Where:

I_{OLCMax} = the maximum channel current for each channel, determined by BC data and R_{IREF} (See Equation 2)
CCR/G/B = the color brightness control value for each color group in the FC1 register (000h to 1FFh)

Table 1 shows the CC data versus the constant-current against I_{OLCMax}.

Device Functional Modes (continued)

Table 1. CC Data vs Current Ratio and Set Current Value

CC DATA (CCR or CCG or CCB)			RATIO OF OUTPUT CURRENT TO I_{olcMax}(%, typical)	OUTPUT CURRENT (mA, R_{IREF} = 7.41 kΩ)	
BINARY	DECIMAL	HEX		BC = 7h (IolcMax =25mA)	BC = 0h (IolcMax=3.2mA)
0 0000 0000	0	00	0	0	0
0 0000 0001	1	01	0.2	0.05	0.006
0 0000 0010	2	02	0.4	0.10	0.013
—	—	—	—	—	—
1 0000 0000 (Default)	256 (Default)	100 (Default)	50.1	12.52	1.621
—	—	—	—	—	—
1 1111 1101	509	1FD	99.6	24.90	3.222
1 1111 1110	510	1FE	99.8	24.95	3.229
1 1111 1111	511	1FF	100.0	25	3.235

9.3.3 Select R_{IREF} For a Given BC

The maximum output current per channel, I_{OLCMax} is determined by resistor R_{IREF} placed between the IREF and IREFGND pins, and the BC code in FC register. The voltage on IREF is typically 1.209V. R_{IREF} can be calculated by Equation 2.

$$Riref(k\Omega) = Viref(V) / I_{OLCMax}(mA) \times Gain \quad (2)$$

Where:

V_{IREF} = the internal reference voltage on IREF (1.209V, typical)

I_{OLCMax} is the largest current for each output at CCR/G/B=1FFh.

Gain = the current gain at a selected BC code (See **Table 2**)

Table 2. Current Gain Versus BC Code

BC DATA		GAIN	RATIO OF GAIN / GAIN_MAX (AT MAX BC)
BINARY	HEX		
000 (recommend)	0 (recommend)	20.0	12.9%
001	1	39.5	25.6%
010	2	58.6	37.9%
011	3	80.9	52.4%
100 (default)	4 (default)	100.0	64.7%
101	5	113.3	73.3%
110	6	141.6	91.7%
111	7	154.5	100%
NOTE: Recommend to use smaller BC code for better performance. For noise immunity purposes, suggest R_{IREF} < 60 kΩ.			

9.3.4 Choosing BC/CC For a Different Application

BC is mainly used for global brightness adjustment between day and night. Suggested BC is 4h, which is in the middle of the range; thus, one can change brightness up and down flexibly.

CC can be used to fine tune the brightness in 512 steps, this is suitable for white balance adjustment between RGB color groups. To get a pure white color, the general requirement for the luminous intensity ratio of R, G, B LED is 3:6:1. Depending on LED's characteristics (Electro-Optical conversion efficiency), the current ratio of R, G, B LED will be much different from this ratio. Usually, the Red LED will need the largest current. One can choose 511d(the max value) CC code for the color group which needs the largest current at first, then choose proper CC code for the other two color groups according to the current ratio requirement of the LED used.

9.3.4.1 Example 1: Red LED Current is 20mA, Green LED Needs 12mA, Blue LED needs 8mA

1. Red LED needs the largest current, so choose 511d for CCR
2. 511 x 12mA / 20mA = 306.6, thus choose 307d for CCG. With same method, choose 204d for CCB.
3. According to the required red LED current, choose 7h for BC.
4. According to Equation 2, R_{IREF} = 1.2V/20mA x 154.5 = 9.27 kΩ

In this example, we choose 7h for BC, instead of using the default 4h. This is because the Red LED current is 20mA, approaching the upper limit of current range. To prevent the constant output current from exceeding the upper limit in case a larger BC code is input accidently, we choose the maximum BC code here.

9.3.4.2 Example 2: Red LED Current is 5mA, Green LED Needs 2mA, Blue LED Needs 1mA.

1. Red LED needs the largest current, so choose 511d for CCR.
2. 511 x 2mA / 5mA = 204.4, thus choose 204d for CCG. With same method, choose 102d for CCB.
3. According to the required blue LED current, choose 0h for BC.
4. According to Equation 2, R_{IREF} = 1.2V / 5mA x 20 = 4.8 kΩ

In this example, we choose 0h for BC, instead of using the default 4h. This is because the Blue LED current is 1mA, which is approaching the lower limit of current range. To prevent the constant output current from exceeding the lower limit in case a lower BC code is input accidently, we choose the min BC code here.

In general, if LED current is in the middle of range(i.e, 10mA), one can just use the default 4h as BC code.

9.3.5 LED Open Detection (LOD)

LOD function detects a fault caused by an open circuit in any LED string, or a short from OUTX*n* to ground with low impedance, by comparing the OUTXn voltage to the LOD detection threshold voltage level set by LODVLT in the FC register. If the OUTX*n* voltage is lower than the programmed voltage, the corresponding output LOD bit will be set to '1' to indicate a opened LED. Otherwise, the output of that LOD bit is '0'. LOD data output by the detect circuit are valid only during the ‘on’ period of that OUTXn output channel. LOD data are always ‘0’ for outputs that are turned off.

9.3.6 Poker Mode

Poker Mode provides the TLC5957 with a flexible PWM bit, from 9 bit to 16 bit. Therefore, data length can be reduced. In high multiplexing applications, Poker Mode can significantly increase visual refresh rate.

9.3.7 Internal Circuit for Caterpillar Removal

Caterpillar effect is a very common issue on LED panels. It is usually caused by an LED lamp open, LED lamp leakage or LED lamp short. The TLC5957 implements an internal circuit that can eliminate the caterpillar issue caused by LED open. This function can be enabled and disabled by LINERESET command. If the function is enabled, the IC automatically detects the broken LED lamp, and the lamp will not light until IC reset.

9.3.8 Internal Pre-charge FET for Ghost Removal

The internal pre-charge FET can prevent ghosting of multiplexed LED modules. One cause of this phenomenon is the charging current for parasitic capacitance of the OUTXn through the LED when the supply voltage switches from one common line to the next common line.

To prevent this unwanted charging current, the TLC5957 uses an internal FET to pull OUTXn up to VCC-1.4V during the common line switching period. Thus, no charging current flows through LED and the ghosting is eliminated.

9.3.9 Thermal Shutdown (TSD)

The thermal shutdown (TSD) function turns off all IC constant-current outputs when the junction temperature (T_J) exceeds 170°C (typ). It resumes normal operation when T_J falls below 160°C (typ).

9.3.10 IREF Resistor Short Protection (ISP)

The Iref resistor short protection (ISP) function prevents unwanted large currents from flowing though the constant-current output when the Iref resistor is shorted accidently. The TLC5957 turns off all output channels when the Iref pin voltage is lower than 0.19V (typ). When the Iref pin voltage goes higher than 0.33V (typ), the TLC5957 resumes normal operation.

9.3.11 Noise Reduction

Large surge currents may flow through the IC and the board on which the device is mounted if all 48 LED channels turn on simultaneously at the 1st GCLK rising edge. This large surge current could induce detrimental noise and electromagnetic interference (EMI) into other circuits.

The TLC5957 separate the LED channels into 12 groups. Each group turns on sequentially with some delay between one group and the next group. By this means, a soft-start feature is provided and the inrush current is minimized.

10 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

10.1 Application Information

Send request via email for Application Note: *Build High Density, High Refresh Rate, Multiplexing LED Panel with TLC5957*

11 Power Supply Recommendations

The V_{CC} power supply voltage should be decoupled by placing a 0.1 µF ceramic capacitor close to VCC pin and GND plane. Depending on panel size, several electrolytic capacitors must be placed on board equally distributed to get a well regulated LED supply voltage (VLED). VLED voltage ripple should be less than 5% of its nominal value. Furthermore, the VLED should be set to the voltage calculated by equation:

VLED > Vf + 0.4V (10mA constant current example) (3)

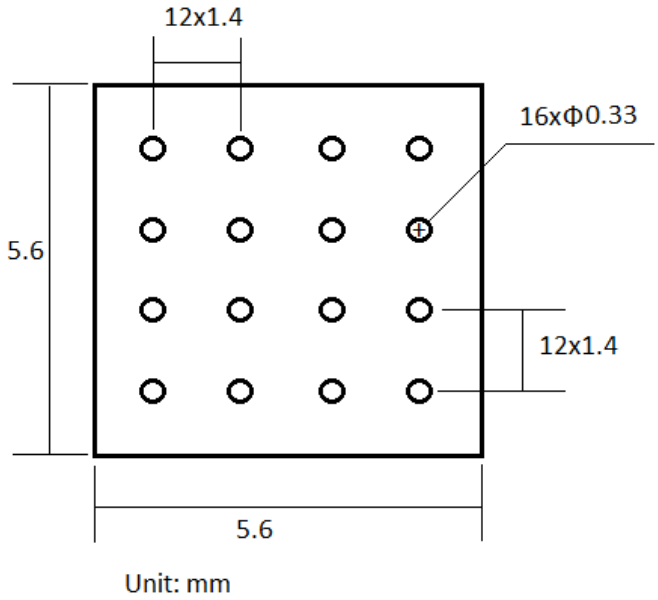
Where: Vf = maximum forward voltage of LED

12 Layout

12.1 Layout Guidelines

1. Place the decoupling capacitor near the VCC pin and GND plane.
2. Place the current programming resistor Riref close to IREF pin and IREFGND pin.
3. Route the GND pattern as widely as possible for large GND currents. Maximum GND current is approximately 1.2A
4. Routing between the LED cathode side and the device OUTXn pin should be as short and straight as possible to reduce wire inductance.
5. The PowerPAD™ must be connected to GND plane because the pad is used as power ground pin internally, there will be large current flow through this pad when all channels turn on. Furthermore, this pad should be connected to a heat sink layer by thermal via to reduce device temperature. One suggested thermal via pattern is shown as below. For more information about suggested thermal via pattern and via size, see " PowerPAD Thermally Enhanced Package", SLMA002G.

12.2 Layout Example



13 Device and Documentation Support

13.1 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

Table 3. Related Links

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
TLC5957	Click here	Click here	Click here	Click here	Click here

13.2 Trademarks

PowerPAD is a trademark of Texas Instruments.

13.3 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

13.4 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

14 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TLC5957RTQR	ACTIVE	QFN	RTQ	56	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 85	5957AB	Samples
TLC5957RTQT	ACTIVE	QFN	RTQ	56	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 85	5957AB	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

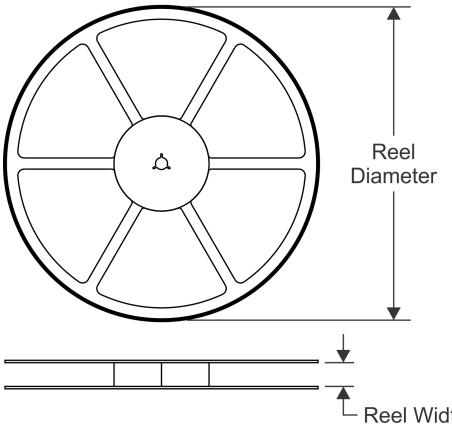
(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

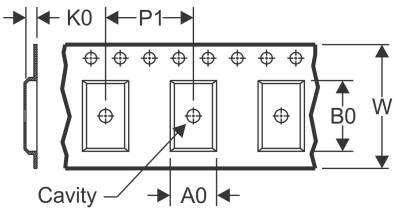
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

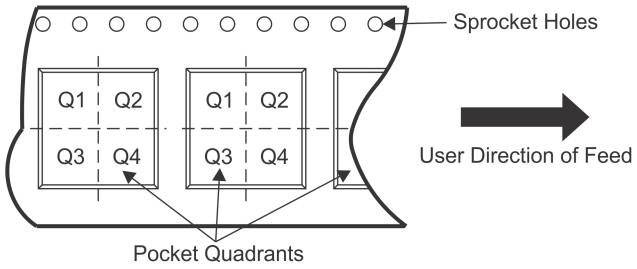


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

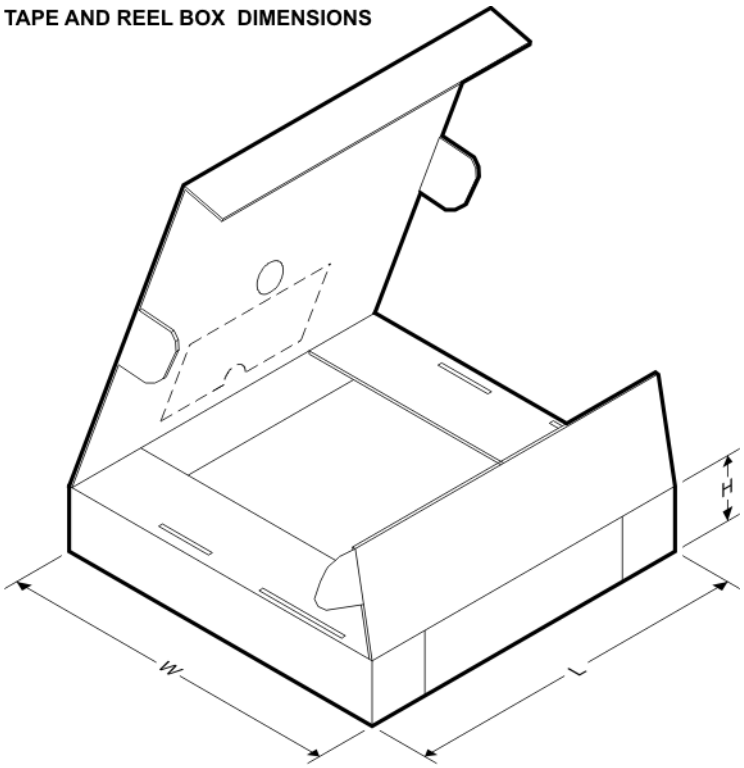
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TLC5957RTQR	QFN	RTQ	56	2000	330.0	16.4	8.3	8.3	1.1	12.0	16.0	Q2
TLC5957RTQT	QFN	RTQ	56	250	180.0	16.4	8.3	8.3	1.1	12.0	16.0	Q2

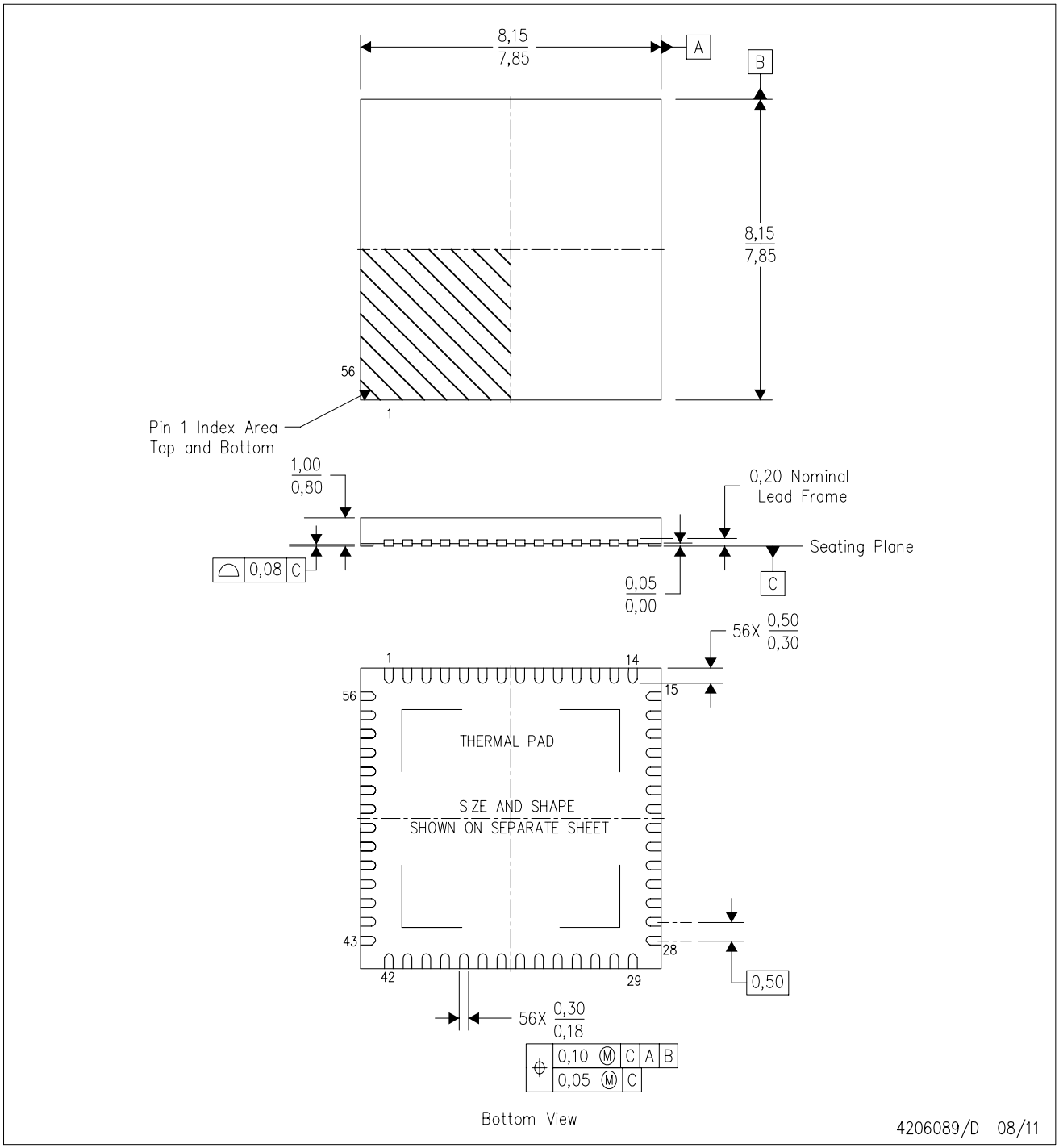
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TLC5957RTQR	QFN	RTQ	56	2000	367.0	367.0	38.0
TLC5957RTQT	QFN	RTQ	56	250	210.0	185.0	35.0

RTQ (S–PVQFN–N56) PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5–1994.
B. This drawing is subject to change without notice.
C. QFN (Quad Flatpack No–Lead) Package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
F. Package complies to JEDEC MO–220.

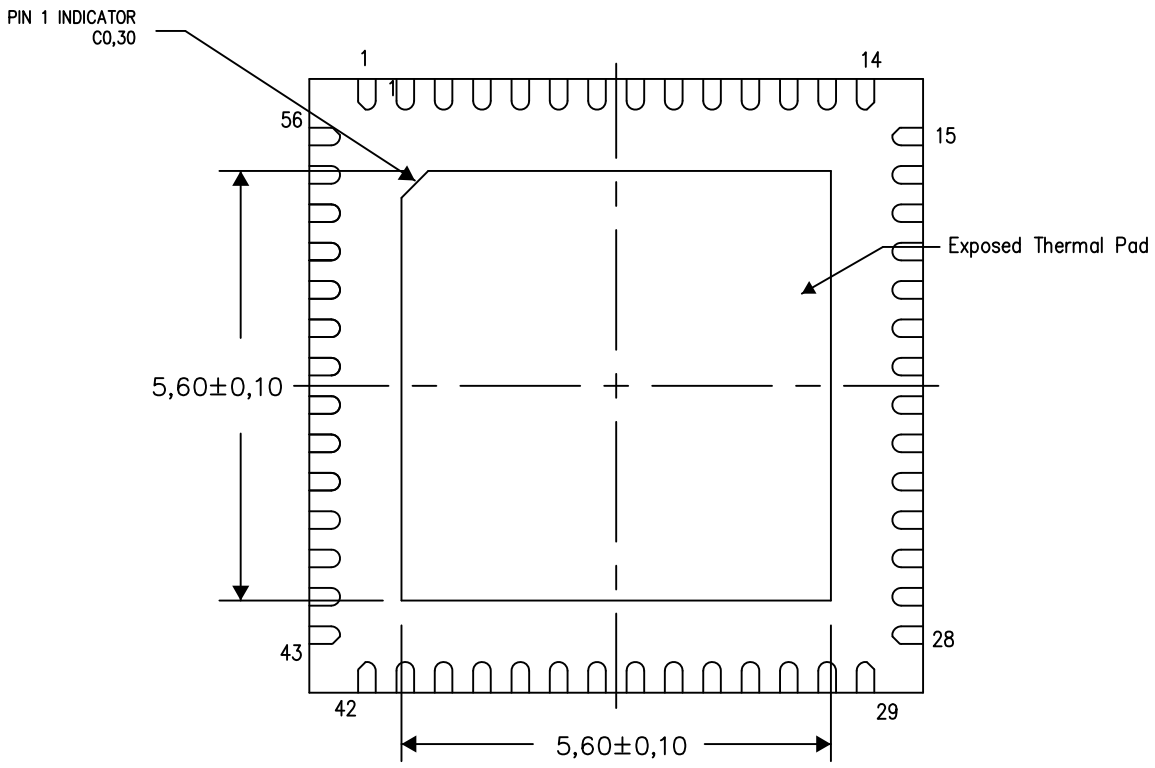
RTQ (S–PVQFN–N56) PLASTIC QUAD FLATPACK NO–LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



Bottom View

Exposed Thermal Pad Dimensions

4206252–8/Q 03/15

NOTE: All linear dimensions are in millimeters

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DLP® Products	www.dlp.com	Consumer Electronics	www.ti.com/consumer-apps
DSP	dsp.ti.com	Energy and Lighting	www.ti.com/energy
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