TS5A22362 0.65-Ω 2-channel SPDT Analog Switches With Negative Signaling Capability

1 Features

- Specified Break-Before-Make Switching
- Negative Signaling Capability: Maximum Swing from –2.75 V to 2.75 V (V_{CC} = 2.75 V)
- Low ON-State Resistance (0.65 Ω Typical)
- Low Charge Injection
- Excellent ON-State Resistance Matching
- 2.3-V to 5.5-V Power Supply (V_{CC})
- Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II
- ESD Performance Tested Per JESD 22
  - 2500-V Human-Body Model (A114-B, Class II)
  - 1500-V Charged-Device Model (C101)
  - 200-V Machine Model (A115-A)

2 Applications

- Cell Phones
- PDAs
- Portable Instrumentation
- Audio Routing
- Medical Imaging

3 Description

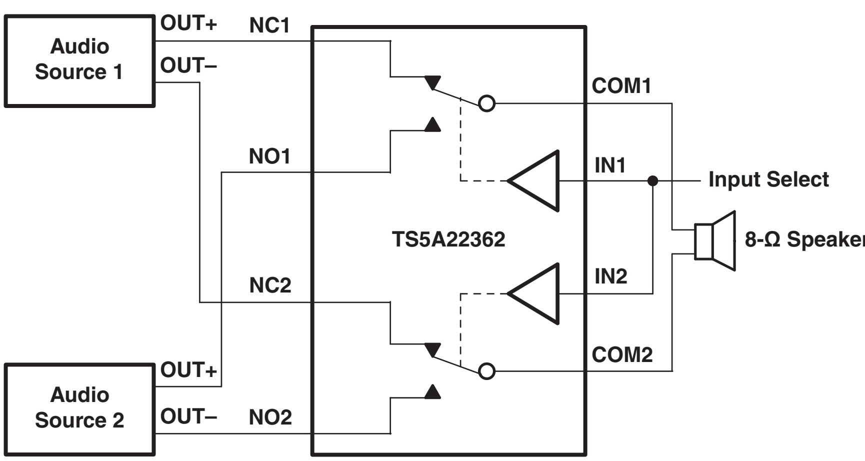
The TS5A22362 is a bidirectional, 2-channel single-pole double-throw (SPDT) analog switch designed to operate from 2.3 V to 5.5 V. The device features negative signal swing capability that allows signals below ground to pass through the switch without distortion. The break-before-make feature prevents signal distortion during the transferring of a signal from one path to another. Low ON-state resistance, excellent channel-to-channel ON-state resistance matching, and minimal total harmonic distortion (THD) performance are ideal for audio applications. The 3.00 mm × 3.00 mm DRC package is also available as a nonmagnetic package for medical imaging application.

Device Information[(1)]

PART NUMBER	PACKAGE	BODY SIZE (NOM)
TS5A22362	VSON (10)	3.00 mm × 3.00 mm
	DSBGA (10)	1.86 mm × 1.36 mm
	VSSOP (10)	3.00 mm × 3.00 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Typical Application Schematic



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4 Revision History

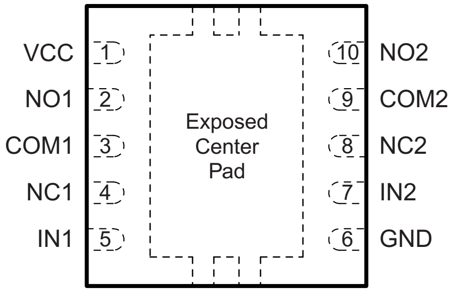
NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision A (August 2015) to Revision B	Page
• Changed C_L TEST CONDITION value for all THD PARAMETERs from 15 pf to 35 pf.	6

Changes from Original (June 2015) to Revision A	Page
• Changed the Functional Block Diagram.	15

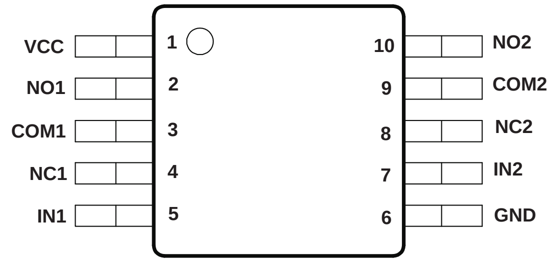
5 Pin Configuration and Functions

DRC Package
10-Pin VSON
Top View

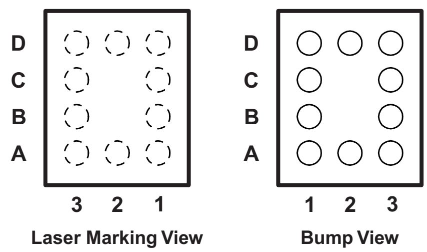


*The exposed center pad, if used, must be connected as a secondary GND or left electrically open.

DGS Package
10-Pin VSSOP
Top View



YZP Package
10-Pin DSBGA
Top View



Pin Functions

PIN				TYPE	DESCRIPTION
NAME	VSON	VSSOP	DSBGA		
VCC	1	1	A2	—	Power Supply
NO1	2	2	A3	I/O	Normally Open (NO) signal path, Switch 1
COM1	3	3	B3	I/O	Common signal path, Switch 1
NC1	4	4	C3	I/O	Normally Closed (NC) signal path, Switch 1
IN1	5	5	D3	I	Digital control pin , Switch 1
GND	6	6	D2	—	Ground
IN2	7	7	D1	I	Digital control pin, Switch 2
NC2	8	8	C1	I/O	Normally Closed (NC) signal path, Switch 2
COM2	9	9	B1	I/O	Common signal path, Switch 2
NO2	10	10	A1	I/O	Normally Open (NO) signal Path, Switch 2

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) (1)

			MIN	MAX	UNIT
V_{CC} (2)	Supply voltage (3)		–0.5	6	V
V_{NC} V_{NO} V_{COM}	Analog voltage (3) (4) (5)		V_{CC} – 6	V_{CC} + 0.5	V
$I_{I/OK}$	Analog port diode current	V_{NC}, V_{NO}, V_{COM} < 0 or V_{NC}, V_{NO}, V_{COM} > V_{CC}	–50	50	mA
I_{NC} I_{NO} I_{COM}	ON-state switch current	V_{NC}, V_{NO}, V_{COM} = 0 to V_{CC}	–150	150	mA
	ON-state peak switch current (6)		–300	300	
I_{NC} (3) (7) (8) I_{NO} (3) (7) (8) I_{COM} (3) (7) (8)	ON-state switch current	V_{NC}, V_{NO}, V_{COM} = 0 to V_{CC}	–350	350	mA
	ON-state peak switch current (6)		–500	500	
V_I	Digital input voltage		–0.5	6.5	V
I_{IK}	Digital input clamp current (3) (4)	V_I < 0	–50	50	mA
I_{CC} I_{GND}	Continuous current through V_{CC} or GND		–100	100	mA
T_{stg}	Storage temperature		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* . Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The algebraic convention, whereby the most negative value is a minimum and the most positive value is a maximum
(3) All voltages are with respect to ground, unless otherwise specified.
(4) The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
(5) This value is limited to 5.5 V maximum.
(6) Pulse at 1-ms duration < 10% duty cycle.
(7) V_{CC} = 3.0 V to 5.0 V, T_A = –40°C to 85°C.
(8) For YZP package only.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 (1)	±2500	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101 (2)	±1500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
V_{CC}	Supply voltage	2.3	5.5	V
V_{NC} V_{NO} V_{COM}	Signal path voltage	V_{CC} – 5.5	V_{CC}	V
V_{IN}	Digital control	GND	V_{CC}	V

6.4 Thermal Information

THERMAL METRIC (1)		TS5A22362 DGS (VSSOP) 10 PINS	TS5A22362 DRC (VSON) 10 PINS	TS5A22362 YZP (DSBGA) 10 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	163.3	44.3	90.9	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	56.4	70.1	0.3	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	83.1	19.3	8.3	°C/W
ψ_{JT}	Junction-to-top characterization parameter	6.8	2.0	3.2	°C/W
ψ_{JB}	Junction-to-board characterization parameter	81.8	19.4	8.3	°C/W

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

6.5 Electrical Characteristics for 2.5-V Supply

V_{CC} = 2.3 V to 2.7 V, T_A = –40°C to 85°C (unless otherwise noted) (1)

PARAMETER		TEST CONDITIONS		T_A	V_{CC}	MIN	TYP	MAX	UNIT
Analog Switch									
V_{COM}, V_{NO}, V_{NC}	Analog signal range					V_{CC} – 5.5		V_{CC}	V
R_{on}	ON-state resistance	V_{NC} or V_{NO} = V_{CC}, 1.5 V, V_{CC} – 5.5 V I_{COM} = –100 mA,	COM to NO or NC, see Figure 13	25°C	2.7 V		0.65	0.94	Ω
				Full				1.3	
ΔR_{on}	ON-state resistance match between channels	V_{NC} or V_{NO} = 1.5 V, I_{COM} = –100 mA,	COM to NO or NC, see Figure 13	25°C	2.7 V		0.023	0.11	Ω
				Full				0.15	
$R_{on(flat)}$	ON-state resistance flatness	V_{NC} or V_{NO} = V_{CC}, 1.5 V, V_{CC} – 5.5 V I_{COM} = –100 mA,	COM to NO or NC, see Figure 13	25°C	2.7 V		0.18	0.46	Ω
				Full				0.5	
$I_{NC(OFF)}$, $I_{NO(OFF)}$	NC, NO OFF leakage current	V_{NC} = 2.25 V, V_{CC} – 5.5 V V_{COM} = V_{CC} – 5.5 V, 2.25 V V_{NO} = Open COM to NO or V_{NO} = 2.25 V, V_{CC} – 5.5 V, V_{COM} = V_{CC} – 5.5 V, 2.25 V V_{NC} = Open COM to NC	See Figure 14	25°C	2.7	–50		50	nA
				Full		–375		375	
$I_{COM(ON)}$	COM ON leakage current	V_{NC} and V_{NO} = Floating, V_{COM} = V_{CC},V_{CC} – 5.5 V	See Figure 15	25°C	2.7 V	–50		50	nA
				Full		–375		375	
Digital Control Inputs (IN) (2)									
V_{IH}	Input logic high			Full		1.4		5.5	V
V_{IL}	Input logic low							0.6	
I_{IH}, I_{IL}	Input leakage current	V_{IN} = V_{CC} or 0		25°C	2.7 V	–250		250	nA
				Full		–250		250	
Dynamic									
t_{ON}	Turnon time	V_{COM} = V_{CC}, R_L = 300 Ω,	C_L = 35 pF, see Figure 17	25°C	2.5 V		44	80	ns
				Full	2.3 V to 2.7 V			120	
t_{OFF}	Turnoff time	V_{COM} = V_{CC}, R_L = 300 Ω,	C_L = 35 pF, see Figure 17	25°C	2.5 V		22	70	ns
				Full	2.3 V to 2.7 V			70	
t_{BBM}	Break-before-make time	See Figure 18		25°C	2.5 V	1	7		ns
Q_C	Charge injection	V_{GEN} = 0, R_{GEN} = 0,	C_L = 1 nF, see Figure 22	25°C	2.5 V		150		pC
$C_{NC(OFF)}$, $C_{NO(OFF)}$	NC, NO OFF capacitance	V_{NC} or V_{NO} = V_{CC} or GND,	See Figure 16	25°C	2.5 V		70		pF
$C_{COM(ON)}$	NC, NO, COM ON capacitance	V_{COM} = V_{CC} or GND, Switch ON, f = 10 MHz	See Figure 16	25°C	2.5 V		370		pF

(1) The algebraic convention, whereby the most negative value is a minimum and the most positive value is a maximum
(2) All unused digital inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, SCBA004.

Electrical Characteristics for 2.5-V Supply (continued)

V_{CC} = 2.3 V to 2.7 V, T_A = –40°C to 85°C (unless otherwise noted) (1)

PARAMETER		TEST CONDITIONS		T_A	V_{CC}	MIN	TYP	MAX	UNIT
C_I	Digital input capacitance	V_I = V_{CC} or GND	See Figure 16	25°C	2.5 V		2.6		pF
BW	Bandwidth	R_L = 50 Ω, –3 dB	See Figure 18	25°C	2.5 V		17		MHz
O_{ISO}	OFF isolation	R_L = 50 Ω	f = 100 kHz, see Figure 20	25°C	2.5 V		–66		dB
X_{TALK}	Crosstalk	R_L = 50 Ω	f = 100 kHz, see Figure 21	25°C	2.5 V		–75		dB
THD	Total harmonic distortion	R_L = 600 Ω, C_L = 35 pF	f = 20 Hz to 20 kHz, see Figure 23	25°C	2.5 V		0.01%		
Supply									
I_{CC}	Positive supply current	V_{COM} and V_{IN} = V_{CC} or GND, V_{NC} and V_{NO} = Floating		25°C	2.7 V		0.2	1.1	µA
				Full				1.3	
I_{CC}	Positive supply current	V_{COM} = V_{CC} – 5.5 V, V_{IN} = V_{CC} or GND, V_{NC} and V_{NO} = Floating		Full	2.7 V			3.3	µA

6.6 Electrical Characteristics for 3.3-V Supply

V_{CC} = 3 V to 3.6 V, T_A = –40°C to 85°C (unless otherwise noted) (1)

PARAMETER		TEST CONDITIONS		T_A	V_{CC}	MIN	TYP	MAX	UNIT
ANALOG SWITCH									
V_{COM}, V_{NO}, V_{NC}	Analog signal range					V_{CC} – 5.5		V_{CC}	V
R_{on}	ON-state resistance	V_{NC} or V_{NO} ≤ V_{CC}, 1.5 V, V_{CC} – 5.5 V, I_{COM} = –100 mA	COM to NO or NC, see Figure 13	25°C	3 V		0.61	0.87	Ω
				Full				0.97	
ΔR_{on}	ON-state resistance match between channels	V_{NC} or V_{NO} = 1.5 V, I_{COM} = –100 mA,	COM to NO or NC, see Figure 13	25°C	3 V		0.024	0.13	Ω
				Full				0.13	
$R_{on(flat)}$	ON-state resistance flatness	V_{NC} or V_{NO} ≤ V_{CC}, 1.5 V, V_{CC} – 5.5 V, I_{COM} = –100 mA	COM to NO or NC, see Figure 13	25°C	3 V		0.12	0.46	Ω
				Full				0.5	
$I_{NC(OFF)}$, $I_{NO(OFF)}$	NC, NO OFF leakage current	V_{NC} = 3 V, V_{CC} – 5.5 V V_{COM} = V_{CC} – 5.5 V, 3 V V_{NO} = Open COM to NO or V_{NO} = 3 V, V_{CC} – 5.5 V, V_{COM} = V_{CC} – 5.5 V, 3 V V_{NC} = Open COM to NC	See Figure 14	25°C	3.6 V	–50		50	nA
				Full		–375		375	
$I_{COM(ON)}$	COM ON leakage current	V_{NC} and V_{NO} = Floating, V_{COM} = V_{CC},V_{CC} – 5.5 V	COM to NO or NC, see Figure 15	25°C	3.6 V	–50		50	nA
				Full		–375		375	
DIGITAL CONTROL INPUTS (IN) (2)									
V_{IH}	Input logic high			Full		1.4		5.5	V
V_{IL}	Input logic low							0.8	
I_{IH}, I_{IL}	Input leakage current	V_{IN} = V_{CC} or 0		25°C	3.6 V	–250		250	nA
				Full		–250		250	
DYNAMIC									
t_{ON}	Turnon time	V_{COM} = V_{CC}, R_L = 300 Ω	C_L = 35 pF, see Figure 17	25°C	3.3 V		34	80	ns
				Full	3 V to 3.6 V			120	

(1) The algebraic convention, whereby the most negative value is a minimum and the most positive value is a maximum
(2) All unused digital inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

Electrical Characteristics for 3.3-V Supply (continued)

V_{CC} = 3 V to 3.6 V, T_A = –40°C to 85°C (unless otherwise noted) (1)

PARAMETER		TEST CONDITIONS		T_A	V_{CC}	MIN	TYP	MAX	UNIT
t_{OFF}	Turnoff time	$V_{COM} = V_{CC}$, R_L = 300 Ω	C_L = 35 pF, see Figure 17	25°C	3.3 V		19	70	ns
				Full	3 V to 3.6 V			70	
t_{BBM}	Break-before-make time	See Figure 18		25°C	3.3 V	1	7		ns
Q_C	Charge injection	V_{GEN} = 0, R_{GEN} = 0	C_L = 1 nF, see Figure 22	25°C	3.3 V		150		pC
$C_{NC(OFF)}$, $C_{NO(OFF)}$	NC, NO OFF capacitance	V_{NC} or V_{NO} = V_{CC} or V_{CC} – 5.5 V	See Figure 16	25°C	3.3 V		70		pF
$C_{COM(ON)}$	NC, NO, COM ON capacitance	V_{COM} = V_{CC} or GND, f = 10 MHz	See Figure 16	25°C	3.3 V		370		pF
C_I	Digital input capacitance	V_I = V_{CC} or GND	See Figure 16	25°C	3.3 V		2.6		pF
BW	Bandwidth	R_L = 50 Ω, –3 dB	Switch ON, see Figure 18	25°C	3.3 V		17.5		MHz
O_{ISO}	OFF isolation	R_L = 50 Ω	f = 100 kHz, see Figure 20	25°C	3.3 V		–68		dB
X_{TALK}	Crosstalk	R_L = 50 Ω	f = 100 kHz, see Figure 21	25°C	3.3 V		–76		dB
THD	Total harmonic distortion	R_L = 600 Ω, C_L = 35 pF	f = 20 Hz to 20 kHz, see Figure 23	25°C	3.3 V		0.008%		
SUPPLY									
I_{CC}	Positive supply current	V_{COM} and V_{IN} = V_{CC} or GND, V_{NC} and V_{NO} = Floating		25°C	3.6 V		0.1	1.2	µA
				Full				1.3	
		V_{COM} = V_{CC} – 5.5 V, V_{IN} = V_{CC} or GND, V_{NC} and V_{NO} = Floating		Full	3.6 V			3.4	µA

6.7 Electrical Characteristics for 5-V Supply

V_{CC} = 4.5 V to 5.5 V, T_A = –40°C to 85°C (unless otherwise noted) (1)

PARAMETER		TEST CONDITIONS		T_A	V_{CC}	MIN	TYP	MAX	UNIT
ANALOG SWITCH									
V_{COM}, V_{NO}, V_{NC}	Analog signal range					V_{CC} – 5.5		V_{CC}	V
R_{on}	ON-state resistance	V_{NC} or V_{NO} = V_{CC}, 1.6 V, V_{CC} = –5.5 V, I_{COM} = –100 mA	COM to NO or NC, see Figure 13	25°C	4.5 V		0.52	0.74	Ω
				Full				0.83	
ΔR_{on}	ON-state resistance match between channels	V_{NC} or V_{NO} = 1.6 V, I_{COM} = –100 mA	COM to NO or NC, see Figure 13	25°C	4.5 V		0.04	0.23	Ω
				Full				0.30	
$R_{on(flat)}$	ON-state resistance flatness	V_{NC} or V_{NO} = V_{CC}, 1.6 V, V_{CC} = –5.5 V, I_{COM} = –100 mA	COM to NO or NC, see Figure 13	25°C	4.5 V		0.076	0.46	Ω
				Full				0.5	
$I_{NC(OFF)}$, $I_{NO(OFF)}$	NC, NO OFF leakage current	V_{NC} = 4.5 V, V_{CC} – 5.5 V, V_{COM} = V_{CC} – 5.5 V, 4.5 V, V_{NO} = Open, COM to NO or V_{NO} = 4.5 V, V_{CC} – 5.5 V, V_{COM} = V_{CC} – 5.5 V, 4.5 V, V_{NC} = Open, COM to NC	See Figure 14	25°C	5.5 V	–50		50	nA
				Full		–375		375	
$I_{COM(ON)}$	COM ON leakage current	V_{NC} and V_{NO} = Floating, V_{COM} = V_{CC}, V_{CC} – 5.5 V	See Figure 15	25°C	5.5 V	–50		50	nA
				Full		–375		375	
DIGITAL CONTROL INPUTS (IN) (2)									

(1) The algebraic convention, whereby the most negative value is a minimum and the most positive value is a maximum
(2) All unused digital inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, SCBA004.

Electrical Characteristics for 5-V Supply (continued)

V_{CC} = 4.5 V to 5.5 V, T_A = –40°C to 85°C (unless otherwise noted) (1)

PARAMETER		TEST CONDITIONS		T_A	V_{CC}	MIN	TYP	MAX	UNIT
V_{IH}	Input logic high			Full		2.4		5.5	V
V_{IL}	Input logic low			Full				0.8	V
I_{IH}, I_{IL}	Input leakage current	V_{IN} = V_{CC} or 0		25°C	5.5 V	–250		250	nA
				Full		–250		250	
DYNAMIC									
t_{ON}	Turnon time	V_{COM} = V_{CC}, R_L = 300 Ω	C_L = 35 pF, see Figure 17	25°C	5 V		27	80	ns
				Full	4.5 V to 5.5 V			80	
t_{OFF}	Turnoff time	V_{COM} = V_{CC}, R_L = 300 Ω	C_L = 35 pF, see Figure 17	25°C	5 V		13	70	ns
				Full	4.5 V to 5.5 V			70	
t_{BBM}	Break-before-make time	V_{NC} = V_{NO} = V_{CC}/2 R_L = 300 Ω	C_L = 35 pF, see Figure 18	25°C	5 V	1	3.5		ns
Q_C	Charge injection	V_{GEN} = 0, R_{GEN} = 0	C_L = 1 nF, see Figure 22	25°C	5 V		10		pC
$C_{NC(OFF)}$, $C_{NO(OFF)}$	NC, NO OFF capacitance	V_{NC} or V_{NO} = V_{CC} or V_{CC} – 5.5 V	See Figure 16	25°C	5 V		70		pF
$C_{COM(ON)}$	NC, NO, COM ON capacitance	V_{COM} = V_{CC} or GND,	See Figure 16	25°C	5 V		370		pF
C_I	Digital input capacitance	V_I = V_{CC} or GND	See Figure 16	25°C	5 V		2.6		pF
BW	Bandwidth	R_L = 50 Ω	See Figure 18	25°C	5 V		18.3		MHz
O_{ISO}	OFF isolation	R_L = 50 Ω	f = 100 kHz, see Figure 20	25°C	5 V		–70		dB
X_{TALK}	Crosstalk	R_L = 50 Ω	f = 100 kHz, see Figure 21	25°C	5 V		–78		dB
THD	Total harmonic distortion	R_L = 600 Ω, C_L = 35 pF	f = 20 Hz to 20 kHz, see Figure 23	25°C	5 V		0.009%		
SUPPLY									
I_{CC}	Positive supply current	V_{COM} and V_{IN} = V_{CC} or GND, V_{NC} and V_{NO} = Floating		25°C	5.5 V		0.2	1.3	µA
				Full				3.5	
		V_{COM} = V_{CC} – 5.5 V, V_{IN} = V_{CC} or GND, V_{NC} and V_{NO} = Floating		Full				5	

6.8 Typical Characteristics

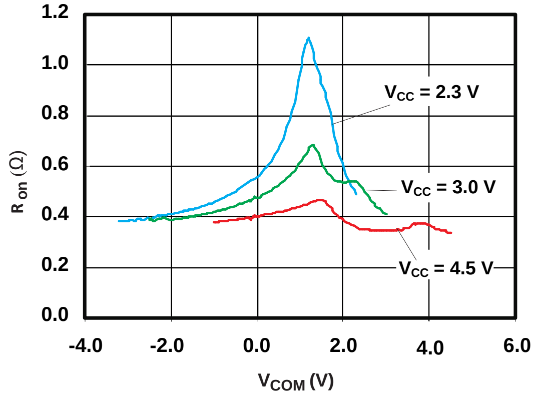


Figure 1. R_{on} vs V_{COM}

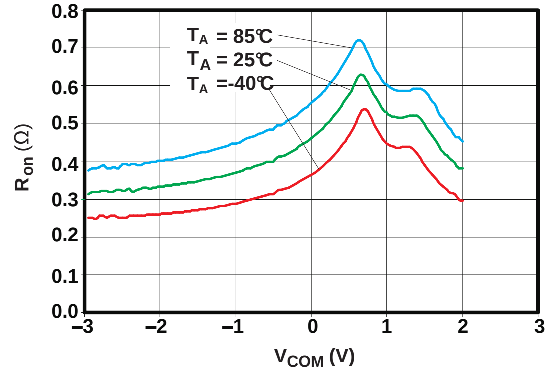


Figure 2. R_{on} vs V_{COM} (V_{CC} = 2.7 V)

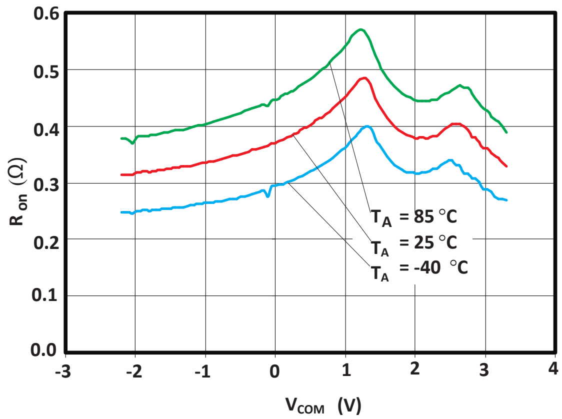


Figure 3. R_{on} vs V_{COM} (V_{CC} = 3.3 V)

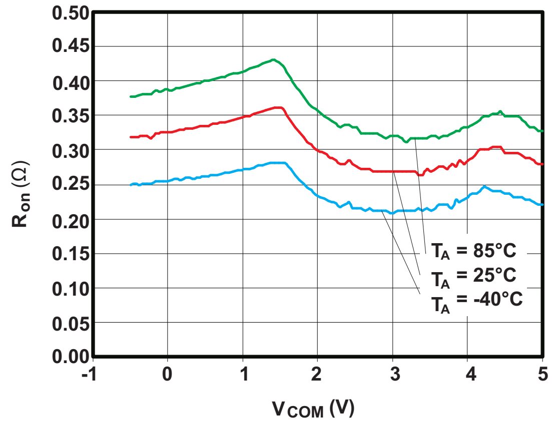


Figure 4. R_{on} vs V_{COM} (V_{CC} = 5 V)

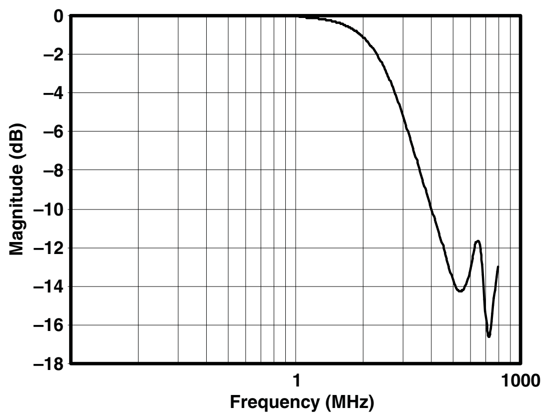


Figure 5. Insertion Loss

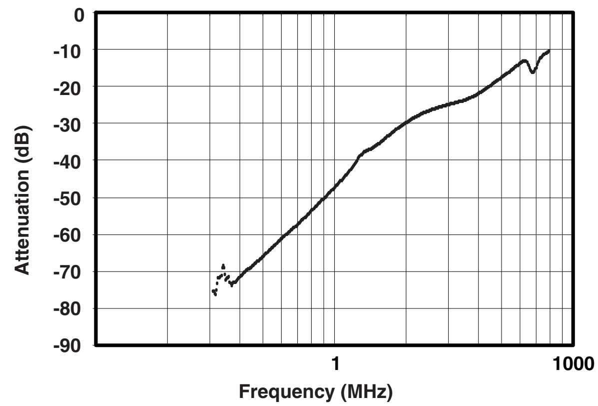


Figure 6. Off Isolation vs Frequency

Typical Characteristics (continued)

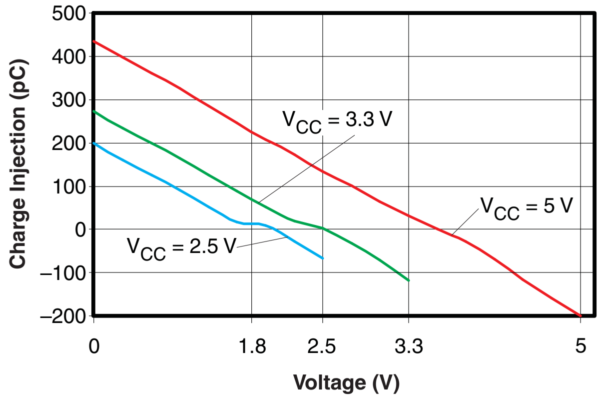


Figure 7. Charge Injection (Q_C) vs V_{COM}

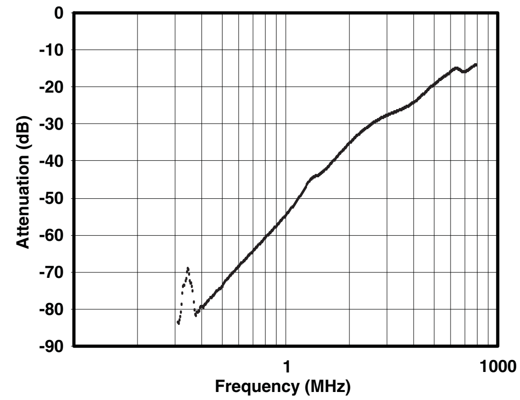


Figure 8. Crosstalk (V_{CC} = 3.3 V)

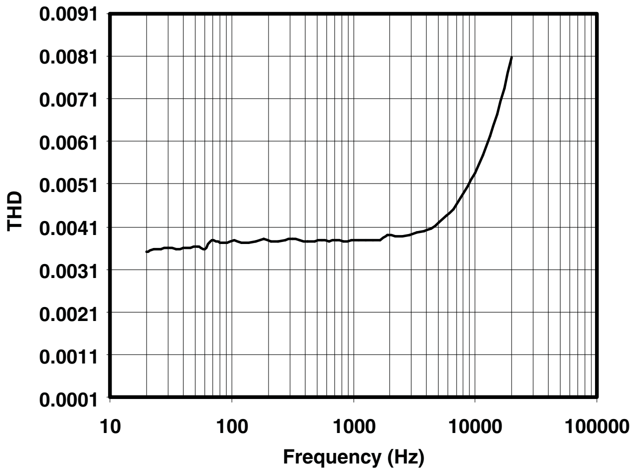


Figure 9. Total Harmonic Distortion vs Frequency

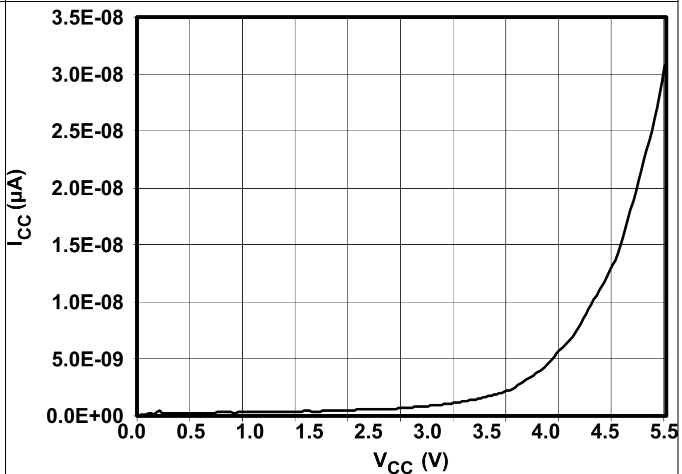


Figure 10. Power-Supply Current vs V_{CC}

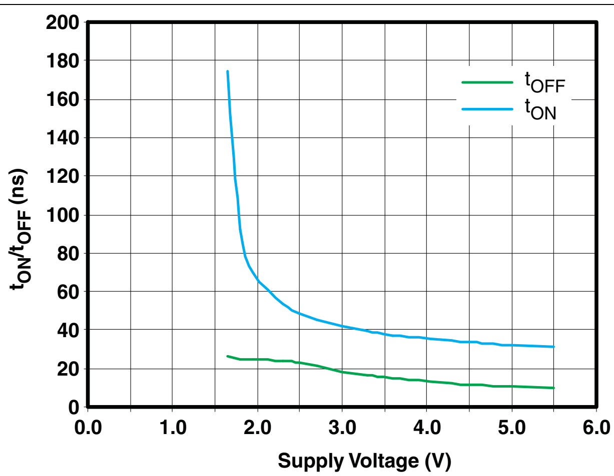


Figure 11. t_{ON} And t_{OFF} vs Supply Voltage

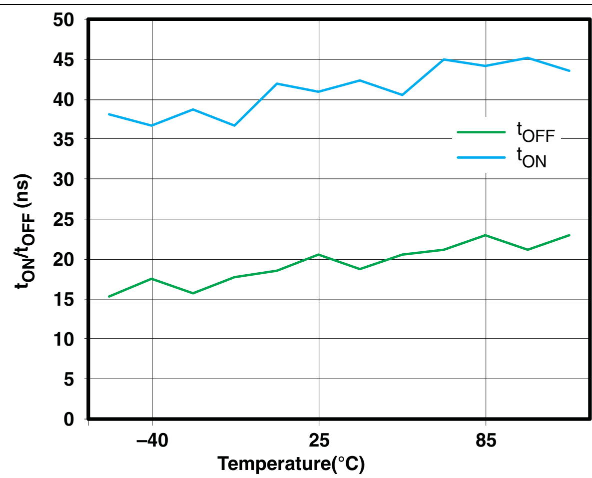


Figure 12. t_{ON} And t_{OFF} vs Temperature (2.5-V Supply)

7 Parameter Measurement Information

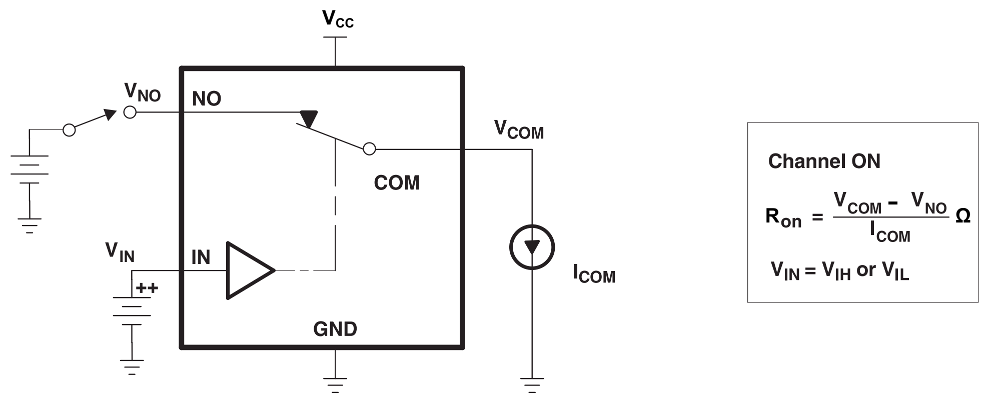


Figure 13. ON-state resistance (R_{on})

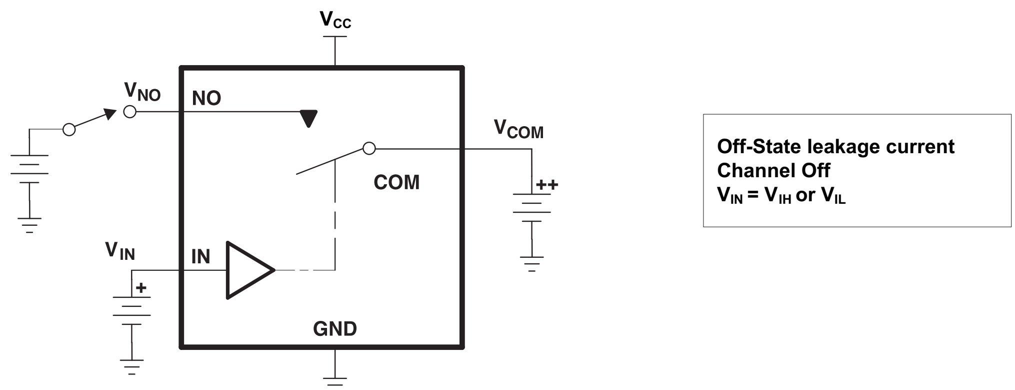


Figure 14. OFF-state leakage current ($I_{COM(OFF)}$, $I_{NO(OFF)}$)

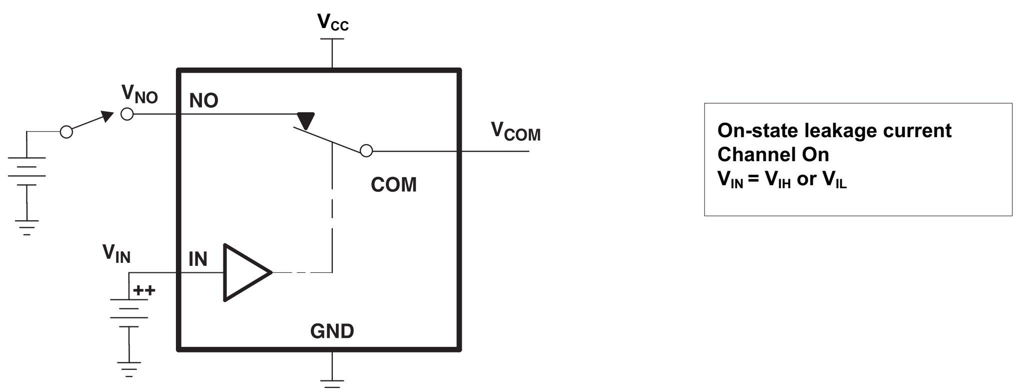
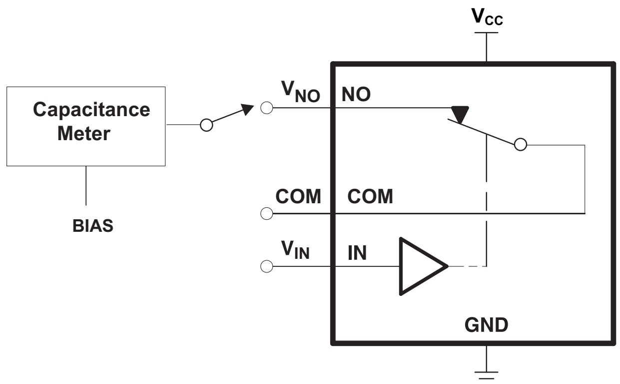


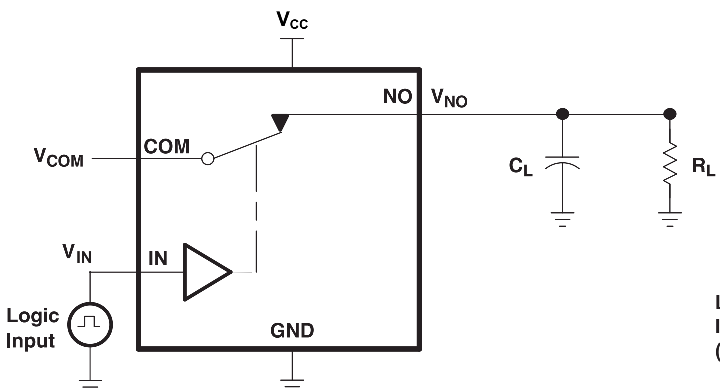
Figure 15. ON-state leakage current ($I_{COM(ON)}$, $I_{NO(ON)}$)

Parameter Measurement Information (continued)

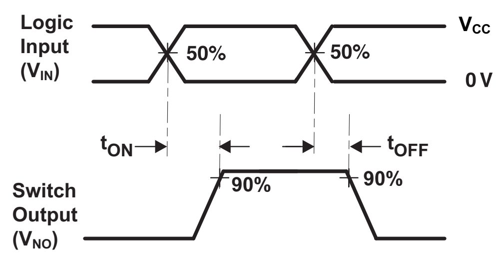


$V_{BIAS} = V_{CC}$ or GND and
$V_{IN} = V_{IH}$ or V_{IL}
Capacitance is measured at NO, COM, and IN inputs during ON and OFF conditions.

Figure 16. Capacitance (C_I, $C_{COM(OFF)}$, $C_{COM(ON)}$, $C_{NO(OFF)}$, $C_{NO(ON)}$)



TEST	R_L	C_L	V_{COM}
t_{ON}	300 Ω	35 pF	V_{CC}
OFF	300 Ω	35 pF	V_{CC}

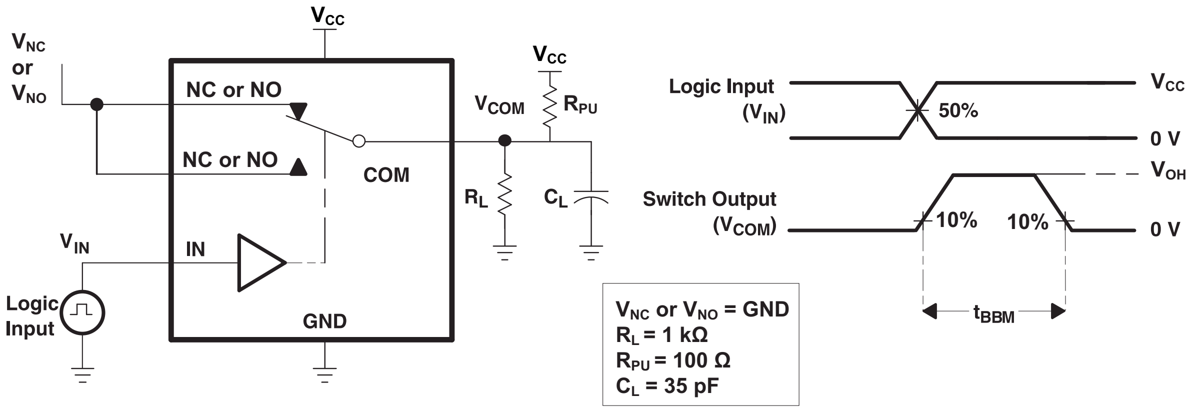


A. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r < 5 ns, t_f < 5 ns.

B. C_L includes probe and jig capacitance.

Figure 17. Turnon (t_{ON}) and Turnoff time (t_{OFF})

Parameter Measurement Information (continued)



A. C_L includes probe and jig capacitance.

B. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r < 5 ns, t_f < 5 ns.

Figure 18. Break-Before-Make Time (t_{BBM})

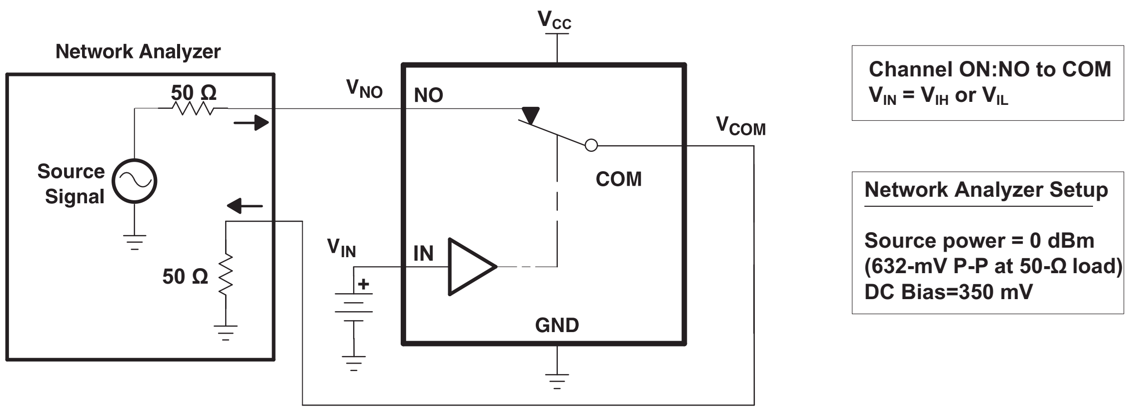


Figure 19. Bandwidth (BW)

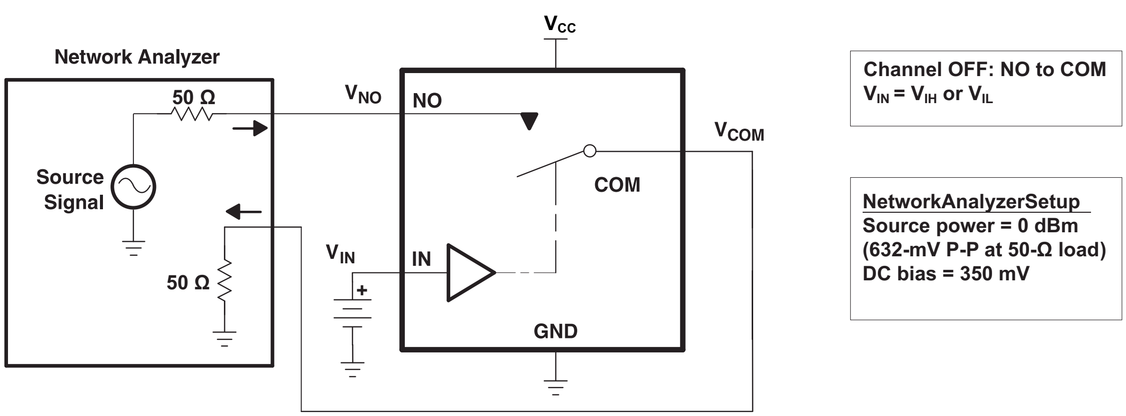


Figure 20. OFF isolation (O_{ISO})

Parameter Measurement Information (continued)

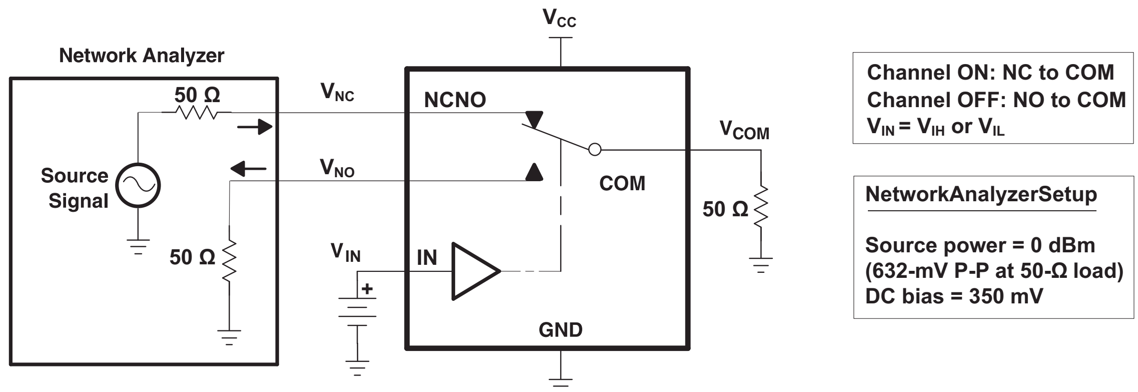
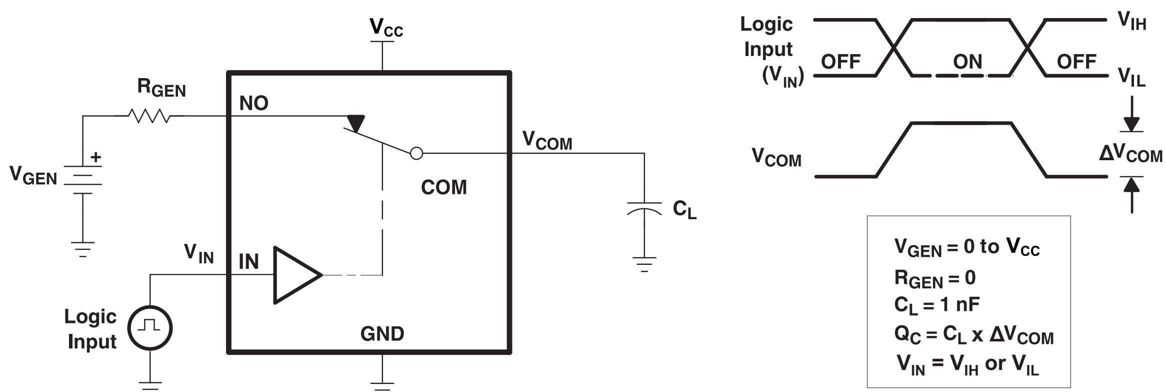


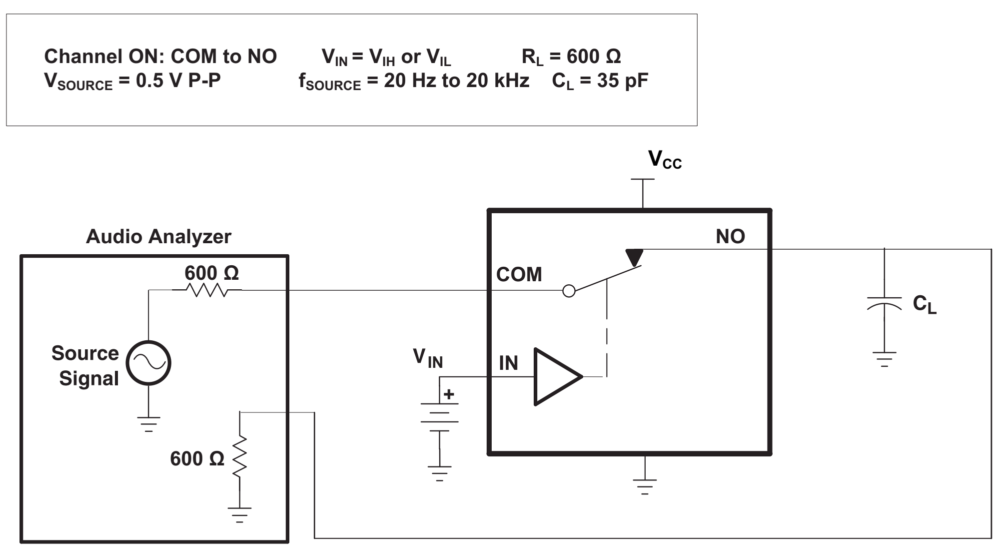
Figure 21. Crosstalk (X_{TALK})



A. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r < 5 ns, t_f < 5 ns.

B. C_L includes probe and jig capacitance.

Figure 22. Charge injection (Q_C)



A. C_L includes probe and jig capacitance.

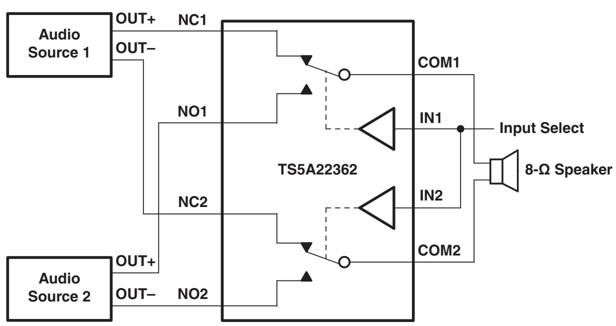
Figure 23. Total Harmonic Distortion (THD)

8 Detailed Description

8.1 Overview

The TS5A22362 is a bidirectional, 2-channel single-pole double-throw (SPDT) analog switches designed to operate from 2.3 V to 5.5 V. The devices feature negative signal capability that allows signals below ground to pass through the switch without distortion. The break-before-make feature prevents signal distortion during the transferring of a signal from one path to another. Low ON-state resistance, excellent channel-to-channel ON-state resistance matching, and minimal total harmonic distortion (THD) performance are ideal for audio applications

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 Negative Signaling Capacity

The TS5A22362 dual SPDT switches feature negative signal capability that allows signals below ground to pass through without distortion. These analog switches operate from a single +2.3-V to +5.5-V supply. The input and output signal swing of the device is dependant of the supply voltage V_{CC}: the devices pass signals as high as V_{CC} and as low as V_{CC} – 5.5 V, including signals below ground with minimal distortion.

Table 1 shows the input/output signal swing the user can get with different supply voltages.

Table 1. Input/Output signal swing

SUPPLY VOLTAGE, V_{CC}	MINIMUM (V_{NC}, V_{NO}, V_{COM}) = V_{CC} – 5.5	MAXIMUM (V_{NC}, V_{NO}, V_{COM}) = V_{CC}
5.5 V	0 V	5.5 V
4.5 V	–1.9 V	4.5 V
3.6 V	–2.5 V	3.6 V
3.0 V	–2.5 V	3.0 V
2.7 V	–2.8 V	2.7 V
2.3 V	–3.2 V	2.3 V

8.4 Device Functional Modes

The function table for TS5A22362 is shown in Table 2

Table 2. Function Table

IN	NC TO COM, COM TO NC	NO TO COM, COM TO NO
L	ON	OFF
H	OFF	ON

9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

Ensure that the device is powered up with a supply voltage on VCC before a voltage can be applied to the signal paths NC and NO.

Tie the digitally controlled inputs select pins IN1 and IN2 to V_{CC} or GND to avoid unwanted switch states that could result if the logic control pins are left floating.

All unused digital inputs of the device must be held at VCC or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, SCBA004.

9.2 Typical Application

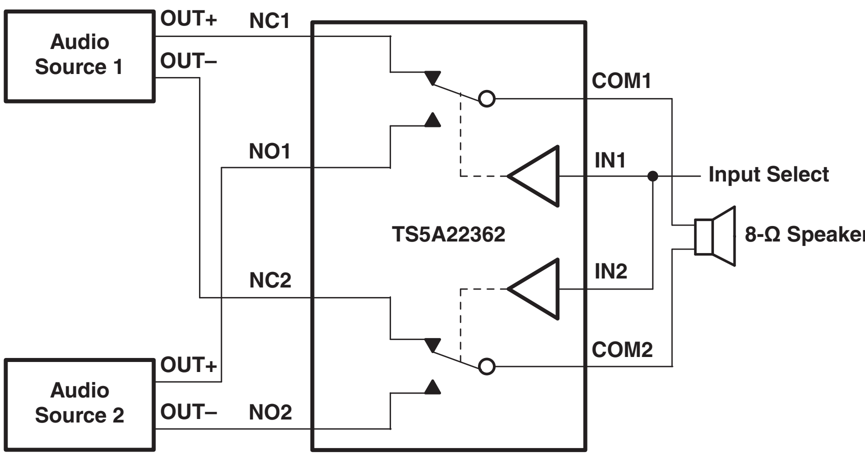


Figure 24. Typical Application

9.2.1 Design Requirements

Tie the digitally controlled inputs select pins IN1 and IN2 to V_{CC} or GND to avoid unwanted switch states that could result if the logic control pins are left floating.

9.2.2 Detailed Design Procedure

Select the appropriate supply voltage to cover the entire voltage swing of the signal passing through the switch because the TS5A22362 operates from a single +2.3-V to +5.5-V supply and the input/output signal swing of the device is dependant of the supply voltage V_{CC}. The device will pass signals as high as V_{CC} and as low as V_{CC} – 5.5 V. Use table 2 as a guide for selecting supply voltage based on the signal passing through the switch.

Ensure that the device is powered up with a supply voltage on VCC before a voltage can be applied to the signal paths NC and NO.

Typical Application (continued)

9.2.3 Application Curve

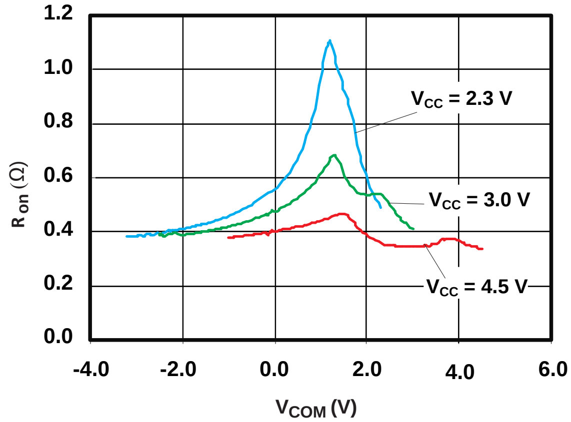


Figure 25. R_{on} vs V_{COM}

10 Power Supply Recommendations

The TS5A22362 operates from a single 2.3-V to 5.5-V supply. The device must be powered up with a supply voltage on VCC before a voltage can be applied to the signal paths NC and NO. It is recommended to include a 100-µs delay after VCC is at voltage before applying a signal on NC and NO paths

It is also good practice to place a 0.1-µF bypass capacitor on the supply pin VCC to GND to smooth out lower frequency noise to provide better load regulation across the frequency spectrum.

11 Layout

11.1 Layout Guidelines

TI recommends placing a bypass capacitor as close to the supply pin VCC as possible to help smooth out lower frequency noise to provide better load regulation across the frequency spectrum.

Minimize trace lengths and vias on the signal paths in order to preserve signal integrity.

11.2 Layout Example

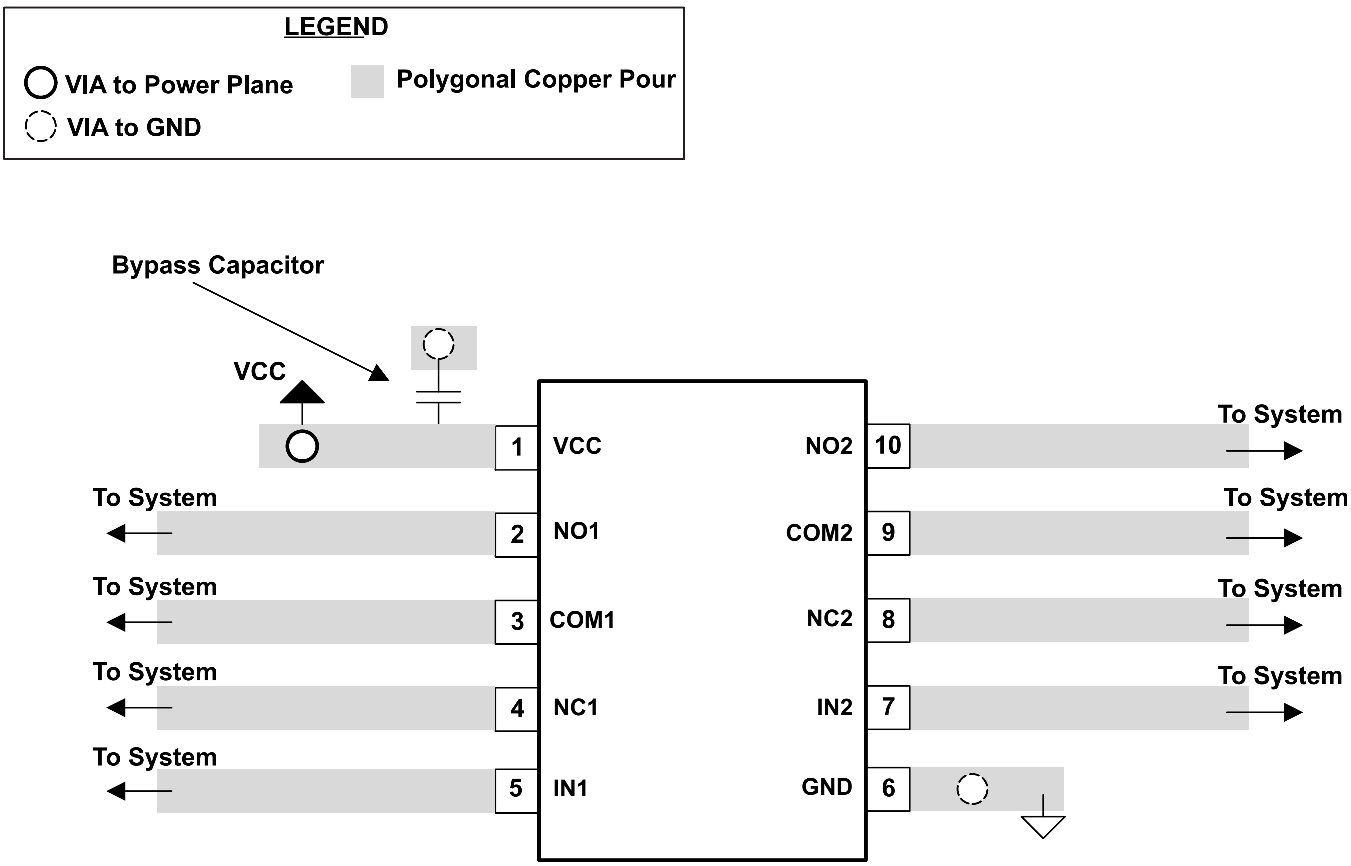


Figure 26. Layout example of TS5A22362

12 Device and Documentation Support

12.1 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

12.2 Trademarks

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

12.3 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

12.4 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TS5A22362DGSR	ACTIVE	VSSOP	DGS	10	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	39R	Samples
TS5A22362DGSRG4	ACTIVE	VSSOP	DGS	10	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	39R	Samples
TS5A22362DRCR	ACTIVE	VSON	DRC	10	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	ZVG	Samples
TS5A22362DRCT-NM	ACTIVE	VSON	DRC	10	250	Green (RoHS & no Sb/Br)	CU SN	Level-2-260C-1 YEAR	-40 to 85	ZVGNM	Samples
TS5A22362YZPR	ACTIVE	DSBGA	YZP	10	3000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 85	(39 ~ 392)	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

[6] Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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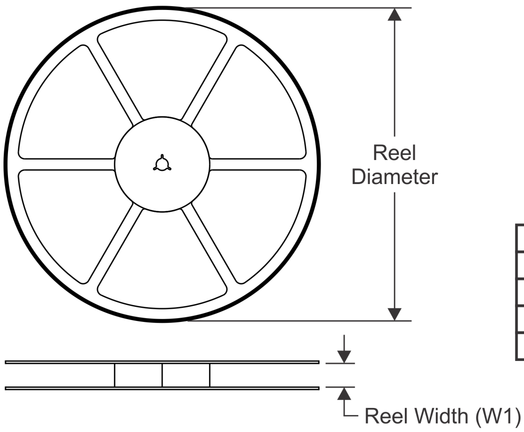
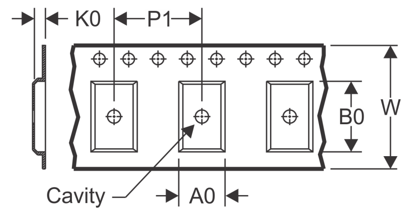
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

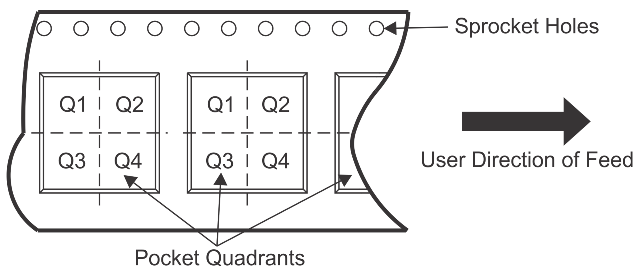


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

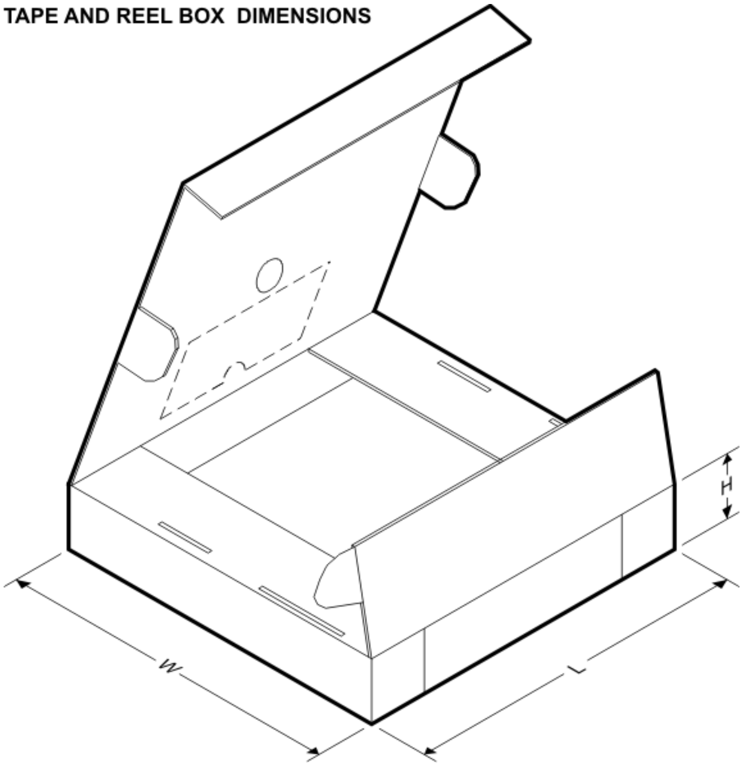
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TS5A22362DGSR	VSSOP	DGS	10	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
TS5A22362DRCR	VSON	DRC	10	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TS5A22362DRCT-NM	VSON	DRC	10	250	180.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TS5A22362YZPR	DSBGA	YZP	10	3000	178.0	9.2	1.49	1.99	0.63	4.0	8.0	Q2

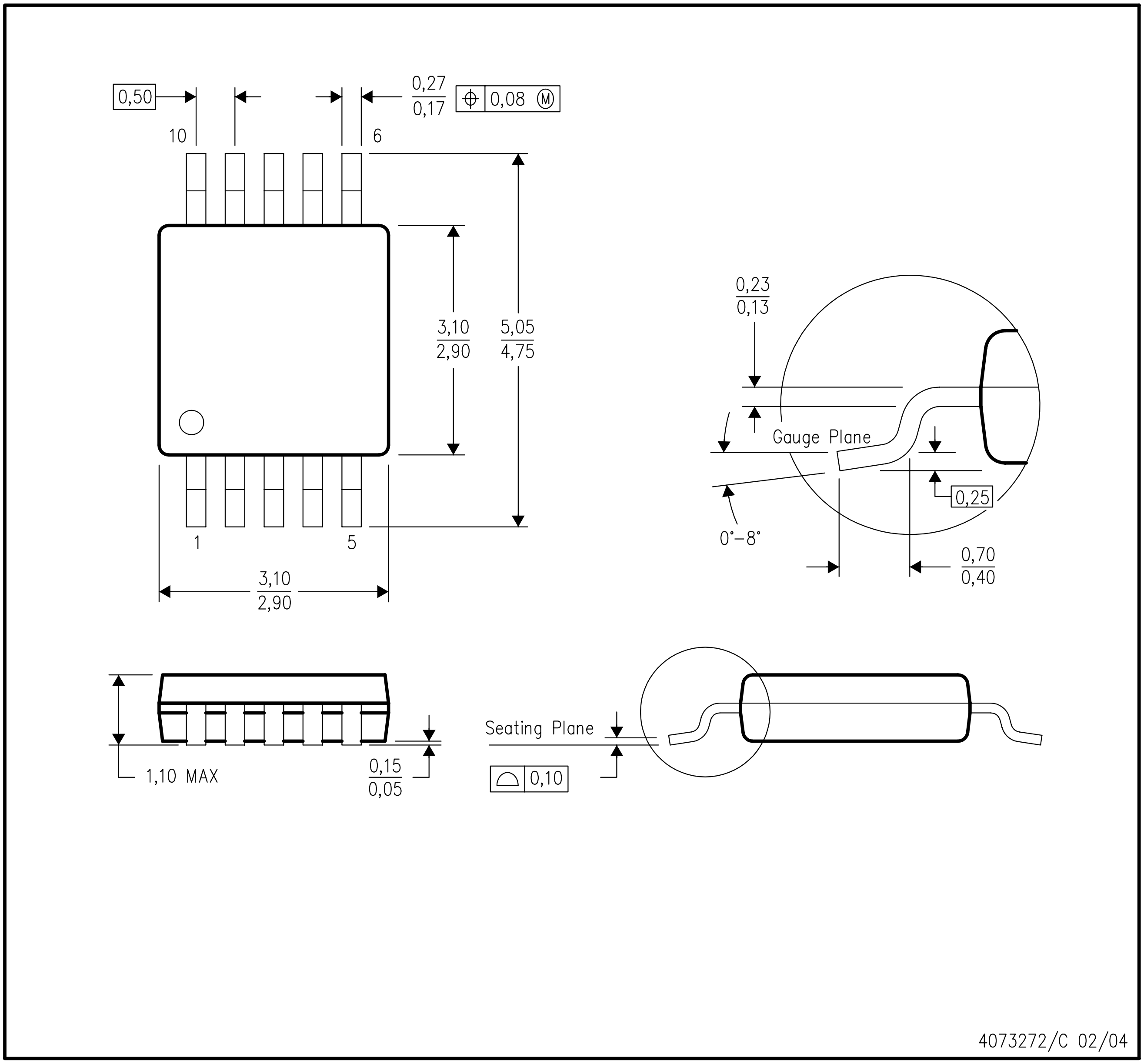
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

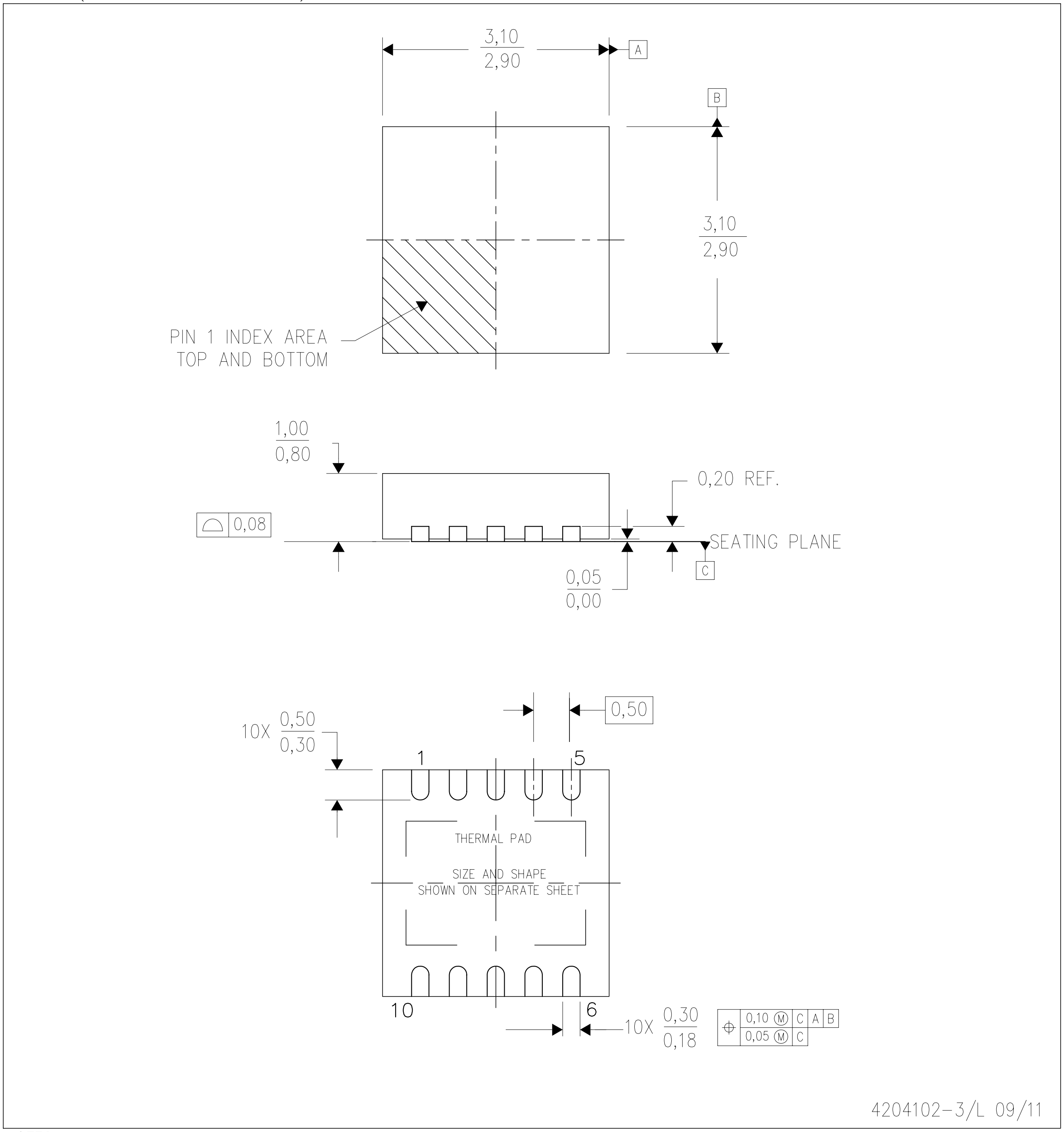
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TS5A22362DGSR	VSSOP	DGS	10	2500	358.0	335.0	35.0
TS5A22362DRCR	VSON	DRC	10	3000	367.0	367.0	35.0
TS5A22362DRCT-NM	VSON	DRC	10	250	210.0	185.0	35.0
TS5A22362YZPR	DSBGA	YZP	10	3000	220.0	220.0	35.0

DGS (S-PDSO-G10) PLASTIC SMALL-OUTLINE PACKAGE



NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion.
D. Falls within JEDEC MO-187 variation BA.

DRC (S-PVSON-N10) PLASTIC SMALL OUTLINE NO-LEAD



NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
- B. This drawing is subject to change without notice.
- C. Small Outline No-Lead (SON) package configuration.
- D. The package thermal pad must be soldered to the board for thermal and mechanical performance, if present.
- E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions, if present

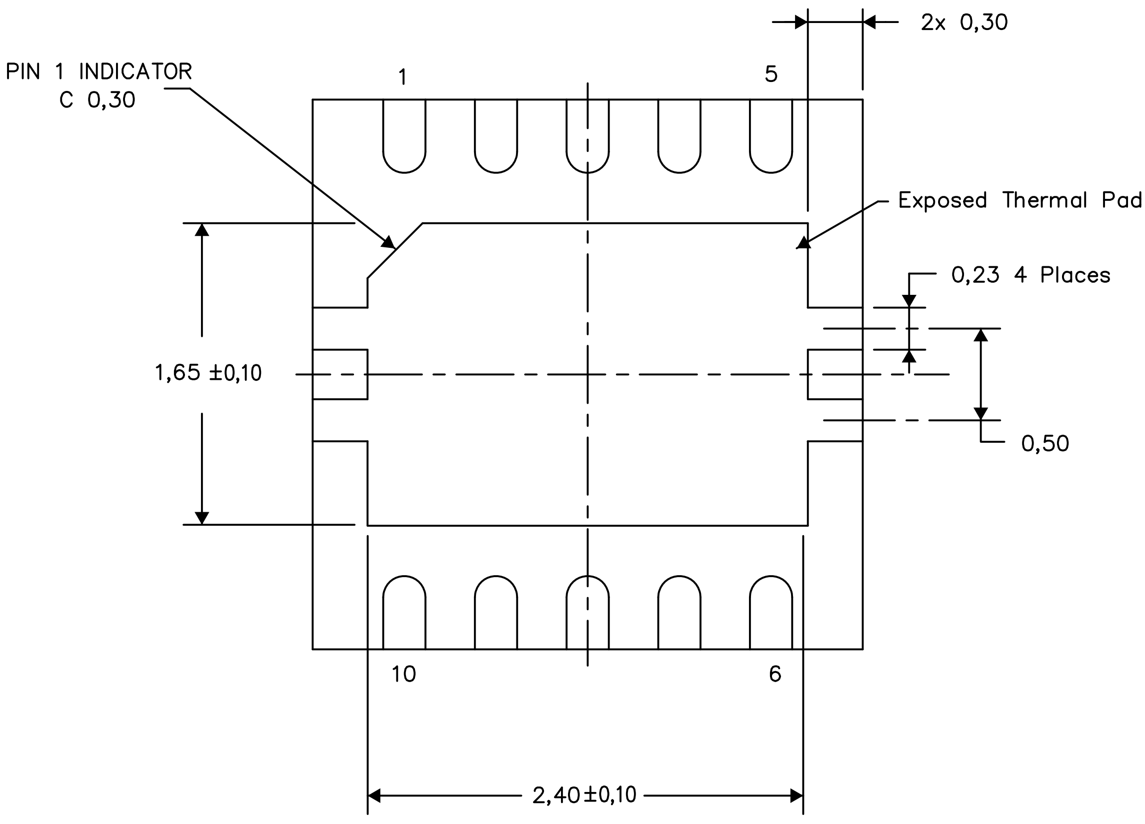
DRC (S–PVSON–N10) PLASTIC SMALL OUTLINE NO–LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.

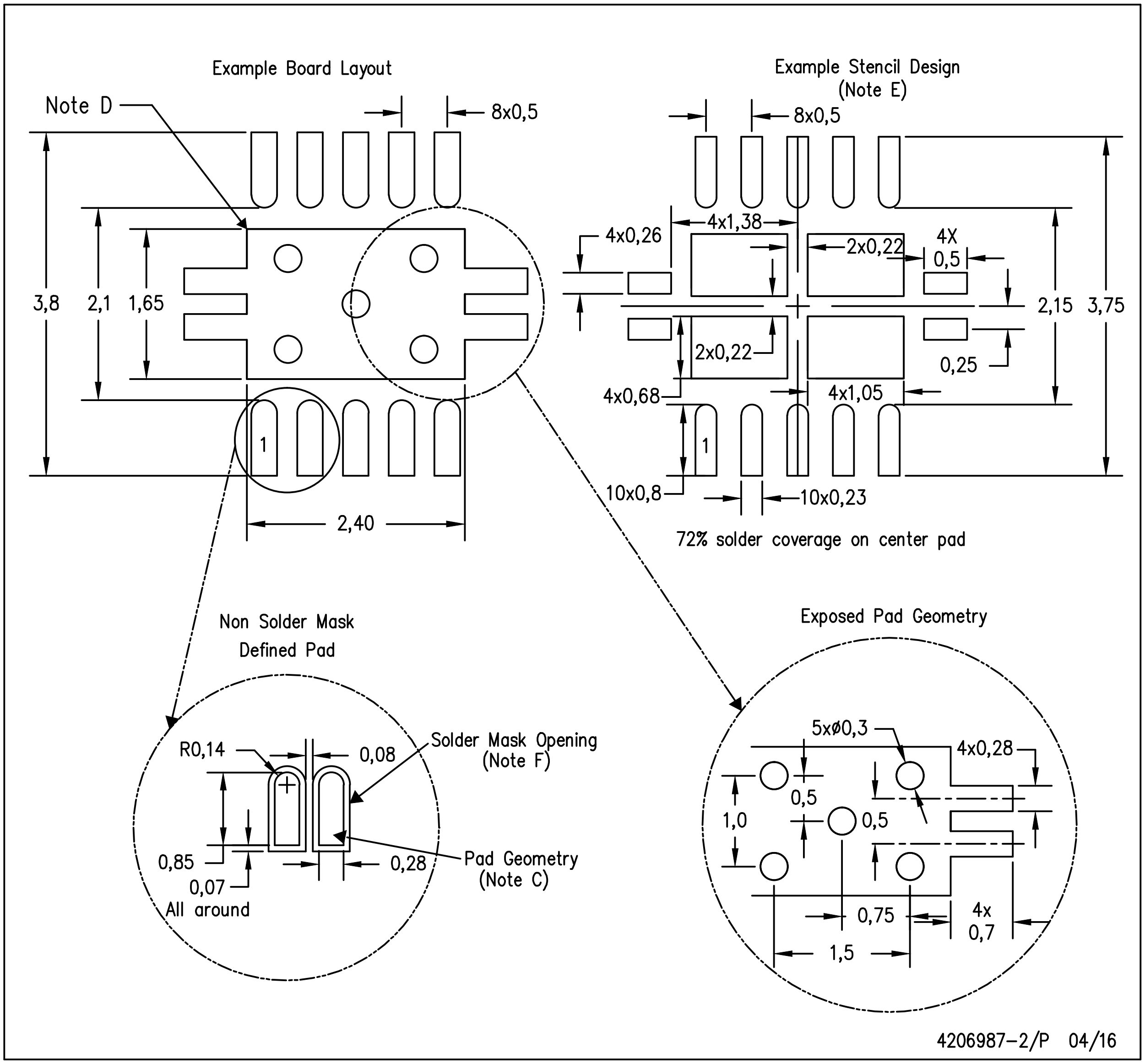


Exposed Thermal Pad Dimensions

4206565–3/Y 08/15

NOTE: A. All linear dimensions are in millimeters

DRC (S–PVSON–N10) PLASTIC SMALL OUTLINE NO–LEAD



NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Publication IPC–7351 is recommended for alternate designs.
- D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat–Pack Packages, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http: //www.ti.com>.
- E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
- F. Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.

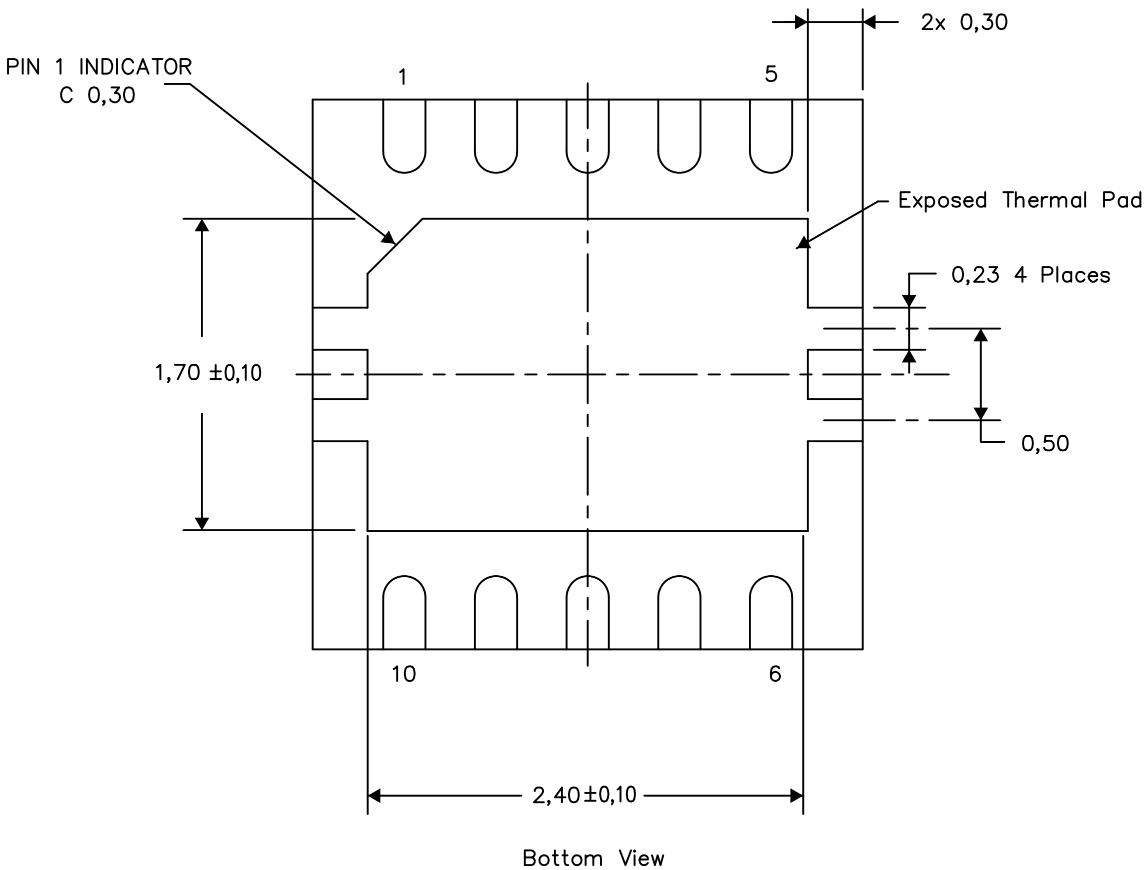
DRC (S–PVSON–N10) PLASTIC SMALL OUTLINE NO–LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.

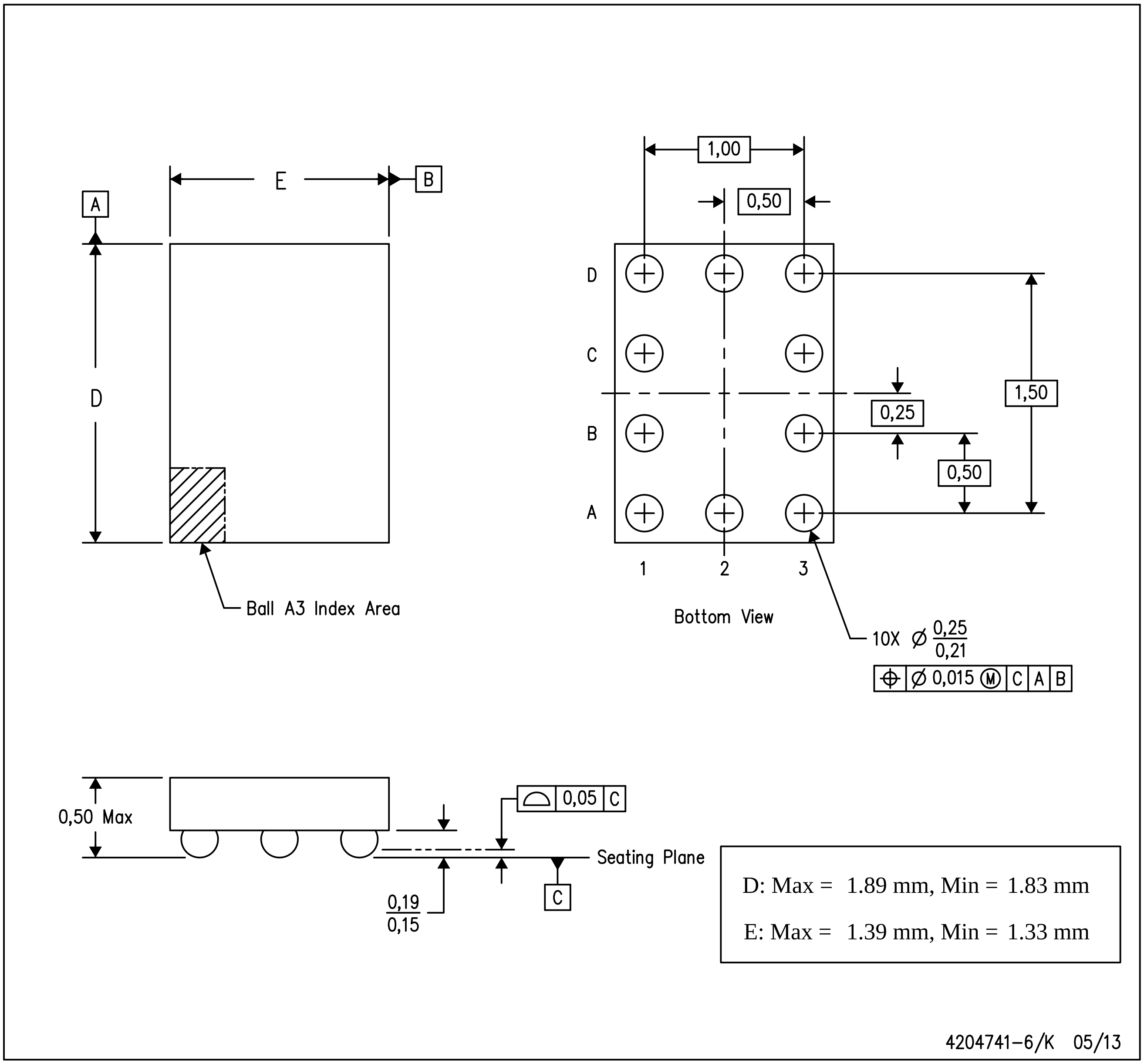


Exposed Thermal Pad Dimensions

4206565–8/Y 08/15

NOTE: A. All linear dimensions are in millimeters

YZP (R-XBGA-N10) (CUSTOM) DIE-SIZE BALL GRID ARRAY



NOTES: A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. NanoFree™ package configuration.

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