EMIPAK-2B PressFit Power Module 3-Levels Half-Bridge Inverter Stage, 150 A

EMIPAK-2B
(package example)

FEATURES

- Trench IGBT technology
- FRED Pt® clamping diodes
- PressFit pins technology
- Exposed Al_2O_3 substrate with low thermal resistance
- Short circuit rated
- Square RBSOA
- Integrated thermistor
- Low internal inductances
- Low switching loss
- PressFit pins locking technology. Patent # US.263.820 B2
- UL approved file E78996
- Material categorization: for definitions of compliance please see www.vishay.com/doc?99912

RoHS
COMPLIANT

PRODUCT SUMMARY	
Q1 to Q4 IGBT	
V_{CES}	650 V
$V_{CE(ON)}$ typical at I_C = 150 A	1.70 V
I_C at T_C = 82 °C	150 A
Speed	8 kHz to 30 kHz
Package	EMIPAK-2B
Circuit	3-levels half bridge inverter stage

DESCRIPTION

VS-ETF150Y65N is an integrated solution for a multi level inverter stage in a single package. The EMIPAK-2B package is easy to use thanks to the PressFit pins and the exposed substrate provides improved thermal performance. The optimized layout also helps to minimize stray parameters, allowing for better EMI performance.

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	TEST CONDITIONS	MAX.	UNITS
Operating junction temperature	T_J		175	°C
Storage temperature range	T_{Stg}		-40 to +150	
RMS isolation voltage	V_{ISOL}	T_J = 25 °C, all terminals shorted, f = 50 Hz, t = 1 s	3500	V
Q1 to Q4 IGBT				
Collector to emitter voltage	V_{CES}		650	V
Gate to emitter voltage	V_{GES}		20	
Pulsed collector current	I_{CM}		450	A
Clamped inductive load current	I_{LM}		180	
Continuous collector current	I_C	T_C = 25 °C	201	A
		T_C = 60 °C	171	
		T_{SINK} = 60 °C	77	
Power dissipation	P_D	T_C = 25 °C	600	W
		T_C = 60 °C	460	

PATENT(S): www.vishay.com/patents
This Vishay product is protected by one or more United States and International patents.

ABSOLUTE MAXIMUM RATINGS				
PARAMETER	**SYMBOL**	**TEST CONDITIONS**	**MAX.**	**UNITS**
D5 - D6 CLAMPING DIODE				
Repetitive peak reverse voltage	V_{RRM}		650	V
Single pulse forward current	I_{FSM}	10 ms sine or 6 ms rectangular pulse, T_J = 25 °C	750	A
Diode continuous forward current	I_F	T_C = 25 °C	161	
		T_C = 60 °C	140	
		T_{SINK} = 60 °C	74	
Power dissipation	P_D	T_C = 25 °C	319	W
		T_C = 60 °C	245	
D1 - D2 - D3 - D4 AP DIODE				
Single pulse forward current	I_{FSM}	10 ms sine or 6 ms rectangular pulse, T_J = 25 °C	500	A
Diode continuous forward current	I_F	T_C = 25 °C	102	
		T_C = 60 °C	92	
		T_{SINK} = 60 °C	57	
Power dissipation	P_D	T_C = 25 °C	238	W
		T_C = 60 °C	182	

Notes

- Absolute Maximum Ratings indicate sustained limits beyond which damage to the device may occur.

(1) V_{CC} = 325 V, V_{GE} = 15 V, L = 500 μH, R_g = 4.7 Ω, T_J = 175 °C

ELECTRICAL SPECIFICATIONS (T_J = 25 °C unless otherwise noted)						
PARAMETER	**SYMBOL**	**TEST CONDITIONS**	**MIN.**	**TYP.**	**MAX.**	**UNITS**
Q1 to Q4 IGBT						
Collector to emitter breakdown voltage	BV_{CES}	V_{GE} = 0 V, I_C = 100 μA	650	-	-	V
Collector to emitter voltage	$V_{CE(ON)}$	V_{GE} = 15 V, I_C = 150 A	-	1.70	2.17	
		V_{GE} = 15 V, I_C = 150 A, T_J = 125 °C	-	1.95	-	
Gate threshold voltage	$V_{GE(th)}$	V_{CE} = V_{GE}, I_C = 5.0 mA	5.0	6.0	8.4	
Temperature coefficient of threshold voltage	$\Delta V_{GE(th)}/\Delta T_J$	V_{CE} = V_{GE}, I_C = 1.0 mA (25 °C to 125 °C)	-	-18	-	mV/°C
Forward transconductance	g_{fe}	V_{CE} = 20 V, I_C = 150 A	-	102	-	S
Transfer characteristics	V_{GE}	V_{CE} = 20 V, I_C = 150 A	-	10.2	-	V
Zero gate voltage collector current	I_{CES}	V_{GE} = 0 V, V_{CE} = 650 V	-	0.1	100	μA
		V_{GE} = 0 V, V_{CE} = 650 V, T_J = 125 °C	-	130	-	
Gate to emitter leakage current	I_{GES}	V_{GE} = ± 20 V, V_{CE} = 0 V	-	-	± 600	nA
D5 - D6 CLAMPING DIODE						
Cathode to anode blocking voltage	V_{BR}	I_R = 500 μA	650	-	-	V
Forward voltage drop	V_{FM}	I_F = 100 A	-	1.64	2.0	
		I_F = 100 A, T_J = 125 °C	-	1.35	-	
Reverse leakage current	I_{RM}	V_R = 650 V	-	0.3	100	μA
		V_R = 650 V, T_J = 125 °C	-	100	-	
D1 - D2 - D3 - D4 AP DIODE						
Forward voltage drop	V_{FM}	I_F = 100 A	-	2.1	2.9	V
		I_F = 100 A, T_J = 125 °C	-	1.64	-	

SWITCHING CHARACTERISTICS (T_J = 25 °C unless otherwise noted)						
PARAMETER	**SYMBOL**	**TEST CONDITIONS**	**MIN.**	**TYP.**	**MAX.**	**UNITS**
Q1 to Q4 IGBT						
Total gate charge (turn-on)	Q_g	I_C = 150 A V_{CC} = 400 V V_{GE} = 15 V	-	310	-	nC
Gate to emitter charge (turn-on)	Q_{ge}		-	95	-	
Gate to collector charge (turn-on)	Q_{gc}		-	130	-	
Input capacitance	C_{ies}	V_{GE} = 0 V V_{CC} = 30 V f = 1 MHz	-	9900	-	pF
Output capacitance	C_{oes}		-	460	-	
Reverse transfer capacitance	C_{res}		-	250	-	
Q1 and Q4 IGBT with D5 and D6 CLAMP DIODE						
Turn-on switching loss	E_{ON}	I_C = 150 A V_{CC} = 325 V V_{GE} = 15 V R_g = 4.7 Ω L = 500 μH (1)	-	0.69	-	mJ
Turn-off switching loss	E_{OFF}		-	3.4	-	
Total switching loss	E_{TOT}		-	4.1	-	
Turn-on delay time	$t_{d(on)}$		-	161	-	ns
Rise time	t_r		-	108	-	
Turn-off delay time	$t_{d(off)}$		-	139	-	
Fall time	t_f		-	91	-	
Turn-on switching loss	E_{ON}	I_C = 150 A V_{CC} = 325 V V_{GE} = 15 V R_g = 4.7 Ω L = 500 μH T_J = 125 °C (1)	-	0.9	-	mJ
Turn-off switching loss	E_{OFF}		-	4.2	-	
Total switching loss	E_{TOT}		-	5.1	-	
Turn-on delay time	$t_{d(on)}$		-	160	-	ns
Rise time	t_r		-	109	-	
Turn-off delay time	$t_{d(off)}$		-	150	-	
Fall time	t_f		-	97	-	
Q2 and Q3 IGBT with D2 and D3 AP DIODE						
Turn-on switching loss	E_{ON}	I_C = 150 A V_{CC} = 325 V V_{GE} = 15 V R_g = 4.7 Ω L = 500 μH (1)	-	0.8	-	mJ
Turn-off switching loss	E_{OFF}		-	4.0	-	
Total switching loss	E_{TOT}		-	4.8	-	
Turn-on delay time	$t_{d(on)}$		-	144	-	ns
Rise time	t_r		-	117	-	
Turn-off delay time	$t_{d(off)}$		-	144	-	
Fall time	t_f		-	98	-	
Turn-on switching loss	E_{ON}	I_C = 150 A V_{CC} = 325 V V_{GE} = 15 V R_g = 4.7 Ω L = 500 μH T_J = 125 °C (1)	-	0.98	-	mJ
Turn-off switching loss	E_{OFF}		-	4.7	-	
Total switching loss	E_{TOT}		-	5.7	-	
Turn-on delay time	$t_{d(on)}$		-	166	-	ns
Rise time	t_r		-	120	-	
Turn-off delay time	$t_{d(off)}$		-	153	-	
Fall time	t_f		-	106	-	
Reverse bias safe operating area	RBSOA	T_J = 175 °C, I_C = 180 A, V_{CC} = 325 V, V_P = 650 V, R_g = 4.7 Ω, V_{GE} = 15 V to 0 V	Fullsquare			
Short circuit safe operating area	SCSOA	R_g = 5.0 Ω, V_{CC} = 400 V, V_P = 600 V, V_{GE} = 15 V to 0, T_J = 150 °C	-	-	5.5	μs

SWITCHING CHARACTERISTICS (T_J = 25 °C unless otherwise noted)						
PARAMETER	**SYMBOL**	**TEST CONDITIONS**	**MIN.**	**TYP.**	**MAX.**	**UNITS**
D5 - D6 CLAMPING DIODE						
Diode reverse recovery time	t_{rr}	V_R = 200 V I_F = 50 A dI/dt = 500 A/μs	-	78	-	ns
Diode peak reverse current	I_{rr}		-	11	-	A
Diode recovery charge	Q_{rr}		-	433	-	nC
Diode reverse recovery time	t_{rr}	V_R = 200 V I_F = 50 A dI/dt = 500 A/μs, T_J = 125 °C	-	155	-	ns
Diode peak reverse current	I_{rr}		-	28	-	A
Diode recovery charge	Q_{rr}		-	2150	-	nC
D1 - D2 - D3 - D4 AP DIODE						
Diode reverse recovery time	t_{rr}	V_R = 200 V I_F = 50 A dI/dt = 500 A/μs	-	82	-	ns
Diode peak reverse current	I_{rr}		-	11	-	A
Diode recovery charge	Q_{rr}		-	363	-	nC
Diode reverse recovery time	t_{rr}	V_R = 200 V I_F = 50 A dI/dt = 500 A/μs, T_J = 125 °C	-	134	-	ns
Diode peak reverse current	I_{rr}		-	22	-	A
Diode recovery charge	Q_{rr}		-	1500	-	nC

Note

(1) Energy losses include “tail” and diode reverse recovery.

INTERNAL NTC - THERMISTOR SPECIFICATIONS				
PARAMETER	**SYMBOL**	**TEST CONDITIONS**	**TYP.**	**UNITS**
Resistance	R25	T_J = 25 °C	5000 ± 5 %	Ω
	R125	T_J = 100 °C	493 ± 5 %	
B-constant	B	$R_2 = R_{25}$ exp. $[B_{25/50}$ $(1/T_2$ - 1/(298.15 K))]	3375 ± 5 %	K
Temperature range			-40 to +125	°C
Maximum operating temperature			220	
Dissipation constant			2	mW/°C
Thermal time constant			8	s

THERMAL AND MECHANICAL SPECIFICATIONS					
PARAMETER	**SYMBOL**	**MIN.**	**TYP.**	**MAX.**	**UNITS**
Q1 to Q4 IGBT- junction to case thermal resistance (per switch)	R_{thJC}	-	-	0.25	°C/W
D5 - D6 Clamping diode - junction to case thermal resistance (per diode)		-	-	0.47	
D1 - D2 - D3 - D4 AP diode - junction to case thermal resistance (per diode)		-	-	0.63	
Q1 to Q4 IGBT - case to sink thermal resistance (per switch)	R_{thCS} (1)	-	0.62	-	
D5 - D6 Clamping diode - case to sink thermal resistance (per diode)		-	0.7	-	
D1 - D2 - D3 - D4 AP diode - case to sink thermal resistance (per diode)		-	0.7	-	
Case to sink thermal resistance per module		-	0.1	-	
Mounting torque (M4)		2	-	3	Nm
Weight		-	45	-	g

Note

(1) Mounting surface flat, smooth, and greased

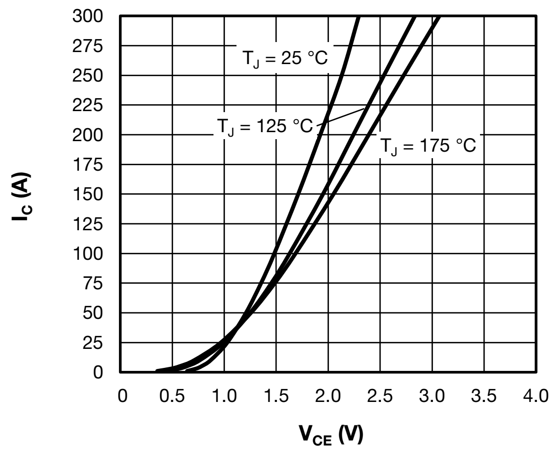


Fig. 1 - I_C vs. V_{CE},
Typical Q1 to Q4 Trench IGBT Output Characteristics,
V_{GE} = 15 V

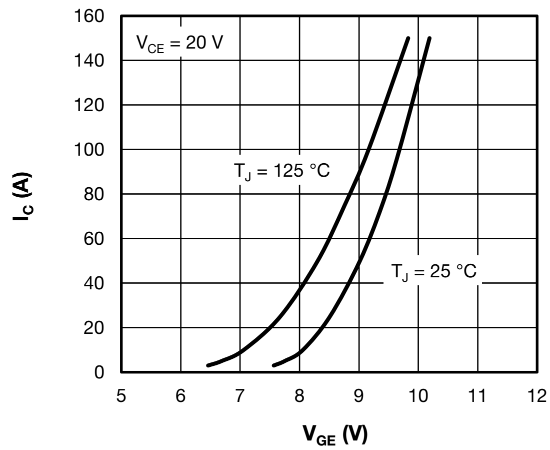


Fig. 4 - I_C vs V_{GE}
Typical Q1 to Q4 Trench IGBT Transfer Characteristics

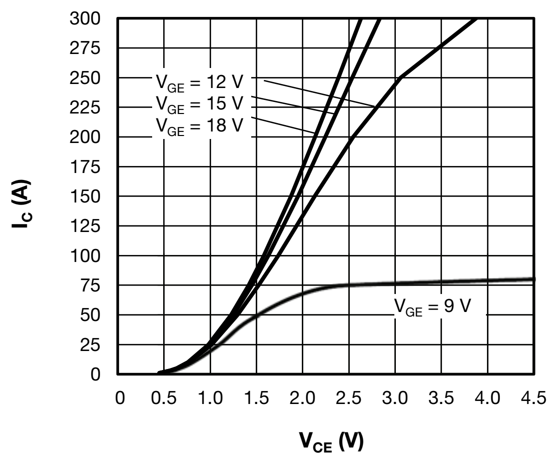


Fig. 2 - I_C vs. V_{CE}
Typical Q1 to Q4 Trench IGBT Output Characteristics,
T_J = 125 °C

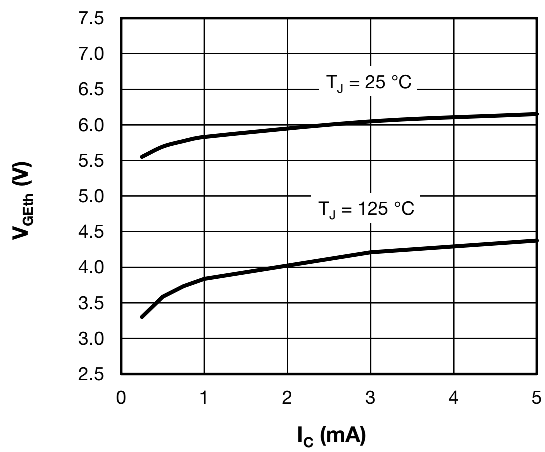


Fig. 5 - V_{GEth} vs. I_C
Typical Q1 to Q4 Trench IGBT Gate Threshold Voltage

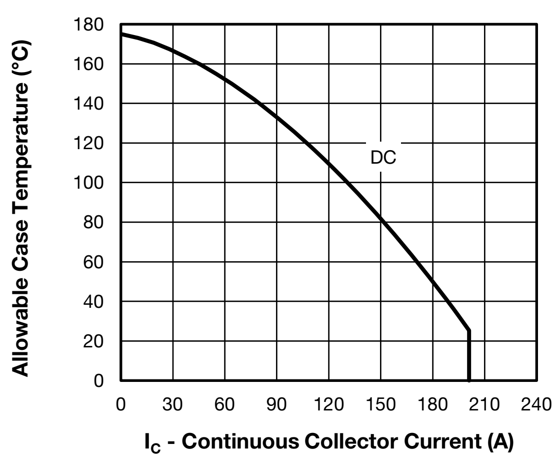


Fig. 3 - Allowable Case Temperature vs. Continuous Collector Current,
Maximum Q1 to Q4 Trench IGBT Continuous Collector Current vs.
Case Temperature

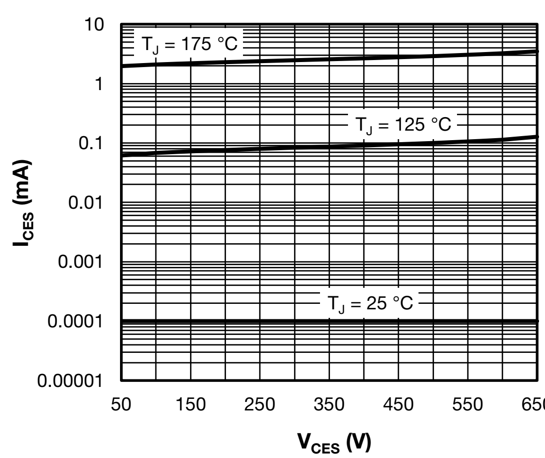


Fig. 6 - I_{CES} vs V_{CES}
Typical Q1 to Q4 Trench IGBT Zero Gate Voltage Collector Current

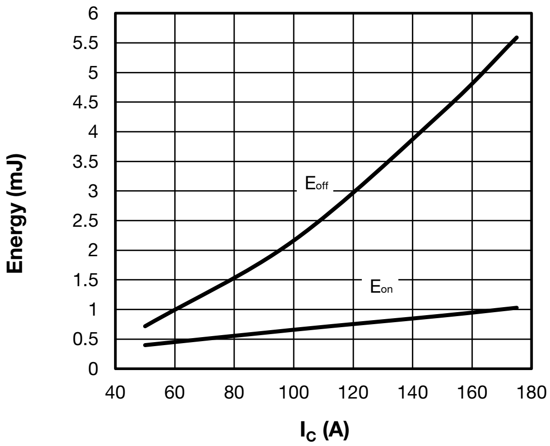


Fig. 7 - Energy Loss vs. I_C
(Typical Q1 - Q4 Trench IGBT Energy Loss vs. I_C
(with D5 - D6 Clamping Diode)),
T_J = 125 °C, V_{CC} = 325 V, R_g = 4.7 Ω, V_{GE} = ± 15 V, L = 500 µH

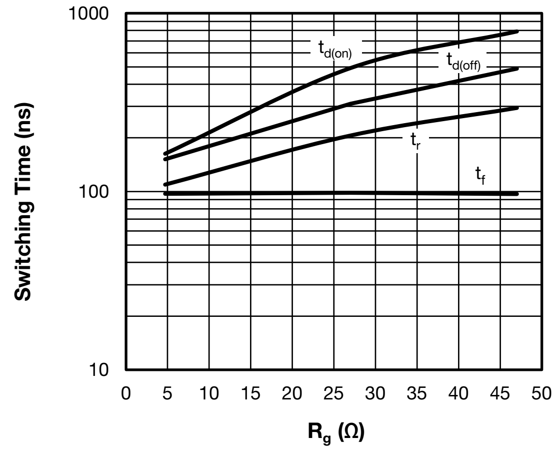


Fig. 10 - Switching Time vs. R_g
(Typical Q1 - Q4 Trench IGBT Switching Time vs. R_g
(with D5 - D6 Clamping Diode)),
T_J = 125 °C, V_{CC} = 325 V, I_C = 150 A, V_{GE} = ± 15 V, L = 500 µH

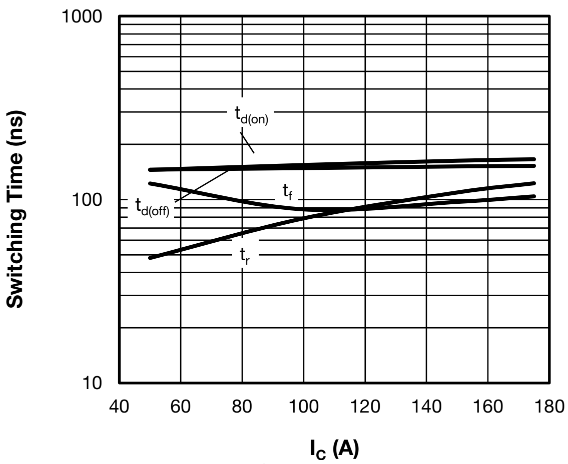


Fig. 8 - Switching Time vs. I_C
(Typical Q1 - Q4 Trench IGBT Switching Time vs. I_C
(with D5 - D6 Clamping Diode)),
T_J = 125 °C, V_{CC} = 325 V, R_g = 4.7 Ω, V_{GE} = ± 15 V, L = 500 µH

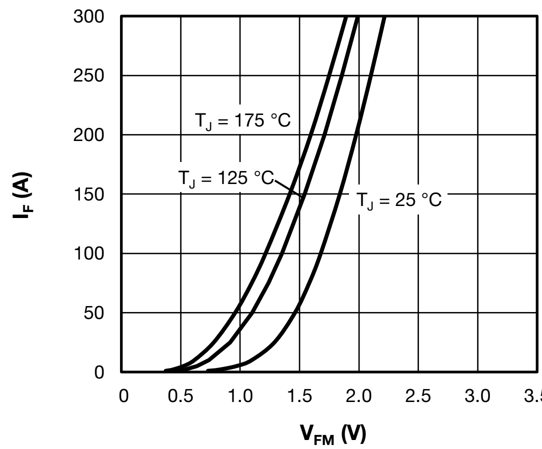


Fig. 11 - I_F vs. V_{FM}
(Typical D5 - D6 Clamping Diode Forward Characteristics)

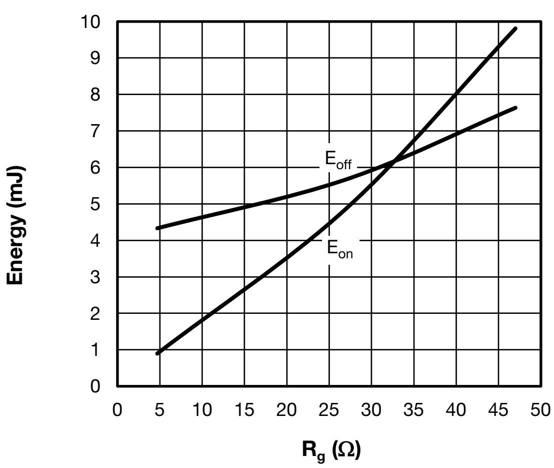


Fig. 9 - Energy Loss vs. R_g
(Typical Q1 - Q4 Trench IGBT Energy Loss vs R_g
(with D5 - D6 Clamping Diode)),
T_J = 125 °C, V_{CC} = 325 V, I_C = 150 A, V_{GE} = ± 15 V, L = 500 µH

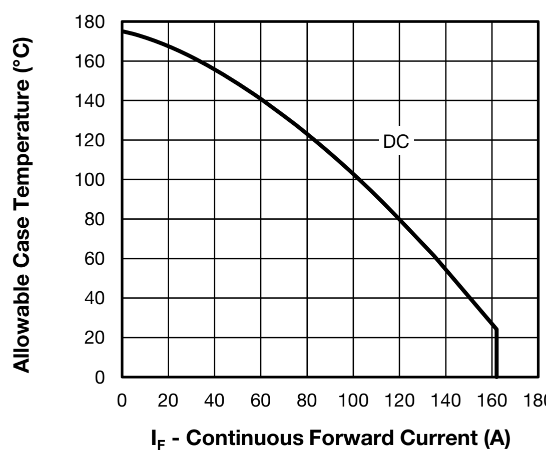


Fig. 12 - Allowable Case Temperature vs. Continuous Forward Current,
(Maximum D5 - D6 Diode Continuous Forward Current vs.
Case Temperature)

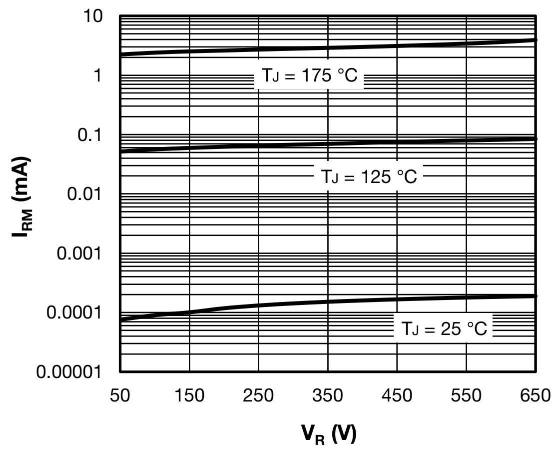


Fig. 13 - I_{RM} vs. V_R
(Typical D5 - D6 Clamping Diode Reverse Leakage Current)

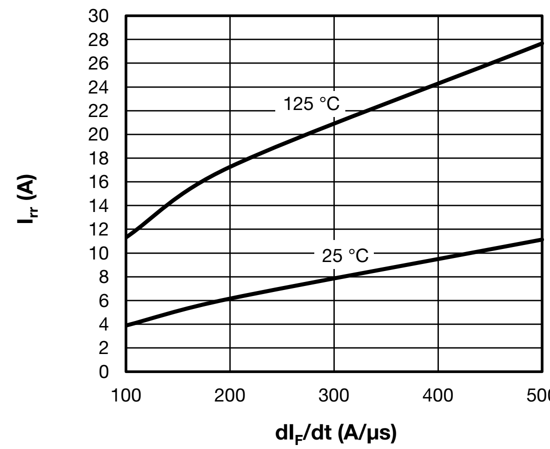


Fig. 15 - I_{rr} vs. dI_F/dt)
(Typical D5 - D6 Clamping Diode Reverse Recovery Current vs. dI_F/dt), V_{rr} = 200 V, I_F = 50 A

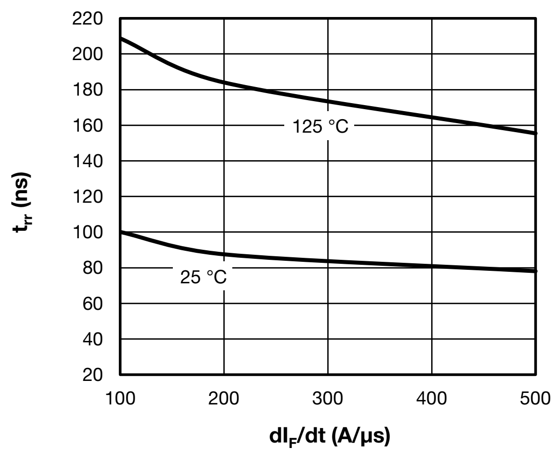


Fig. 14 - t_{rr} vs. dI_F/dt
(Typical D5 - D6 Clamping Diode Reverse Recovery Time vs. dI_F/dt), V_{rr} = 200 V, I_F = 50 A

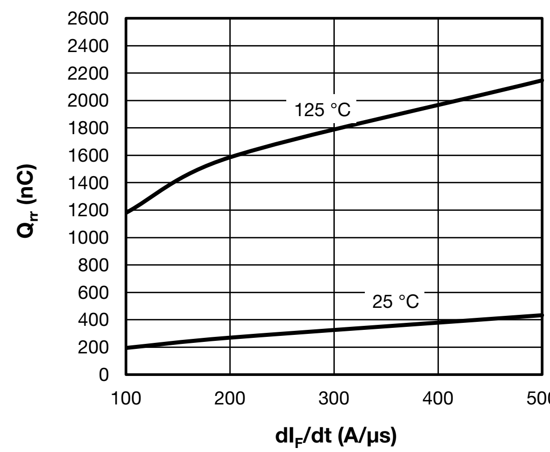


Fig. 16 - Q_{rr} vs. dI_F/dt)
(Typical D5 - D6 Clamping Diode Reverse Recovery Charge vs. dI_F/dt)), V_{rr} = 200 V, I_F = 50 A

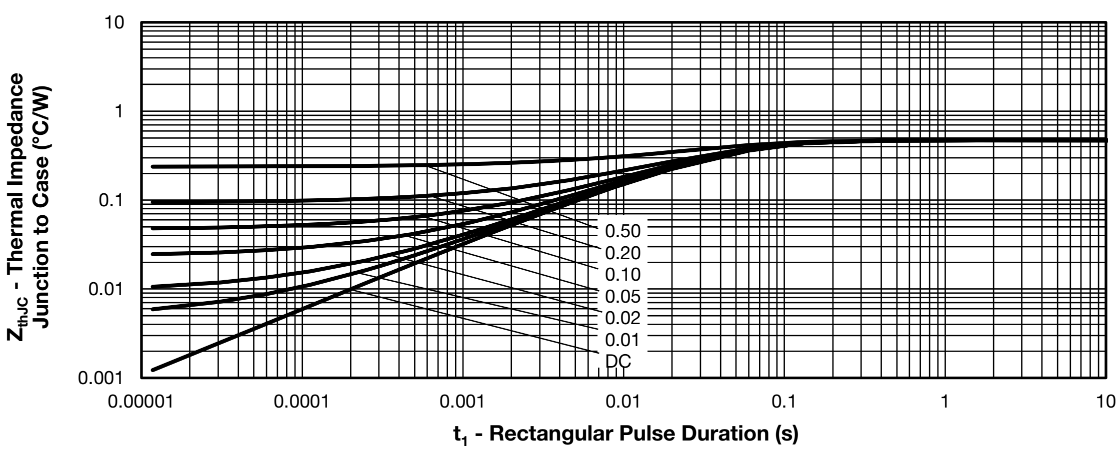


Fig. 17 - Z_{thJC} vs. t1 Rectangular Pulse Duration (Maximum Thermal Impedance Z_{thJC} Characteristics - (D5 - D6 Clamping Diode))

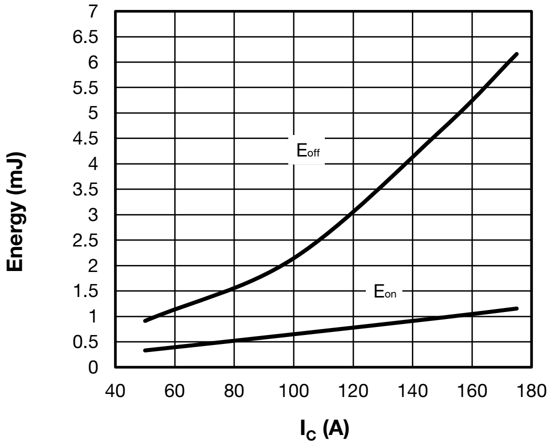


Fig. 18 - Energy Loss vs. I_C
(Typical Q2 - Q3 Trench IGBT Energy Loss vs. I_C
(with D2 - D3 Antiparallel Diode)),
T_J = 125 °C, V_{CC} = 325 V, R_g = 4.7 Ω, V_{GE} = ± 15 V, L = 500 µH

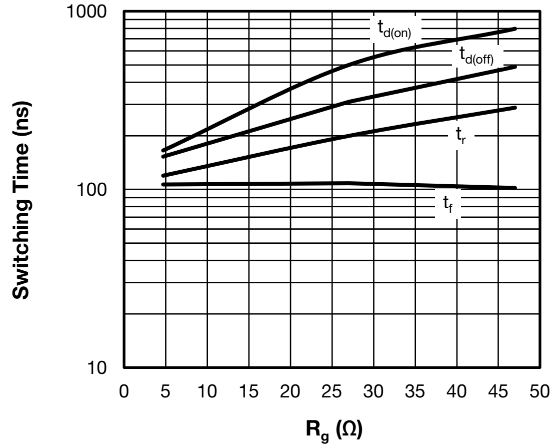


Fig. 21 - Switching Time vs. R_g (Typical Q2 - Q3 Trench IGBT Switching Time vs. R_g (with D2 - D3 Antiparallel Diode)),
T_J = 125 °C, V_{CC} = 325 V, I_C = 150 A, V_{GE} = ± 15 V, L = 500 µH

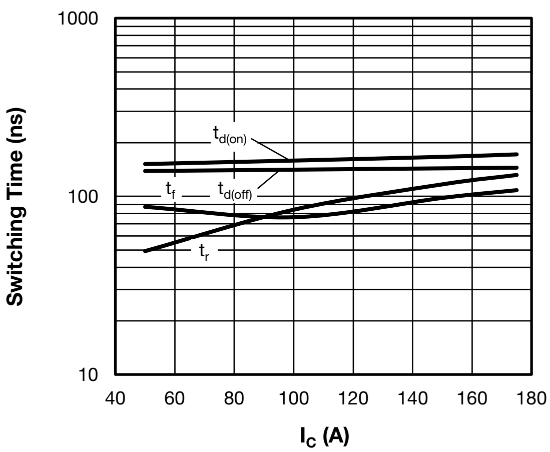


Fig. 19 - Switching Time vs. I_C
(Typical Q2 - Q3 Trench IGBT Switching Time vs. I_C
(with D2 - D3 Antiparallel Diode)),
T_J = 125 °C, V_{CC} = 325 V, R_g = 4.7 Ω, V_{GE} = ± 15 V, L = 500 µH

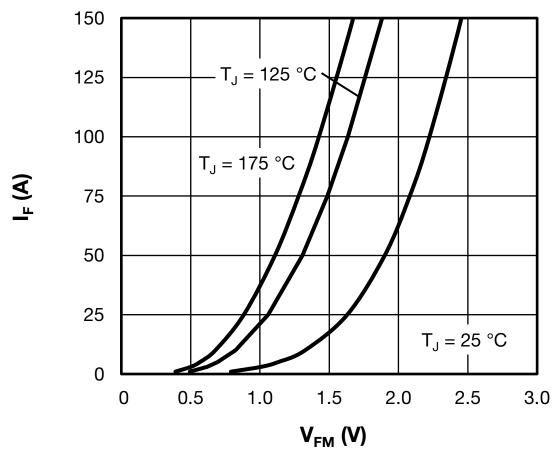


Fig. 22 - I_F vs. V_{FM}
(Typical D1 - D2 - D3 - D4 Antiparallel Diode Forward Characteristics)

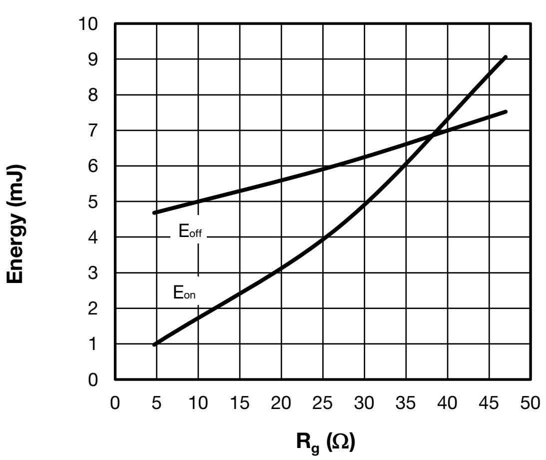


Fig. 20 - Energy Loss vs. R_g
(Typical Q2 - Q3 Trench IGBT Energy Loss vs. R_g
(with D2 - D3 Antiparallel Diode)),
T_J = 125 °C, V_{CC} = 325 V, I_C = 150 A, V_{GE} = ± 15 V, L = 500 µH

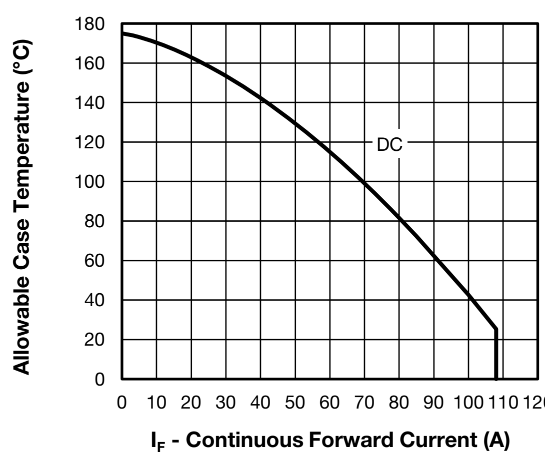


Fig. 23 - Allowable Case Temperature vs. Continuous Forward Current,
(Maximum D1- D2 - D3 - D4 Diode Continuous Forward Current vs. Case Temperature)

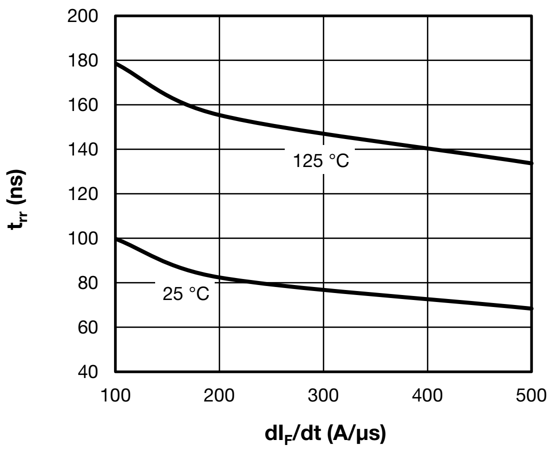


Fig. 24 - t_{rr} vs. dI_F/dt
(Typical D1 - D2 - D3 - D4 Antiparallel Diode Reverse Recovery Time vs. dI_F/dt), V_{rr} = 200 V, I_F = 50 A

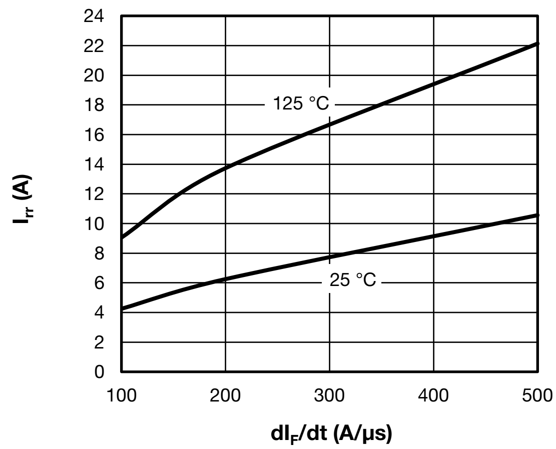


Fig. 25 - I_{rr} vs. dI_F/dt
(Typical D1 - D2 - D3 - D4 Antiparallel Diode Reverse Recovery Current vs. dI_F/dt), V_{rr} = 200 V, I_F = 50 A

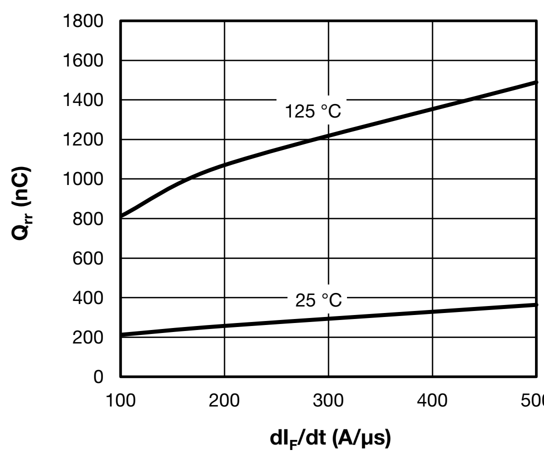


Fig. 26 - Q_{rr} vs. dI_F/dt
(Typical D1 - D2 - D3 - D4 Antiparallel Diode Reverse Recovery Charge vs. dI_F/dt), V_{rr} = 200 V, I_F = 50 A

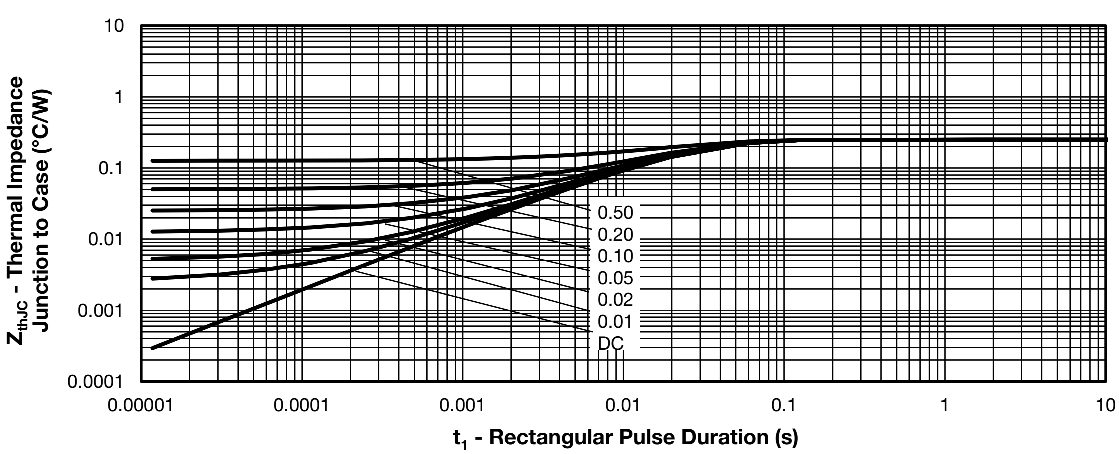


Fig. 27 - Z_{thJC} vs. t1 Rectangular Pulse Duration (Maximum Thermal Impedance Z_{thJC} Characteristics - (Q2 - Q3 Trench IGBT))

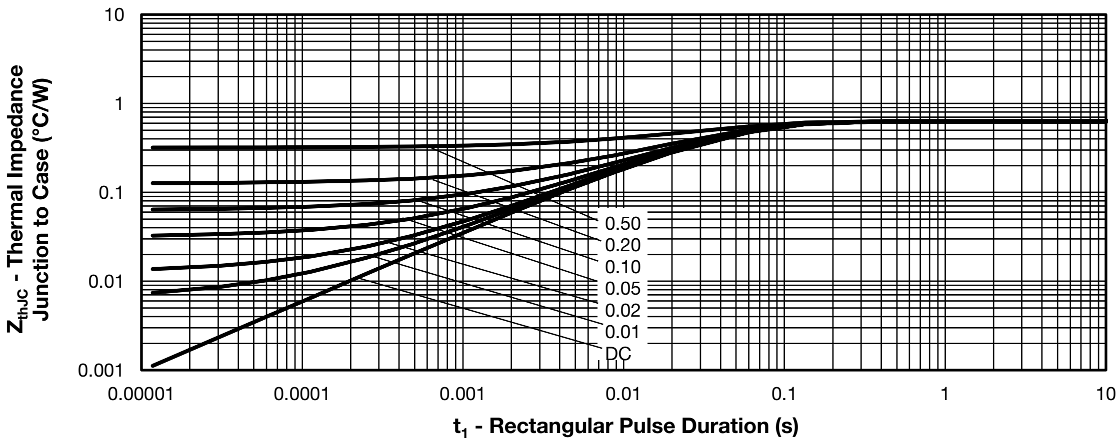


Fig. 28 - Z_{thJC} vs. t1 Rectangular Pulse Duration (Maximum Thermal Impedance Z_{thJC} Characteristics - (D1 - D2 - D3 - D4 Antiparallel Diode))

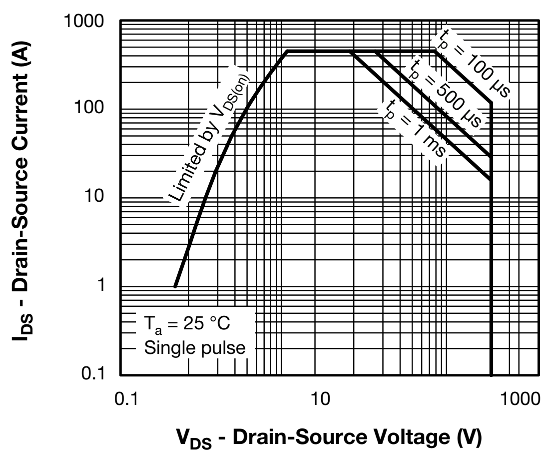


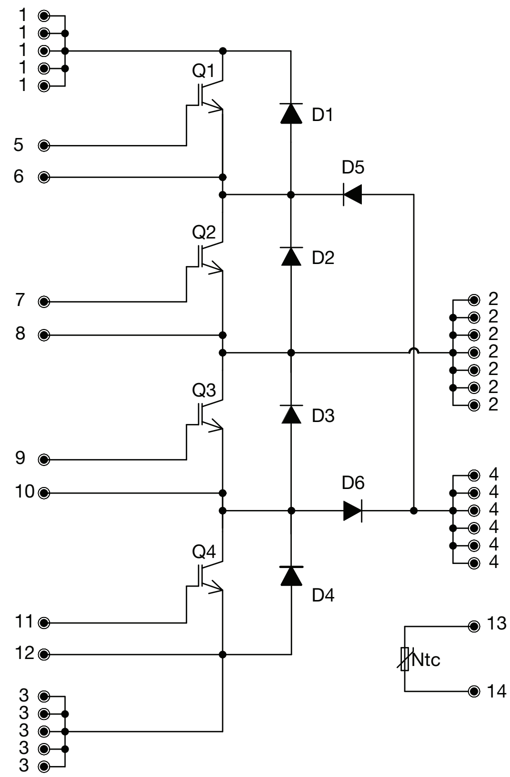
Fig. 29 - SOA

ORDERING INFORMATION TABLE

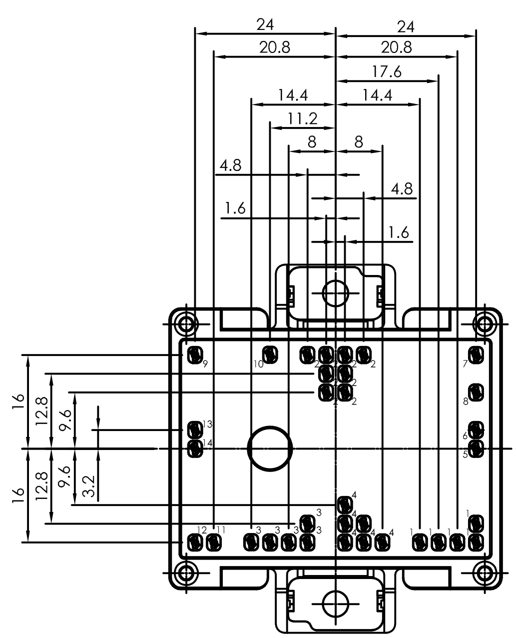
Device code	VS-	ET	F	150	Y	65	N
	1	2	3	4	5	6	7

1	-	Vishay Semiconductors product
2	-	Package indicator (ET = EMIPAK-2B)
3	-	Circuit configuration (F = 3-levels half-bridge inverter stage)
4	-	Current rating (150 = 150 A)
5	-	Switch die technology (Y = trench IGBT)
6	-	Voltage rating (65 = 650 V)
7	-	Diode die technology (N = ultrafast diode)

CIRCUIT CONFIGURATION



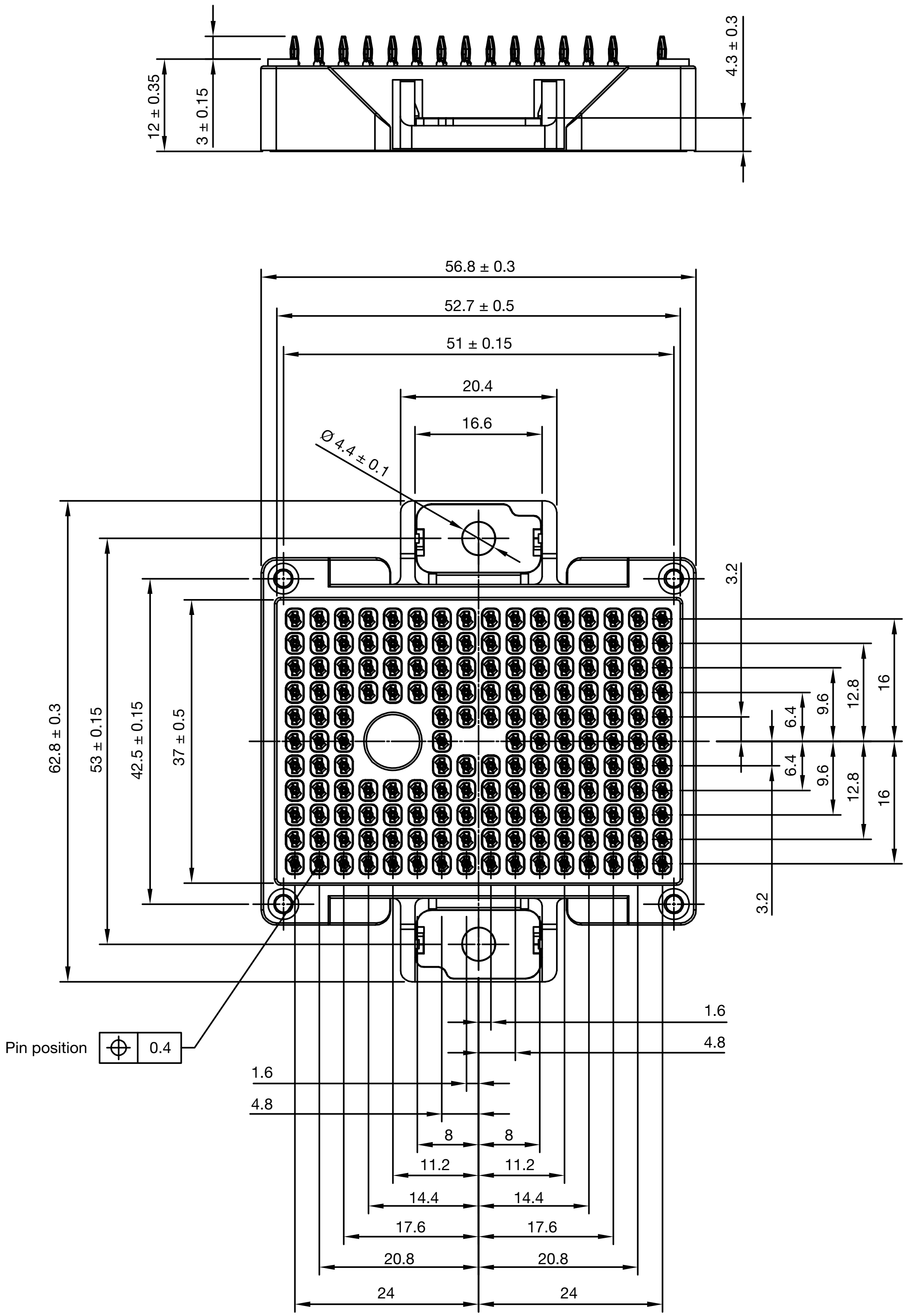
PACKAGE in millimeters



LINKS TO RELATED DOCUMENTS	
Dimensions	www.vishay.com/doc?95559

EMIPAK-2B PressFit

DIMENSIONS in millimeters



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