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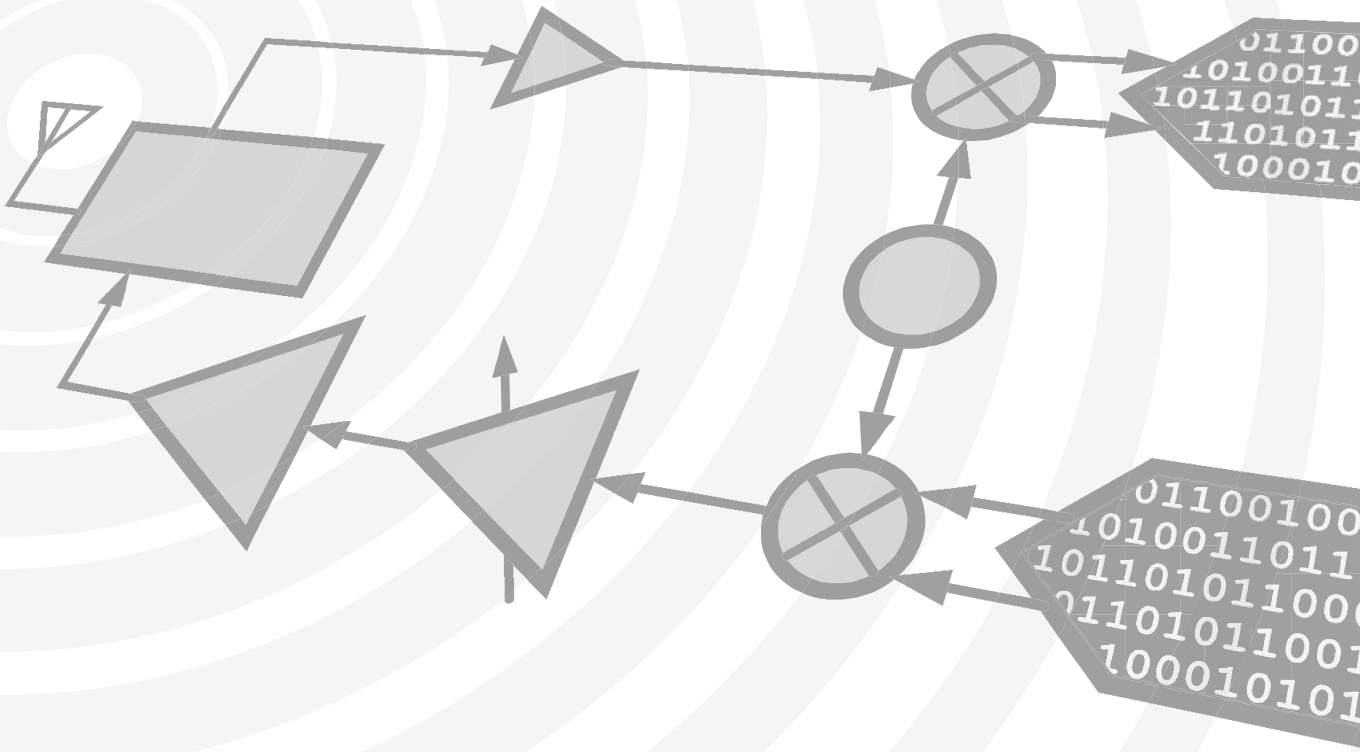

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HMC794* Product Page Quick Links

Last Content Update: 11/01/2016

Comparable Parts

View a parametric search of comparable parts

Evaluation Kits

- HMC794LP3E Evaluation Board

Documentation

Data Sheet

- HMC794 Data Sheet

Reference Materials

Quality Documentation

- Package/Assembly Qualification Test Report: 16L 3x3mm QFN Package (QTR: 11003 REV: 02)
- Package/Assembly Qualification Test Report: LP2, LP2C, LP3, LP3B, LP3C, LP3D, LP3F, LP3G (QTR: 2014-0364)
- Semiconductor Qualification Test Report: BiCMOS-A (QTR: 2013-00235)

Design Resources

- HMC794 Material Declaration
- PCN-PDN Information
- Quality And Reliability
- Symbols and Footprints

Discussions

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Sample and Buy

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Technical Support

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HMC794LP3E

2 GHz LOW NOISE PROGRAMMABLE DIVIDER (N = 1 to 4)

Typical Applications

The HMC794LP3E is ideal for:

- LO Generation with Low Noise Floor
- Clock Generators
- Mixer LO Drive
- Military Applications
- Test Equipment
- Sensors

Features

Low Noise Floor: -163 dBc/Hz at 10 MHz offset and -160 dBc/Hz at 100 kHz offset

Programmable Frequency Divider, N = 1, 2, 3 or 4

200 MHz to 2 GHz Input Frequency Range

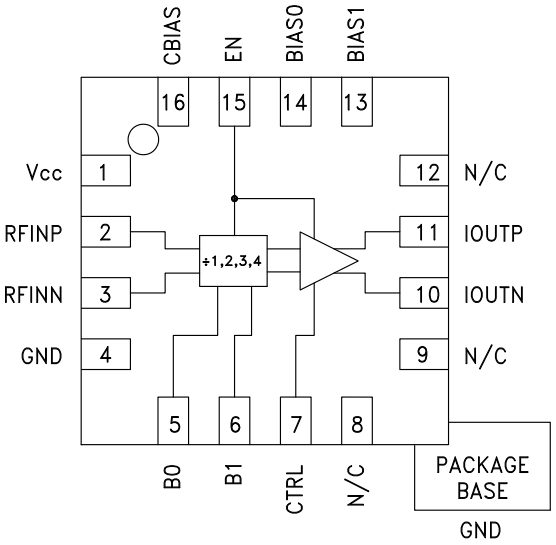
50% Duty Cycle Outputs

Up to +10 dBm Output Power

Sleep Mode: Consumes <1 µA

16 Lead 3X3 mm SMT Package: $9mm^2$

Functional Diagram



General Description

The HMC794LP3E is a SiGe BiCMOS low noise programmable frequency divider in a 3x3mm lead-less surface mount package. The circuit can be programmed to divide from N = 1 to N = 4 in the 200 MHz to 2 GHz input frequency range. The high level output power (up to 10 dBm) with a very low SSB phase noise and 50% duty cycle makes this device ideal for low noise clock generation, LO generation and LO drive applications. Configurable bias controls allow power minimization of up to 20%.

Electrical Specifications, T_A = +25° C, Vcc = +5V, Z_O = 50Ω, Bias1 = GND

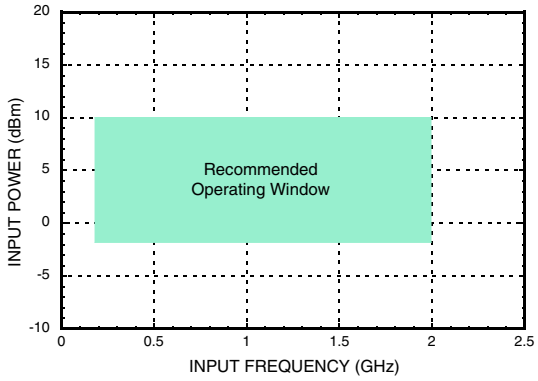
Parameter	Conditions	Min.	Typ.	Max.	Units
RF Input Characteristics					
Max RF Input Frequency				2	GHz
Min RF Input Frequency		200			MHz
RF Input Power	Note: best SSB Phase Noise for Pin > 5 dBm	-2	3	10	dBm
Divider Output Characteristics					
Differential Output Power	Programmable in 2 steps (see the Pout plots for each division ratio)	-3	10	12	dBm
SSB Phase Noise @ 10 MHz Offset	+5 dBm Input Power, 2 GHz Input		-163		dBc/Hz
SSB Phase Noise @ 100 kHz Offset			-160		dBc/Hz
SSB Phase Noise @ 10 kHz Offset			-153		dBc/Hz
Duty Cycle for Differential Mode	+5 dBm Input Power		50 ±3		%
Logic Inputs					
VIH Input High Voltage		3		5	V
VIL Input Low Voltage		0		0.4	V

Electrical Specifications, T_A = +25° C, Vcc = +5V, Z_O = 50Ω, Bias1 = GND *(Continued)*

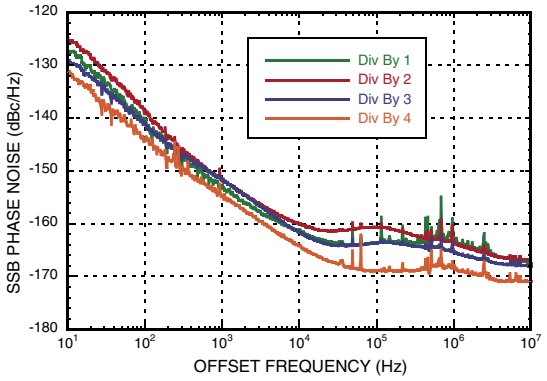
Parameter	Conditions	Min.	Typ.	Max.	Units
Power Supplies					
Vcc	Analog Supply	4.75	5	5.25	V
Current Consumption					
Itot - Total Current Consumption	5V Supply	100		150	mA
Itot - Total Current Consumption [1]	5V supply, CTRL = 0V, BIAS0 = 0V CTRL = 0V, BIAS0 = 5V CTRL = 5V, BIAS0 = 0V	100 109 115		130 150 150	mA mA mA
Sleep Current	EN = 0V			1	µA
CBias Reference Voltage [2]	Measured with 10 GΩ Volt meter		3.8		V

[1] Bias0 = 0V, for maximum frequency range; Bias0 = 5V, for better phase noise floor; CTRL = 5V, for maximum output power
[2] CBias voltage pin cannot drive external load. It must be measured with a 10 GΩ volt meter such as Agilent 34410A, typical 10 MOhms DVM will read erroneously.

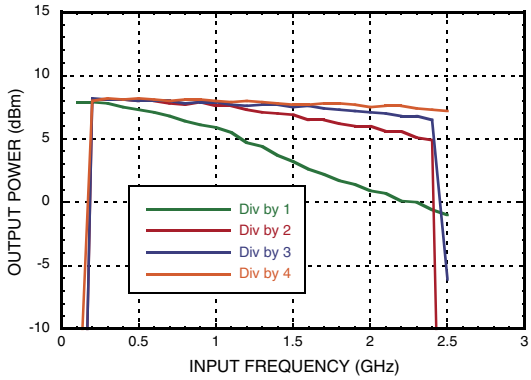
Input Sensitivity Window



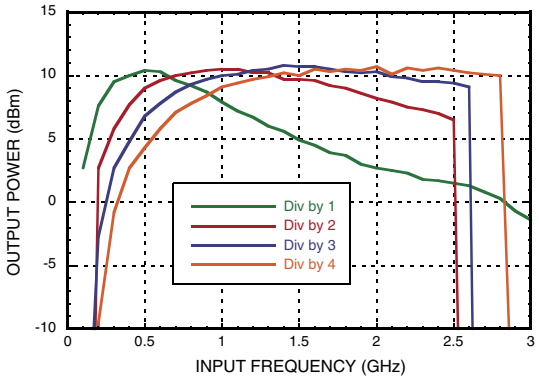
Residual Phase Noise Divide by 1, 2, 3 & 4, (Differential) [3]



Pout vs. Div Ratio [4], (Single-Ended)



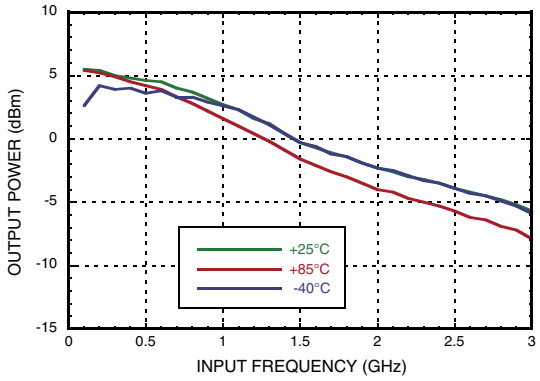
Pout vs. Div Ratio [4], (Differential)



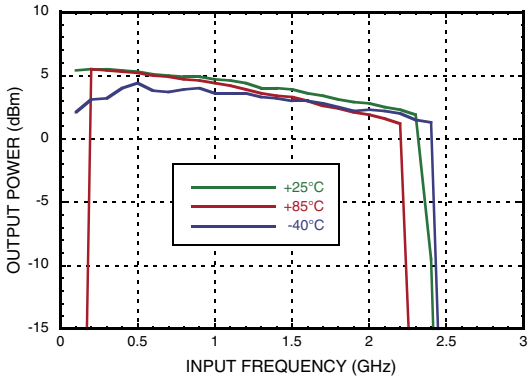
[3] CTRL = +5V, Bias0 = 0V, Pin = +8 dBm @ 2 GHz
[4] CTRL = +5V, Bias0 = 0V, Pin = +4 dBm

2 GHz LOW NOISE PROGRAMMABLE DIVIDER (N = 1 to 4)

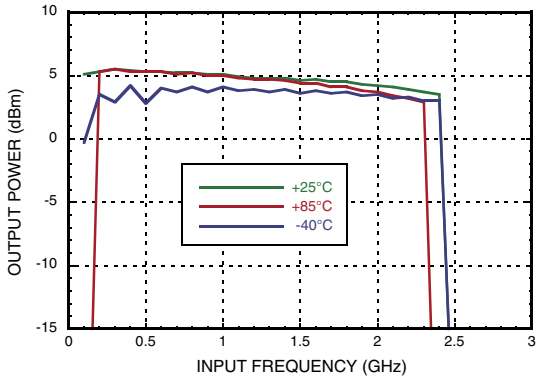
Pout Divide-by-1 vs. Temperature [1], (Single-Ended)



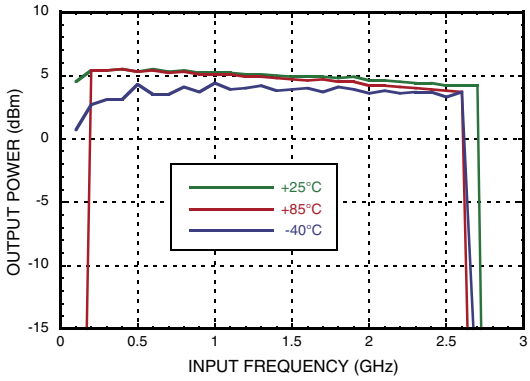
Pout Divide-by-2 vs. Temperature [1], (Single-Ended)



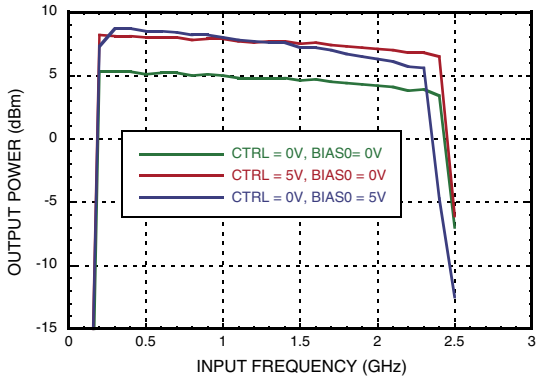
Pout Divide-by-3 vs. Temperature [1], (Single-Ended)



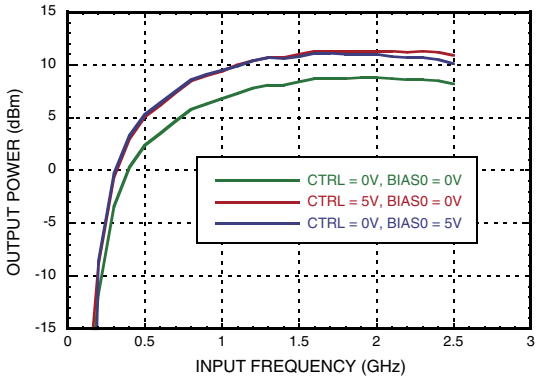
Pout Divide-by-4 vs. Temperature [1], (Single-Ended)



Pout Divide-by-3 vs. CTRL & Bias0 [2] (Single-Ended)

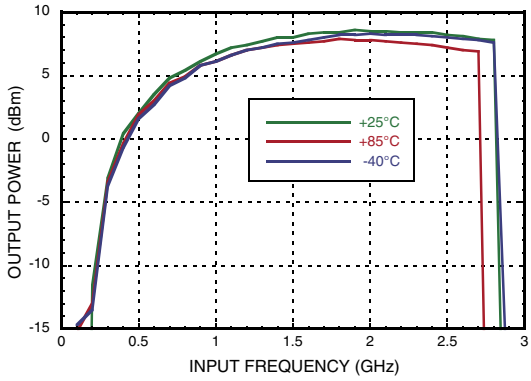


Pout Divide-by-4 vs. CTRL & Bias0 [2] (Differential)

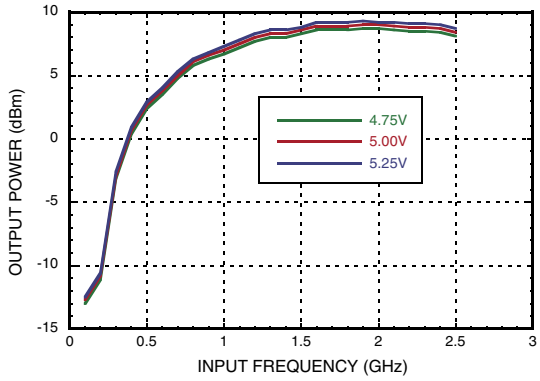


[1] CTRL = 0V, Bias0 = 0V, Pin = +4 dBm [2] Pin = +4 dBm

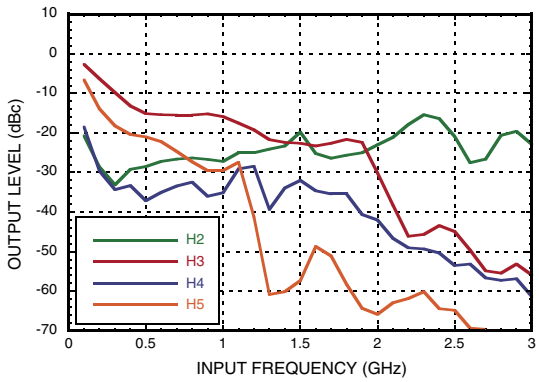
Pout Divide-by-4 vs. Temperature [1], (Differential)



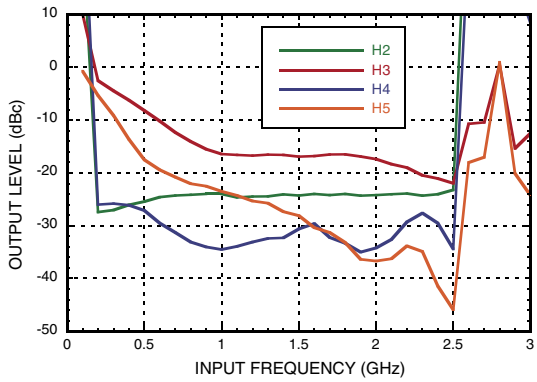
Pout Divide-by-4 vs. Supply Voltage [1], (Differential)



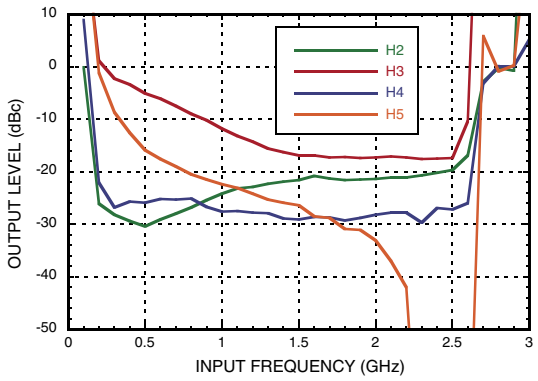
Divide-by-1 Harmonics [1], (Differential)



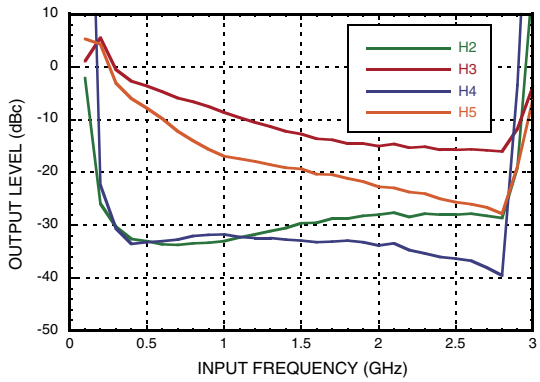
Divide-by-2 Harmonics [1], (Differential)



Divide-by-3 Harmonics [1], (Differential)



Divide-by-4 Harmonics [1], (Differential)

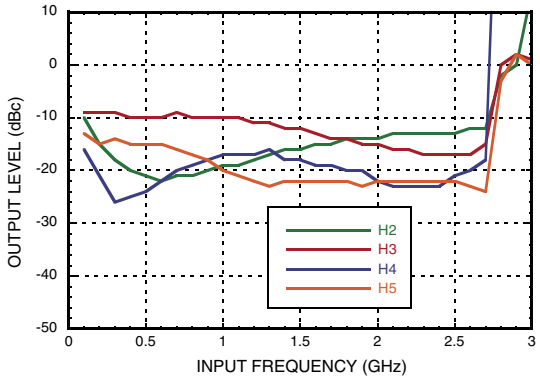


[1] CTRL = 0V, Bias0 = 0V, Pin = +4 dBm

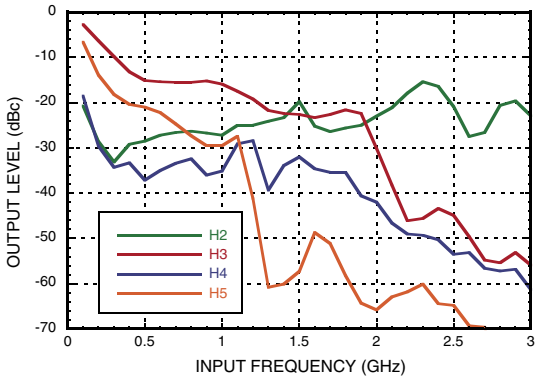
HMC794LP3E

2 GHz LOW NOISE PROGRAMMABLE DIVIDER (N = 1 to 4)

Divide-by-4 Harmonics [1], (Differential)



Divide-by-4 Harmonics [2], (Single-Ended)



Absolute Maximum Ratings

RF Input Power	13 dBm
Supply Voltage (Vcc)	5.5V
Control Inputs (B0, B1, CTRL, Bias0, EN)	5.5V
Junction Temperature	125 °C
Continuous Pdiss (T = 85 °C) (derate 33 mW/ °C above 85 °C)	1.3W
Thermal Resistance (Junction to ground paddle)	30 °C/W
Storage Temperature	-65 to +125 °C
Operating Temperature	-40 to +85 °C
ESD Sensitivity (HBM)	Class 1A

ELECTROSTATIC SENSITIVE DEVICE
OBSERVE HANDLING PRECAUTIONS

Programming Truth Table for Frequency Division Ratios

B1	B0	Divide-by
0	0	1
0	1	2
1	0	3
1	1	4
0 = Logic Low 1 = Logic High		

Digital Control Input Voltages

State	B0, B1, CTRL, BIAS1, BIAS0, EN
Low	0 to 0.4V
High	3V to 5V

Typical Supply Current vs. Vcc

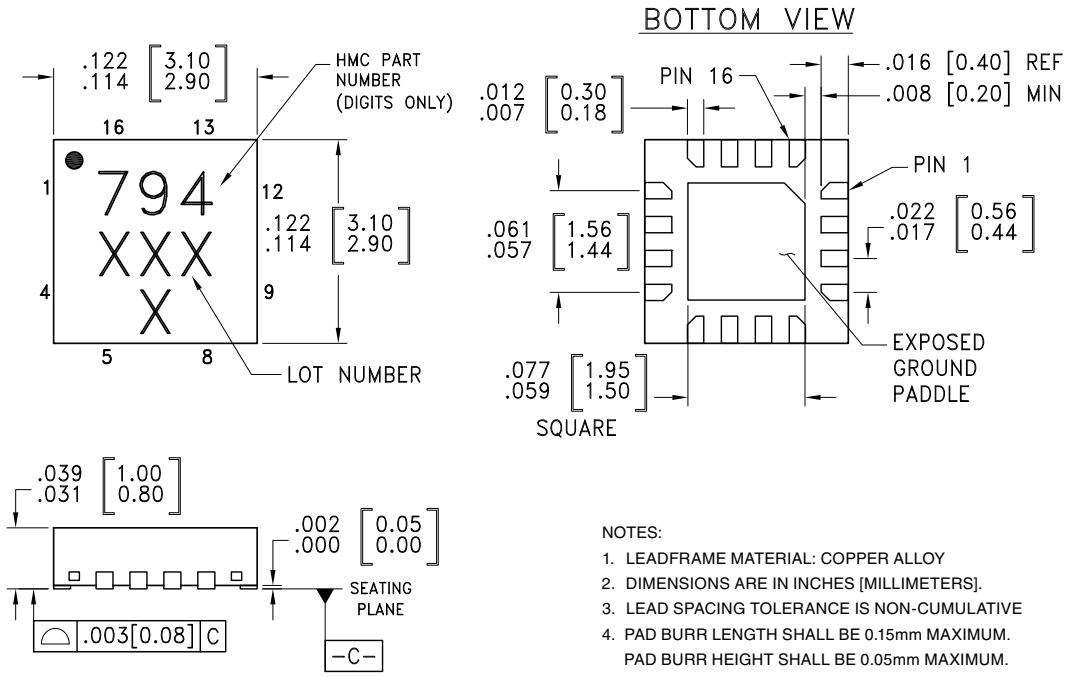
Vcc (V)	Icc (mA)
4.75	105*
5.00	115*
5.25	125*

Note: HMC794LP3E will work over full voltage range above.
* For CTRL = 0V, Bias0 = 0V

[1] CTRL = 5V, Bias0 = 0V, Pin = +4 dBm [2] CTRL = 0V, Bias0 = 0V, Pin = +4 dBm

2 GHz LOW NOISE PROGRAMMABLE DIVIDER (N = 1 to 4)

Outline Drawing



NOTES:

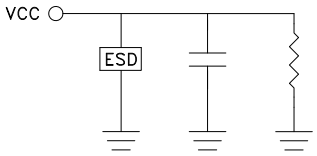
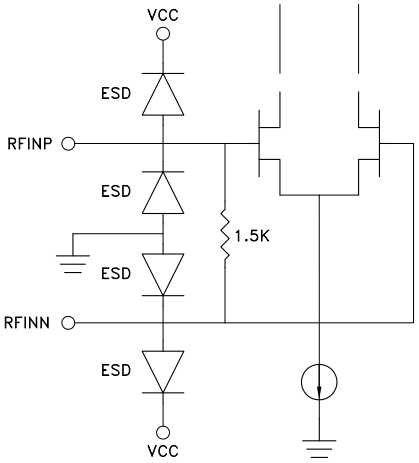
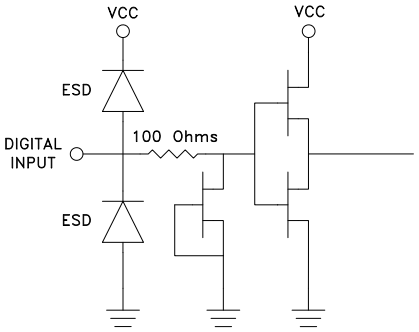
1. LEADFRAME MATERIAL: COPPER ALLOY
2. DIMENSIONS ARE IN INCHES [MILLIMETERS].
3. LEAD SPACING TOLERANCE IS NON-CUMULATIVE
4. PAD BURR LENGTH SHALL BE 0.15mm MAXIMUM. PAD BURR HEIGHT SHALL BE 0.05mm MAXIMUM.
5. PACKAGE WARP SHALL NOT EXCEED 0.05mm.
6. ALL GROUND LEADS AND GROUND PADDLE MUST BE SOLDERED TO PCB RF GROUND.
7. REFER TO HITTITE APPLICATION NOTE FOR SUGGESTED PCB LAND PATTERN.

Package Information

Part Number	Package Body Material	Lead Finish	MSL Rating	Package Marking [1]
HMC794LP3E	RoHS-compliant Low Stress Injection Molded Plastic	100% matte Sn	MSL1 [2]	794 XXX

[1] 4-Digit lot number XXXX
[2] Max peak reflow temperature of 260 °C

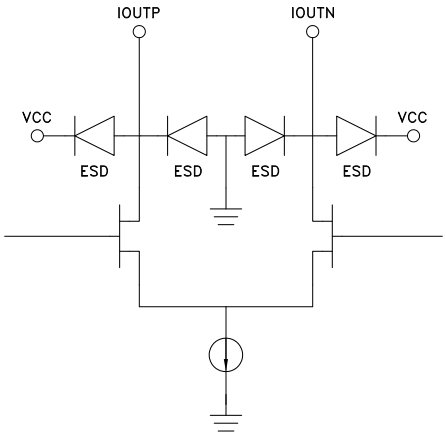
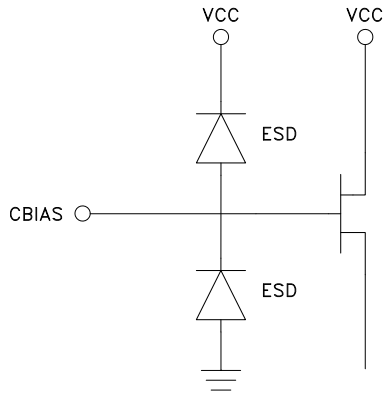
Pin Description

Pin Number	Function	Description	Interface Schematic
1	Vcc	+5V Voltage Supply	
2	RFINP	RF Positive Input. Input is DC coupled, external DC blocks required..	
3	RFINN	RF Negative Input. Input is DC coupled, external DC blocks required...	
4	GND	this pin must be connected to RF/DC ground.	
5	B0	Division ratio (LSB) See programming truth table.	
6	B1	Division ratio (MSB) See programming truth table.	
7	CTRL	Divider Output Buffer Power Control	
13	BIAS1	For proper operation this pin should be grounded.	
14	BIAS0	Digital Core Bias Control [1]	
15	EN	Chip Enable	
8, 9, 12	N/C	No connection required. This pin may be connected to ground, without affecting performance.	

[1] Divider Core Bias Control Bit

Bias0 = 0V, Divider Core Minimum Bias
Bias0 = 5V, Divider Core Maximum Bias

Pin Description *(Continued)*

Pin Number	Function	Description	Interface Schematic
10	IOUTN	Divider Negative Output, Open Drain. Typically 100 Ohms connected to Vcc.	
11	IOUTP	Divider Positive Output, Open Drain. Typically 100 Ohms connected to Vcc.	
16	CBIAS	External Bypass Decoupling for Precision/Low Noise Bias Circuit	

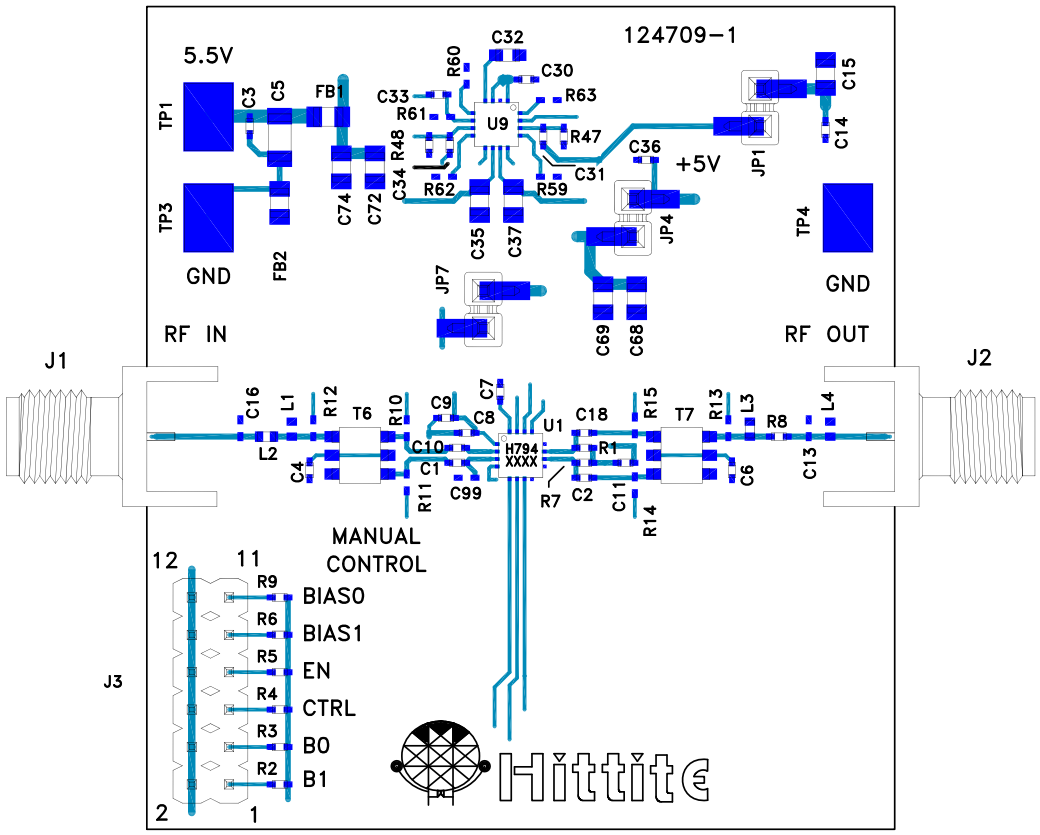
Application Note:

The HMC794LP3E is a high performance RF divider. Such dividers are high gain devices with internal feedback. The device will oscillate if used with AC coupled RF inputs and if no RF input is applied. Normally, if the RF input signal is removed the device should be disabled, or it should be placed in divide by 1 mode. The device is stable in divide by one mode with no RF input. The device will oscillate in divide 2, 3, or 4 modes with no RF input. In general very small RF input levels will stop all oscillations. At the minimum rated RF input sensitivity level or higher, no oscillations or spurious signals exist and excellent low noise performance is achieved.

For input frequency lower than 200 MHz, square wave input signal is recommended.

The divider output power for the differential mode, shows a roll off at lower frequencies due to the limited frequency range of the T6 & T7 (4:1) RF transformers, 500 MHz to 3000 MHz.

Evaluation PCB



List of Materials for Evaluation PCB 124842 [1]

Item	Description
J3	DC Connectors
J7, J8	SMA-F Johnson Connector
C1, C2, C4, C6, C10, C11 C12, C18	1 nF Capacitor, 0402 Pkg.
C3, C9, C14, C30, C31, C33, C34, C36	0.1 µF Capacitor, 0402 Pkg.
C5	10 µF Capacitor, 1206 Pkg.
C7	10,000 pF Capacitor, 0402 Pkg.
C8	10 pF Capacitor, 0402 Pkg.
C15, C35, C37, C68, C69, C72, C74	4.7 µF Capacitor, 0805 Pkg.
C32	1 µF Capacitor, 0603 Pkg.
R1, R7	100 Ohm, Resistor, 0402 Pkg.
R2 - R6, R9	100 kOhm, Resistor, 0402 Pkg.
R8, L2	0 Ohm, Resistor, 0402 Pkg.
R47	27 k Ohm, Resistor, 0402 Pkg.
R48	15 k Ohm, Resistor, 0402 Pkg.

Item	Description
T6, T7	4:1 RF Transformer, MABACT0065
TP1, TP3, TP4	PC Compact SMT
FB1, FB2	Murata BLM21AG02SNID
U1	HMC794LP3E Programmable Divider
U9	Hittite Ultra Low Noise Quad Regulator
PCB [2]	124709 Eval Board

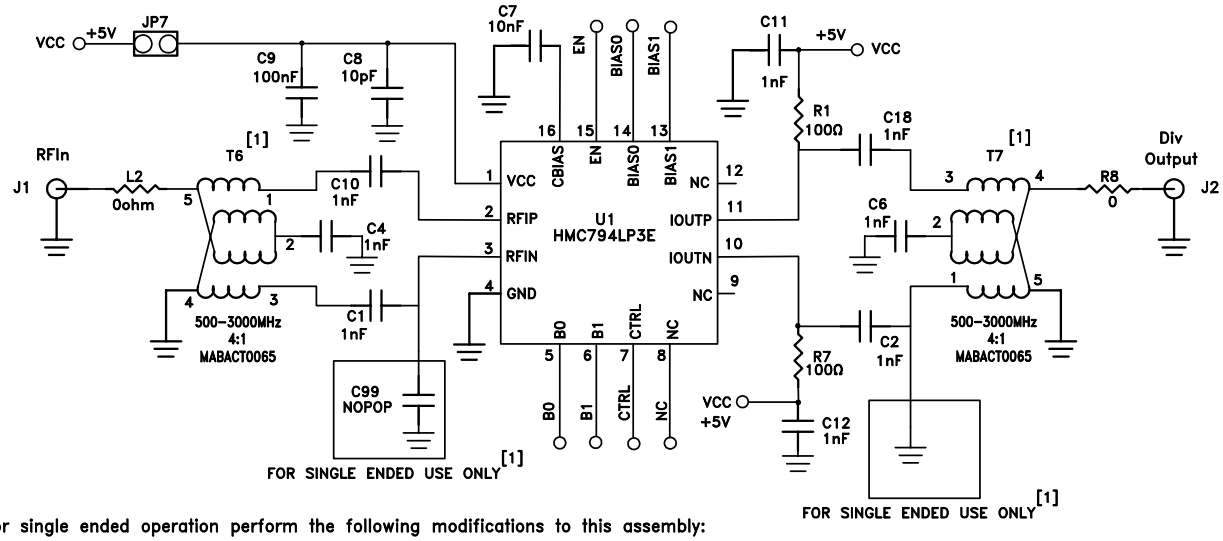
[1] Reference this number when ordering complete evaluation PCB

[2] Circuit Board Material: Rogers 4350 or Arlon 25FR

The circuit board used in the application should use RF circuit design techniques. Signal lines should have 50 Ohm impedance while the package ground leads and backside ground paddle should be connected directly to the ground plane similar to that shown. A sufficient number of via holes should be used to connect the top and bottom ground planes. The evaluation circuit board shown is available from Hittite upon request.

2 GHz LOW NOISE PROGRAMMABLE DIVIDER (N = 1 to 4)

Evaluation PCB Schematic



[1] For single ended operation perform the following modifications to this assembly:
1) Remove T6 and T7, C4 and C6
2) Install 0Ω resistors (jumpers) over the following pads:
   a) Pads 1 and 2 on T6 location
   b) Pads 5 and 6 on T6 location
   c) Pads 2 and 3 on T7 location
   d) Pads 4 and 6 on T7 location
3) Install 100pF cap in location C99
4) Install jumper wire at location Pad 1 on T7 to Ground. Remove solder mask to reveal ground plane in this area.

Input Voltage Range
5.3V min, 5.5V nom, 6.0 V max
Current 110mA to 165mA